AN-1682 LM3679TL Evaluation Board

1 Introduction

The LM3679TL evaluation board is a working demonstration of a step down DC-DC converter. This application report contains information about the evaluation board. For further information on buck converter topology, device electrical characteristics, and component selection, see the device-specific data sheet.

2 General Description

The LM3679TL, a high efficient step down DC-DC switching buck converter, steps down a constant voltage for cell phones, PDA's, and many other applications from a single Li-ion battery ranging from 2.5 V to 5.5 V. The automatic intelligent switching between PFM and PWM provides high efficiency throughout the I_{OUT} range. The LM3679 is available in a 1.8 V output voltage option in a 5-bump DSBGA and ultra thin UR package*****. Using the UR package along with specific external components, allows for a low profile solution size with a max height of 0.55 mm. A switching frequency of 3 MHz (typ.) permits use of miniature surface mount external components.

NOTE: Contact Texas Instruments for the UR samples.

3 Operating Conditions

- V_{IN} range: 2.5 V ≤ V_{IN} ≤ 5.5 V
- Recommended load current: 0 mA ≤ I_{OUT} ≤ 350 mA
- Ambient temperature (T_A) range: -30°C to +85°C
- Junction temperature (T_J) range: -30°C to +125°C

4 Typical Application

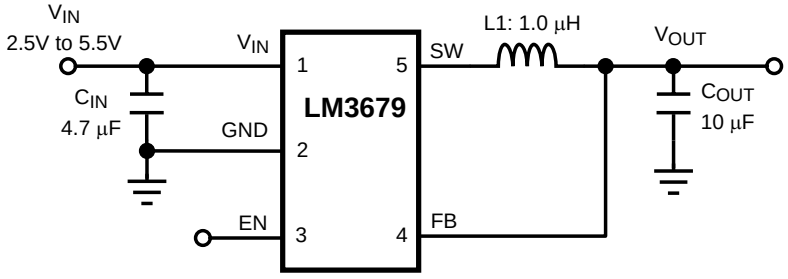

Figure 1. Typical Application Circuit

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5 Connection Diagram and Package Mark Information

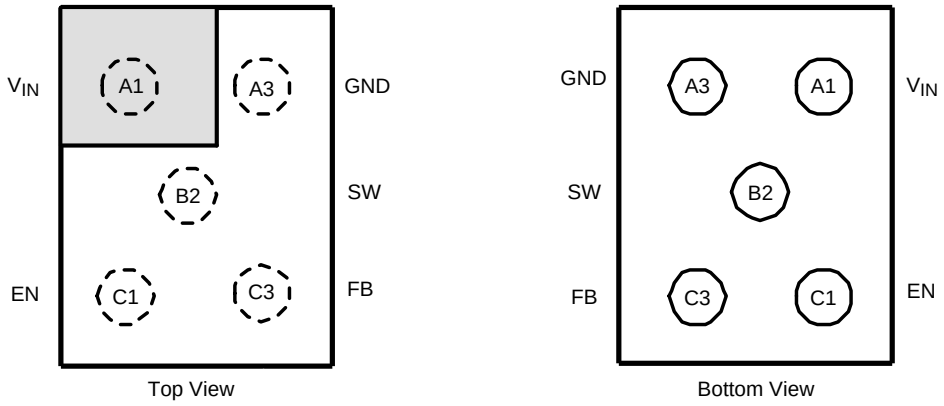

Figure 2. 5-Bump DSBGA and YPD Package

6 Pin Descriptions

Pin No	Name	Description
A1	V_{IN}	Power supply input. Connect to the input filter capacitor (see Figure 1)
A3	GND	Ground pin
C1	EN	Enable input. The device is in shutdown mode when voltage to this pin is <0.4 V and enabled when >1.0 V. Do not leave this pin floating.
C3	FB	Feedback analog input. Connect directly to the output filter capacitor for fixed voltage versions.
B2	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier.

7 Powering the LM3679 for Bench Measurement

When powering the LM3679 with a bench power supply, it is recommended to place a 100 µF tantalum capacitor across the V_{IN} and GND supply terminals of the bench power supply. This capacitor reduces the input spike caused by the power supply and long power cables. The combination of the power supply and inductance within the power cables produce a large voltage spike that may damage the device. In addition, consideration must be given to the enable pin of the device. The enable should never be taken high, until minimum specified operating voltage of 2.7 V is reached. The enable pin should also never exceed the input voltage.

8 Evaluation Board Layout

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA/YPD package and board pads. These poor solder joints can result in erratic or degraded performance.

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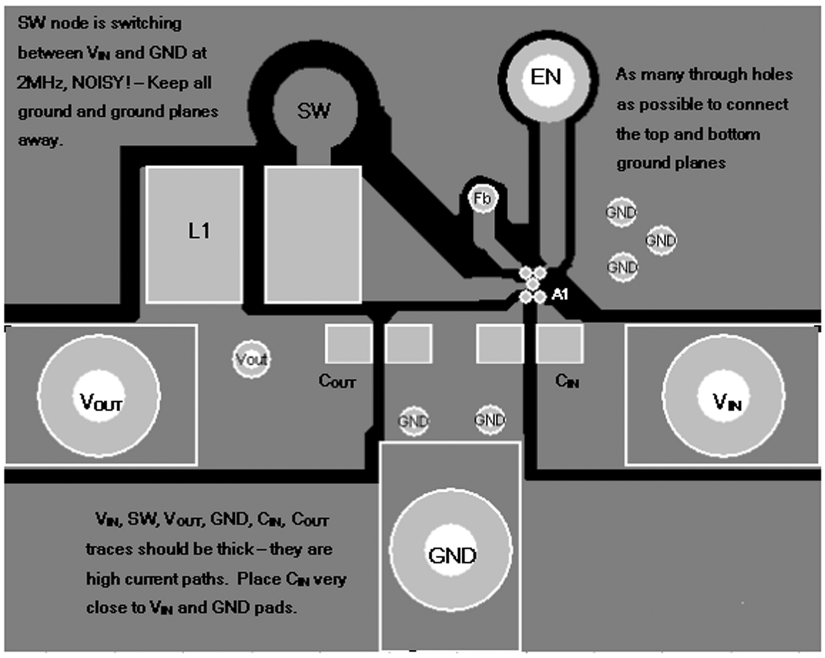

Figure 3. Top Layer (5-bump DSBGA/YPD)

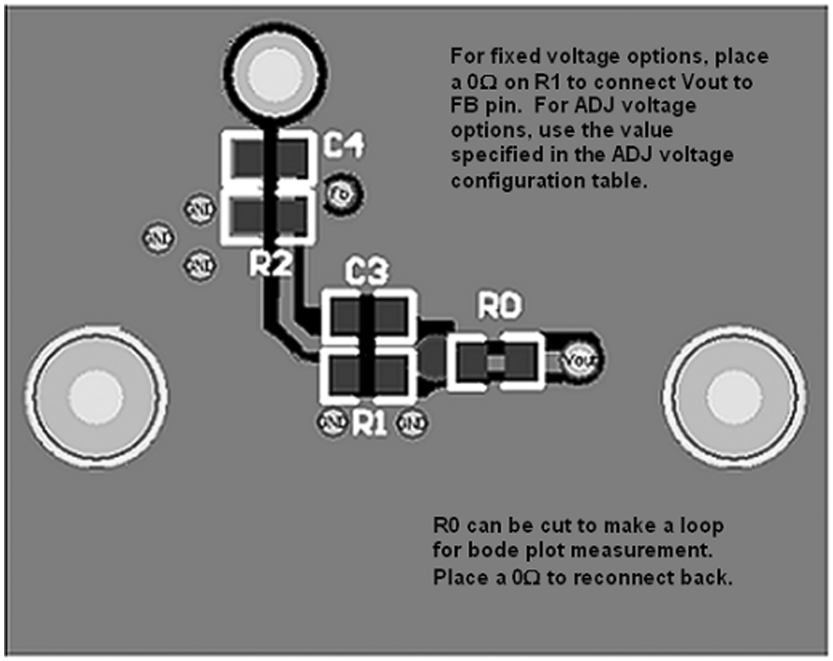

Figure 4. Bottom Layer (5-bump DSBGA/YPD)

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8.1 Board Layout Considerations

1. Place the LM3679 on 10.82 mil pads. As a thermal relief, connect to each pad with a 7 mil wide, approximately 7 mil long trace, and then incrementally increase each trace to its optimal width. The important criterion is symmetry to ensure the solder bumps on the re-flow evenly (*see DSBGA Package Assembly and Use*).
2. Place the LM3679, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
3. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the LM3679 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3679 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. Connect the ground pins of the LM3679, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3679 by giving it a low-impedance ground connection.
5. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces
6. Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The voltage feedback trace must remain close to the LM3679 circuit and should be routed directly from FB to V_{OUT} at the output capacitor and should be routed opposite to noise components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
7. Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive pre-amplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

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9 Bill of Materials (BOM) For Common Configurations

Table 1. Bill of Materials (BOM) For Common Configurations

	Manufacture	Manufacture No	Description
LM3679 - 1.8 V FIXED			
C1 (input C)	TDK	C1608X5R0J475	4.7 µF, 6.3 V, 0603, 10%
C2 (output C)	TDK	C1608X5R0J106	10 µF, 6.3 V, 0603, 10%
L1 (inductor)	FDK	MIPSA2520D	1.0 µH inductor, DCR = 100mΩ
R1 (V_{OUT} to V_{FB})	Vishay	CRCW06030R00F	0 Ω, 0603, 1%
R2 (V_{FB} to GND)	None		
C3 (V_{OUT} to V_{FB})	None		
C4 (V_{FB} to GND)	None		
LM3679 - 1.8 V FIXED (Low Profile Application, 0.55 max height) (1)			
C1 (input C)	Taiyo-Yuden	JMK107BJ475K	4.7 µF, 6.3 V, 0603, (0.5 mm height)
C2 (output C)	Taiyo-Yuden	JMK107BJ475K	4.7 µF, 6.3 V, 0603, (0.5 mm height) X 2
L1 (inductor)	Murata	LQM21PN1R0M	1.0 µH inductor, (0.55 mm max height)
R1 (V_{OUT} to V_{FB})	None		
R2 (V_{FB} to GND)	None		
C3 (V_{OUT} to V_{FB})	None		
C4 (V_{FB} to GND)	None		
COMMON TO ALL			
V_{IN} banana jack - red	Johnson Components	108-0902-001	Connector, insulated banana jack (red)
V_{OUT} banana jack - yellow	Johnson Components	108-0907-001	Connector, insulated banana jack (yellow)
GND banana jack - black	Johnson Components	108-0903-001	Connector, insulated banana jack (black)
Post for EN	Turrent	1573-2	Upright post from eval board
Post for V_{IN}	Turrent	1502-2	Upright post from eval board
Post for V_{OUT}	Turrent	1502-2	Upright post from eval board
Post for GND	Turrent	1502-2	Upright post from eval board

(1) Contact Texas Instruments for the UR samples.

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