AN-1722 LM3678 Evaluation Board

1 Introduction

The LM3678 evaluation board is a working demonstration of a synchronous buck DC-DC converter. This document contains information about the evaluation board. For more details and electrical characteristics about the converter operation, see the *High-Performance Miniature 1.5-A Step-Down DC-DC Converter for Handheld Applications Data Sheet* (SNVS464).

2 Operating Range

- V_{IN} range: 2.5 V to 5.5 V
- Recommended load current: up to 1.5A
- V_{OUT} = 0.8/1.2 V

3 Package

WSON-10 no-pullback (3mm x 3mm x 0.8mm)

4 Typical Application

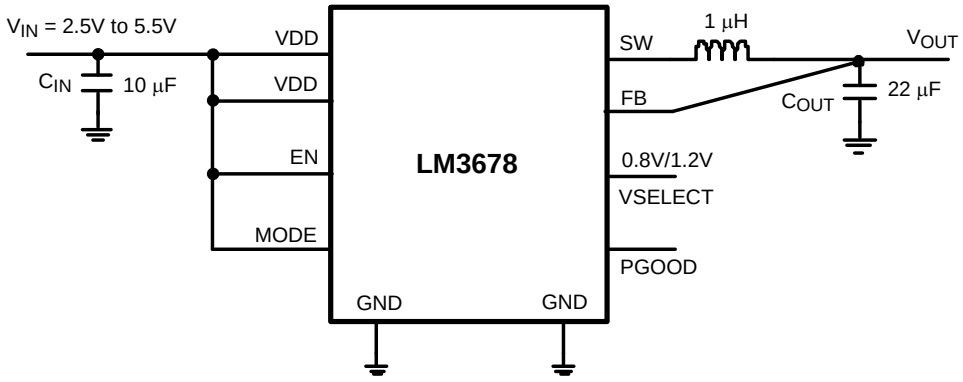


Figure 1. Typical Application Circuit

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5 Connection Diagrams

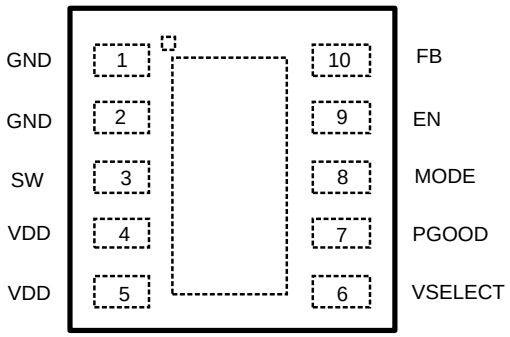


Figure 2. Top View

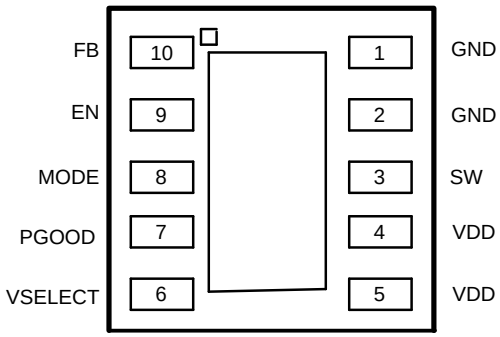


Figure 3. Bottom View

Note: Figure 1 through Figure 3 are not to any actual scale

6 Pin Descriptions

Pin No	Name	Description
1	GND	Ground
2	GND	
3	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
4	V_{DD}	Power supply input. Connect to the input filter capacitor (Figure 1).
5	V_{DD}	
6	VSELECT	Output Voltage Select. For Example : VSELECT = LOW V_{OUT} = 0.8 V VSELECT = HIGH, V_{OUT} = 1.2 V
7	PGOOD	Power Good Flag. This common drain logic output is pulled to ground when the output voltage is not within ± 7.5% of regulation.
8	MODE	Mode Control Pin: Mode = 1 selects forced PWM mode Mode = 0 selects auto PFM-PWM mode
9	EN	Enable Pin. The device is in shutdown mode when voltage to this pin < 0.4 V and enabled when > 1.0 V. Do not leave this pin floating.
10	FB	Feedback Analog Input. Connect directly to the output filter capacitor for fixed voltage versions.
DAP	DAP	Die Attach Pad; connect the DAP to GND on PCB layout to enhance thermal performance. It should not be used as a primary ground connection.

7 Powering the LM3678 for Bench Measurements

When powering the LM3678 with a bench power supply, it is recommended to place a 100 µF tantalum capacitor across the V_{IN} and GND supply terminals of the bench power supply. This capacitor reduces the input spike caused by the power supply and long power cables. The combination of the power supply and inductance within the power cables produce a large voltage spike that may damage the device. In addition, consideration must be given to the enable pin of the device. The enable should never be taken high, until the minimum ensured operating voltage of 2.7 V is reached. The enable pin should also never exceed the input voltage.

8 Operating Information

The LM3678 evaluation board is set for the following default positions:

- V_{OUT} = 1.2 V, for 0.8 V, set VSELECT pin to low via jumper
- Mode = H (PWM mode), for Auto mode, set mode = Low (move jumper to inner position).
- EN pin is tied to V_{IN} via a jumper

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9 Evaluation Board Layout

LM3678 is a four-layer board designed to maximize the performance. The top layer consists of high-current path and the bottom layer for low-current and logic signals path. The inner layer 1 and layer 2 are dedicated for PGND (power GND) and SGND (analog and logic GND). For optimum performance, it is recommended to separate the PGND and SGND pins and join them together at the start GND on the PCB.

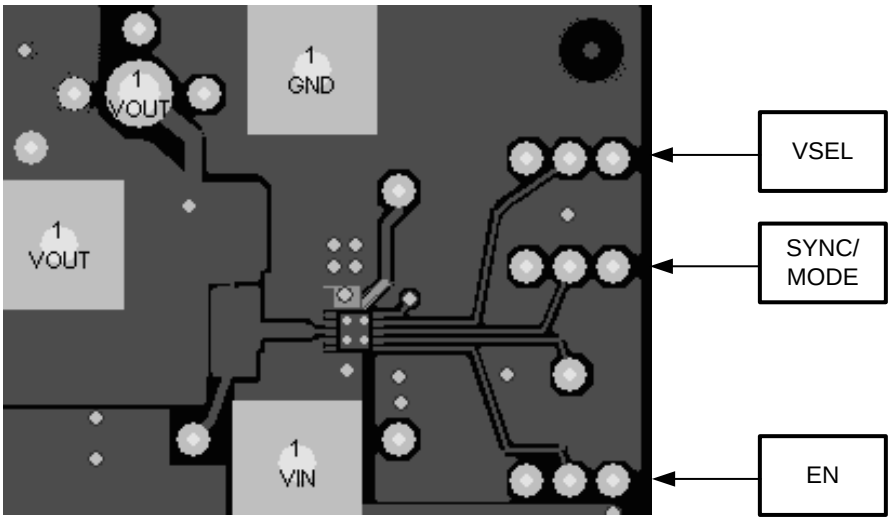


Figure 4. Top Layer

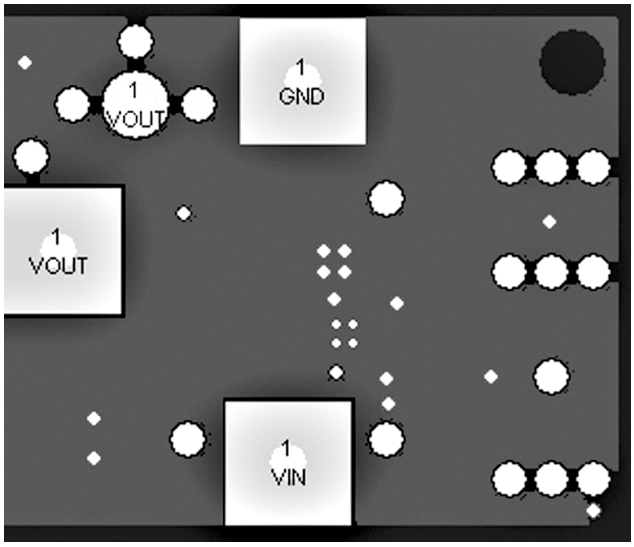


Figure 5. Mid Layer 1

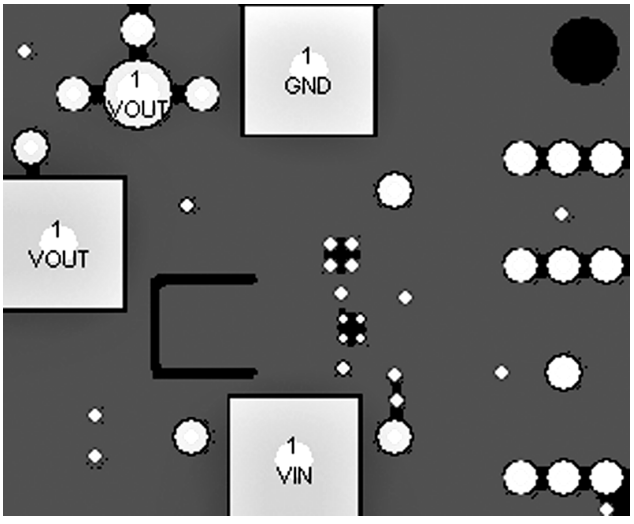


Figure 6. Mid Layer 2

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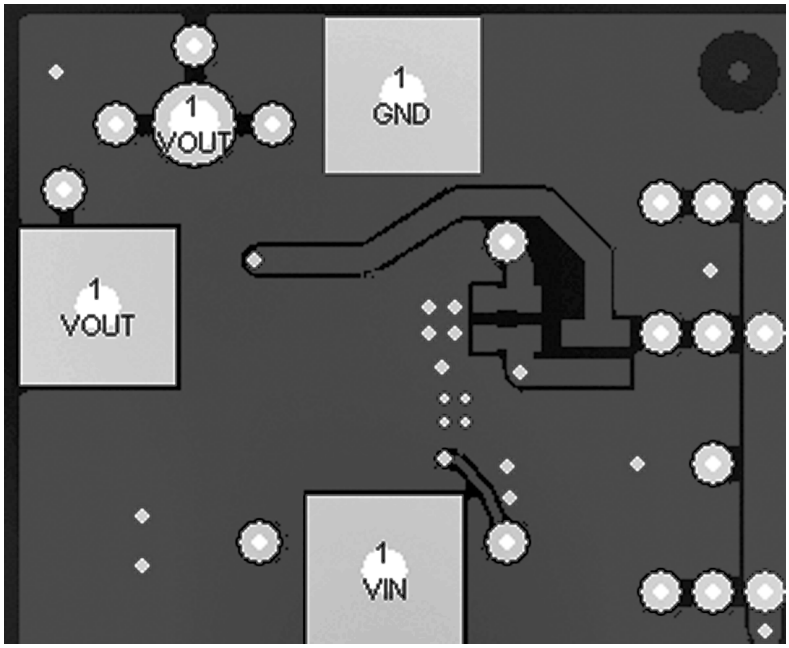


Figure 7. Bottom Layer

10 Bill of Materials (BOM) for LM3678

Table 1. Bill of Materials (BOM)

Component Name	Manufacturer	Specification	Case Size
LM3678	NSC	WSON-10	3 mm x 3 mm x 0.8 mm
C1 = 10 µF	Taiyo-Yuden	JMK212BJ106K	0805 (2012)
C2 = 22 µF		JMK212BJ226MG	0805 (2012)
Inductor	Taiyo-Yuden	NR4012T-1RON	4 mm x 4 mm x 1.2 mm
R1	Vishay/any manufacturer	0603	0Ω

Table 2. Test Point

V_{SEL}, Mode and EN	Header	3 in Series 3 (3 x 1)
V_{SEL}, Mode and EN	Jumper Female (Handle centerline)	A26242–ND
V_{IN} banana jack - red	Johnson Components	108–0902–001
V_{OUT} banana jack - yellow	Johnson Components	108–0907–001
GND banana jack - black	Johnson Components	108–0903–001

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