AN-1623 LM3668 Evaluation Board

1 Introduction

The LM3668 evaluation board is a working demonstration of a synchronous buck-boost DC-DC converter. This document contains information about the evaluation board. For more details and electrical characteristics about the converter operation, see the device-specific data sheet.

2 Operating Range

- V_{IN} range: 2.5 V to 5.5 V
- For 2.8 V/3.3 V and 3.0 V/3.4 V versions:
  - 1A maximum load current for V_{IN} = 2.8 V to 5.5 V
  - 800mA maximum load current for V_{IN} = 2.7 V
  - 600mA maximum load current for V_{IN} = 2.5 V
- For 4.5 V/5 V version:
  - 1A maximum load current for V_{IN} = 3.9 V to 5.5 V
  - 800mA maximum load current for V_{IN} = 3.4 V to 3.8 V
  - 700mA maximum load current for V_{IN} = 3.0 V to 3.3 V
  - 600mA maximum load current for V_{IN} = 2.7 V to 2.9 V

3 Package

WSON–12 no-pullback (3 mm x 3 mm x 0.8 mm)

4 Typical Application

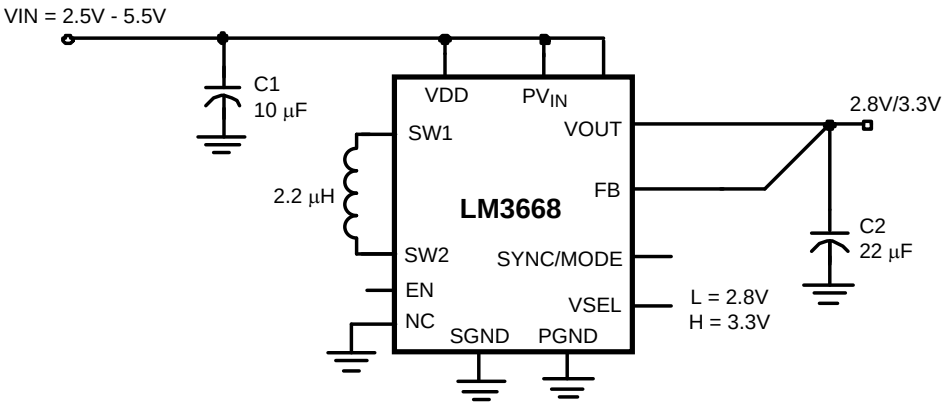

Figure 1. Typical Application Circuit

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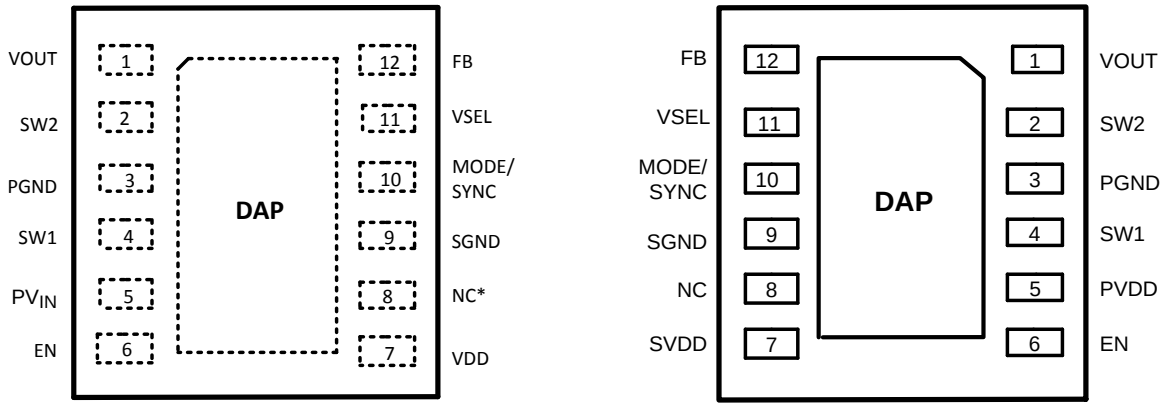

NOTE: The above figures are not to any actual scale.

5 Pin Descriptions

Pin No	Pin Name	Description
1	V_{OUT}	Connect to output capacitor.
2	SW2	Switching Node connection to the internal PFET switch (P2) and NFET synchronous rectifier (N2).
3	PGND	Power Ground.
4	SW1	Switching Node connection to the internal PFET switch (P1) and NFET synchronous rectifier (N1).
5	PV_{IN}	Supply to the power switch, connect to the input capacitor.
6	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low.
7	V_{DD}	Signal Supply input. If board layout is not optimum an optional 1µF ceramic capacitor is suggested as close to this pin as possible.
8	NC	No connect. Connect this pin to SGND on PCB layout.
9	SGND	Analog and Control Ground.
10	MODE/SYNC	Mode = LOW, Automatic Mode. Mode= HI, Forced PWM Mode SYNC = external clock synchronization from 1.6MHz to 2.7MHz (When SYNC function is used, device is forced in PWM mode).
11	VSEL	Voltage selection pin; (i.e., 2.8 V/3.3 V option) Logic input low = 2.8 V and logic high = 3.3 V to set output Voltage.
12	FB	Feedback Analog Input. Connect to the output at the output filter.
DAP	DAP	Die Attach Pad, connect the DAP to SGND on PCB layout to enhance thermal performance. It should not be used as a primary ground connection.

6 Bill Of Materials

Component Name	Manufacturer	Specification	Case Size
LM3668	TI	WSON-12	3 mm x 3 mm x 0.8 mm
C_{IN} = 10 µF	Taiyo-Yuden	JMK212BJ106K	0805(2012)
C_{OUT} = 22 µF (2.8 V/3.3 V, 3.0 V/3.4 V)		JK212BJ226MG	0805(2012)
C_{OUT} = 22 µF (4.5 V/5.0 V)		LMK212BJ226MMG	0805(2012)
C_{IN}_ V_{DD} = 4.7 µF		JMK212BJ475M	0805(2012)
Inductor	Coilcraft	LPS4018–222L	4mm x 4mm x 1.8mm

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7 Operating Information

The LM3668 evaluation board is set for the following default positions:

- V_{OUT} = 3.3 V, for V_{OUT} = 2.8 V move VSEL pin to Low via jumper
- SYNC mode = H (PWM mode), for auto mode, set SYNC = low (move jumper to inner position). Do not leave this pin floating.
- EN pin is tied to V_{IN} via a jumper
- It is not recommended to start up the device with full load at minimum input voltage

8 Evaluation Board Layout

LM3668EVB is a four-layer board designed to maximize the performance. Top layer consists of high current path; bottom layer is for low current and logic signals path. Inner layer 1 and layer 2 are dedicated for PGND (power GND) and SGND (analog and logic GND). For optimum performance, it is recommended to separate the PGND and SGND pins and join them together at the "star GND" on the PCB. The star GND traces on the PCB board should be close to the device power GND pin.

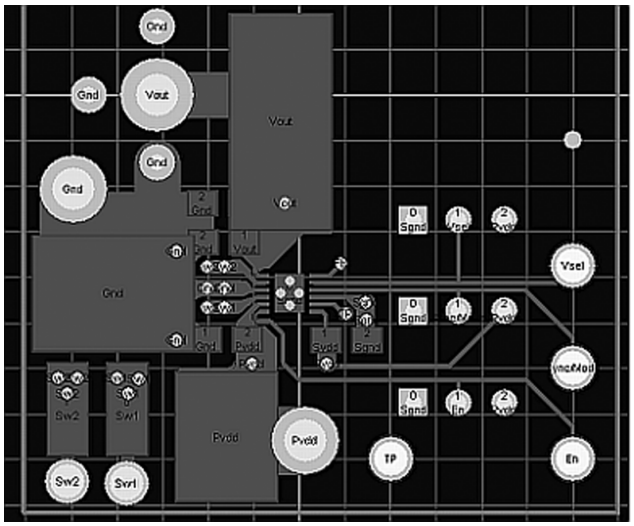

Figure 2. Top Layer

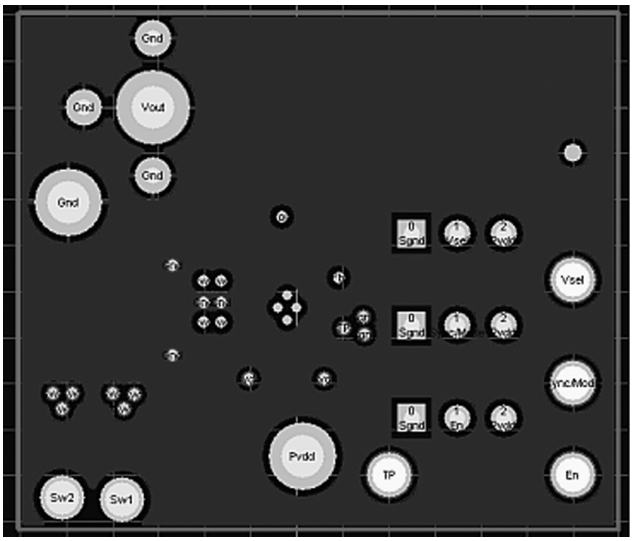

Figure 3. GND Inner Layer 1

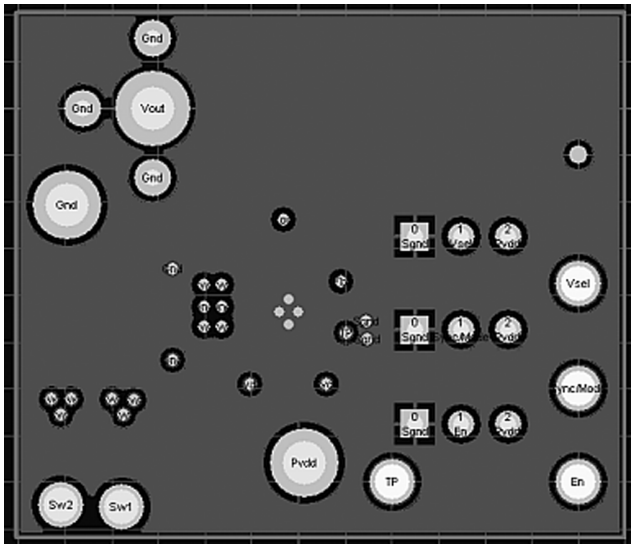

Figure 4. SGND Inner Layer 2

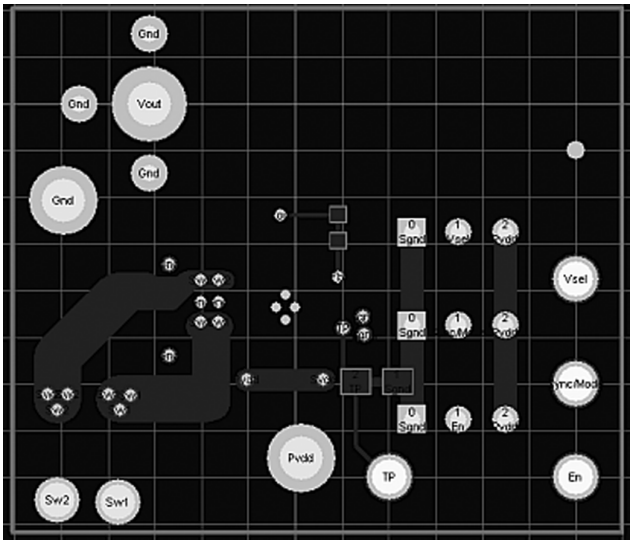

Figure 5. Bottom Layer

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