National Semiconductor

PRELIMINARY
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LM3520
Integrated White LED Driver with Organic LED Display Power Supply

General Description

The LM3520 is a dual step-up DC/DC converter, designed to drive up to 5 white LEDs with a constant current and to power an organic LED display with a constant voltage.

A single external resistor is used to set the maximum LED current. The LED current can be adjusted by applying a PWM signal to the EN pin. For higher efficiency the LM3520 operates with pulse frequency modulation (PFM) control scheme when the sub-display is enabled. When Main display is enabled, the device is operating in PWM mode.

Overvoltage protection circuitry and a 1MHz switching frequency allow for the use of small, low cost external components.

Additional features include a low-side NFET switch that can turn off the LED string with no DC current path to ground.

The LM3520 is available in a small 14-pin thermally-enchanced LLP package.

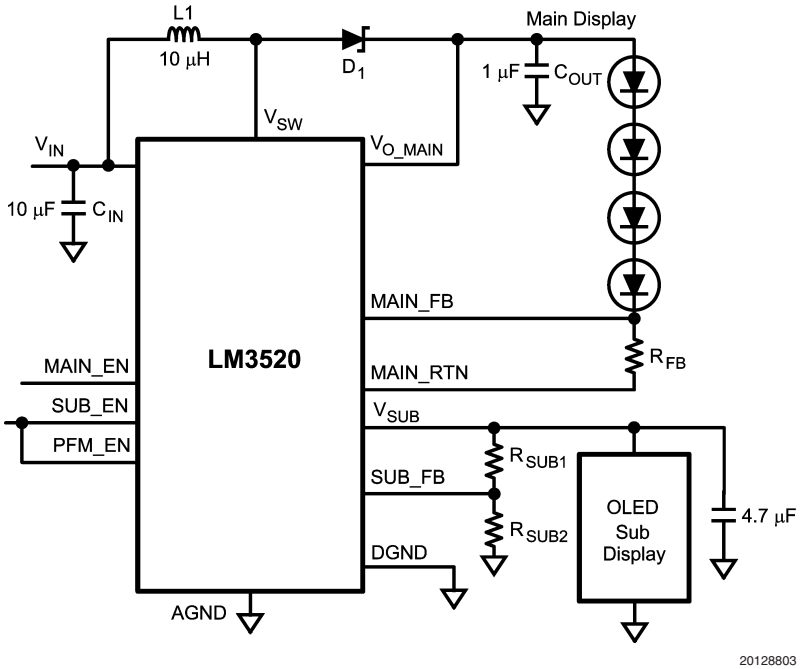
Features

- Integrated OLED and white-LED driver
- 80% efficiency
- Drives up 5 LEDs at 20mA/3.6V and 4 LEDs at 30mA/3.6V for main-display
- Up to 20V @ 50mA/3.6V for sub-display
- True shutdown isolation
- Small External Components
- 1 MHz Switching Frequency
- 23V OverVoltage Protection
- Wide Input Voltage Range: 2.7V to 5.5V
- Cycle-By-Cycle Current Limit
- PWM Dimming Control
- Low Profile 14-Pin LLP(3mm x 4mm x 0.8mm)

Applications

- Flip-phones/Clam-shell Cellular Phones
- Handheld Devices
- High-fashion cellular phones
- White LED Backlighting
- Digital Cameras

Typical Applications



Main Display with OLED Sub Display

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Functional Block Diagram

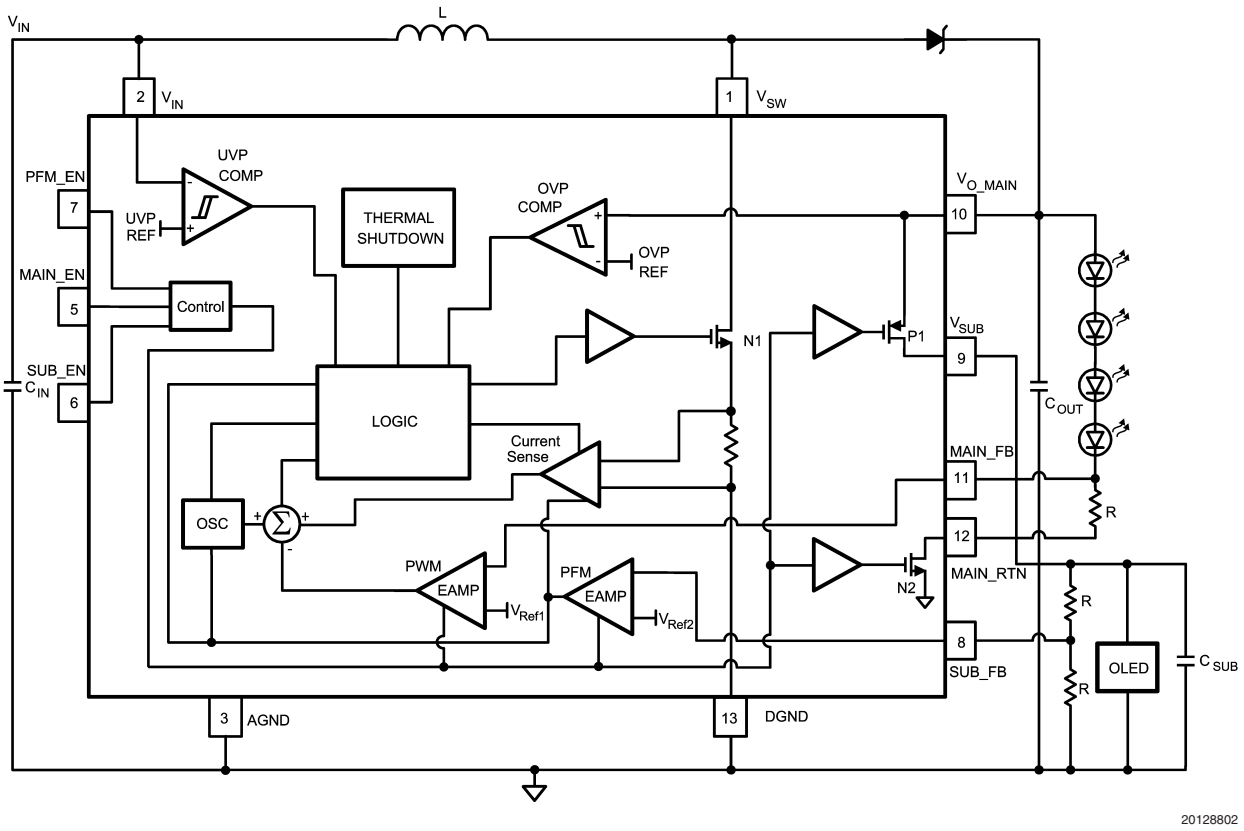


FIGURE 1. Functional Block Diagram

Pin Description

Pin #	Pin Name	Description
1	V_{SW}	Switching Voltage
2	V_{IN}	Input Voltage
3	AGND	Analog Ground
4	NC	No Connect
5	MAIN_EN	Main Enable
6	SUB_EN	Sub Display Enable
7	PFM_EN	PFM mode: OLED sub-display, pin must be tied to SUB_EN
8	SUB_FB	Sub Display Feedback
9	V_{SUB}	Sub Display Power Supply Voltage
10	V_{O_MAIN}	Main Output Voltage
11	MAIN_FB	Main Display Feedback
12	MAIN_RTN	Main Display Return Voltage
13	DGND	Digital Ground
14	NC	No Connect

Ordering Information

Order Number	Package	NSC Package Marking	Supplied As
LM3520SD	LLP-14	L133B	1000 units, Tape and Reel
LM3520SDX		L133B	4500 units, Tape and Reel

Operation Modes

LM3520 has two operating modes; *Figure 2* shows main display in PWM current mode operation, the appropriate selection of R_{FB} resistor in series with four white LEDs set the output current driving the main display. *Figure 3* shows Sub display in PFM mode, the appropriate selection of R_{SUB1} and R_{SUB2} resistors set the output voltage driving the OLED subdisplay.

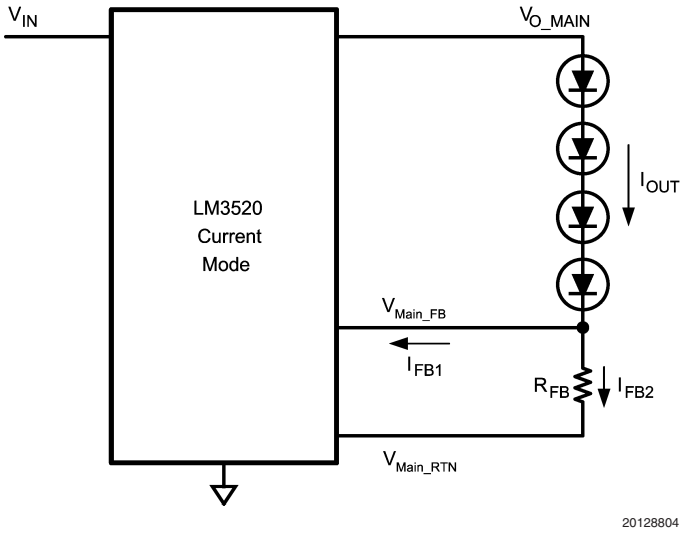


FIGURE 2. Main Display

$$I_{LED} = \frac{(V_{MAIN_FB} - V_{MAIN_RTN})}{R_{FB}}$$

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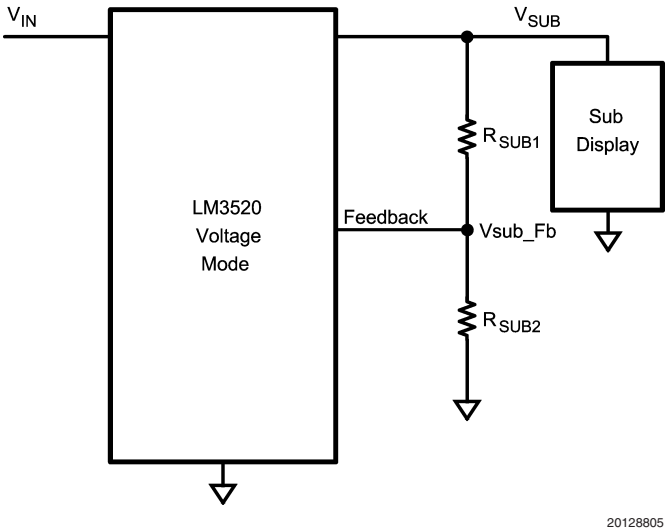


FIGURE 3. Sub Display

$$V_{SUB} = \frac{(R_{SUB1} + R_{SUB2})}{R_{SUB2}} * V_{SUB_FB}$$

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* Note: The current I_{FB1} is very small and is negligible.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}	−0.3V to +7.5V
V_{O_MAIN}	−0.3V to +25V
V_{SW}	−0.3V to V_{OUT} +0.3V
Main_FB, Main_RTN	−0.3V to +7.5V
MAIN_EN, PFM_EN & SUB_EN(Note 2)	−0.3V to +7.5V
Continuous Power Dissipation (Note 3)	Internally Limited
Maximum Junction Temperature (T_{J-MAX})	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Maximum Lead Temperature (Soldering, 10 sec)	+265˚C
ESD Rating (Note 4)	
Human Body Model:	2.0 kV
Machine Model:	200V

Operating Ratings

Input Voltage Range	2.7V to 5.5V
Junction Temperature (T_J) Range	−40˚C to +125˚C
Ambient Temperature (T_A) Range (Note 3)	−40˚C to +85˚C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), Leadless Lead frame Package (Note 5)	55˚C/W

Electrical Characteristics (Notes 6, 7)

Limits in standard typeface are for T_J = +25˚C. Limits in **boldface** type apply over the full operating junction temperature range (−40˚C ≤ = T_J ≤ +125˚C). Unless otherwise noted: specifications apply to the LM3520. V_{IN} = 3.6V, V(En) > 1.0V, C_{IN} = 10 µF (Note 8).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Enable Threshold	MAIN_EN = low SUB_EN = low				**0.3**	V
	MAIN_EN = high SUB_EN = high		**0.95**			
	PFM_EN = low				**0.3**	V
	PFM_EN = high		**0.95**			
I_{EN}	Enable Pin Current	MAIN_EN = 3.6V (Note 10)		3	**5**	µA
		SUB_EN = 3.6V (Note 10)		3	**5**	
		PFM_EN = 3.6V		3	**5**	
I_Q	Quiescent Current, Device Not Switching (PWM mode)	MAIN_FB > 0.5V		0.5	**1.3**	mA
	Quiescent Current, Device Not Switching (PFM mode)	SUB_FB > 1.0V		0.25	**0.45**	
	Quiescent Current, Device Switching	MAIN_FB = 0V or SUB_FB = 0V (open loop)		1.75	**4.5**	
	Power Off Current (Shutdown)	MAIN_EN = low SUB_EN = low PFM_EN = low		0.1	**2**	µA
V_{FB}	Feedback Voltage (MAIN_FB)	V_{IN} = 3.6V	0.455	0.5	0.545	V
	Feedback Voltage (SUB_FB)	V_{IN} = 3.6V	**1.18**	1.23	**1.28**	
I_B	FB Pin Leakage Current	MAIN_FB = 0.5V (Note 9)		10		nA
	FB Pin Bias Current	SUB_FB = 1.0V (Note 9)		50		
$I_{Current\ Limit}$	Switch Current Limit	V_{MAIN_FB} = 0V, V_{IN} = 3.6V	**0.518**	0.7	**0.917**	A
R_{DS}(ON)	Main_Switch R_{DS}(ON), N1	I_{SW} = 300 mA		0.5		Ω
	PMOS Switch R_{DS}(ON), P1	I_{PMOS} = 20 mA		3		
	MAIN_RTN R_{DS}(ON), N2	I_{Main_RTN} = 30 mA		3		
$I_{main_RTN_leakage}$	Main_RTN Leakage Current	V_{Main_RTN} = 0.5V, V_{IN} = 3.6V			**0.2**	µA
D_{Limit}	Duty Cycle Limit at PWM & PFM	V_{FB} = 0V, V_{IN} = 3.6V		90		%
F_{SW}	Switching Frequency	V_{IN} = 3.6V	**0.8**	1.1	**1.4**	MHz
I_{Leak}	Switch Leakage Current	V_{SW} = 24V		0.01	**0.5**	µA

Electrical Characteristics (Notes 6, 7) Limits in standard typeface are for T_J = +25˚C. Limits in **boldface** type apply over the full operating junction temperature range (−40˚C ≤ = T_J ≤ +125˚C). Unless otherwise noted: specifications apply to the LM3520. V_{IN} = 3.6V, V(En) > 1.0V, C_{IN} = 10 µF (Note 8). (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OVP	Output Over-Voltage Protection (Main & Sub Displays)	ON Threshold	**22.2**	23.2	**24.2**	V
		OFF Threshold	**21.5**	22.5	**23.5**	
UVP	Input Under-Voltage Protection	ON Threshold	**2.3**	2.4	**2.5**	V
		OFF Threshold	**2.35**	2.45	**2.55**	
$I_{Vout_main_leak}$	V_{OUT} Leakage Current	V_{OUT} = V_{IN}, MAIN_EN = SUB_EN = 0V		0.1		nA
$I_{Vout_main_bias}$	V_{OUT} Bias Current at No Load	V_{OUT} = 20V, SUB_EN = 0		60	**150**	µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: Enable signal must not be higher than Input voltage.

Note 3: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 4: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Note 5: Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 101.6mm x 76.2mm x 1.6mm. Thickness of the copper layers are 2oz/1oz/1oz/2oz. The middle layer of the board is 60mm x 60mm. Ambient temperature in simulation is 22˚C, still air.

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Note 6: All voltage is with respect toGND.

Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 8: C_{IN} and C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

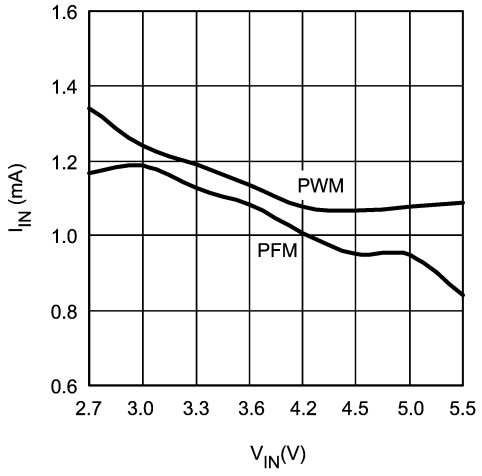
Note 9: Feedback current flows out of the Sub_ FB pin.

Note 10: Current flows into the pin.

Typical Performance Characteristics

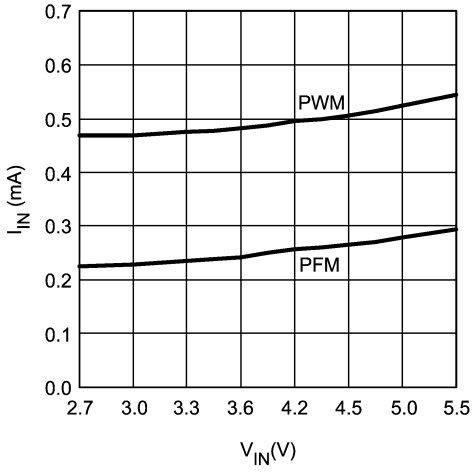
Typical Application circuit Figure 1, V_{IN} = 3.6V, L = 10µH, D = CMMSHI-40, C_{IN} = 10µF, C_{OUT} = 1µF , T_A = 25˚C , Unless otherwise Stated.

Switching Quiescent Current vs. Vin (Disconnected LEDs from VO_Main & Rsub1 from Vsub) Close Loop



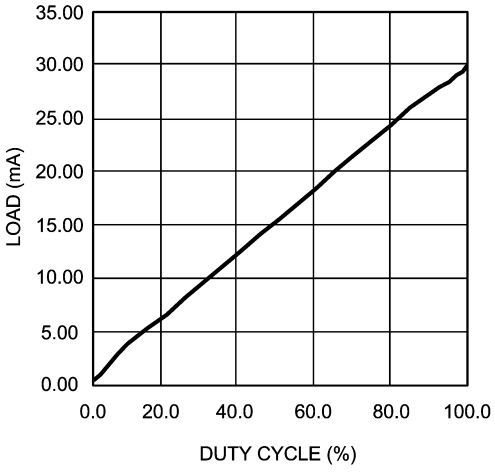
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Non-Switching Quiescent Current vs. Vin (Disconnected Rfb from LED & Rsub2 from Vsub) Close Loop



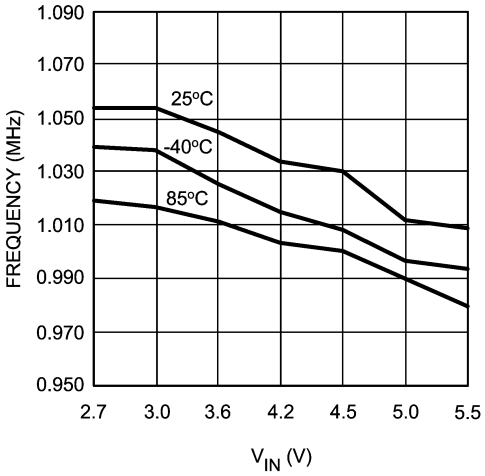
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Duty Cycle vs. Load Current (PWM at Main_EN) V_{IN} = 3.6V



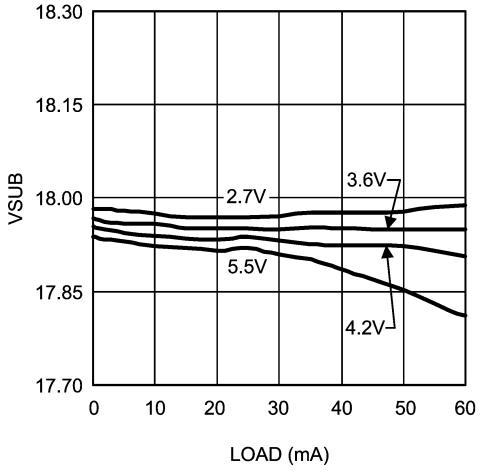
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Oscillator Frequency vs. Vin



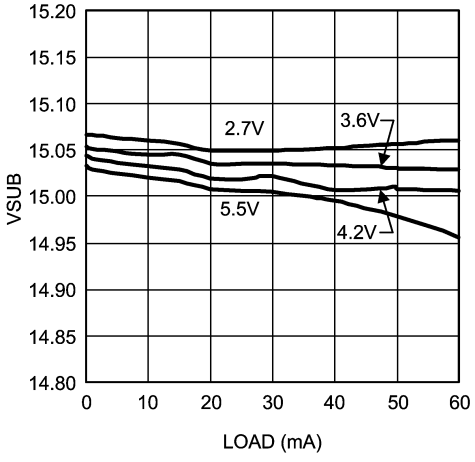
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Vsub(18V) vs. Load



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Vsub (15V) vs. Load

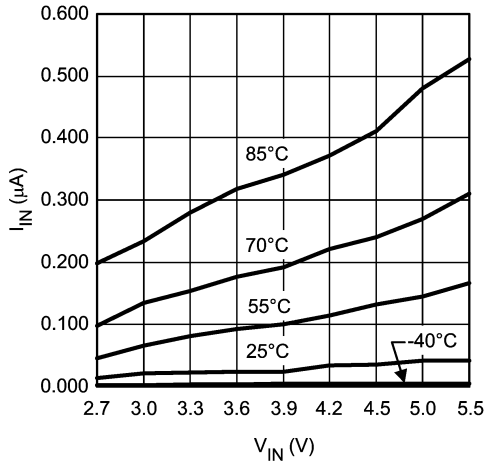


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Typical Performance Characteristics

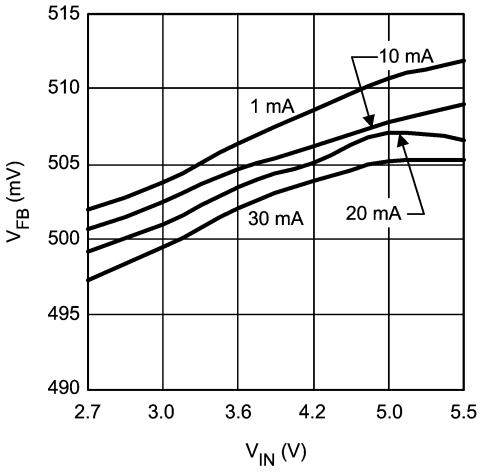
Typical Application circuit Figure 1, V_{IN} = 3.6V, L = 10µH, D = CMMSHI-40, C_{IN} = 10µF, C_{OUT} = 1µF , T_A = 25˚C , Unless otherwise Stated. (Continued)

Shutdown Current vs. Vin



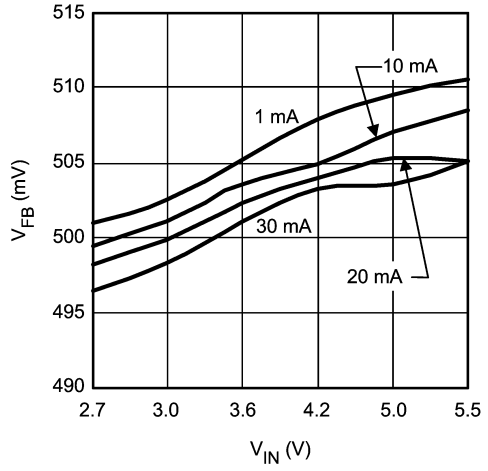
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Feedback Voltage vs. Vin (4 LEDs)



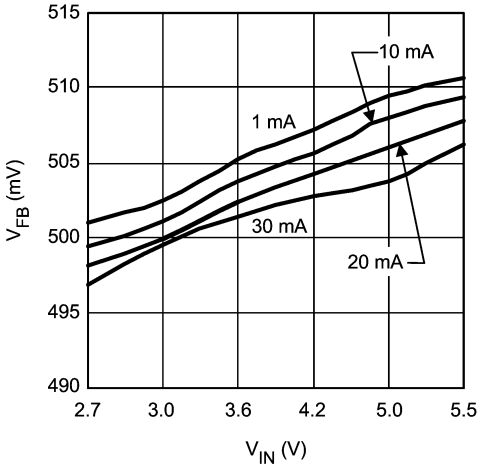
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Feedback Voltage vs. Vin (3 LEDs)



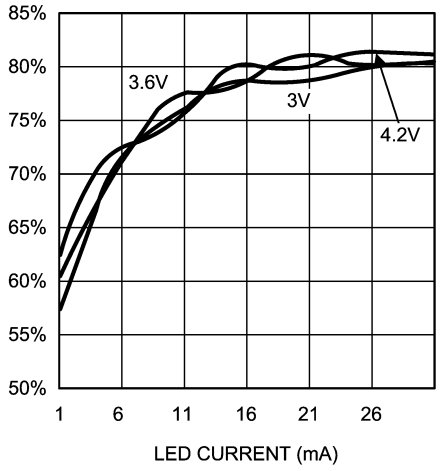
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Feedback Voltage vs. Vin (2 LEDs)



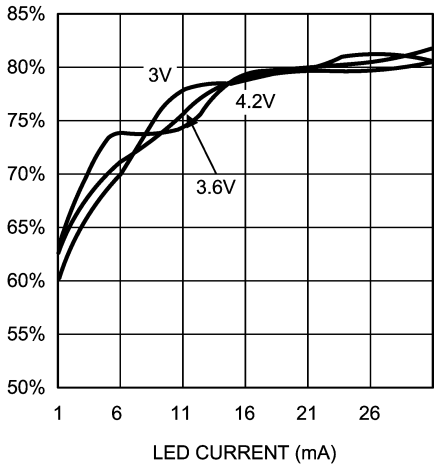
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Main Display Efficiency (4 LEDs)



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Main Display Efficiency (3 LEDs)

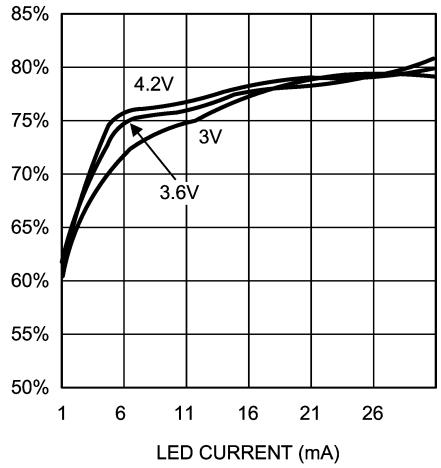


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Typical Performance Characteristics

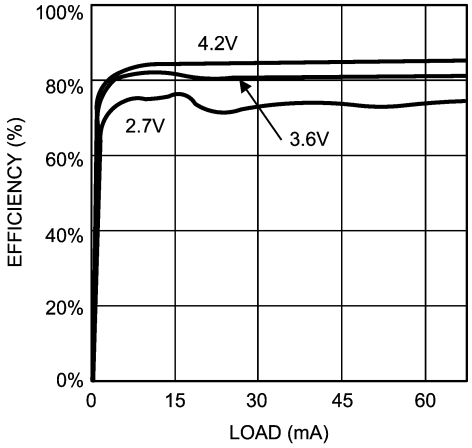
Typical Application circuit Figure 1, V_{IN} = 3.6V, L = 10µH, D = CMMSHI-40, C_{IN} = 10µF, C_{OUT} = 1µF , T_A = 25˚C , Unless otherwise Stated. (Continued)

Main Display Efficiency (2 LEDs)



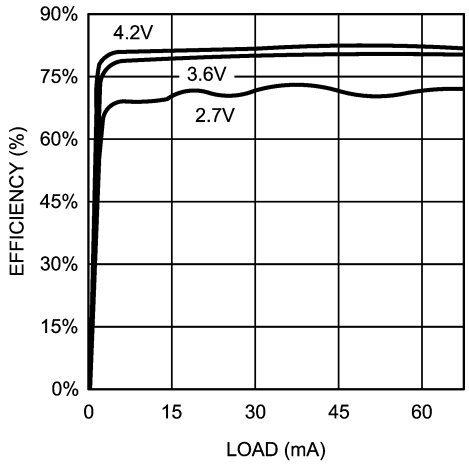
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Vsub Efficiency vs. Load (Vsub = 15V)



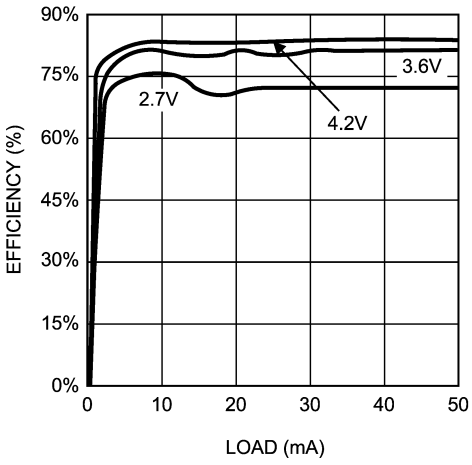
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Vsub Efficiency vs. Load (Vsub = 18V)



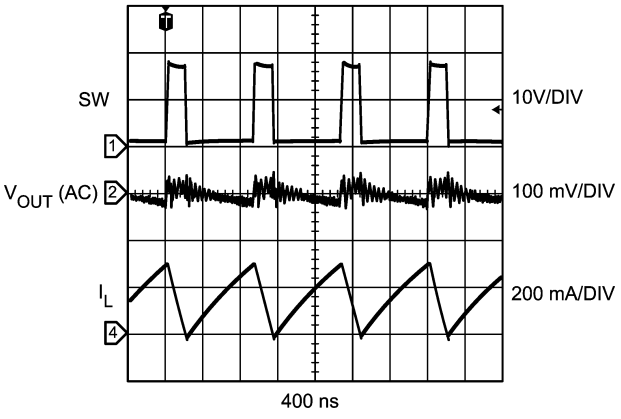
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Vsub Efficiency vs. Load (Vsub = 20V)



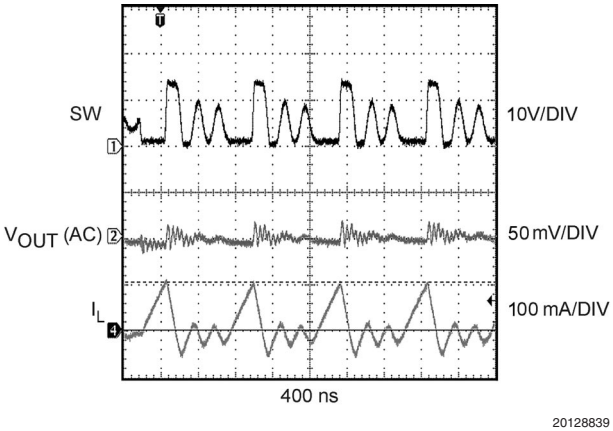
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Typical PWM Switching Waveform (Vin = 3.6V at 30mA LED Current)



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Typical PWM Switching Waveform (Vin = 3.6V at 4mA LED Current)

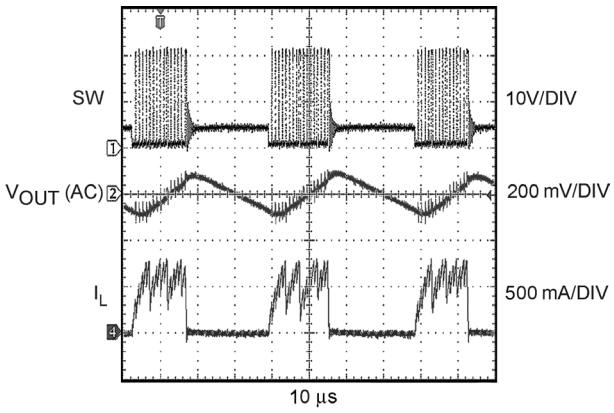


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Typical Performance Characteristics

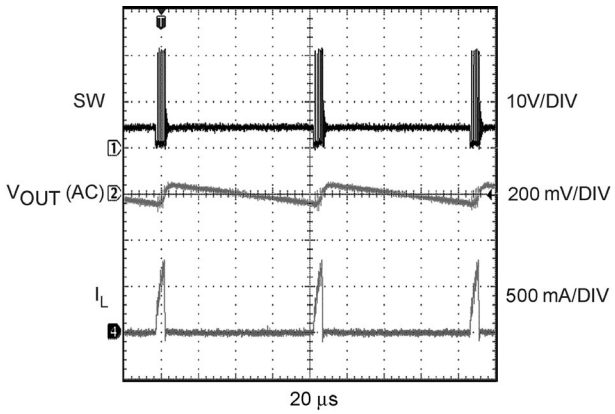
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Typical PFM Switching Waveform (Vin = 3.6V, at 30mA Load Current)



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Typical PFM Switching Waveform (Vin = 3.6V at 4mA Load Current)



20128840

Circuit Description

The LM3520 is designed for White LED & OLED backlighting in mobile phone applications. It has a main display loop which can drive up to 5 white LEDS in series and a sub display loop which is designed to drive OLED up to 20V/50 mA. The main display loop employs a fixed frequency current mode scheme to regulate the LED current. The sub display loop employs a fixed frequency gated oscillator scheme to regulate the output voltage. The device has two independent control pins to enable the Main or Sub displays. Note that both displays can not be ON at the same time.

PWM Operation

The LM3520 utilizes a synchronous Current Mode PWM control scheme to regulate the feedback voltage over all load and line conditions for the main display. The LM3520 is internally compensated preventing the need for external compensation components yielding a compact solution. The operation can best be understood referring to the functional block diagram. The LM3520 operates as follows: During the first cycle, the oscillator sets the driver logic and turns on the NMOS power device conducting current through the inductor and reverse biases the external diode isolating the output from the V_{SW} node.

The LED current is supplied by the output capacitor when the NMOS power device is active. During this cycle, the output voltage of the EAMP controls the current through the inductor. This voltage will increase for larger loads and decrease for smaller loads limiting the peak current in the inductor. The sum of the EAMP voltage and voltage ramp is compared with the sensed switch voltage. Once these voltages are equal, the PWM COMP will then reset the logic turning off the NMOS power device and forward biasing the external diode to the white LED load and flows through the diode to the white LED load and output capacitor. The inductor current recharges the output capacitor and supplies the current for the white LED branches. The oscillator then sets the driver logic again repeating the process.

PFM Operation

The LM3520 utilizes a gated oscillator control scheme for the sub-display. There is a hysteresis window to regulate the output voltage. The oscillator frequency is the same as the frequency in PWM control. The Duty cycle of the oscillator signal is always set to maximum. During the first part of each switching cycle, the internal NMOS switch is turned on until the PFM current limit is reached. When the NMOS is off, the voltage of the inductor reverses and forces current through the diode to the output capacitor. This process continues until the upper comparator hysteresis is reached at which point the NMOS is disabled until the lower comparator threshold is reached and the process repeats again.

Current Limit Protection

The LM3520 has current limiting protection to prevent excessive stress on itself and external components during overload conditions. The internal current limit comparator will disable the NMOS power device at a typical switch peak current limit of 700 mA.

Output Over-Voltage Protection

The LM3520 contains dedicated circuitry for monitoring the output voltage. In the event that the primary LED network is disconnected the output will increase and be limited to 23.2V (typ.). There is a ~1V hysteresis associated with this circuitry, which will turn the NMOS off when the output voltage is at 24.2V(max.) until the output voltage reach 22.5V(typ.) or lower. The 23.5V limit allows the use of 25V 1 µF ceramic output capacitors creating an overall small solution for white LED applications.

Under Voltage Protection

The LM3520 has an UVP comparator to turn the NMOS power device off in case the input voltage or battery voltage is too low preventing an on state of the power device conducting large amounts of current.

Reliability and Thermal Shutdown

The LM3520 has an internal thermal shutdown function to protect the die from excessive temperatures. The thermal shutdown trip point is typically 160˚C, Normal operation resumes when the temperature drops below 140˚C.

Startup

The LM3520 does not include a power on reset circuit and relies on external signal to monitor enable signal. In the event of under voltage condition, the device enable pin must be brought low until the input voltage is above the minimum guarantee voltage (2.7V).

Application Information

SETTING LED CURRENT

The White LED current is set using the following equation:

For main display:

$$I_{LED} = \frac{(V_{MAIN_FB} - V_{MAIN_RTN})}{R_{FB}} \qquad (1)$$

(1)

PWM CONTROL

The LED current can be controlled using a PWM signal on the enable pin with frequencies in the range of 100 Hz to 1 kHz. LM3520 LED current can be controlled with PWM signal frequencies above 1 kHz but LED current is not linearly porportional to the duty cycle. The maximum LED current would be achieved using the equation above with 100% duty cycle, ie. The enable pin is always high.

SETTING SUB VOLTAGE

Sub-display voltage is be set by choosing R_{SUB1} and R_{SUB2} as illustrated in *Figure 4*. V_{SUB} is calculated as follow:

$$V_{SUB} = \frac{(R_{SUB1} + R_{SUB2})}{R_{SUB2}} V_{SUB_FB} \qquad (2)$$

(2)

Application Information (Continued)

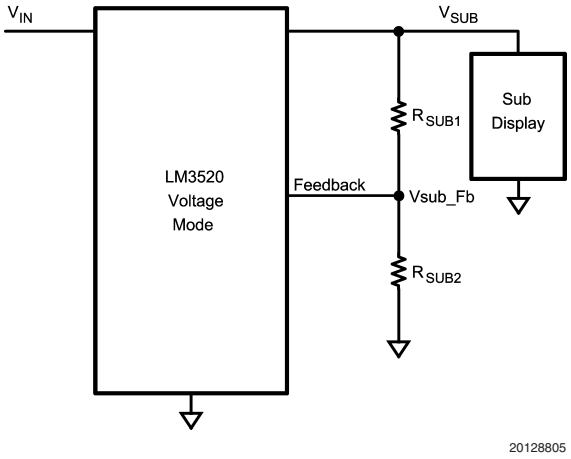


FIGURE 4.

The above equation to solve for R_{SUB1} .

$$R_{SUB1} = (V_{SUB}/V_{SUB_FB} - 1)R_{SUB2} \quad (3)$$

The LM3520 is optimized for 20V at 30 mA over the input voltage range, for higher output current up to 50mA is achieveable with a minimum input of 3.6V. If lower V_{SUB} is desired, the output current capability will be higher.

Using V_{SUB} in Current Mode Configuration

If V_{sub} is used to drive a string of LEDs, instead of using figure 3 configuration (voltage mode). The LEDs can be arranged in current mode configuration to control load current.

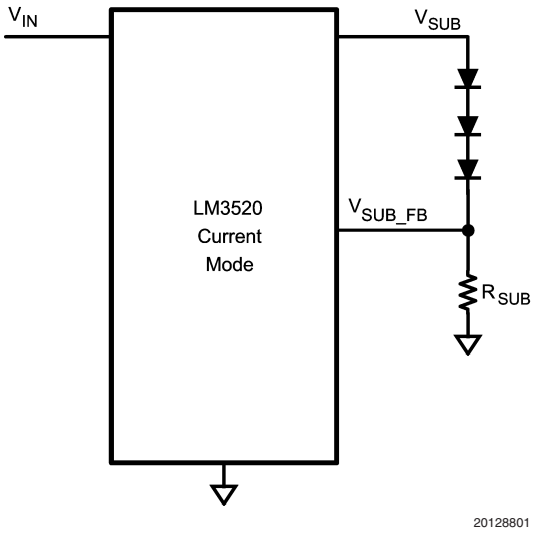


FIGURE 5.

MAIN & SUB ENABLE

The LM3520 has two independent enable pins to control the main and sub displays. A high on the Main Enable signal will enable the main display. While a high on the Sub Enable pin will enable the sub display. The PFM_EN pin must tied to SUB_EN for enabling the Sub display. Both Main & Sub enable pins should not be ON at the same time during normal operation. If for any reason, the main and Sub enable are high, the main display will enable by default and the sub display will disable by default. The following truth table summarize the logic state.

TABLE 1.

Main_EN	Sub_EN	Main	Sub
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	OFF

INDUCTOR SELECTION

The inductor used with LM3520 must have a saturation current greater than the device switch peak current limit. Choosing inductors with low DCR decreases power losses and increases efficiency. A 10 µH inductor is optimal for the applications. If a smaller inductor is used, the larger the inductor ripple current. Care must be taken to select the inductor such that the peak current rating of the inductor accounts for maximum load current for the operating condition. It is best to select an inductor with a peak current rating of the maximum switch peak current of the device. The following equation is useful for determining the inductor value for a given application condition. Where I_{OUT_MAX} = maximum output load current, V_{OUT} = output voltage, V_{IN_MIN} = minimum input voltage, V_{DIODE} = diode forward voltage, I_{Peak} = Peak Current and f_{max} = maximum switch frequency.

$$Lmin = \frac{2 \times I_{OUT_MAX} \times (V_O - V_{IN_MIN} - V_{DIODE})}{I^2_{Peak} \times f_{max}}$$

TABLE 2.

Suppliers	Website
Coilcraft	www.coilcraft.com
Cooper Bussmann	www.cooperET.com
Murata	www.murata.com

DIODE SELECTION

To maintain high efficiency, the average current rating of the schottky diode should be larger than the peak inductor current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage. Some recommended diodes are MBR0530T1 from ON semiconductor and CMMSHI-40 from Central Semiconductor.

CAPACITOR SELECTION

Choose low ESR capacitors for the output to minimize output voltage ripple. Ceramic capacitors such as X5R and X7R are recommended for use as input and output filiters. These capacitors provide an ideal balance between small size, cost, reliability and performance. Do not use Y5V ceramic capacitors as they have poor dielectric performance over temperature and poor voltage characteristic for a given value. For most applications, a 1 µF ceramic output capaci-

Application Information (Continued)

tor is sufficient for the main-display. A minimum of 4.7µF output capacitor is recommended for V_{SUB} output. Larger output capacitor can be used to reduce ripple voltage. The LM3520 has a maximum OVP of 24.2V, a 25V minimum rated capacitor voltage is recommended for the application to ensure proper biasing.

Local bypassing for the input is needed on LM3520. Multilayer ceramic capacitors with low ESR are a good choice for this as well. A 10 µF capacitor is sufficient for most applications. Using larger capacitance decreases input voltage ripple on the input. Extra attention is required if smaller case size capacitor is used in the application. Smaller case size capacitor typically has less capacitance for a given bias voltage as compared to a larger case size capacitor with the same bias voltage. Please contact the capacitor manufacturer for detail information regarding capacitance verses case size. Table 3 lists several capacitor suppliers.

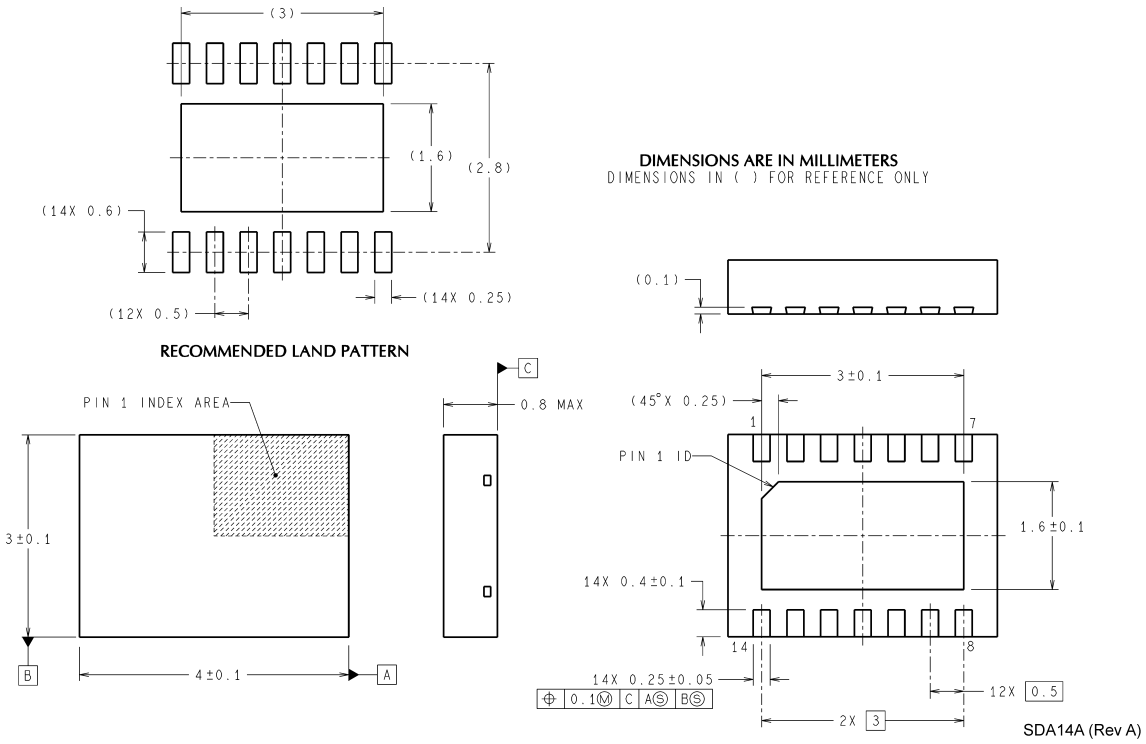
TABLE 3.

Suppliers	Website
TDK	www.tdk.com
AVX	www.avxcorp.com
Murata	www.murata.com

LAYOUT CONSIDERATIONS

As for any high frequency switcher, it is important to place the external components as close as possible to the IC to maximize device performance. Below are some layout recommendations: 1) Place input filter and output filter capacitors close to the IC to minimize copper trace resistance which will directly effect the overall ripple voltage. 2) Place the feedback network resistors in the Main and Sub display close to the IC. 3) Route noise sensitive trace away from noisy power components. 4) Connect the ground pins and filter capacitors together via a ground plane to prevent switching current circulating through the ground plane. Similarly the ground connection for the feedback network should tie directly to GND plane. If no ground plan is available, the ground connections should tie directly to the device GND pin. Additional layout consideration regarding the LLP package can be found in Application AN1187

Physical Dimensions inches (millimeters) unless otherwise noted



14–Pin LLP
NS Package Number SDA14A

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