February 2004

National Semiconductor

LM3211
Step-up PWM DC/DC Converter Integrated with 4 Buffers

General Description

The LM3211 is a compact bias solution for TFT displays. It has a current mode PWM step-up DC/DC converter with a 1.4A, 0.17Ω internal switch. Capable of generating 8V at 300mA from a Lithium Ion battery, the LM3211 is ideal for generating bias voltages for large screen LCD panels. The LM3211 can be operated at switching frequencies of 600kHz or 1.25MHz, allowing for easy filtering and low noise. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. The LM3211 uses a patented internal circuitry to limit startup inrush current of the boost switching regulator without the use of an external softstart capacitor. An external softstart pin enables the user to tailor the softstart to a specific application. The LM3211 contains 4 Gamma buffers capable of supplying 35mA source and sink. The TSSOP-20 package ensures a low profile overall solution.

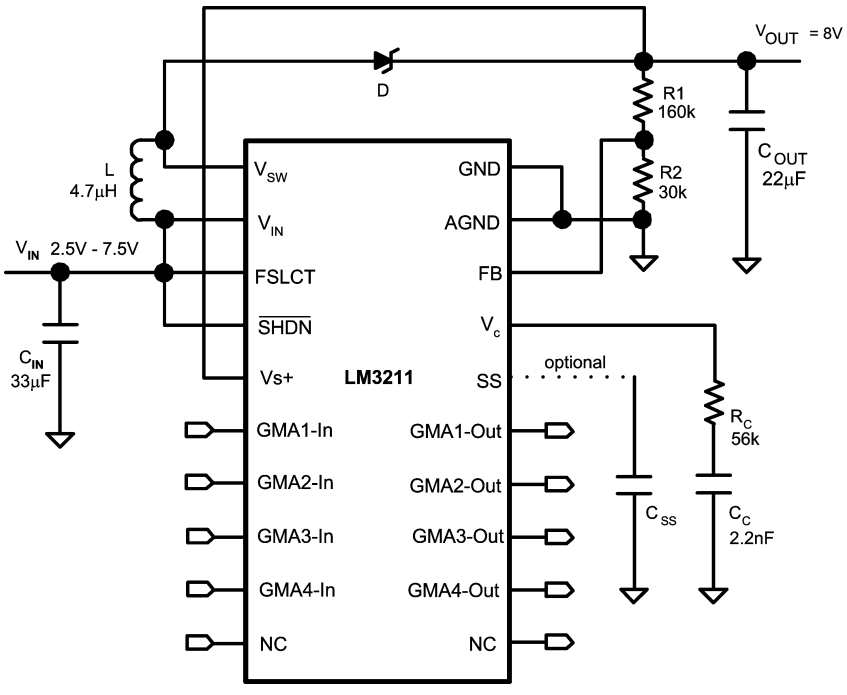
Features

- 1.4A, 0.17Ω, internal power switch
- V_{IN} operating range: 2.2V to 7.5V
- 600kHz/1.25MHz selectable frequency step-up DC/DC converter
- 20 pin TSSOP package
- Inrush current limiting circuitry
- External softstart override
- 4 Gamma buffers

Applications

- LCD Bias Supplies
- Handheld Devices
- Portable Applications
- Cellular Phones/Digital Cameras

Typical Application Circuit

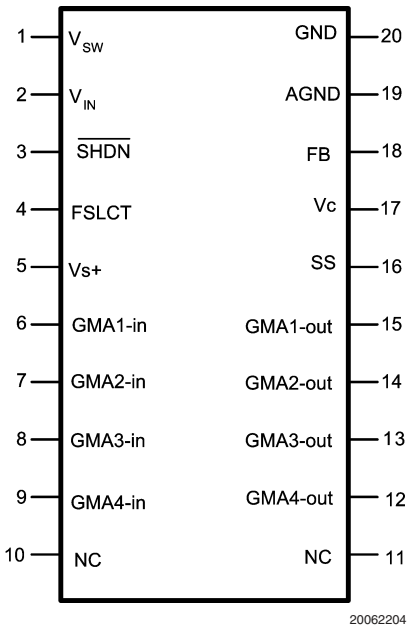


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Connection Diagram

Top View



20062204

TSSOP 20 package
T_{JMAX} = 125˚C, θ_{JA} = 120˚C/W (Note 1)

Pin Description

Pin	Name	Function
1	V_{SW}	Power switch input.
2	V_{IN}	Switching Regulator Power input.
3	$\overline{SHDN}$	Shutdown pin, active low.
4	FSLCT	Frequency Select pin. FSLCT = V_{IN} for 1.25 MHz, FSLCT = AGND or floating for 600kHz.
5	Vs+	Gamma Buffer input supply.
6	GMA1-in	Gamma Buffer input.
7	GMA2-in	Gamma Buffer input.
8	GMA3-in	Gamma Buffer input.
9	GMA4-in	Gamma Buffer input.
10	NC	No Connection, leave open.
11	NC	No Connection, leave open.
12	GMA4-out	Gamma Buffer output.
13	GMA3-out	Gamma Buffer output.
14	GMA2-out	Gamma Buffer output.
15	GMA1-out	Gamma Buffer output.
16	SS	Soft start pin.
17	V_C	Boost Compensation Network Connection.
18	FB	Output Voltage Feedback input.
19	AGND	Gamma Buffer ground, Analog ground connection for Regulator.
20	GND	Switch Power Ground.

Pin Functions

V_{SW}(Pin 1): This is the drain of the internal NMOS power switch. Minimize the metal trace area connected to this pin to minimize EMI.

V_{IN}(Pin 2): Input Supply Pin. Bypass this pin with a capacitor as close to the device as possible. The capacitor should connect between V_{IN} and GND.

$\overline{SHDN}$(Pin 3): Shutdown Pin. The shutdown pin signal is active low. A voltage of less than 0.3V disables the device. A voltage greater than 0.85V enables the device.

FSLCT(Pin 4): Frequency Select Pin. Connecting FSLCT to AGND selects a 600 kHz operating frequency for the switching regulator. Connecting FSLCT to V_{IN} selects a 1.25 MHz operating frequency. If FSLCT is left floating, the switching frequency defaults to 600 kHz.

Vs+(Pin 5): Supply pin for the four Gamma buffers. Bypass this pin with a capacitor as close to the device as possible. The capacitor should connect between Vs+ and GND.

GMA1-in(Pin 6): Gamma Buffer input pin.

GMA2-in(Pin 7): Gamma Buffer input pin.

GMA3-in(Pin 8): Gamma Buffer input pin.

GMA4-in(Pin 9): Gamma Buffer input pin.

NC(Pin 10): No Connection.

NC(Pin 11): No Connection.

GMA4-out(Pin 12): Gamma Buffer output pin.

GMA3-out(Pin13): Gamma Buffer output pin.

GMA2-out(Pin 14): Gamma Buffer output pin.

GMA1-out(Pin 15): Gamma Buffer output pin.

SS(Pin 16): Softstart pin. Connect capacitor to SS pin and AGND to slowly ramp inductor current on startup.

V_C(Pin 17): Compensation Network for Boost switching regulator. Connect resistor/capacitor network between V_C pin and AGND for boost switching regulator AC compensation.

FB(Pin 18): Feedback pin. Set the output voltage by selecting values of R1 and R2 using:

$$R1 = R2 \left(\frac{V_{OUT}}{1.265V} - 1 \right)$$

Connect the ground of the feedback network to the AGND plane, which can be tied directly to the GND pin.

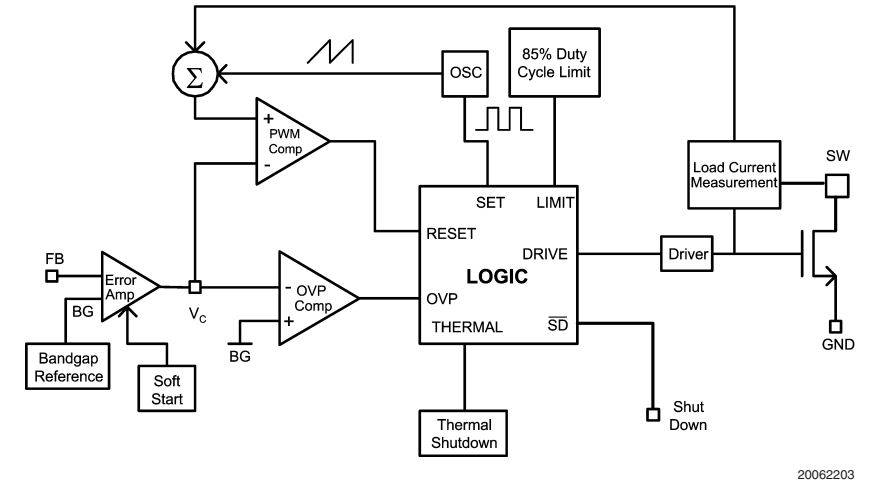
AGND(Pin 19): Analog ground pin. Ground connection for the Gamma buffers and the boost switching regulator. AGND must be tied directly to GND at the pins.

GND(Pin 20): Power ground pin. Ground connection for the NMOS power device of the boost switching regulator. GND must be tied directly to AGND at the pins.

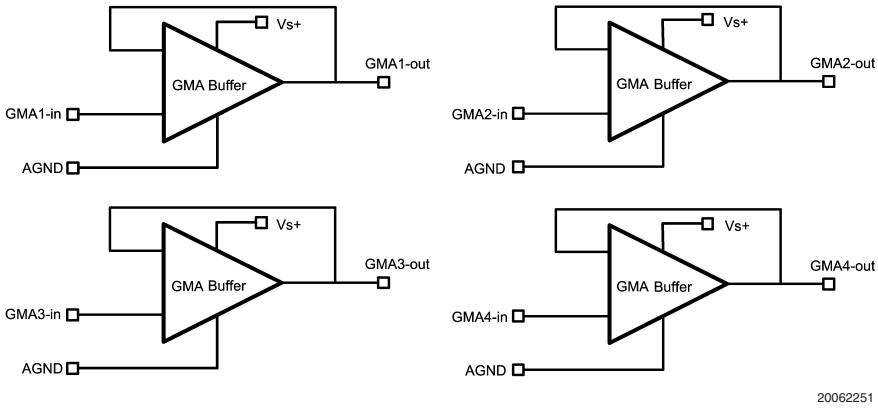
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM3211MT-ADJ	TSSOP-20	MTC20	73 Units, Rail
LM3211MTX-ADJ	TSSOP-20	MTC20	2500 Units, Tape and Reel

Block Diagrams



20062203



20062251

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}	-0.3V to 7.5V
V_{SW} Voltage	-0.3V to 18V
FB Voltage	-0.3V to 7V
V_C Voltage	0.965V to 1.565V
$\overline{SHDN}$ Voltage	-0.3V to V_{IN}
FSLCT Voltage	AGND to V_{IN}
Supply Voltage, Vs+	-0.3V to 14V
Buffer Input Voltage	Rail-to-Rail
Buffer Output Voltage	Rail-to-Rail

ESD Ratings (Note 3)

Human Body Model	2kV
Machine Model	150V

Operating Conditions

Operating Temperature	–40˚C to +125˚C
Storage Temperature	–65˚C to +150˚C
Supply Voltage, V_{IN}	2.2V to 7.5V
V_{SW} Voltage	17V
Supply Gamma Buffer, Vs+	4V to 14V

Electrical Characteristics

Specifications in standard type face are for T_J = 25˚C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = –40˚C to +125˚C). Unless otherwise specified, V_{IN} =2.2V and Vs+ = 8V.

Switching Regulator

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
I_Q	Quiescent Current	Not Switching, FSCLT = 0V		1.6	**2**	mA
		Not Switching, FSCLT = V_{IN}		1.65	**2.2**	
		Switching, FSCLT = 0V		2.5	**3**	
		Switching, FSCLT = V_{IN}		3.4	**4**	
		Shutdown mode		6	**15**	µA
V_{FB}	Feedback Voltage		**1.239**	1.265	**1.291**	V
$\%V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation			0.03	**0.05**	%/V
I_{CL}	Switch Current Limit (Note 6)	V_{IN} = 2.5V, V_{OUT} = 8V		1.4		A
R_{DSON}	Switch R_{DSON} (Note 7)	V_{IN} = 2.7V		170		mΩ
I_B	FB Pin Bias Current(Note 8)			30	**90**	nA
V_{IN}	Input Voltage Range		**2.2**		**7.5**	V
I_{SS}	Soft Start Current		**5**	11	**15**	µA
T_{SS}	Internal Soft Start Ramp Time	FSLCT = 0V		6.7	**12**	mS
g_m	Error Amp Transconductance	ΔI = 5µA	**60**	135	**250**	µmho
A_V	Error Amp Voltage Gain			135		V/V
D_{MAX}	Maximum Duty Cycle		**78**	85		%
f_S	Switching Frequency	FSLCT = 0V	**500**	600	**700**	kHz
		FSLCT = V_{IN}	**0.9**	1.25	**1.5**	MHz
I_L	Switch Leakage Current	V_{SW} = 17V		0.185	**20**	µA
$\overline{SHDN}$	$\overline{SHDN}$ Threshold	Output High	**0.85**	0.6		V
		Output Low		0.6	**0.3**	V
$I_{\overline{SHDN}}$	Shutdown Pin Current	0V ≤ $\overline{SHDN}$ ≤ V_{IN}		0.5	**1**	µA
UVP	On Threshold		**1.8**	1.9	**2**	V
	Off Threshold		**1.7**	1.8	**1.9**	V
	Hysteresis			100		mV

Electrical Characteristics

Specifications in standard type face are for T_J = 25˚C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40˚C to +125˚C). Unless otherwise specified, V_{IN} =2.2V and Vs+ = 8V.

BUFFERS

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
V_{OS}	Input offset voltage			2.5	10	mV
$\Delta V_{os}/\Delta T$	Offset Voltage Drift			8		µV/˚C
I_B	Input Bias Current			170	**800**	nA
CMVR	Input Common-mode Voltage Range		0.05		Vs+-0.05	V
Z_{IN}	Input Impedance			400		kΩ
C_{IN}	Input Capacitance			1		pF
I_{OUT}	Continuous Output Current	Vs+=8V, Source	**30**	39	**47**	mA
		Vs+=8V, Sink	**−45**	−37	**−27**	
		Vs+=12V, Source	**35**	48	**59**	
		Vs+=12V, Sink	**−54**	−44	**−32**	
V_{OUT} Swing		R_L=10k, Vo min.			**0.075**	V
		R_L=10k, Vo max.	**7.88**			
		R_L=2k, Vo min.			**0.075**	
		R_L=2k, Vo max.	**7.85**			
A_{VCL}	Voltage Gain	R_L =2 kΩ	**0.994**	0.998		V/V
		R_L=10 kΩ	**0.9985**	0.9999		
NL	Gain Linearity	R_L =2 kΩ, Buffer input=0.5 to (Vs+-0.5V)		0.01		%
Vs+	Supply Voltage		**4**		**12**	V
PSRR	Power Supply Rejection Ratio	Vs+ = 4 to 12V		90	**316**	µV/V
Is+	Supply Current/Amplifier	Vo = Vs+/2, No Load		0.75	**1.2**	mA
SR	Slew Rate	C_L =150pf		5.3		V/µs
BW	Bandwidth	-3dB,R_L =10 kΩ, C_L =100pf		3		MHz
ϕ_M	Phase Margin	C_L =100pf		78		Deg˚

Note 1: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = $(T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

Note 2: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 4: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested or guaranteed through statistical analysis. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 5: Typical numbers are at 25˚C and represent the most likely norm.

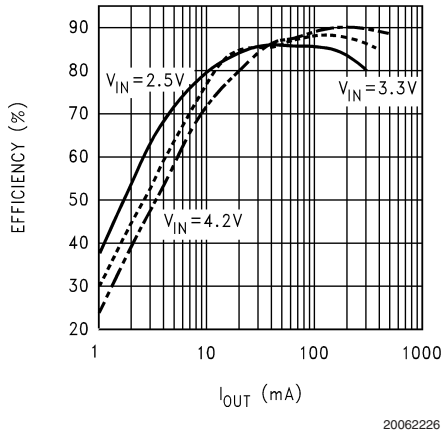
Note 6: Duty cycle affects current limit due to ramp generator. See Switch Current Limit vs. V_{IN} and Switch Current Limit vs. Temperature graphs in the *Typical Performance Characteristics* section.

Note 7: See *Typical Performance Characteristics* section for Tri-Temperature data for R_{DSON} vs. V_{IN}.

Note 8: Bias current flows into FB pin.

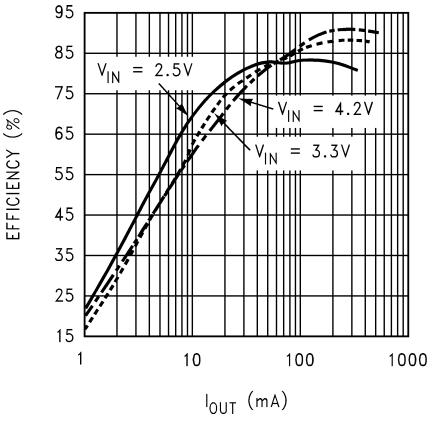
Typical Performance Characteristics

Efficiency vs. Load Current (V_{OUT} = 8V, f_S = 600 kHz)



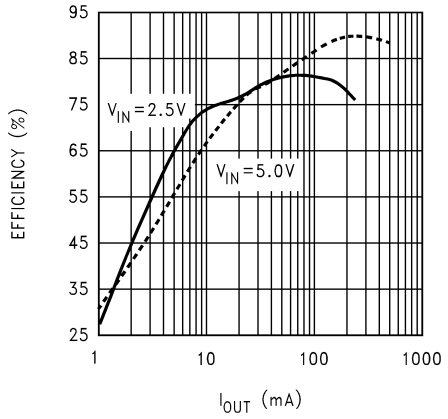
20062226

Efficiency vs. Load Current (V_{OUT} = 8V, f_S = 1.25 MHz)



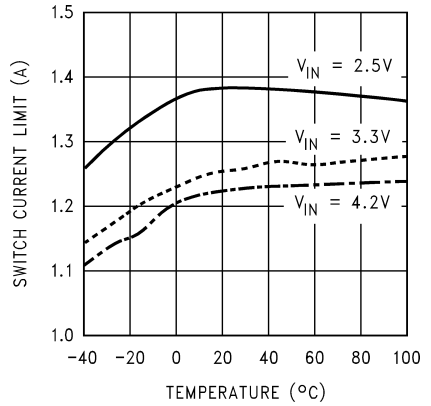
20062225

Efficiency vs. Load Current (V_{OUT} = 10V, f_S = 1.25 MHz)



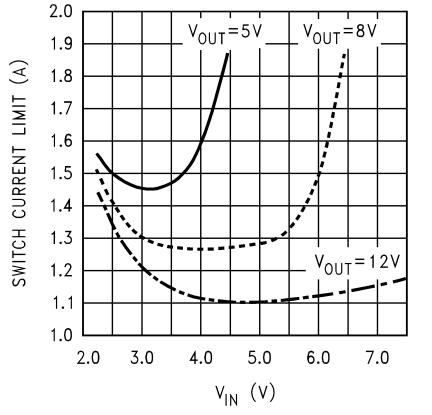
20062260

Switch Current Limit vs. Temperature (V_{OUT} = 8V)



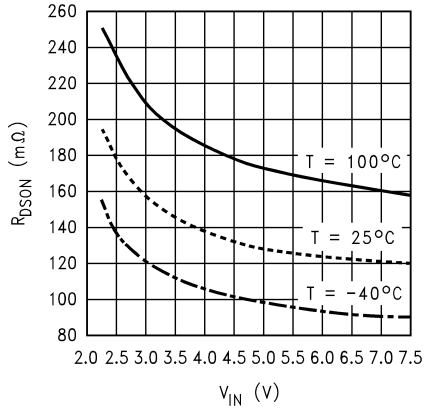
20062220

Switch Current Limit vs. V_{IN}



20062222

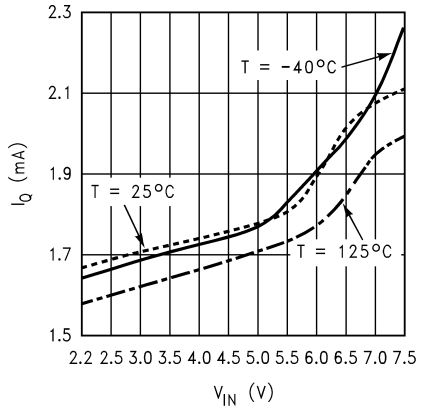
R_{DSON} vs. V_{IN} (I_{SW} = 1A)



20062227

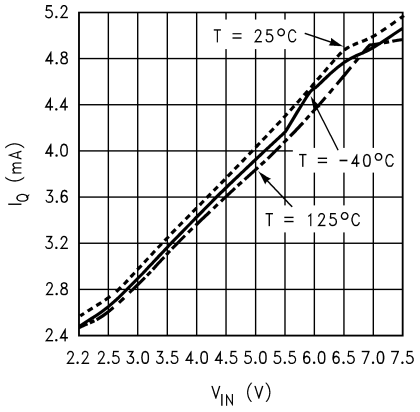
Typical Performance Characteristics (Continued)

I_Q vs. V_{IN} (600 kHz, not switching)



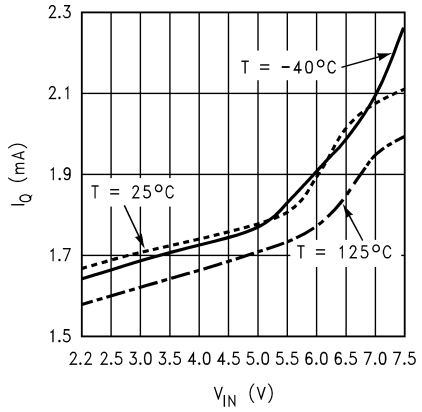
20062221

I_Q vs. V_{IN} (600 kHz, switching)



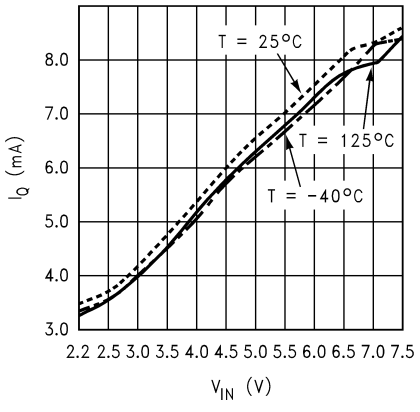
20062229

I_Q vs. V_{IN} (1.25 MHz, not switching)



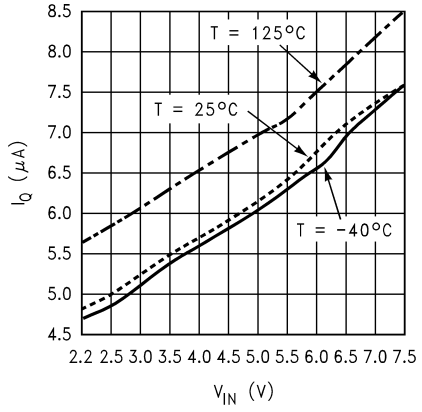
20062221

I_Q vs. V_{IN} (1.25 MHz, switching)



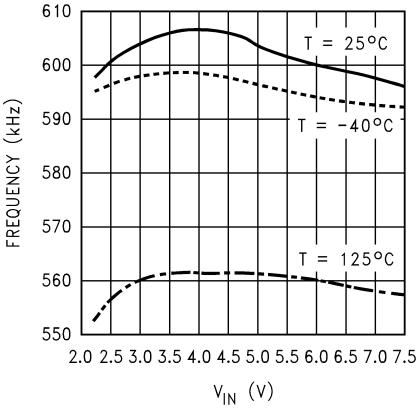
20062219

I_Q vs. V_{IN} (In shutdown)



20062218

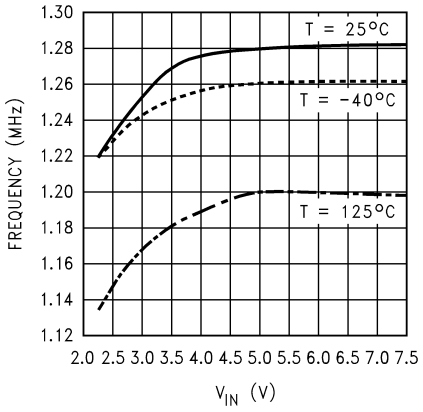
Frequency vs. V_{IN} (600 kHz)



20062223

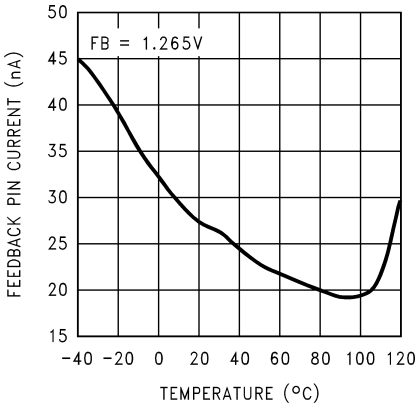
Typical Performance Characteristics (Continued)

Frequency vs. V_{IN} (1.25 MHz)



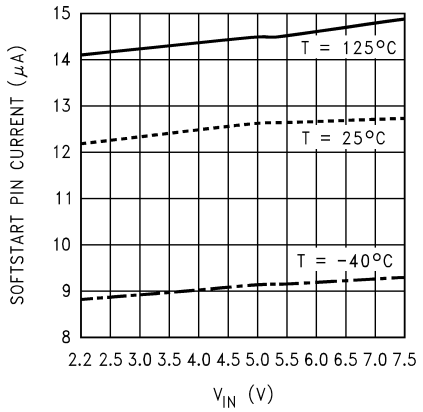
20062224

Feedback Pin Current vs. Temperature



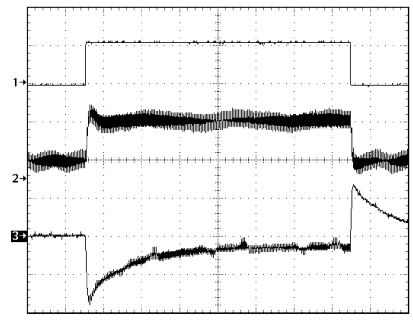
20062257

C_{SS} Pin Current vs. V_{IN}



20062258

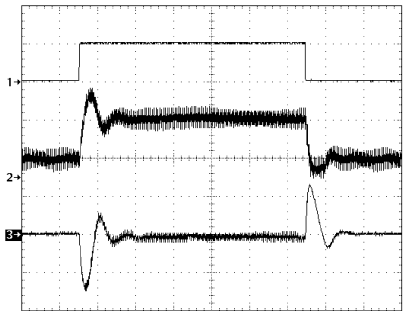
Load Transient Response



20062276

V_{OUT} = 8V, V_{IN} = 3V, F = 1.25MHz
1) Load, 80mA to 260mA to 80mA
2) I_L, 500mA/div, DC
3) V_{OUT}, 100mV/div, AC
T = 100µs/div

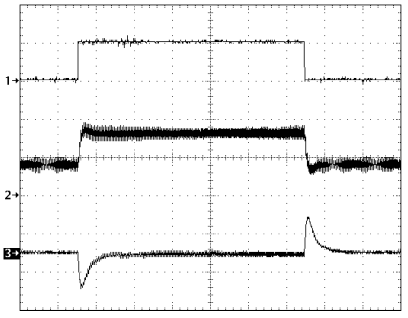
Load Transient Response



20062283

V_{OUT} = 8V, V_{IN} = 3V, F = 600kHz
1) Load, 80mA to 260mA to 80mA
2) I_L, 500mA/div, DC
3) V_{OUT}, 200mV/div, AC
T = 100µs/div

Load Transient Response

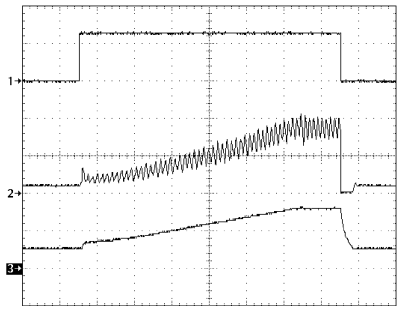


20062275

V_{OUT} = 10V, V_{IN} = 5V, F = 1.25MHz
1) Load, 195mA to 385mA to 195mA
2) I_L, 500mA/div, DC
3) V_{OUT}, 500mV/div, AC
T = 100µs/div

Typical Performance Characteristics (Continued)

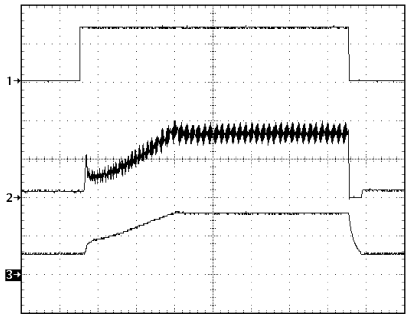
Internal Soft Start



20062279

V_{OUT} = 8V, V_{IN} = 3V, R_{LOAD} = 27Ω, C_{SS} = none, F = 600kHz
1) SHDN, 1V/div, DC
2) I_L, 500mA/div, DC
3) V_{OUT}, 5V/div, DC
T = 1ms/div

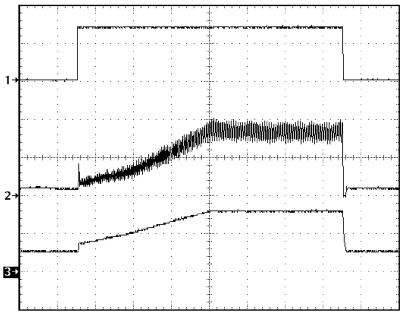
Internal Soft Start



20062277

V_{OUT} = 8V, V_{IN} = 3V, R_{LOAD} = 27Ω, C_{SS} = none, F = 1.25MHz
1) SHDN, 1V/div, DC
2) I_L, 500mA/div, DC
3) V_{OUT}, 5V/div, DC
T = 1ms/div

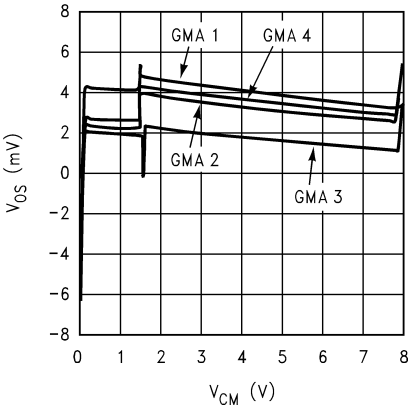
External Soft Start



20062278

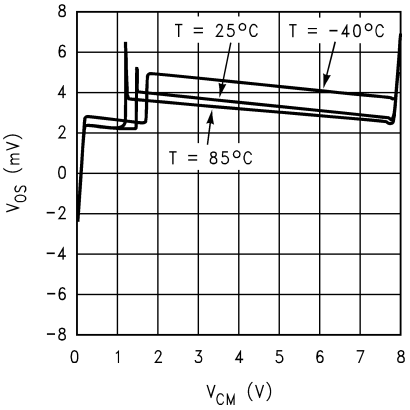
V_{OUT} = 8V, V_{IN} = 3V, R_{LOAD} = 27Ω, C_{SS} = 330nF, F = 1.25MHz
1) SHDN, 1V/div, DC
2) I_L, 500mA/div, DC
3) V_{OUT}, 5V/div, DC
T = 4ms/div

Input Offset Voltage vs. Common Mode Voltage (3 units)



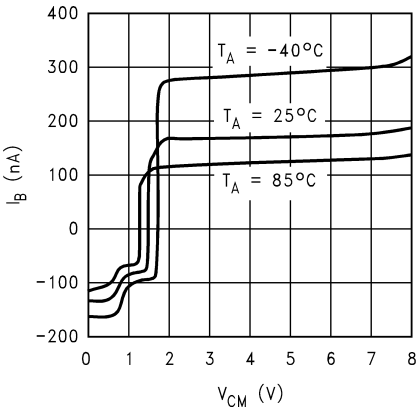
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Input Offset Voltage vs. Common Mode Voltage (Over Temperature)



20062262

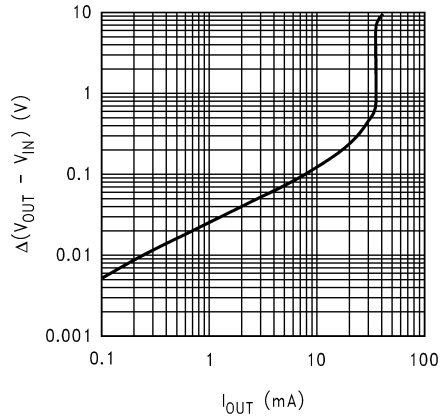
Input Bias Current vs. Common Mode Voltage



20062263

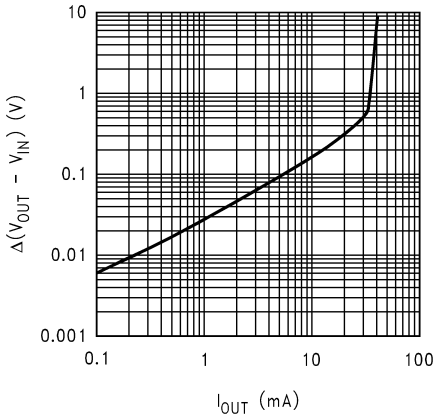
Typical Performance Characteristics (Continued)

Output Voltage vs. Output Current (sinking)



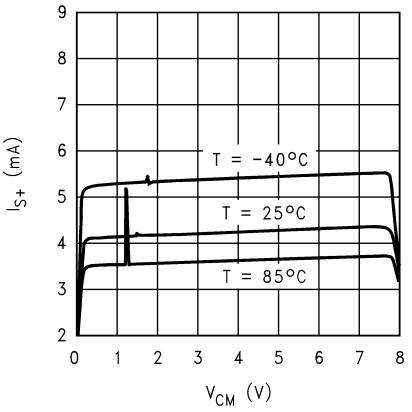
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Output Voltage vs. Output Current (sourcing)



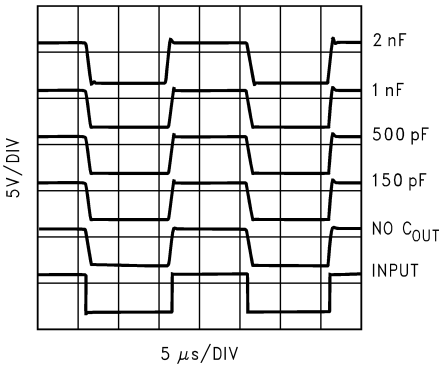
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Supply Current vs. Common Mode Voltage



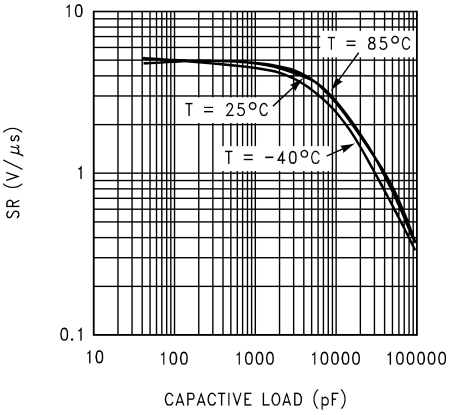
20062266

Large Signal Step Response



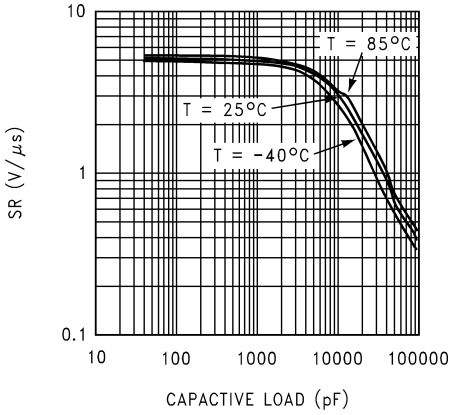
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Positive Slew Rate vs. Capacitive Load



20062269

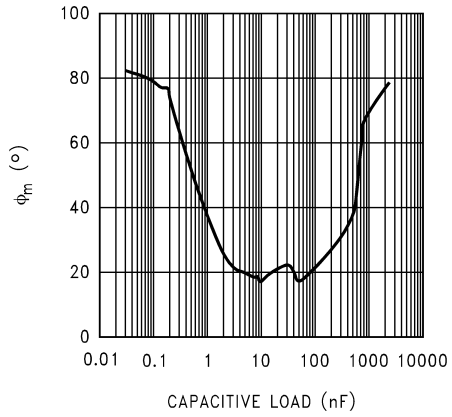
Negative Slew Rate vs. Capacitive Load



20062270

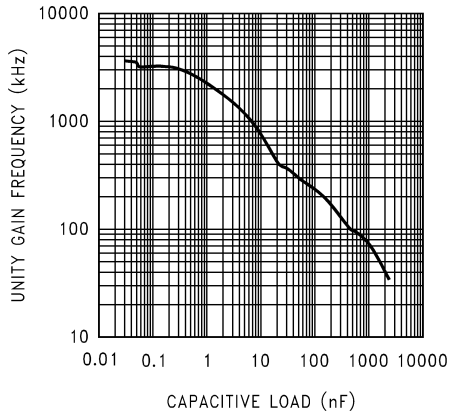
Typical Performance Characteristics (Continued)

Phase Margin vs. Capacitive Load



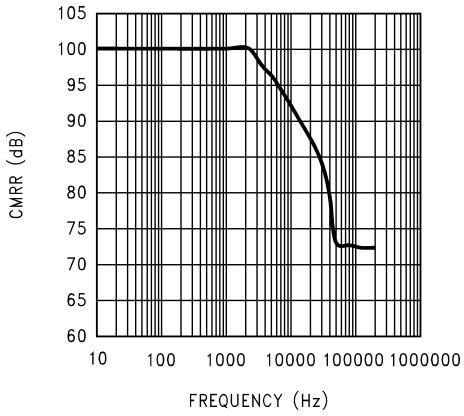
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Unity Gain Frequency vs. Capacitive Load



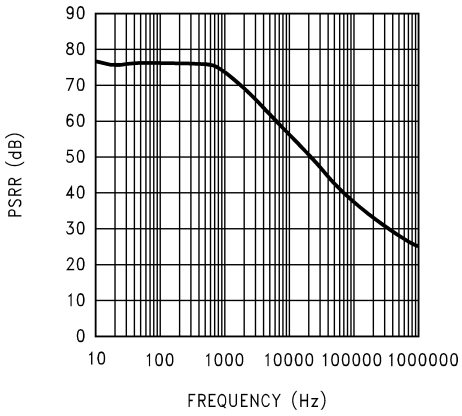
20062272

CMRR vs. Frequency



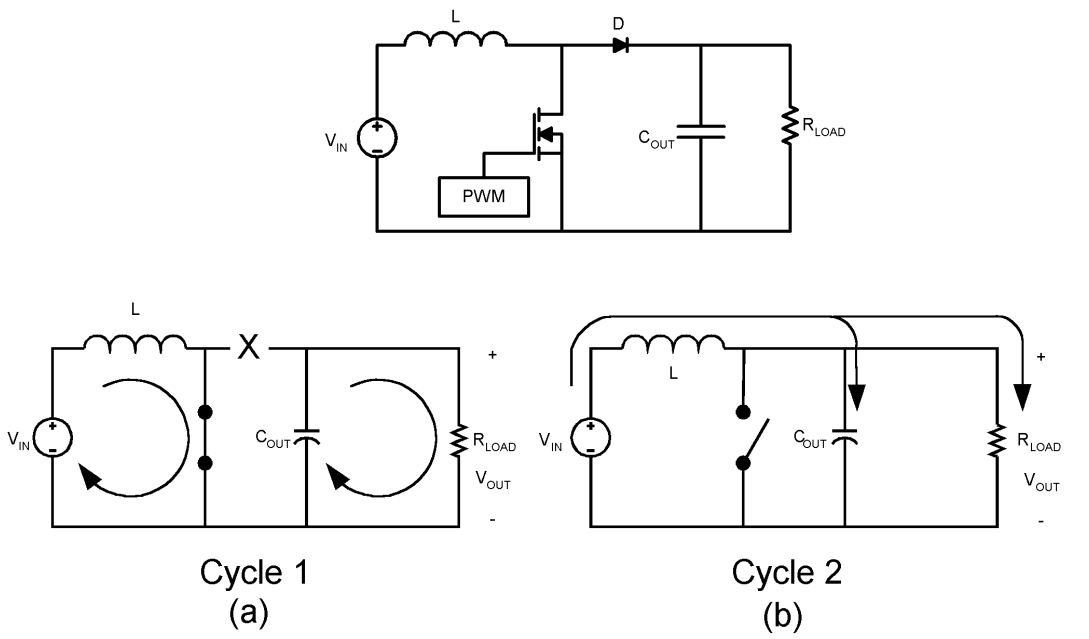
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PSRR vs. Frequency



20062274

Operation



20062202

FIGURE 1. Simplified Boost Converter Diagram
(a) First Cycle of Operation (b) Second Cycle Of Operation

CONTINUOUS CONDUCTION MODE

The LM3211 is a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in *Figure 1* (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT}.

The second cycle is shown in *Figure 1* (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1-D},\ D' = (1-D) = \frac{V_{IN}}{V_{OUT}}$$

where D is the duty cycle of the switch, D and D' will be required for design calculations

SETTING THE OUTPUT VOLTAGE

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in the typical operating circuit. The feedback pin voltage is 1.265V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$R1 = R2\left(\frac{V_{OUT}}{1.265V} - 1\right)$$

SOFT-START CAPACITOR

The LM3211 has patented internal circuitry that is used to limit the inductor inrush current on start-up. This inrush current limiting circuitry serves as a soft-start. However, many applications may require much more soft-start than what is available with the internal circuitry. The external SS pin is used to tailor the soft-start for a specific application. A 11µA current charges the external soft-start capacitor, Css. The soft-start time can be estimated as:

$$Tss = Css*0.6V/11\mu A$$

The minimum soft-start time is set by the internal soft-start circuitry, typically 7ms for 600kHz operation and approximately half that for 1.25MHz operation. Only longer soft-start times may be implemented using the SS pin and a capacitor C_{SS}. If a shorter time is designed for using the above equation, the internal soft-start circuitry will override it.

Due to the unique nature of the dual internal/external soft-start, care was taken in the design to ensure temperature stable operation. As you can see with the Iss data in the Electrical Characterisitcs table and the graph "Soft-Start Current vs. V_{IN}" in the *Typical Performance Characterisitcs* section, the soft start curent has a temperature coefficient and would lead one to believe there would be significant variation with temperature. Though the current has a temperature coefficient the actual programmed external soft start time does not show this extreme of a temperature variation. As you can see in the following transient plots:

Operation (Continued)

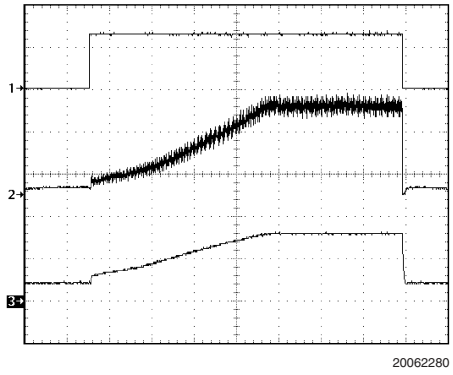
V_{OUT} = 8V, V_{IN} = 2.5V, R_L = 27Ω, C_{SS} = 330nF, T = 4ms/div, F = 1.25MHz.

Trace:

1) $\overline{SHDN}$, 1V/div, DC Coupled

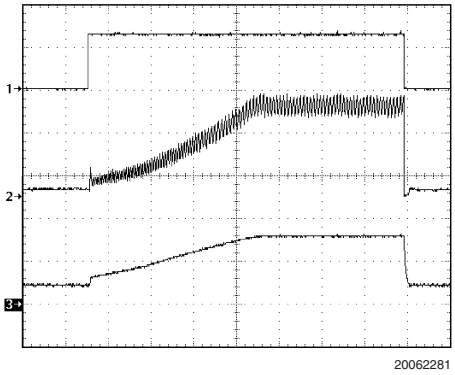
2) I_L, 0.5A/div, DC Coupled

3) V_{OUT}, 5V/div, DC Coupled



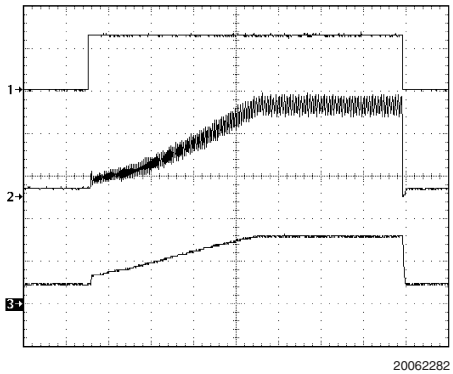
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T_A = –20˚C



20062281

T_A = 27˚C

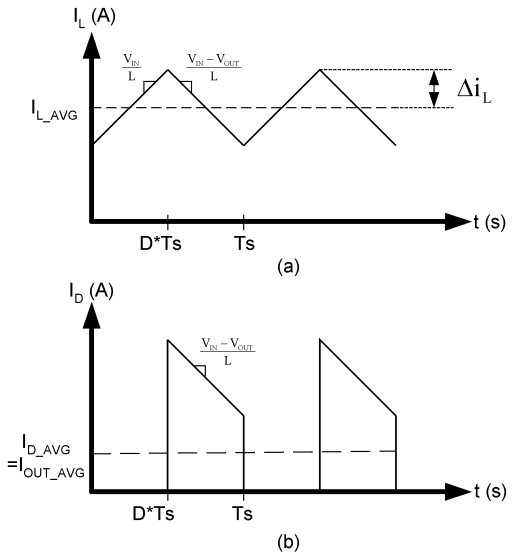


20062282

T_A = 85˚C

When programming the softstart time externally, simply use the equation given in the *Soft-Start Capacitor* section above. This equation uses the typical room temperature value of the soft start current, 11µA, to set the soft start time.

INTRODUCTION TO COMPENSATION



20062205

FIGURE 2. (a) Inductor current. (b) Diode current.

The LM3211 is a current mode PWM boost converter. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see *Figure 2* (a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%. A 10µH inductor is recommended for most 600 kHz applications, while a 4.7µH inductor may be used for most 1.25 MHz applications. If the duty cycle is approaching the maximum of 85%, it may be necessary to increase the inductance by as much as 2X. See *Inductor and Diode Selection* for more detailed inductor sizing.

The LM3211 provides a compensation pin (V_C) to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_C be used for the compensation network, as shown in the typical application circuit. For any given application, there exists a unique combination of R_C and C_C that will optimize the performance of the LM3211 circuit in terms of its transient response. The series combination of R_C and C_C introduces a pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi R_C C_C} \text{ Hz}$$

$$f_{PC} = \frac{1}{2\pi (R_C + R_O) C_C} \text{ Hz}$$

where R_O is the output impedance of the error amplifier, approximately 1MΩ. For most applications, performance can be optimized by choosing values within the range 5kΩ ≤ R_C ≤ 60kΩ (R_C can be up to 200kΩ if C_{C2} is used, see *High Output Capacitor ESR Compensation*) and 680pF ≤ C_C ≤

Operation (Continued)

4.7nF. Refer to the *Applications Information* section for recommended values for specific circuits and conditions. Refer to the *Compensation* section for other design requirement.

COMPENSATION FOR BOOST DC/DC

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation, in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

INDUCTOR AND DIODE SELECTION

Although the inductor sizes mentioned earlier are fine for most applications, a more exact value can be calculated. To ensure stability at duty cycles above 50%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

$$L > \frac{V_{IN} R_{DSON}}{0.144\ fs} \left[\frac{\left(\frac{D}{D'}\right)^2 - 1}{\left(\frac{D}{D'}\right) + 1} \right] \text{(in H)}$$

where fs is the switching frequency, D is the duty cycle, and R_{DSON} is the ON resistance of the internal switch taken from the graph "R_{DSON} vs. V_{IN}" in the *Typical Performance Characteristics* section. This equation is only good for duty cycles greater than 50% (D>0.5), for duty cycles less than 50% the recommended values may be used. The corresponding inductor current ripple as shown in *Figure 2* (a) is given by:

$$\Delta i_L = \frac{V_{IN} D}{2Lfs} \text{ (in Amps)}$$

The inductor ripple current is important for a few reasons. One reason is because the peak switch current will be the average inductor current (input current or I_{LOAD}/D') plus Δi_L. As a side note, discontinuous operation occurs when the inductor current falls to zero during a switching cycle, or Δi_L is greater than the average inductor current. Therefore, continuous conduction mode occurs when Δi_L is less than the average inductor current. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The typical current waveform for the diode in continuous conduction mode is shown in *Figure 2* (b). The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45˚) is desired for the best stability and transient response. For the purpose of stabilizing the LM3211, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin. A discussion of the right half plane zero and checking the crossover using the DC gain will follow.

INPUT AND OUTPUT CAPACITOR SELECTION

The switching action of a boost regulator causes a triangular voltage waveform at the input. A capacitor is required to reduce the input ripple and noise for proper operation of the regulator. The size used is dependant on the application and board layout. If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10µF should be used for the less stressful conditions while a 22µF to 47µF capacitor may be required for higher power and dynamic loads. Larger values and/or lower ESR may be needed if the application requires very low ripple on the input source voltage.

The choice of output capacitors is also somewhat arbitrary and depends on the design requirements for output voltage ripple. It is recommended that low ESR (Equivalent Series Resistance, denoted R_{ESR}) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the peak to peak output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \approx 2\Delta i_L R_{ESR} \text{ (in Volts)}$$

A minimum value of 10µF is recommended and may be increased to a larger value. After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi(R_{ESR} + R_L)C_{OUT}} \text{ (in Hz)}$$

$$f_{Z1} = \frac{1}{2\pi R_{ESR} C_{OUT}} \text{ (in Hz)}$$

Where R_L is the minimum load resistance corresponding to the maximum load current. The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the *High Output Capacitor ESR Compensation* section.

Operation (Continued)

RIGHT HALF PLANE ZERO

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90˚ in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

$$\text{RHPzero} = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD} L} \text{ (in Hz)}$$

where I_{LOAD} is the maximum load current.

SELECTING THE COMPENSATION COMPONENTS

The first step in selecting the compensation components R_C and C_C is to set a dominant low frequency pole in the control loop. Simply choose values for R_C and C_C within the ranges given in the *Introduction to Compensation* section to set this pole in the area of 10Hz to 500Hz. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ (in Hz)}$$

where R_O is the output impedance of the error amplifier, approximately 1MΩ. Since R_C is generally much less than R_O, it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero f_{ZC}. f_{ZC} is created to cancel out the pole created by the output capacitor, f_{P1}. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of f_{P1} over the expected loads and then set the zero f_{ZC} to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi C_C R_C} \text{ (in Hz)}$$

Now R_C can be chosen with the selected value for C_C. Check to make sure that the pole f_{PC} is still in the 10Hz to 500Hz range, change each value slightly if needed to ensure both component values are in the recommended range. After checking the design at the end of this section, these values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance circuit. For improved transient response, higher values of R_C should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimal performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

HIGH OUTPUT CAPACITOR ESR COMPENSATION

When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, C_{C2}, directly from the compensation pin V_C to ground, in parallel with the series combination of R_C and C_C. The pole should be placed at the same frequency as f_{Z1}, the ESR zero. The equation for this pole follows:

$$f_{PC2} = \frac{1}{2\pi C_{C2}(R_C // R_O)} \text{ (in Hz)}$$

To ensure this equation is valid, and that C_{C2} can be used without negatively impacting the effects of R_C and C_C, f_{PC2} must be greater than $10f_{ZC}$.

CHECKING THE DESIGN

The final step is to check the design. This is to ensure a bandwidth of ½ or less of the frequency of the RHP zero. This is done by calculating the open-loop DC gain, A_{DC}. After this value is known, you can calculate the crossover visually by placing a –20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than ½ the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved by adding C_{C2} as discussed earlier in the section. The equation for A_{DC} is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left\langle\left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right)\frac{g_m R_O D'}{R_{DSON}}\{[(\omega c \text{Leff}) // R_L] // R_L\}\right\rangle \text{ (in dB)}$$

$$\omega c \cong \frac{2fs}{nD'} \text{ (in rad/s)}$$

$$\text{Leff} = \frac{L}{(D')^2}$$

$$n = 1 + \frac{2mc}{m1} \text{ (no unit)}$$

$$mc \cong 0.072fs \text{ (in V/s)}$$

$$m1 \cong \frac{V_{IN} R_{DSON}}{L} \text{ (in V/s)}$$

where R_L is the minimum load resistance, V_{IN} is the maximum input voltage, g_m is the error amplifier transconductance found in the *Electrical Characteristics* table, and R_{DSON} is the value chosen from the graph "R_{DSON} vs. V_{IN} " in the *Typical Performance Characteristics* section.

BUFFER COMPENSATION

The Gamma buffers in the LM3211 are internally compensated. They will remain stable with no capacitive load while sourcing or sinking current. Any capacitance presented by a load in an application will only provide further stability.

Operation (Continued)

LAYOUT CONSIDERATIONS

The LM3211 uses two separate ground connections, GND for the driver and NMOS power device of the boost regulator and AGND for the sensitive analog control circuitry of the boost regulator and the V_{COM} and Gamma buffers. The AGND and GND pins should be tied directly together at the package, see *Figure 3* and *Figure 4*. The feedback, softstart, and compensation networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the AGND pin, as in *Figure 3*. If no analog ground plane is available then the ground connections of the feedback, softstart, and compensation networks must tie directly to the AGND pin, as show in *Figure 4*. Connecting these networks to the GND pin can inject noise into the system and effect performance. For 600kHz operation the FSLCT pin should be tied to an analog ground plane or directly to the AGND pin. For 1.25MHz operation the FSLCT pin should be tied to the V_{IN} pin.

The input bypass capacitor C_{IN} must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN}, close to the V_{IN} pin, to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, should also be placed close to the IC. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple and efficiency. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency.

The layout of the Gamma buffer traces is important to minimize noise injected into them. Route all input and output traces for the buffers away from the inductor and the high power switching traces used for the boost switcher. For best performance route these traces on the opposite side of the board from the high current switching traces and use a ground plane between the two sides for shielding.

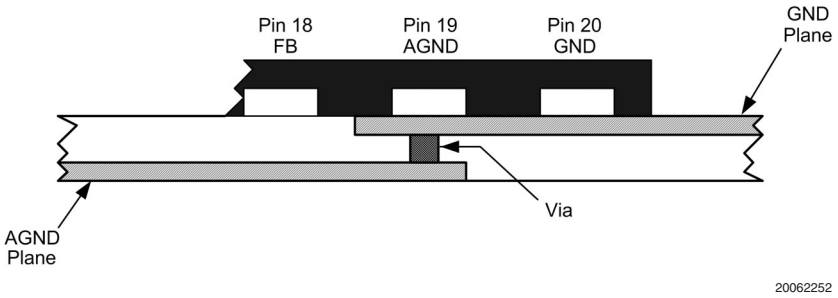


FIGURE 3. Multi-Layer Layout

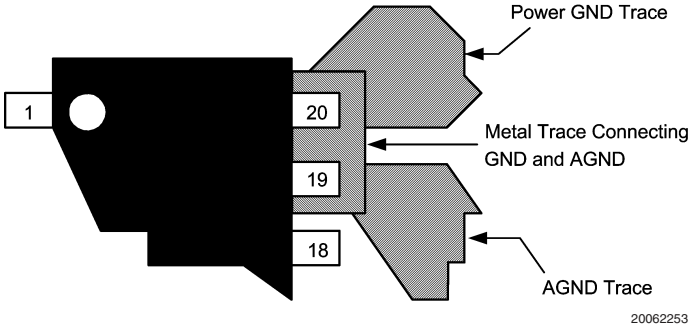


FIGURE 4. Single Layer Layout

Application Information

Some recommended Inductors (others may be used)

Manufacturer	Inductor	Contact Information
Coilcraft	DO3316 series	www.coilcraft.com
Coiltronics	DRQ73 series	www.cooperet.com
Pulse	P0751 series	www.pulseeng.com
Sumida	CDRH8D28 series	www.sumida.com

Some recommended Input and Output Capacitors (others may be used)

Manufacturer	Capacitor	Contact Information
Vishay Sprague	293D, 592D, and 595D series tantalum	www.vishay.com
Taiyo Yuden	High capacitance MLCC ceramic	www.t-yuden.com
Cornell Dubilier	ESRD seriec Polymer Aluminum Electrolytic SPV and AFK series V-chip series	www.cde.com
Panasonic	High capacitance MLCC ceramic EEJ-L series tantalum	www.panasonic.com

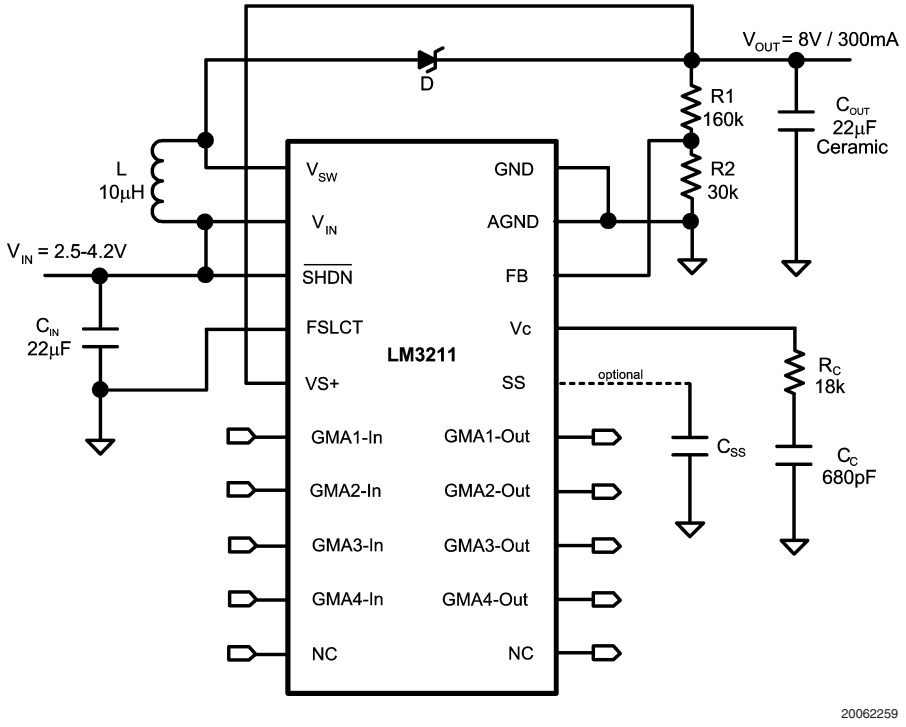


FIGURE 5. 600kHz, 8V Application

Application Information (Continued)

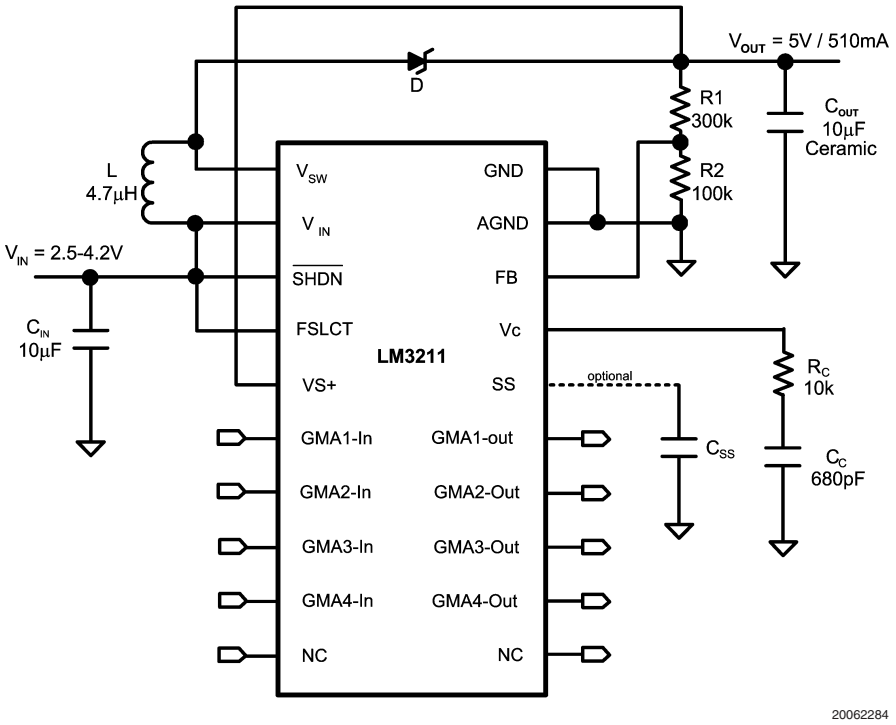


FIGURE 6. 1.25MHz, 5V Application

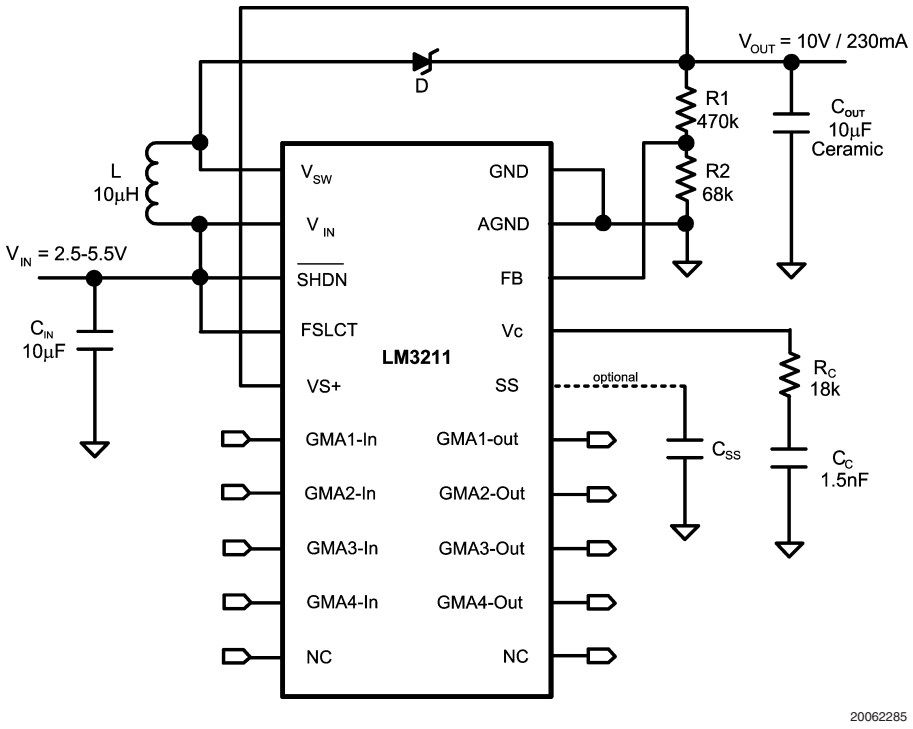


FIGURE 7. 1.25MHz, 10V Application

Application Information (Continued)

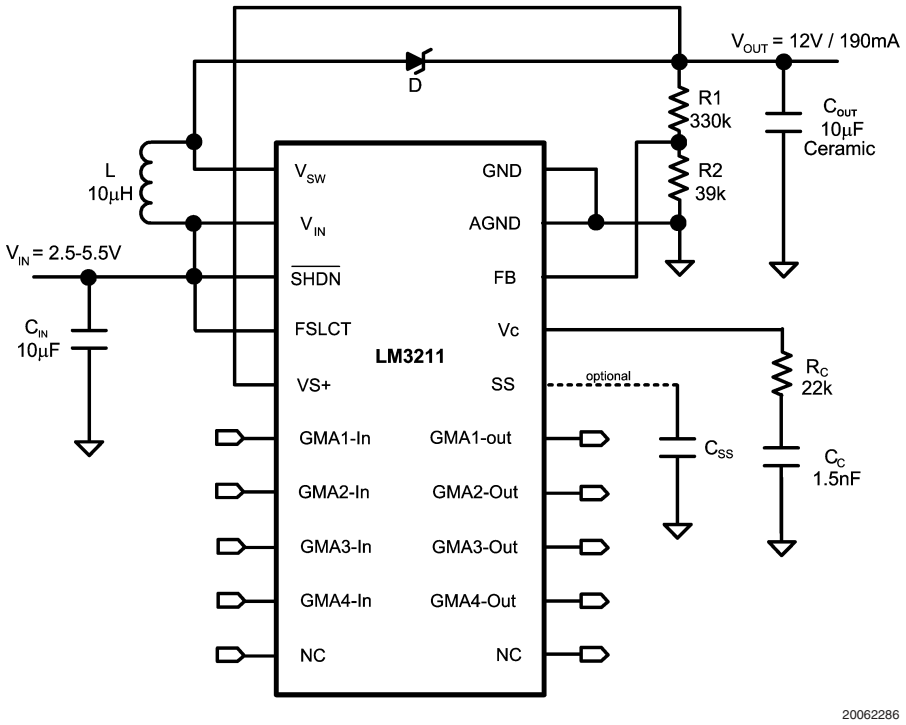
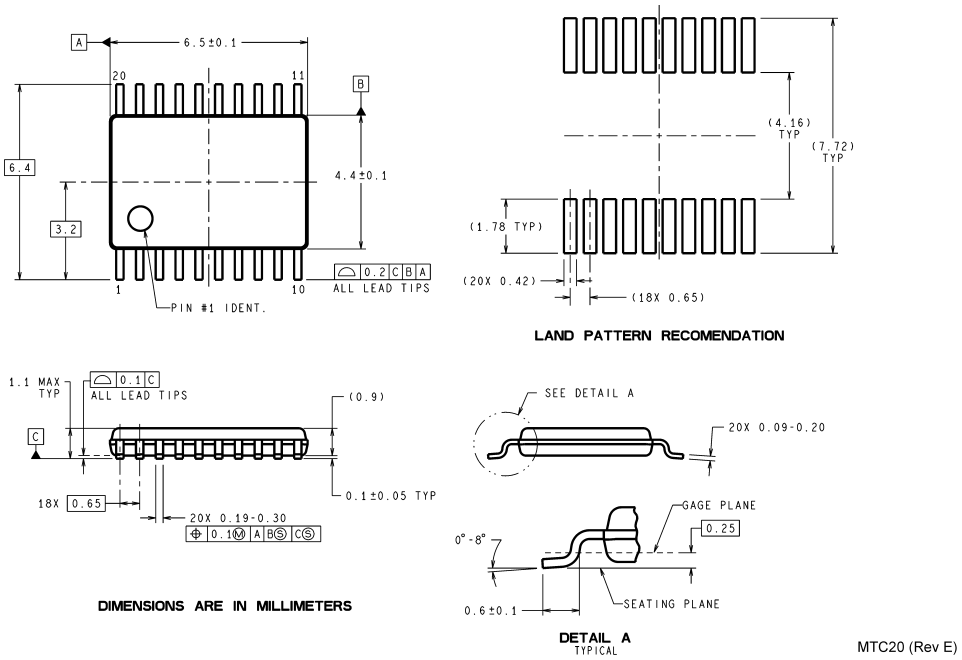


FIGURE 8. 1.25MHz, 12V Application

Physical Dimensions inches (millimeters) unless otherwise noted



MTC20 (Rev E)

TSSOP-20 Pin Package (MTC)
For Ordering, Refer to Ordering Information Table
NS Package Number MTC20

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