National Semiconductor

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# LM3000

# Dual Synchronous Emulated Current-Mode Controller

## General Description

The LM3000 is a dual output synchronous buck controller which is designed to convert input voltages ranging from 3.3V to 18.5V down to output voltages as low as 0.6V. The two outputs switch at a constant programmable frequency of 200 kHz to 1.5 MHz, with the second output 180 degrees out of phase from the first to minimize the input filter requirements. The switching frequency can also be phase locked to an external frequency. A CLKOUT provides an external clock 90 degrees out of phase with the main clock so that a second chip can be run out of phase with the main chip. The emulated current-mode control utilizes bottom side FET sensing to provide fast transient response and current limit without the need for external current sense resistors or RC networks. Separate Enable, Soft-Start and Track pins allow each output to be controlled independently to provide maximum flexibility in designing system power sequencing.

The LM3000 has a full range of protection features which include input under-voltage lock-out (UVLO), power good (PGOOD) signals for each output, over-voltage crowbar and hiccup mode during short circuit events.

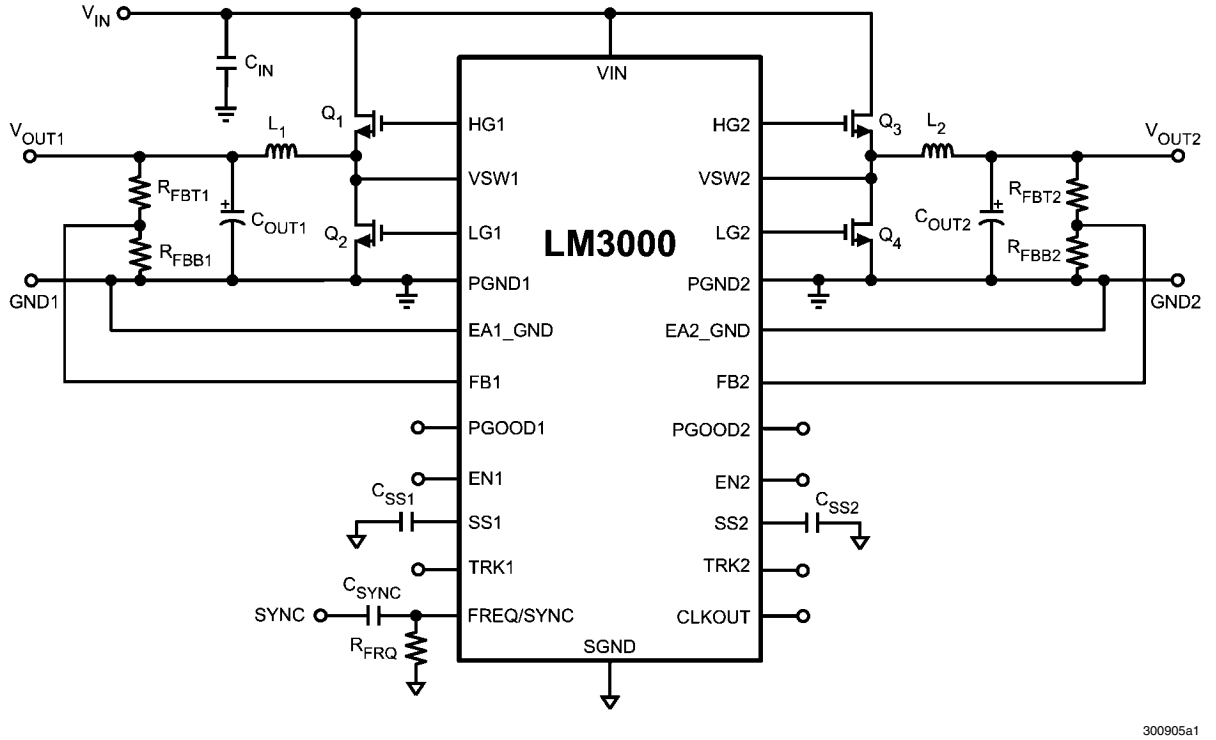
## Features

- $V_{IN}$ range from 3.3V to 18.5V
- Output voltage from 0.6V to 80% of $V_{IN}$
- Remote differential output voltage sensing
- 1% accuracy at FB pin
- Interleaved operation reduces input capacitors
- Frequency sync/adjust from 200 kHz to 1.5 MHz
- Startup with pre-bias load
- Independent power good, enable, soft-start and track
- Programmable current limit without external sense resistor
- Hiccup mode short circuit protection

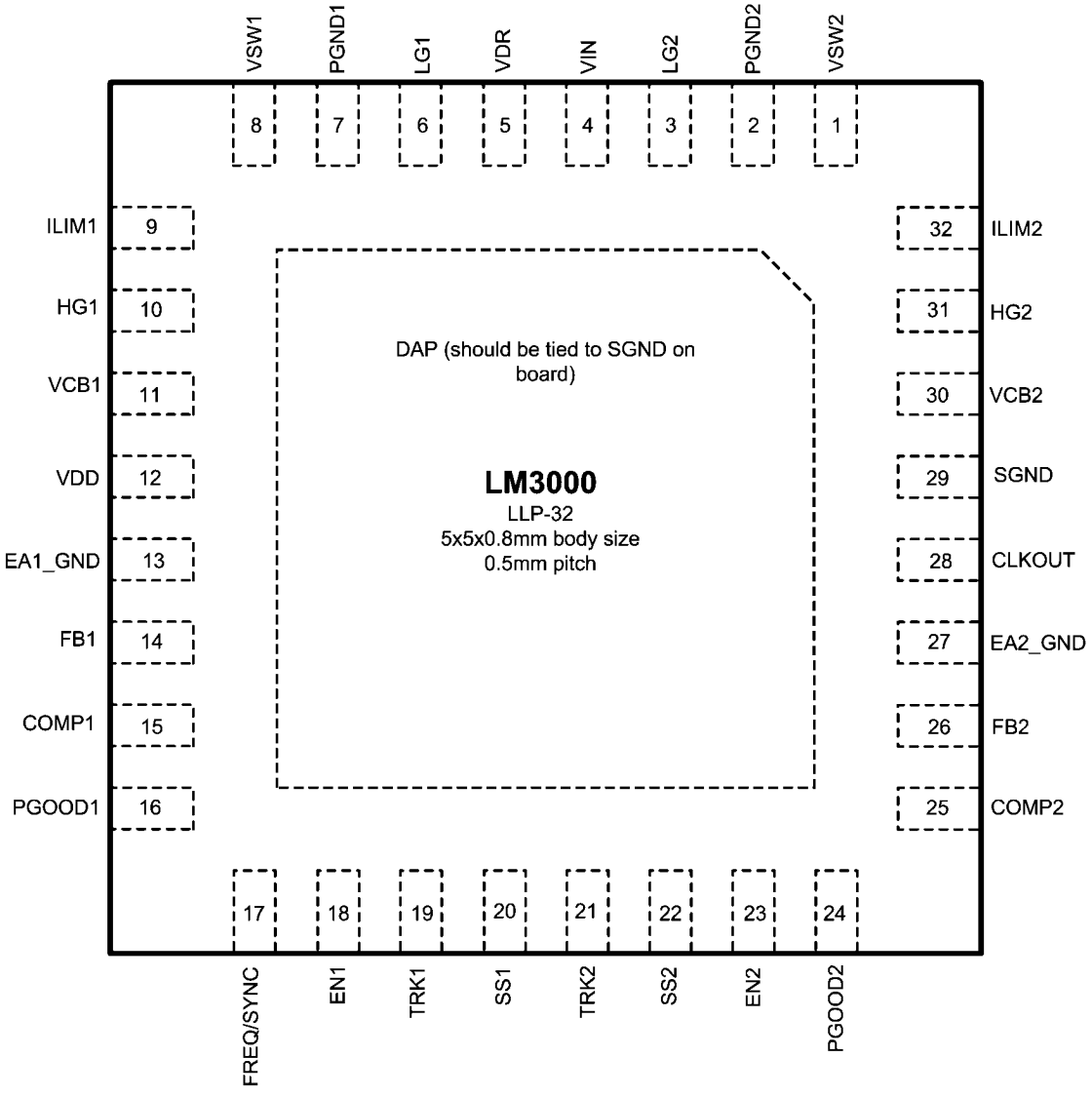
## Applications

- DC Power Distribution Systems
- Graphic Cards - GPU and Memory ICs
- FPGA, CPLD, and ASICs
- Embedded Processor
- 1.8V and 2.5V I/O Supplies
- Networking Equipment (Routers, Hubs)

## Simplified Application



## Connection Diagram




**Top View**
**32-Lead LLP**

## Ordering Information

| Order Number | Package Marking | Package Type | NSC Package Drawing | Supplied As |
|---|---|---|---|---|
| LM3000ASQ | 3000A | 32-Lead LLP | SQA32A | 1000 Units Tape and Reel |
| LM3000ASQX | 3000A | 32-Lead LLP | SQA32A | 4500 Units Tape and Reel |
| LM3000SQ | 3000 | 32-Lead LLP | SQA32A | 1000 Units Tape and Reel |
| LM3000SQX | 3000 | 32-Lead LLP | SQA32A | 4500 Units Tape and Reel |

## Pin Descriptions

| Pin # | Name | Description |
|---|---|---|
| 1 | VSW2 | Switch node sense for channel 2. |
| 2 | PGND2 | Power ground for channel 2 low-side drivers.* |
| 3 | LG2 | Channel 2 low-side gate drive for external MOSFET. |
| 4 | VIN | Chip supply voltage, input to the VDD and VDR regulators. (3.3V to 18.5V) |
| 5 | VDR | Supply for low-side gate drivers. |
| 6 | LG1 | Channel 1 low-side gate drive for external MOSFET. |
| 7 | PGND1 | Power ground for channel 1 low-side drivers.* |
| 8 | VSW1 | Switch node sense for channel 1. |
| 9 | ILIM1 | Current limit setting input for channel 1. |
| 10 | HG1 | Channel 1 high-side gate drive for external MOSFET. |
| 11 | VCB1 | Boost voltage for channel 1 high-side driver. |
| 12 | VDD | Supply for control circuitry. |
| 13 | EA1_GND | Error amplifier ground sense for channel 1.* |
| 14 | FB1 | Error amplifier input for channel 1. |
| 15 | COMP1 | Error amplifier output for channel 1. |
| 16 | PGOOD1 | Power good signal for channel 1 under-voltage and over-voltage. |
| 17 | FREQ/SYNC | Frequency set / synchronization input for internal PLL. |
| 18 | EN1 | Channel 1 enable input. Used to set the emulated current slope for channel 1. |
| 19 | TRK1 | Channel 1 track input. |
| 20 | SS1 | Channel 1 soft-start. |
| 21 | TRK2 | Channel 2 track input. |
| 22 | SS2 | Channel 2 soft-start. |
| 23 | EN2 | Channel 2 enable input. Used to set the emulated current slope for channel 2. |
| 24 | PGOOD2 | Power good signal for channel 2 under-voltage and over-voltage. |
| 25 | COMP2 | Error amplifier output for channel 2. |
| 26 | FB2 | Error amplifier input for channel 2. |
| 27 | EA2_GND | Error amplifier ground sense for channel 2.* |
| 28 | CLKOUT | Output clock. CLKOUT is shifted 90 degrees from SYNC input. |
| 29 | SGND | Local signal ground.* |
| 30 | VCB2 | Boost voltage for channel 2 high-side driver. |
| 31 | HG2 | Channel 2 high-side gate drive for external MOSFET. |
| 32 | ILIM2 | Current limit setting input for channel 2. |
|  | DAP | Exposed die attach pad. Connect the DAP directly to SGND.* |

*The LM3000 offers true remote ground sensing to achieve very tight line and load regulation. For best layout practice, the EA1_GND, and EA2_GND should be tied to the ground end of the output capacitor (or output terminal) for $V_{OUT1}$ and $V_{OUT2}$ respectively. Inside the LM3000, the two power ground nodes PGND1 and PGND2 are physically isolated from each other and also isolated from the internal signal ground SGND. In order to achieve the best cross-channel noise rejection, it is advised to keep these three grounds isolated from each other for the most part in the board layout and only tie them together at the ground terminals.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| VIN to SGND, PGND | -0.3V to 20V |
| VSW1, VSW2 to SGND, PGND | -3V to 20V |
| VDD, VDR to SGND, PGND (Note 3) | -0.3V to 5.5V |
| VCB1, VCB2 to SGND ,PGND | 24V |
| VCB1 to VSW1, VCB2 to VSW2 | 5.5V |
| FB1, FB2 to SGND, PGND | -0.3V to 3.0V |
| All other input pins to SGND, PGND (Note 4) | -0.3V to 5.5V |
| Junction Temperature ($T_{J-MAX}$) | 150°C |
| Storage Temperature Range | -65°C to +150°C |
| Maximum Lead Temperature Soldering, 5 seconds | 260°C |
| ESD Rating HBM (Note 2) | 2000V |

## Operating Ratings (Note 1)

| | |
|---|---|
| Input Voltage Range | |
| VDD = VDR = VIN (Note 3) | 3.3V to 5.5V |
| VIN | 3.3V to 18.5V |
| Junction Temperature ($T_J$) Range | –40°C to +125°C |

## Electrical Characteristics

Limits in standard type are for $T_J$ = 25°C only; limits in **boldface type** apply over the junction temperature ($T_J$) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise noted, VIN = 12.0V, $I_{EN1}$ = $I_{EN2}$ = 40 µA.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{FB}$ | FB Pin Voltage FB1, FB2 (LM3000A) | -20°C to +85°C | 0.594 | 0.6 | 0.606 | V |
| | | | **0.591** | 0.6 | **0.609** | |
| $V_{FB}$ | FB Pin Voltage FB1, FB2 (LM3000) | -20°C to +85°C | 0.591 | 0.6 | 0.609 | V |
| | | | **0.588** | 0.6 | **0.612** | |
| $\Delta V_{FB}/V_{FB}$ | Line Regulation VDD = VIN = VDR | 3.3V < VIN < 5.5, COMP = 1.5V | | 0.15 | | % |
| | Line Regulation VIN > 6V | 6V < VIN < 18.5V, COMP = 1.5V | | 0.3 | | % |
| | Load Regulation | VIN = 12.0V, 1.0V < COMP < 1.4V | | 0.1 | | % |
| $I_q$ | VIN Operating Current | | | 5 | | mA |
| $I_{SD}$ | VIN Shutdown Current | $I_{EN1}$ , $I_{EN2}$ < 5 µA | | 50 | | µA |
| $I_{EN}$ | EN Input Threshold Current | $I_{EN}$ Rising | | 15 | **35** | µA |
| | | Hysteresis | | 10 | | |
| $I_{LIM}$ | Source Current ILIM1, ILIM2 | $V_{ILIM1}$, $V_{ILIM2}$ = 0V | 17 | 20 | 23 | µA |
| $I_{SS}$ | Soft-Start Pull-Up Current | $V_{SS}$ = 0.5V | 5.5 | 8.5 | 11.5 | µA |
| $V_{HICCUP}$ | COMP Pin Hiccup Thresholds | COMP Threshold High | | 2.85 | | V |
| | | Hysteresis | | 50 | | mV |
| $t_{DELAY}$ | Hiccup Delay | | | 16 | | Cycles |
| $t_{COOL}$ | Cool-Down Time Until Restart | | | 4096 | | Cycles |
| $V_{OVP}$ | Over-Voltage Protection Threshold | As a % of Nominal Output Voltage | **110** | 115 | **120** | % |
| | | Hysteresis | | 3 | | |
| $V_{UVP}$ | Under-Voltage Protection Threshold | As a % of REF1, REF2 (see Block Diagram) | | 85 | | % |
| **GATE DRIVE** | | | | | | |
| $I_{CB}$ | VCB Pin Leakage Current | VCB - VSW = 5.5V | | 250 | | nA |
| $R_{DS1}$ | Top FET Drive Pull-Up On-Resistance | VCB - VSW = 4.5V, VCB - HG = 100 mV | | 3 | | Ω |
| $R_{DS2}$ | Top FET Drive Pull-Down On-Resistance | VCB - VSW = 4.5V, HG - VSW = 100 mV | | 2 | | Ω |
| $R_{DS3}$ | Bottom FET Drive Pull-Up On-Resistance | VDR - PGND = 5V, VDR - LG = 100 mV | | 2 | | Ω |
| $R_{DS4}$ | Bottom FET Drive Pull-Down On-Resistance | VDR - PGND = 5V, LG - PGND = 100 mV | | 1 | | Ω |

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | |
| $f_{SW}$ | Switching Frequency | $R_{FRQ}$ = 100 kΩ | | 230 | | kHz |
| | | $R_{FRQ}$ = 42.2 kΩ | **425** | 500 | **575** | kHz |
| | | $R_{FRQ}$ = 10 kΩ | | 1550 | | kHz |
| $V_{SYNC}$ | Threshold for Synchronization at the FREQ/SYNC Pin | Rising | 2.2 | | | V |
| | | Falling | | | 0.6 | |
| $f_{SYNC}$ | SYNC Range | | 200 | | 1500 | kHz |
| $t_{SYNC}$ | SYNC Pulse Width | | 100 | | | ns |
| $t_{SYNC-TRS}$ | SYNC Rise/Fall Time | | | | 10 | ns |
| $D_{MAX}$ | Maximum Duty cycle | | | 85 | | % |
| **ERROR AMPLIFIER** | | | | | | |
| $I_{FB}$ | FB Pin Bias Current | FB = 0.6V | | 20 | | nA |
| $I_{SOURCE}$ | COMP Pin Source Current | FB = 0.5V, COMP = 1.0V | | 80 | | µA |
| $I_{SINK}$ | COMP Pin Sink Current | FB = 0.7V, COMP = 0.7V | | 80 | | µA |
| $V_{COMP-HI}$ | COMP Pin Voltage High Clamp | | 2.80 | 3.0 | 3.2 | V |
| $V_{COMP-LO}$ | COMP Pin Voltage Low Clamp | | | 0.48 | | V |
| $V_{OS-TRK}$ | Offset Using TRK Pin | TRK = 0.45V | -9.0 | 0 | 9.0 | mV |
| $g_m$ | Transconductance | | | 1400 | | µS |
| $f_{BW}$ | Unity Gain Bandwidth Frequency | | | 10 | | MHz |
| **INTERNAL VOLTAGE REGULATOR** | | | | | | |
| $V_{VDD}$ | Internal Core Regulator Voltage | No External Load | | 5.15 | | V |
| $V_{VDD-ON}$ | UVLO Thresholds | VDD Rising | | 2.12 | | V |
| | | Hysteresis | | 0.14 | | |
| $V_{VDD-DO}$ | Internal Core Regulator Dropout Voltage | No External Load | | 1.1 | | V |
| $I_{VDD-ILIM}$ | Internal Core Regulator Current Limit | VDD Short to Ground | | 80 | | mA |
| $V_{VDR}$ | Regulator for External MOSFET Drivers | $I_{VDR}$ = 100 mA | | 5.2 | | V |
| $V_{VDR-DO}$ | Driver Regulator Dropout Voltage | $I_{VDR}$ = 100 mA | | 1.0 | | V |
| $I_{VDR-ILIM}$ | Driver Regulator Current Limit | VDR Short to Ground | | 450 | | mA |
| **PGOOD OUTPUT** | | | | | | |
| $R_{PG-ON}$ | PGOOD On-Resistance | FB1 = FB2 = 0.47V | | 250 | | Ω |
| $I_{OH}$ | PGOOD High Leakage Current | $V_{PGOOD}$ = 5V | | 100 | | nA |
| **THERMAL RESISTANCE** | | | | | | |
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance | LLP-32 Package (Note 5) | | 26.4 | | °C/W |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For guaranteed specifications and conditions, see the Electrical Characteristics table.

**Note 2:** Human Body Model (HBM) is 100 pF capacitor discharged through a 1.5k resistor into each pin. Applicable standard is JESD22-A114C.

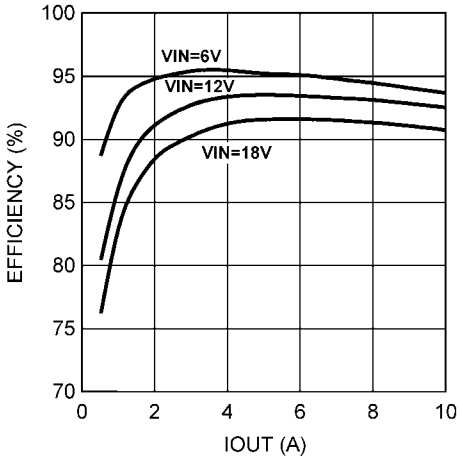
**Note 3:** VDD and VDR are outputs of the internal linear regulator. Under normal operating conditions where VIN > 5.5V, they must not be tied to any external voltage source. In an application where VIN is between 3.3V to 5.5V, it is recommended to tie the VDD, VDR and VIN pins together, especially when VIN may drop below 4.5V. In order to have better noise rejection under these conditions, a 10Ω, 1µF input filter may be used for the VDD pin.

**Note 4:** HG1, HG2, LG1, LG2 and CLKOUT are all output pins and should not be tied to any external power supply. COMP1 and COMP2 are also outputs and should not be tied to any lower output impedance power source. PGOOD1 and PGOOD2 are open drain outputs, with a pull-down resistance of about 250Ω. Each of them may be tied to an external voltage source less than 5.5V through an external resister greater than 3kΩ, although 10kΩ and above are preferred to reduce the necessary signal ground current.

**Note 5:** Tested on a four layer JEDEC board. Four vias provided under the exposed pad. See JEDEC standards JESD51-5 and JESD51-7.

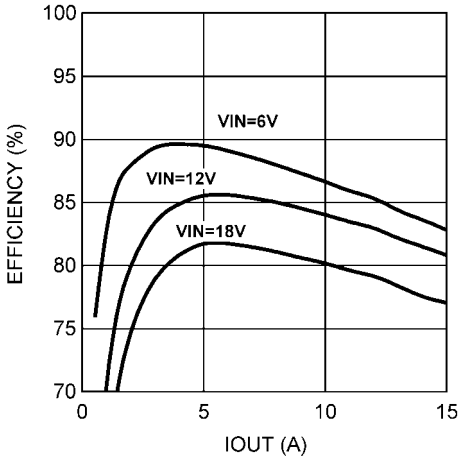
## Typical Performance Characteristics

**3.3V Output Efficiency at 500 kHz**



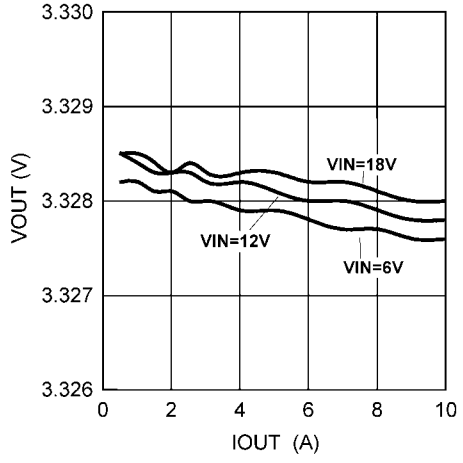

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**1.2V Output Efficiency at 500 kHz**



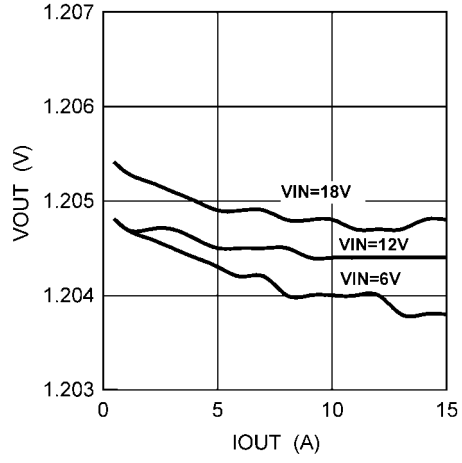

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**3.3V Output Load and Line Regulation**



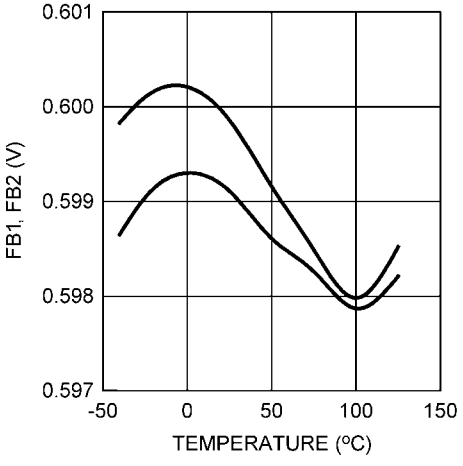

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**1.2V Output Load and Line Regulation**



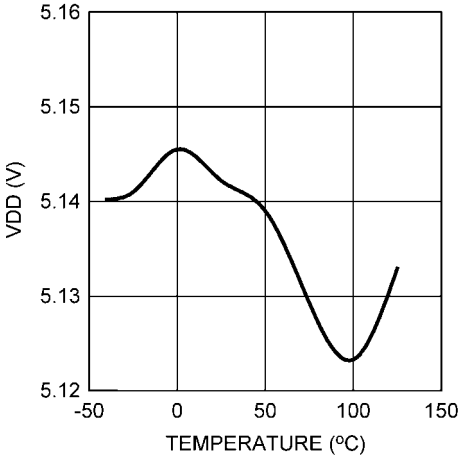

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**FB1, FB2 Reference vs Temperature**



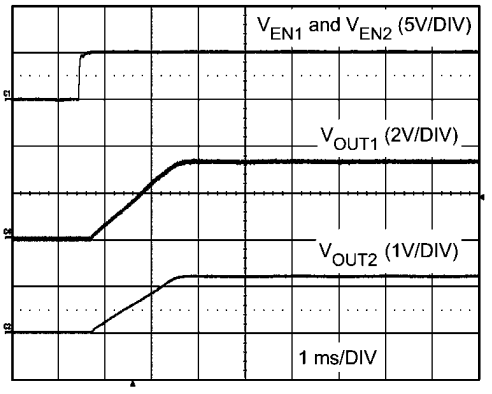

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**VDD Voltage vs Temperature**



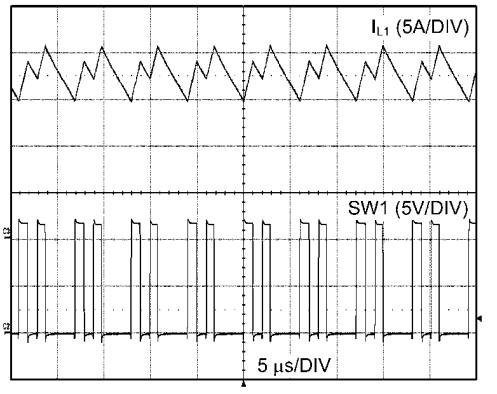

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**Soft-Start without Load**



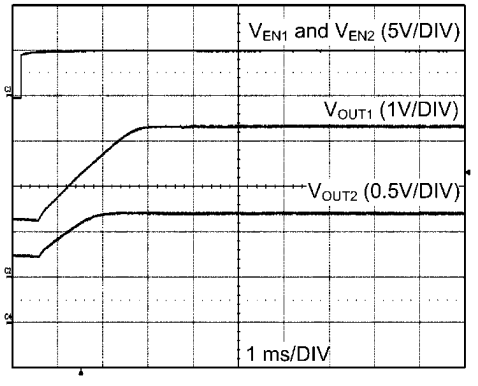

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**Pulse Skipping during Over-Current Condition**



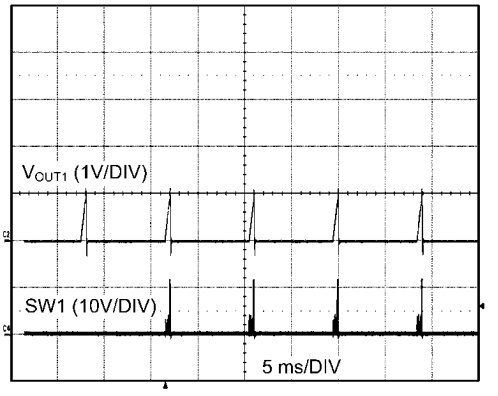

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**No Load Soft-Start with Pre-Bias**



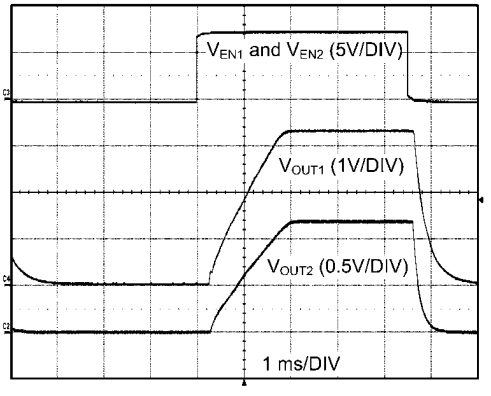

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**Output Short Circuit Hiccup**



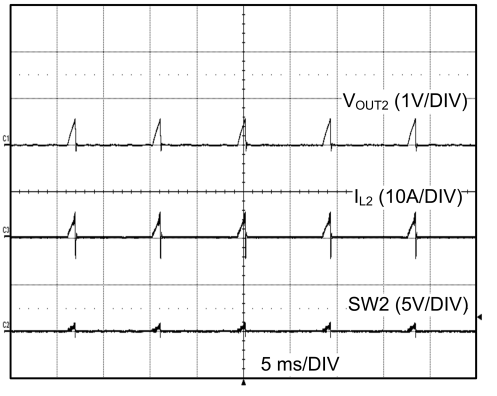

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**Soft-Start with Load**



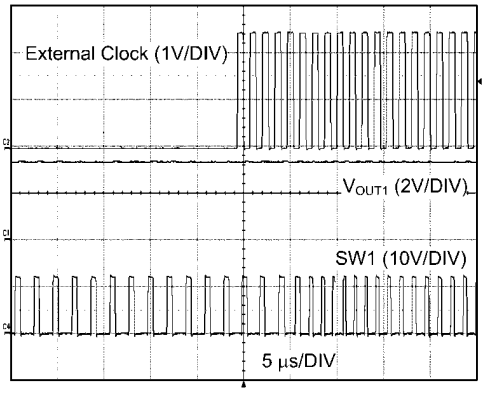

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**Switch Node Short Circuit Hiccup**



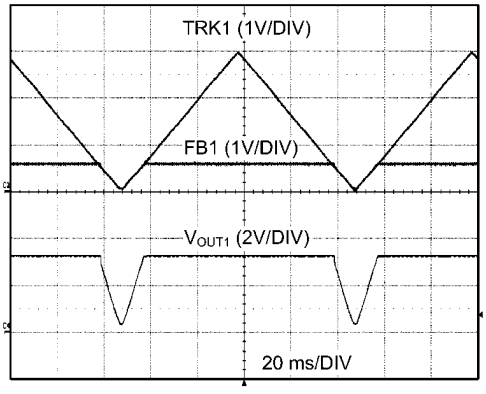

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**External Clock Synchronization**



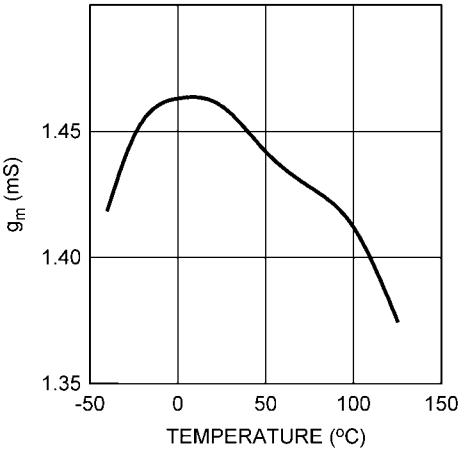

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**External Tracking**



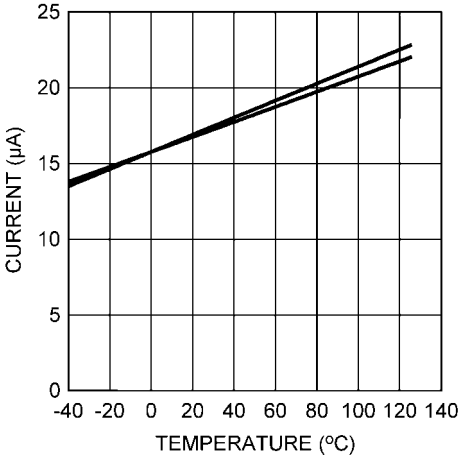

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**Error Amplifier Transconductance vs Temperature**



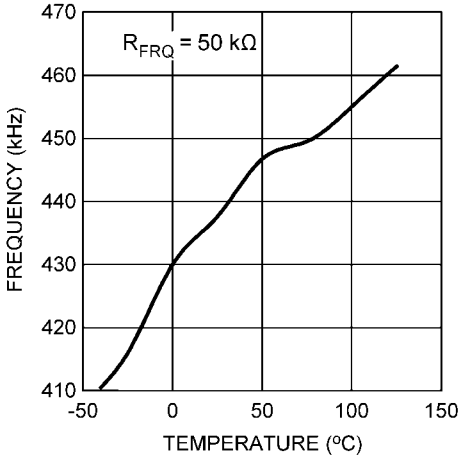

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**Enable Current Threshold vs Temperature**



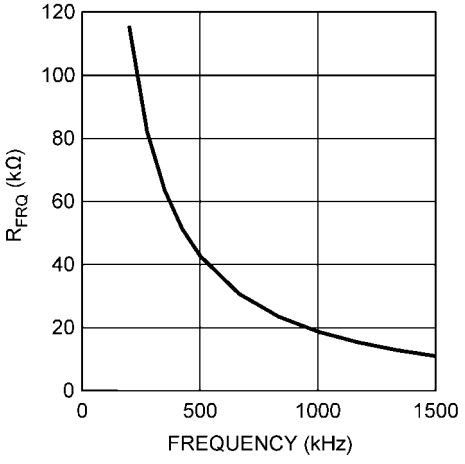

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**Switching Frequency vs Temperature**



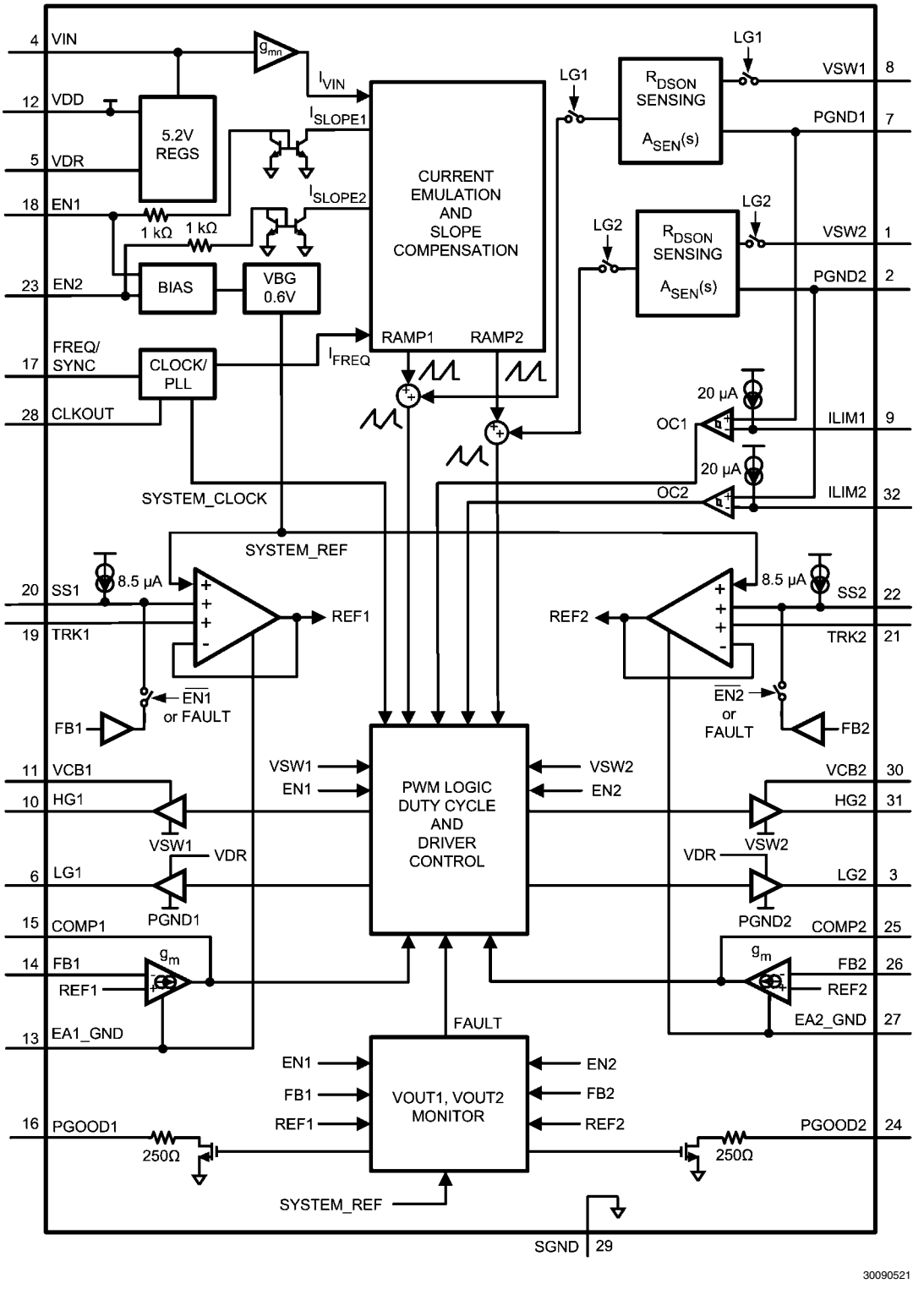

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**$R_{FRQ}$ vs Switching Frequency**




30090506

## Block Diagram



# Functional Description

## THEORY OF OPERATION

The LM3000 is a dual emulated current-mode PWM synchronous controller. Unlike traditional peak current-mode controllers which sense the current while the high-side FET is on, the LM3000 senses current while the low-side FET is on. It then emulates the peak current waveform and uses that information to regulate the output voltage. The blanking time when the high-side FET first turns on that is normally associated with high-side sensing is not needed, allowing high-side ON pulses as low as 50 ns. The LM3000 therefore has both excellent line transient response and the ability to regulate low output voltages from high input voltages.

## STARTUP

After the EN1 or EN2 current exceeds the enable ON threshold and the voltage at the VDD pin reaches 2.2V, an internal 8.5 µA current source charges the soft-start capacitor of the enabled channel. Once soft-start is complete the converter enters steady state operation. Current limit is enabled during soft-start in case of a short circuit at the output. The soft-start time is calculated as:

$$t_{SS} = \frac{C_{SS} \times 0.6V}{8.5\ \mu A}$$

To avoid current limit during startup, the soft-start time $t_{SS}$ should be substantially longer than the time required to charge $C_{OUT}$ to $V_{OUT}$ at the maximum output current. To meet this requirement:

$$t_{SS} > \frac{V_{OUT} \times C_{OUT}}{I_{LIMIT} - I_{OUT}}$$

## STARTUP INTO OUTPUT PRE-BIAS

If the output capacitor of the LM3000 has been charged up to some pre-bias level before the converter is enabled, the chip will force the soft-start capacitor to the same voltage as the FB pin. This will cause the output to ramp up from the existing output voltage without discharging it. During the soft-start ramp, the low-side FET is disabled whenever the COMP voltage is below the active regulation voltage range.

## LOW INPUT VOLTAGE

The LM3000 includes an internal 5.2V linear regulator connected from the VIN pin to the VDD pin. This linear regulator feeds the logic and FET drive circuitry. For input voltages less than 5.5V, the VIN, VDD and VDR pins can be tied together externally. This allows the full input voltage to be used for driving the power FETs and also minimizes conduction loss in the LM3000.

## TRACKING

The LM3000 has individual tracking inputs which control each output during soft-start. This allows the output voltage slew rates to be controlled for loads that require precise sequencing. When the tracking function is not being used the TRK1 or TRK2 pins should be connected directly to the VDD pin.

During start-up, the error amplifier will follow the lower of the SS or TRK voltages. For design margin, the soft-start time $t_{SS}$ should be set to 75% of the minimum expected rise time of the controlling supply. In the event that the LM3000 is enabled with a pre-biased master supply controlling track, the soft-start capacitor will control the tracking output voltage rise time. Pulling TRK down after a normal startup will cause the output voltage to follow the track signal.

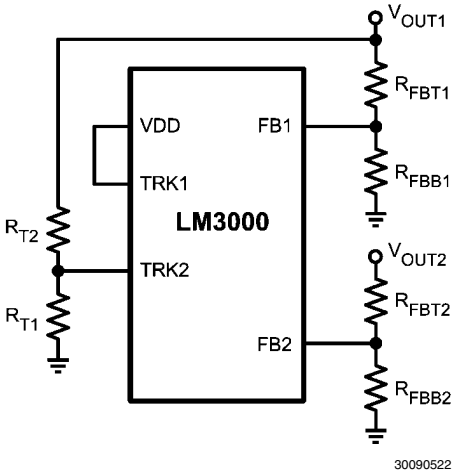



**FIGURE 1. Tracking with $V_{OUT1}$ Controlling $V_{OUT2}$**

*Figure 1* shows a tracking example with the highest output voltage at $V_{OUT1}$ controlling $V_{OUT2}$. Tracking may be set so that $V_{OUT1}$ and $V_{OUT2}$ both rise together. For this case, the equation governing the values of the tracking divider resistors $R_{T1}$ and $R_{T2}$ is:

$$0.75 = V_{OUT1} \times \frac{R_{T1}}{R_{T1} + R_{T2}}$$

A value of 10 kΩ 1% is recommended for $R_{T1}$ as a good compromise between high precision and low quiescent current through the divider. Using an example of $V_{OUT1}$ = 3.3V and $V_{OUT2}$ = 1.2V, the value of $R_{T2}$ is 34.4 kΩ 1%. A timing diagram for $V_{OUT1}$ controlling $V_{OUT2}$ is shown in *Figure 2*. Note that the TRK pin must finish at least 100 mV higher than the 0.6V reference to achieve the full accuracy of the LM3000 regulation. To meet this requirement the tracking voltage is offset by 150 mV. The tracking output voltage will reach its final value at 80% of the controlling output voltage.

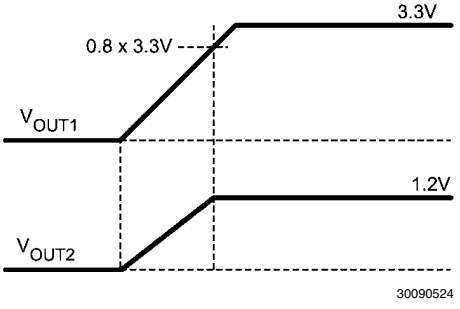



**FIGURE 2. Tracking with $V_{OUT1}$ Controlling $V_{OUT2}$**

Alternatively, the tracking feature can be used to create equal slew rates for the output voltages. In order to track properly, use the highest output voltage to control the slew rate. In this case, the tracking resistors are found from:

$$V_{OUT2} = V_{OUT1} \times \frac{R_{T1}}{R_{T1} + R_{T2}}$$

Again, a value of 10 kΩ 1% is recommended for $R_{T1}$. For the example case of $V_{OUT1}$ = 5V and $V_{OUT2}$ = 1.8V, $R_{T2}$ is 17.8 kΩ 1%. A timing diagram for the case of equal slew rates is shown in *Figure 3*.

Either method ensures that the output voltage of the tracking supply always reaches regulation before the output voltage of the controlling supply.

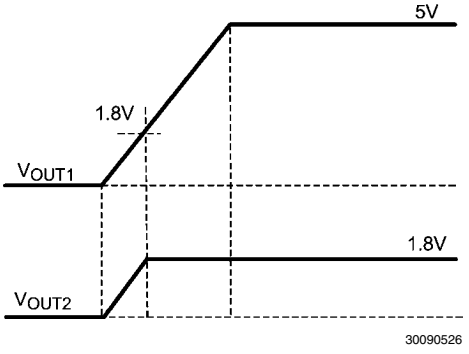



**FIGURE 3. Tracking with Equal Slew Rates**

The LM3000 can track the output of a master power supply by connecting a resistor divider to the TRK pins as shown in *Figure 4*. For equal start times, the tracking resistors are determined by:

$$0.75 = V_{MASTER} \times \frac{R_{T1}}{R_{T1} + R_{T2}}$$

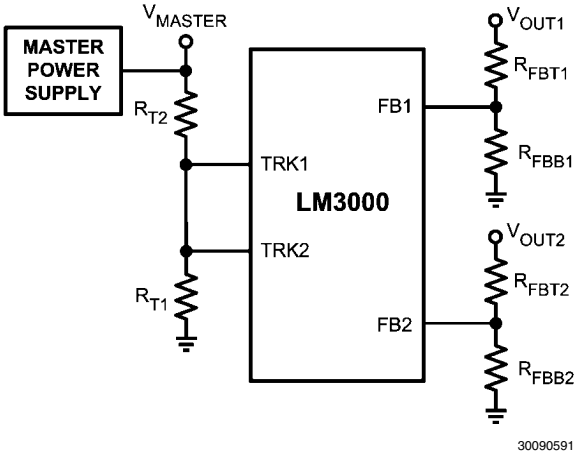



**FIGURE 4. Tracking a Master Supply with Equal Start Time**

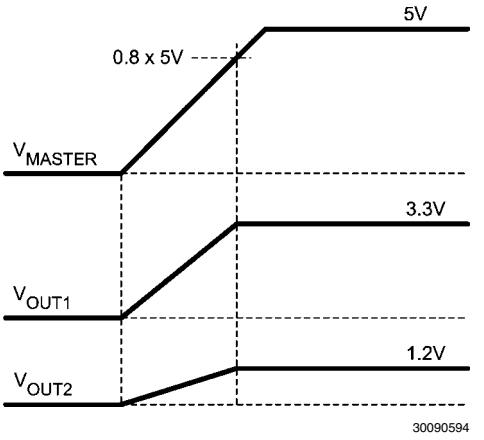



**FIGURE 5. Tracking a Master Supply with Equal Start Time**

For equal slew rates, the circuit of *Figure 6* is used. The relationship for the tracking divider is set by:

$$V_{OUT1} = V_{MASTER} \times \frac{R_{T1} + R_{T2}}{R_{T1} + R_{T2} + R_{T3}}$$

$$V_{OUT2} = V_{MASTER} \times \frac{R_{T1}}{R_{T1} + R_{T2} + R_{T3}}$$

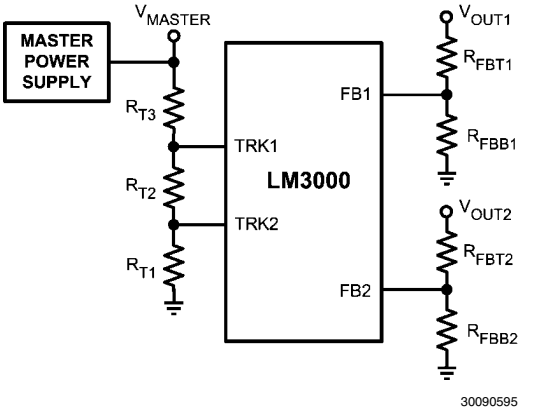



**FIGURE 6. Tracking a Master Supply with Equal Slew Rates**

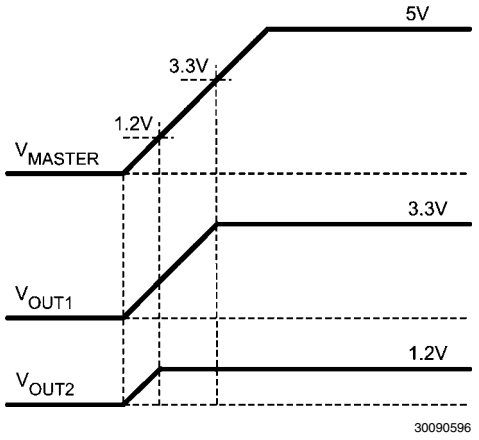



**FIGURE 7. Tracking a Master Supply with Equal Slew Rates**

### Continuous Conduction Mode

The LM3000 controls the output voltage by adjusting the duty cycle of the power MOSFETs with trailing edge pulse width modulation. The output inductor and capacitor filter the square wave produced as the power MOSFETs switch the input voltage, thereby creating a regulated output voltage. The dc level of the output voltage is determined by feedback resistors using the following equation:

$$V_{OUT} = 0.6 \times \frac{R_{FBB} + R_{FBT}}{R_{FBB}}$$

The output inductor current can flow from the drain to the source of the low-side MOSFET, which keeps the converter in continuous-conduction-mode (CCM). CCM has the advantage of constant frequency and nearly constant duty cycle ($D = V_{OUT} / V_{IN}$) over all load conditions, and also allows the converter to sink current at the output if needed.

## FREQUENCY SETTING

The switching frequency of the internal oscillator is set by a resistor, $R_{FRQ}$, connected from the FREQ/SYNC pin to SGND. The proper resistor for a desired switching frequency $f_{SW}$ can be selected from the curves in the Typical Performance Characteristics section labeled "$R_{FRQ}$ vs Switching Frequency" or by using the following equation:

$$R_{FRQ} = \frac{2.48 \times 10^{10}}{f_{SW} \times \left(1 + \frac{f_{SW}}{3.4 \times 10^{6}}\right)} - 1000$$

Where $f_{SW}$ is the switching frequency in Hz.

## FREQUENCY SYNCHRONIZATION

The switching frequency of the LM3000 can be synchronized by an external clock or other fixed frequency signal in the range of 200 kHz to 1.5 MHz. The external clock should be applied through a 100 pF coupling capacitor as shown in *Figure 8*. In order for the oscillator to synchronize properly, the minimum amplitude of the SYNC signal is 2.2V and the maximum amplitude is VDD. The minimum pulse width both positive and negative is 100 ns. The nominal dc voltage at the FREQ/SYNC pin is 0.6V, which is also the clamp voltage level for the falling edge of the SYNC pulse. Depending on the pulse width and frequency, $C_{SYNC}$ may be adjusted to provide sufficient amplitude of the signal at the FREQ/SYNC. It is possible to drive this pin directly from a 0 to 2.2V logic output, though not recommended for the typical application.

Circuits that use an external clock should still have a resistor $R_{FRQ}$ connected from the FREQ/SYNC pin to ground. $R_{FRQ}$ is selected using the equation from the Frequency Setting section to match the external clock frequency. This allows the controller to continue operating at approximately the same switching frequency if the external clock fails and the coupling capacitor on the clock side is grounded or pulled to logic high.

In the case of no external clock edges at startup, the internal oscillator will be controlled by the external set resistor until the first clock edge is detected. After the first edge, the PLL will lock within a few clock cycles, after which any missing edges will cause the oscillator to be programmed by $R_{FRQ}$. If $R_{FRQ}$ is chosen to program the oscillator very close to the external clock frequency, the PLL will lock very quickly and there will be very little disturbance in the switching frequency.

Care must be taken to prevent errant pulses from triggering the synchronization circuitry. In circuits that will not synchronize to an external clock, $C_{SYNC}$ should be connected from the FREQ/SYNC pin to SGND as a noise filter. When a clock pulse is first detected, the LM3000 begins switching at the external clock frequency. Noise or a short burst of clock pulses may result in variations of the switching frequency due to loss of lock by the PLL.

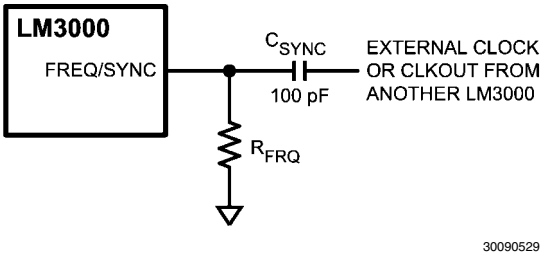



**FIGURE 8. Clock Synchronization Circuit**

In the case where two LM3000 controllers are used, the CLKOUT of the first controller can be used as a synchronization input for the second controller. Note that the CLKOUT is 90 degrees out of phase with the main controller clock, so that the four phases of the two controllers are separated for minimum input ripple current.

## MOSFET GATE DRIVE

The LM3000 has two sets of gate drivers designed for driving N-channel MOSFETs in a synchronous mode. Power for the high-side driver is supplied through the VCB pin. For the high-side gate HG to turn on the top FET, the VCB voltage must be at least one $V_{GS(th)}$ greater than $V_{IN}$. This voltage is supplied from a local charge pump which consists of a Schottky diode and bootstrap capacitor, shown in *Figure 9*. For the Schottky, a rating of at least 250 mA and 30V is recommended. A dual package may be used to supply both VCB1 and VCB2.

Both the bootstrap and the low-side FET driver are fed from VDR, which is the output of a 5V internal linear regulator. This regulator has a dropout voltage of approximately 1V. The drive voltage for the top FET driver is about $V_{DR}$ - 0.5 at light load condition and about $V_{DR}$ at normal to full load condition. This information is needed to select the type of MOSFETs used, as well as calculate the losses in driving them.

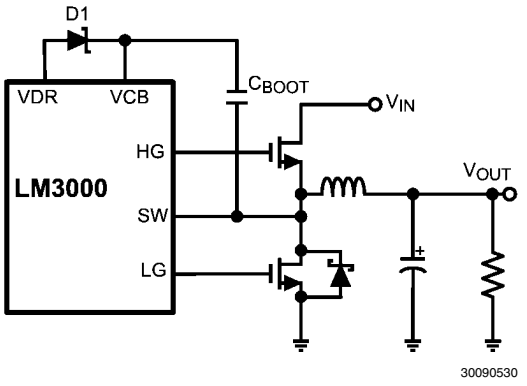



**FIGURE 9. Bootstrap Circuit**

## UVLO

For the case where VIN is > VDD, the VIN UVLO thresholds are determined by the VDD UVLO comparator and the VDD dropout voltage. This sets the rising threshold for VIN at approximately 3V, with 30 mV of hysteresis.

For the case where VIN is < 5.5V and tied to VDD and VDR, the UVLO trip point is 2.12V rising. UVLO consists of turning off the top and bottom FETs and remaining in that condition until VDD rises above 2.12V. The falling trip point is 140 mV below the rising trip point.

## CURRENT LIMIT

The current limit of the LM3000 is realized by sensing the current in the low-side FET while the output current circulates through it. This voltage ($I_{OUT} \times R_{DS(on)_LO}$) is compared against the voltage of a fixed, internal 20 µA current source and a user-selected resistor, $R_{LIM}$, connected between the switch node and the ILIM pin. Once a current limit event is sensed, the high-side switch is disabled for the following cycle and the low-side FET is kept on during this time. If sixteen consecutive current limit cycles occur, the part enters hiccup mode.

The value of $R_{LIM}$ for a desired current limit $I_{ILIMIT}$ can be selected by the following equation:

$$R_{LIM} = \frac{I_{LIMIT} \times R_{DS(on)_LO}}{20\ \mu A}$$

## HICCUP MODE

During hiccup mode the LM3000 disables both the high-side and low-side MOSFETs, and remains in this state for 4096 switching cycles. After this cool down period the circuit restarts again through the normal soft-start sequence. If the shorted fault condition persists, hiccup will retrigger once the soft-start has finished. This occurs when the SS voltage is greater than 0.7V and switching has reached the continuous conduction mode state.

There is a coarse high-side current limit which senses the voltage across the high-side MOSFET. The threshold is approximately 0.5V, which may provide some level of protection for a catastrophic fault. Hiccup will immediately trigger after two consecutive high-side current limit fault events.

## POWER GOOD

Power good pins PGOOD1 and PGOOD2 are available to monitor the output status of the two channels independently. The PGOOD1 pin connects to the output of an open drain MOSFET, which will remain open while Channel 1 is within the normal operating range. PGOOD1 goes low (low impedance to ground) under the following three conditions:

1. Channel 1 is turned off.
2. OVP on Channel 1.
3. UVP on Channel 1.

PGOOD2 functions in a similar manner. UVP tracks REF1, REF2 as shown in the block diagram. OVP sets a fault which turns off the high gate and turns on the low gate. This discharges the output voltage until it has fallen 3% below the OVP threshold.

PGOOD may be pulled up through a resistor to any voltage which is < 5.5V. When using VDD for the pull-up voltage, a typical value of 100 kΩ is used to minimize loading on VDD.

## ENABLE

A fixed external voltage source and resistors to EN1 and EN2 are used to independently enable each output. The LM3000 can be put into a low power shutdown mode by pulling the EN1 and EN2 pins to ground, or by applying 0V to the enable resistors. During shutdown both the high-side and low-side FETs are disabled. The quiescent current during shutdown is approximately 30 µA.

The enable pins also control the emulated current ramp amplitude by programming the current into EN1 and EN2. The recommended range for $I_{EN}$ is 40 µA to 160 µA. See the Applications Information section under Control Loop Compensation for the complete design method.

# Application Information

The most common circuit controlled by the LM3000 is a non-isolated, synchronous buck regulator. The buck regulator steps down the input voltage and has a duty ratio D of:

$$D = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta}$$

Where η is the estimated converter efficiency.

The following is a design example selecting components for the Typical Application Schematic of *Figure 24*. The circuit is designed for two outputs of 3.3V at 8A and 1.2V at 15A from an input voltage of 6V to 18V. This circuit is typical of a 'brick' module and has a height requirement of 6.5mm or less. Other assumptions used to aid in circuit design are that the expected load is a small microprocessor or ASIC with fast load transients, and that the type of MOSFETs used are in SO-8 or its equivalent packages such as PowerPAK®, PQFN and LFPAK (LFPAK-i).

## SWITCHING FREQUENCY

The selection of switching frequency is based on the tradeoff between size, cost and efficiency. In general, a lower frequency means larger, more expensive inductors and capacitors. A higher switching frequency generally results in a smaller but less efficient solution, because the power MOSFET gate capacitances must be charged and discharged more often in a given amount of time. For this application a frequency of 500 kHz is selected. 500 kHz is a good compromise between the size of the inductor and MOSFETs, transient response and efficiency. Following the equation given for $R_{FRQ}$ in the Frequency Setting section, for 500 kHz operation a 42.2 kΩ 1% resistor is used.

## MOSFETS

Selection of the power MOSFETs is governed by a tradeoff between size, cost and efficiency. Buck regulators that use a controller IC and discrete MOSFETs tend to be most efficient for output currents of 4A to 20A.

Losses in the high-side FET can be broken down into conduction loss, gate charge loss and switching loss. Conduction, or $I^2R$ loss is approximately:

$$P_{COND_HI} = D \times (I_{OUT}^2 \times R_{DS(on)_HI} \times 1.3)$$
(High-side FET)

$$P_{COND_LO} = D \times (I_{OUT}^2 \times R_{DS(on)_LO} \times 1.3)$$
(Low-side FET)

In the above equations the factor 1.3 accounts for the increase in MOSFET $R_{DS(on)}$ due to self heating. Alternatively, the 1.3 can be ignored and the $R_{DS(on)}$ of the MOSFET estimated using the $R_{DS(on)}$ vs. Temperature curves in the MOSFET datasheets.

The gate charge loss results from the current driving the gate capacitance of the power MOSFETs, and is approximated as:

$$P_{DR} = V_{IN} \times (Q_{G_HI} + Q_{G_LO}) \times f_{SW}$$

Where $Q_{G_HI}$ and $Q_{G_LO}$ are the total gate charge of the high-side and low-side FETs respectively at the typical 5V driver voltage. Gate charge loss differs from conduction and switching losses in that the majority of dissipation occurs in the LM3000.

The switching loss occurs during the brief transition period as the FET turns on and off, during which both current and voltage are present in the channel of the FET. This can be approximated as the following:

$$P_{SW_ON} = V_{IN} \times I_{L_VL} \times \alpha \times R_{G_ON} \times \left( \frac{Q_{GD}}{V_{DR} - V_{PLT2}} + C_{ISS} \times Ln\left( \frac{V_{DR} - V_{TH}}{V_{DR} - V_{PLT1}} \right) \right)$$

$$P_{SW_OFF} = V_{IN} \times I_{L_PK} \times \beta \times R_{G_OFF} \times \left( \frac{Q_{GD}}{V_{PLT2}} + C_{ISS} \times Ln\left( \frac{V_{PLT2}}{V_{TH}} \right) \right)$$

Where $Q_{GD}$ is the high-side FET Miller charge with a $V_{DS}$ swing between 0 to $V_{IN}$; $C_{ISS}$ is the input capacitance of the high-side MOSFET in its off state with $V_{DS} = V_{IN}$. α and β are fitting coefficient numbers, which are usually between 0.5 to 1, depending on the board level parasitic inductances and reverse recovery of the low-side power MOSFET body diode. Under ideal condition, setting α = β = 0.5 is a good starting point. Other variables are defined as:

$$I_{L_VL} = I_{OUT} - 0.5 \times \Delta I_L$$

$$I_{L_PK} = I_{OUT} + 0.5 \times \Delta I_L$$

$$V_{PLT1} \approx V_{TH} + \frac{I_{L_VL}}{g_{mFET_HI}}$$

$$V_{PLT2} \approx V_{TH} + \frac{I_{L_PK}}{g_{mFET_HI}}$$

$$R_{G_ON} = 8.5 + R_{G_INT} + R_{G_EXT}$$

$$R_{G_OFF} = 2.8 + R_{G_INT} + R_{G_EXT}$$

Switching loss is calculated for the high-side FET only. 8.5 and 2.8 represent the LM3000 high-side driver resistance in the transient region. $R_{G_INT}$ is the gate resistance of the high-side FET, and $R_{G_EXT}$ is the external gate resistance if applicable. $R_{G_EXT}$ may be used to damp out excessive parasitic ringing at the switch node.

For this example, the maximum drain-to-source voltage applied to either MOSFET is 18V. The maximum drive voltage at the gate of the high-side MOSFET is 5V, and the maximum drive voltage for the low-side MOSFET is 5V. The selected MOSFET must be able to withstand 18V plus any ringing from drain to source, and be able to handle at least 5V plus ringing from gate to source. If the duty cycle of the converter is small, then the high-side MOSFET should be selected with a low gate charge in order to minimize switching loss whereas the bottom MOSFET should have a low $R_{DSON}$to minimize conduction loss.

For a typical input voltage of 12V and output currents of 8A and 12A, the MOSFET selections for the design example are HAT2168 for the high-side MOSFET and RJK0330DPB for the low-side MOSFET.

A 3Ω resistor for $R_{CBT}$ is added in series with the VDR regulator output, as shown in *Figure 24*. This helps to control the MOSFET turn-on and ringing at the switch node, without affecting the MOSFET turn-off.

To improve efficiency, 3A, 40V Schottky diodes are placed across the low-side MOSFETs. The external Schottky diodes have a much lower forward voltage than the MOSFET body diode, and help to minimize the loss due to the body diode recovery characteristic.

## OUTPUT INDUCTORS

The first criterion for selecting an output inductor is the inductance itself. In most buck converters, this value is based on the desired peak-to-peak ripple current, $\Delta I_L$ that flows in the inductor along with the load current. As with switching frequency, the selection of the inductor is a tradeoff between size and cost. Higher inductance means lower ripple current and hence lower output voltage ripple. Lower inductance results in smaller, less expensive devices. An inductance that gives a ripple current of 1/6 to 1/3 of the maximum output current is a good starting point. ($\Delta I_L$ = (1/6 to 1/3) x $I_{OUT}$). Minimum inductance is calculated from this value, using the maximum input voltage as:

$$L_{MIN} = \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \times \Delta I_L} \times D$$

By calculating in terms of amperes, volts, and megahertz, the inductance value will come out in micro henries.

The inductor ripple current is found from the minimum inductance equation:

$$\Delta I_L = \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \times L_{ACTUAL}} \times D$$

The second criterion is inductor saturation current rating. The LM3000 has an accurately programmed valley current limit. During an instantaneous short, the peak inductor current can be very high due to a momentary increase in duty cycle. Since this is limited by the coarse high-side switch current limit, it is advised to select an inductor with a larger core saturation margin and preferably a softer roll off of the inductance value over load current.

For the design example, standard values of 1.2 µH for the 1.2V, 15A output and 2.7 µH for the 3.3V, 8A output are chosen to fall within the $\Delta I_L$ = (1/6 to 1/3) x $I_{OUT}$ range.

The dc loss in the inductor is determined by its series resistance $R_L$. The dc power dissipation is found from:

$$P_{DC} = I_{OUT}^2 \times R_L$$

The ac loss can be estimated from the inductor manufacturer's data, if available. The ac loss is set by the peak-to-peak ripple current $\Delta I_L$ and the switching frequency $f_{SW}$.

## OUTPUT CAPACITORS

The output capacitors filter the inductor ripple current and provide a source of charge for transient load conditions. A wide range of output capacitors may be used with the LM3000 that provide excellent performance. The best performance is typically obtained using aluminum electrolytic, tantalum, polymer, solid aluminum, organic or niobium type chemistries in parallel with a ceramic capacitor. The ceramic capacitor provides extremely low impedance to reduce the output ripple voltage and noise spikes, while the aluminum or other capacitors provide a larger bulk capacitance for transient loading and series resistance for stability.

When selecting the value for the output capacitor the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple can be approximated as:

$$\Delta V_O = \Delta I_L \times \sqrt{R_C^2 + \left(\frac{1}{8 \times f_{SW} \times C_O}\right)^2}$$

Where $\Delta V_O$ (V) is the peak to peak output voltage ripple, $\Delta I_L$ (A) is the peak to peak inductor ripple current, $R_C$ (Ω) is the equivalent series resistance or ESR of the output capacitor, $f_{SW}$ (Hz) is the switching frequency, and $C_O$ (F) is the output capacitance. The amount of output ripple that can be tolerated is application specific. A general recommendation is to keep the output ripple less than 1% of the rated output voltage. The output capacitor selection will also affect the output voltage droop and overshoot during a load transient. The peak transient of the output voltage during a load current step is dependent on many factors. Given sufficient control loop bandwidth an approximation of the transient voltage can be obtained from:

$$V_P = \frac{L \times \Delta I_O^2}{2 \times C_O \times V_L} + \frac{R_C^2 \times C_O \times V_L}{2 \times L}$$

Where $V_P$ (V) is the output voltage transient and $\Delta I_O$ (A) is the load current step change. $C_O$ (F) is the output capacitance, L (H) is the value of the inductor and $R_C$ (Ω) is the series resistance of the output capacitor. $V_L$ (V) is the minimum inductor voltage, which is duty cycle dependent.

For D < 0.5, $V_L = V_{OUT}$

For D > 0.5, $V_L = V_{IN} - V_{OUT}$

This shows that as the input voltage approaches $V_{OUT}$, the transient droop will get worse. The recovery overshoot remains fairly constant.

The loss associated with the output capacitor series resistance can be estimated as:

$$P_{CO} = R_C \times \frac{\Delta I_L^2}{\sqrt{12}}$$

### Output Capacitor Design Procedure

For the design example $V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, D = $V_{OUT}$ / $V_{IN}$ = 0.275, L = 2.7 µH, $\Delta I_L$ = 1.8A, $\Delta I_O$ = 8A and $V_P$ = 0.15V.

To meet the transient voltage specification, the maximum $R_C$ is:

$$R_C \leq \frac{V_P}{\Delta I_O}$$

For the design example, the maximum $R_C$ is 18.75 mΩ. Choose $R_C$ = 15 mΩ as the design limit.

From the equation for $V_P$, the minimum value of $C_O$ is:

$$C_O \geq \frac{L \times \Delta I_O^2}{V_P \times V_L} \times \frac{1}{1 + \sqrt{1 - \left(\frac{R_C \times \Delta I_O}{V_P}\right)^2}}$$

For D < 0.5, $V_L = V_{OUT}$

For D > 0.5, $V_L = V_{IN} - V_{OUT}$

With $R_C = V_P / \Delta I_O$ this reduces to:

$$C_O \geq \frac{L \times \Delta I_O^2}{V_P \times V_L}$$

With $R_C = 0$ this reduces to:

$$C_O \geq \frac{L \times \Delta I_O^2}{2 \times V_P \times V_L}$$

Since D < 0.5, $V_L = V_{OUT}$. With $R_C$ = 15 mΩ, the minimum value for $C_O$ is 218 µF.

The minimum control loop bandwidth $f_C$ is given by:

$$f_C \geq \frac{\Delta I_O}{2 \times \pi \times C_O \times V_P}$$

For the design example, the minimum value for $f_C$ is 39 kHz. A 220 µF, 15 mΩ polymer capacitor in parallel with a 22 µF, 3 mΩ ceramic will meet the target output voltage ripple and transient specification.

For the 1.2V, 15A output, two 220 µF, 15 mΩ polymer capacitors in parallel with a 22 µF, 3 mΩ ceramic are chosen to meet the target design specifications.

## INPUT CAPACITORS

The input capacitors for a buck regulator are used to smooth the large current pulses drawn by the inductor and load when the high-side MOSFET is on. Due to this large ac stress, input capacitors are usually selected on the basis of their ac rms current rating rather than bulk capacitance. Low ESR is beneficial because it reduces the power dissipation in the capacitors. Although any of the capacitor types mentioned in the Output Capacitor section can be used, ceramic capacitors are common because of their low series resistance. In general the input to a buck converter does not require as much bulk capacitance as the output.

The input capacitors should be selected for rms current rating and minimum ripple voltage. The equation for the rms current and power loss of the input capacitor in a single phase can be estimated as:

$$I_{CIN(RMS)} \approx I_O \times \sqrt{D \times (1 - D)}$$

$$P_{CIN} \approx I_O^2 \times D \times (1 - D) \times R_{CIN}$$

Where $I_O$ (A) is the output load current and $R_{CIN}$ (Ω) is the series resistance of the input capacitor. Since the maximum values occur at D = 0.5, a good estimate of the input capacitor rms current rating in a single phase is one-half of the maximum output current.

Neglecting the series inductance of the input capacitance, the input voltage ripple for a single phase can be estimated as:

$$\Delta V_{IN} = \frac{I_O \times D \times (1 - D)}{C_{IN} \times f_{SW}} + \left( I_O + \frac{\Delta I_L}{2} \right) \times R_{CIN}$$

By defining the maximum input voltage ripple, the minimum requirement for the input capacitance can be calculated as:

$$C_{IN} \geq \frac{I_O \times D \times (1 - D)}{\left( \Delta V_{IN} - \left( I_O + \frac{\Delta I_L}{2} \right) \times R_{CIN} \right) \times f_{SW}}$$

For the dual output design operating 180° out of phase, the general equation for the input capacitor rms current is approximated as:

$$I_{CIN(RMS)} \approx \sqrt{\begin{array}{c}(I1^2 \times D1) + (I2^2 \times D2) \\ + (2 \times I1 \times I2 \times D3) \\ - (I1 \times D1 + I2 \times D2)^2\end{array}}$$

Where the output currents are I1, I2 and the duty cycles are D1, D2 respectively. D3 represents the overlapping effective duty cycle, which adds to the RMS current.

$$D3 = MAX(MIN(D1 - 0.5 , D2) , 0) + MAX(MIN(D2 - 0.5 , D1) , 0)$$

If D > 0.5 for both or D < 0.5 for both, the worst case rms current occurs with one output at full load and the other at no load. The maximum rms current can be approximated as:

$$I_{CIN(RMS)MAX} \approx 0.5 \times MAX(I1 , I2)$$

If D > 0.5 for one and D < 0.5 for the other, the worst case rms current becomes:

$$I_{CIN(RMS)MAX} \approx 0.707 \times \sqrt{I1^2 + I2^2}$$

In most applications for point-of-load power supplies, the input voltage is the output of another switching converter. This output often has a lot of bulk capacitance, which may provide adequate damping.

When the converter is connected to a remote input power source through a wiring harness, a resonant circuit is formed by the line impedance and the input capacitors. If step input voltage transients are expected near the maximum rating of the LM3000, a careful evaluation of the ringing and possible overshoot at the device VIN pin should be completed. To minimize overshoot make $C_{IN} > 10 \times L_{IN}$. The characteristic source impedance and resonant frequency are:

$$Z_S = \sqrt{\frac{L_{IN}}{C_{IN}}} \qquad f_S = \frac{1}{2 \times \pi \times \sqrt{L_{IN} \times C_{IN}}}$$

The converter exhibits a negative input impedance which is lowest at the minimum input voltage:

$$Z_{IN} = -\frac{V_{IN}^2}{P_{OUT}}$$

The damping factor for the input filter is given by:

$$\delta = \frac{1}{2} \times \left( \frac{R_{LIN} + R_{CIN}}{Z_S} + \frac{Z_S}{Z_{IN}} \right)$$

Where $R_{LIN}$ is the input wiring resistance and $R_{CIN}$ is the series resistance of the input capacitors. The term $Z_S / Z_{IN}$ will always be negative due to $Z_{IN}$.

When δ = 1, the input filter is critically damped. This may be difficult to achieve with practical component values. With δ < 0.2, the input filter will exhibit significant ringing. If δ is zero or

negative, there is not enough resistance in the circuit and the input filter will sustain an oscillation.

When operating near the minimum input voltage, an aluminum electrolytic capacitor across $C_{IN}$ may be needed to damp the input for a typical bench test setup. Any parallel capacitor should be evaluated for its rms current rating. The current will split between the ceramic and aluminum capacitors based on the relative impedance at the switching frequency. Using a square wave approximation, the rms current in each capacitor is found from:

$$C1 = C_{IN1} \quad R1 = R_{CIN1} \quad C2 = C_{IN2} \quad R2 = R_{CIN2}$$

$$X_1 \approx \frac{1}{2.2 \times \pi \times f_{SW} \times C1}$$

$$X_2 \approx \frac{1}{2.2 \times \pi \times f_{SW} \times C2}$$

$$I_{CIN1(RMS)} = \frac{I_{CIN(RMS)} \times \sqrt{R2^2 + X2^2}}{\sqrt{(R1 + R2)^2 + (X1 + X2)^2}}$$

$$I_{CIN2(RMS)} = \frac{I_{CIN(RMS)} \times \sqrt{R1^2 + X1^2}}{\sqrt{(R1 + R2)^2 + (X1 + X2)^2}}$$

### Input Capacitor Design Procedure

Ceramic capacitors are sized to support the required rms current. Aluminum electrolytic capacitors are used for damping. Treating each phase separately, find the minimum value for the ceramic capacitor from:

$$C_{IN} \geq \frac{I_O \times D \times (1 - D)}{\Delta V_{IN} \times f_{SW}}$$

For the design example allowing 0.25V input voltage ripple, the worst case occurs for the 3.3V, 8A output at D = 0.5. The minimum value is $C_{IN}$ = 16 µF. For the 1.2V, 15A output, the worst case D = 1.2V / 6V = 0.2. Then $C_{IN}$ = 4.8 µF. Find the rms current rating for each from:

$$I_{CIN(RMS)} \approx I_O \times \sqrt{D \times (1 - D)}$$

Using the same criteria, results are 4A rms for the 3.3V phase and 3A rms for the 1.2V phase. Manufacturer data for 10 µF, 25V, X5R capacitors in a 1206 package allows for 3A rms with a 20°C temperature rise. For the design example, using two ceramic capacitors for each phase will meet both the input voltage ripple and rms current target. Since the series resistance is so low at about 5 mΩ per capacitor, a parallel aluminum electrolytic is used for damping. A good general rule is to make the damping capacitor at least five times the value of the ceramic. By sizing the aluminum such that it is primarily resistive at the switching frequency, the design is greatly simplified since the ceramic is primarily reactive. In this case the approximation for the rms current in the damping capacitor is:

$$I_{CIN2(RMS)} \approx \frac{I_{CIN(RMS)}}{2.2 \times \pi \times f_{SW} \times R_{CIN2} \times C_{IN1}}$$

Where $C_{IN2}$ is the damping capacitance, $R_{CIN2}$ is its series resistance and $C_{IN1}$ is the ceramic capacitance. A 150 µF, 50V, 0.18Ω, 670 mA capacitor in a 10 mm x 10.2 mm package is chosen for each input. Calculated rms current for the 3.3V phase is 322 mA, with 242 mA calculated for the 1.2V phase.

### CURRENT LIMIT

For the design example, the desired current limit set point is chosen to be 150% of the maximum load current. To account for the tolerance of the internal current source and allowing $R_{DS(on)}$ = 4 mΩ for the low-side MOSFET at elevated temperature, a target of 23A is used for the 1.2V output, with 13A for the 3.3V output. Following the equation from the Current Limit section the values for $R_{LIM}$ are 4.64 kΩ, 1% for the 1.2V output and 2.67 kΩ, 1% for the 3.3V output.

### TRACK

Tracking for the design example is configured such that $V_{OUT1}$ is controlling $V_{OUT2}$. The divider values are set so that both outputs will rise together, with $V_{OUT2}$ reaching its final value just before $V_{OUT1}$. Following the method in the Tracking section and allowing for a 120 mV offset between FB and TRK, standard 1% values are selected for $R_{T1}$ = 10 kΩ and $R_{T2}$ = 35.7 kΩ.

### SOFT START

To prevent over-shoot, the soft start time is set to be longer than the time it would take to charge the output voltage at current limit. Following the equations in the Startup section for $V_{OUT1}$ and $V_{OUT2}$:

$$t_{SS1(MIN)} = (3.3V \times 242\ \mu F) / (13A - 8A) = 160\ \mu s$$

$$t_{SS2(MIN)} = (1.2V \times 462\ \mu F) / (23A - 15A) = 69\ \mu s$$

Choosing a value of $C_{SS1}$ = 27 nF, the soft start time is:

$$t_{SS1} = (27\ nF \times 0.6V) / 8.5\ \mu A = 1.9\ ms$$

To ensure that $V_{OUT2}$ tracks $V_{OUT1}$, $t_{SS2}$ is set at two-thirds of $t_{SS1}$ by making $C_{SS2}$ = 18 nF.

### VDD, VDR and VCB CAPACITORS

VDD is used as the supply for the internal control and logic circuitry. A 1 µF ceramic capacitor provides sufficient filtering for VDD.

VDR provides power for both the high-side and low-side MOSGET gate drives, and is sized to meet the total gate drive current. Allowing for $\Delta V_{VDR}$ = 100 mV of ripple, the minimum value for $C_{VDR}$ is found from:

$$C_{VDR} \geq \frac{Q_{G_HI} + Q_{G_LO}}{\Delta V_{VDR}}$$

Using $Q_{G_HI}$ = 15 nC and $Q_{G_LO}$ = 30 nC with a 5V gate drive, the minimum value for $C_{VDR}$ = 0.45 µF.

VCB provides power for the high-side gate drive, and is sized to meet the required gate drive current. Allowing for $\Delta V_{VCB}$ = 100 mV of ripple, the minimum value for $C_{BOOT}$ is found from:

$$C_{BOOT} \geq \frac{Q_{G_HI}}{\Delta V_{VCB}}$$

To use the minimum number of different components, $C_{VDR}$ and $C_{BOOT}$ are also selected as 1 µF ceramic for the design example.

## CONTROL LOOP COMPENSATION

The LM3000 uses emulated peak current-mode PWM control to correct changes in output voltage due to line and load transients. This unique architecture combines the fast line transient response of peak current-mode control with the ability to regulate at very low duty cycles. In order to facilitate the use of MOSFET $R_{DS(on)}$ sensing, the control ramp is set by the enable voltage and a resistor to the enable pin. This stabilizes the modulator gain from variations in MOSFET resistance over temperature, providing a robust design solution.

The control loop is comprised of two parts. The first is the power stage, which consists of the duty cycle modulator, output filter and load. The second part is the error amplifier, which is a transconductance amplifier with a typical gm of 1400 µmho (or 1400 µS). *Figure 10* shows the power stage and error amplifier components.

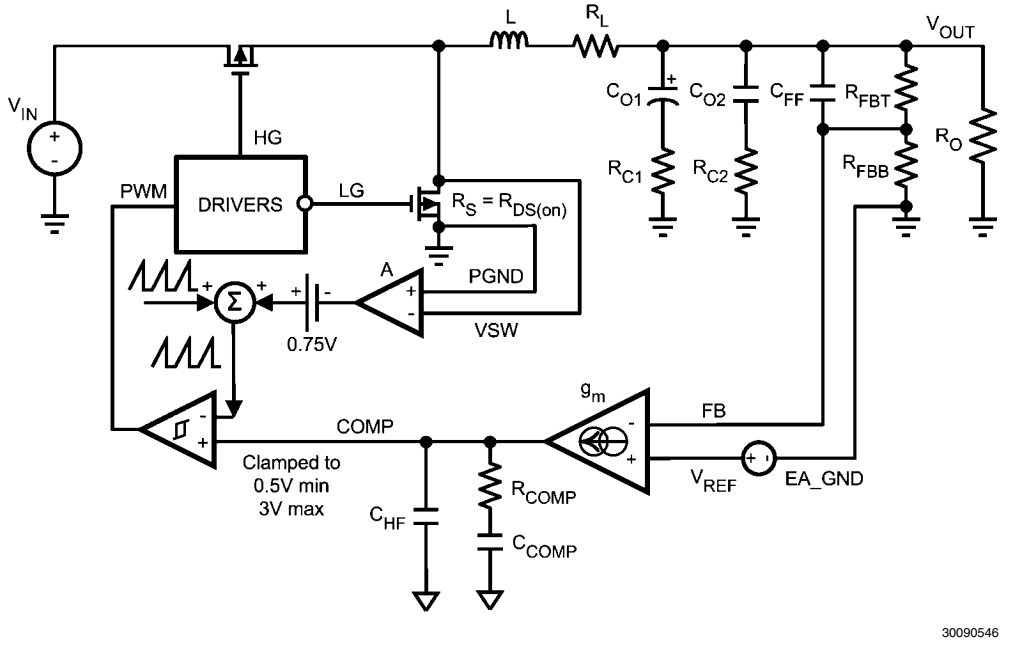



**FIGURE 10. Power Stage and Error Amplifier**

The power stage transfer function (also called the control-to-output transfer function) in a buck converter can be written as:

$$\frac{\hat{v}_O}{\hat{v}_C} = A_{VP} \times \frac{1 + \frac{s}{\omega_Z}}{1 + \frac{s}{\omega_P \times Q_P} + \frac{s^2}{\omega_P^2}}$$

Where:

$$A_{VP} = \frac{K_m}{K_D} \qquad K_m = \frac{1}{(D - 0.5) \times R_i \times \frac{T}{L} + K_{SL}}$$

$$K_D = 1 + \frac{K_m \times R_i}{R_O} \qquad \omega_Z = \frac{1}{C_O \times R_C}$$

$$\omega_P \times Q_P = \frac{K_D}{\frac{L}{R_O} + C_O \times (K_m \times R_i + R_C)} \qquad \omega_P^2 = \frac{K_D}{L \times C_O}$$

With:

$$D = \frac{V_O}{V_{IN}} \qquad R_i = A \times R_S \qquad T = \frac{1}{f_{SW}}$$

For the emulated peak current-mode control, $K_m$ is the dc modulator gain and $R_i$ is the current-sense gain. $K_{SL}$ is the proportional slope compensation, which is set by the enable resistor $R_{EN}$ and enable voltage $V_{EN}$.

*Figure 11* shows a more detailed view of the current sense amplifier, which includes a three stage filter for increased noise immunity. The effective gain and phase are shown in *Figure 12* and *Figure 13*. The equivalent current sense gain A = 7.

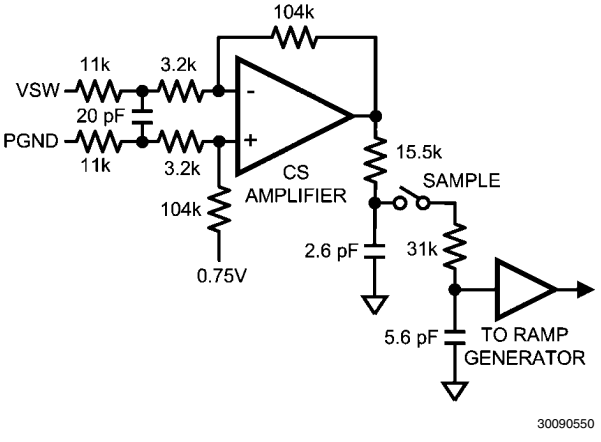



**FIGURE 11. Current Sense Amplifier and Filter**

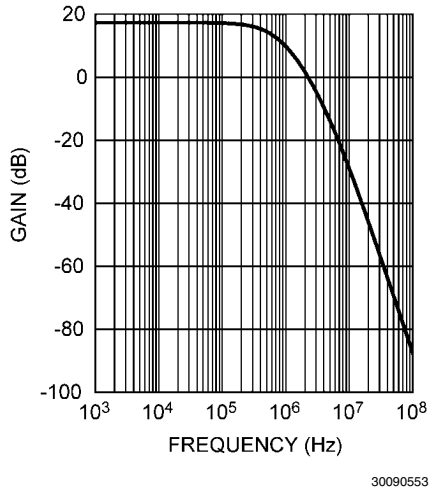



**FIGURE 12. Current Sense Amplifier Gain**

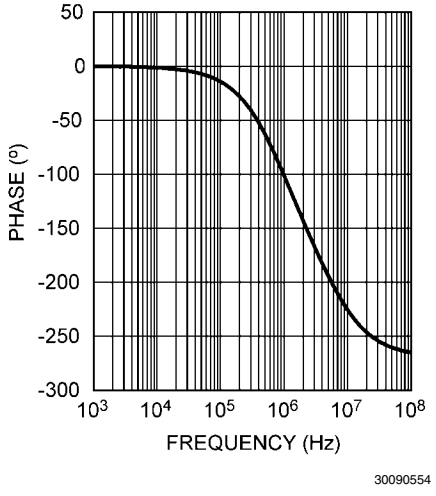



**FIGURE 13. Current Sense Amplifier Phase**

A relatively high value of slope compensating ramp is used to stabilize the gain. This minimizes the effect of the current sense filter on the control loop and swamps out the need for a sampling-gain term. When designing within the recommended operating range, there is no tendency toward subharmonic oscillation. The proportional slope compensation is defined as:

$$K_{SL} = \frac{I_{SL} \times K_{SW}}{I_{EN}} \qquad I_{SL} = 8.05\ \mu A$$

$$K_{SW} = 1 + \frac{f_{SW}}{3400000} \qquad I_{EN} = \frac{V_{EN} - 0.75}{R_{EN} + 2000}$$

$I_{SL}$ is the internal current source scale factor, $K_{SW}$ is the switching frequency correction factor and $I_{EN}$ is the external enable current. The recommended range for $I_{EN}$ is 40 µA to 160 µA. With $V_{EN}$ = 5V, this corresponds to a range for $R_{EN}$ of 25 kΩ to 100 kΩ. For operation below 4.2V input, the maximum enable current is limited, as shown in *Figure 14*. At the minimum input of 3.3V, a value of 80 µA maximum corresponds to $R_{EN}$ = 50 kΩ with $V_{EN}$ = 5V. The minimum enable current is set by the enable bias circuit to ensure proper turn-on above the threshold. A minimum enable voltage of 3V is recommended to keep the temperature coefficient of the 0.75V internal $V_{BE}$ from becoming a significant error term.

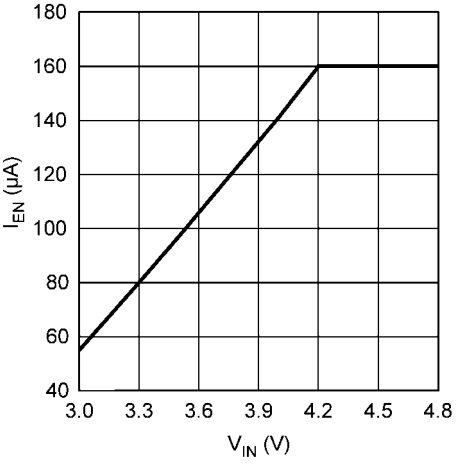



**FIGURE 14. Maximum Enable Current vs. Input Voltage**

Typical frequency response of the gain and the phase for the power stage are shown in *Figure 15* and *Figure 16*. It is designed for $V_{IN}$ = 12V, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 8A, $V_{EN}$ = 5V and a switching frequency of 500 kHz. The power stage component values are:

L = 2.7 µH, $R_L$ = 3.4 mΩ, $C_{O1}$ = 220 µF, $R_{C1}$ = 15 mΩ, $C_{O2}$ = 22 µF, $R_{C2}$ = 3 mΩ, $R_O = V_{OUT} / I_{OUT}$ = 0.41Ω, $R_S = R_{DS(on)}$ = 4 mΩ and $R_{EN}$ = 43 kΩ.

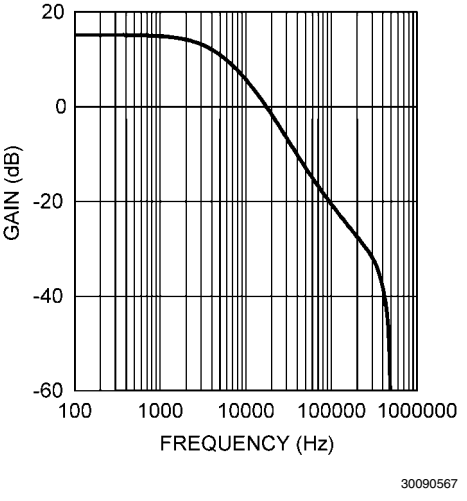



**FIGURE 15. Power Stage Gain**

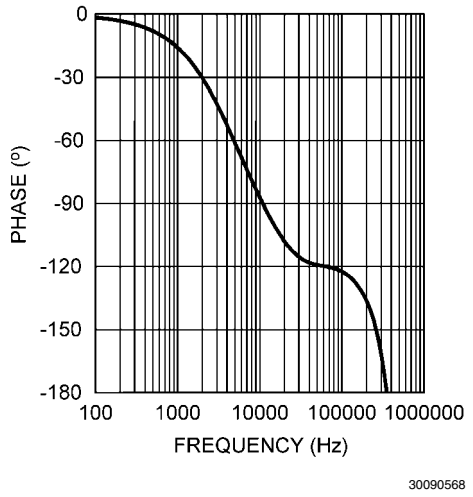



**FIGURE 16. Power Stage Phase**

The effective total PWM ramp height is controlled by $R_{EN}$. Higher $R_{EN}$ creates a higher ramp voltage, providing more noise immunity and less variation in the modulator gain over temperature. Lower $R_{EN}$ requires less $R_C$ (output capacitor ESR) for the desired phase margin and a more ideal current-mode behavior.

*Figure 17* shows the transconductance amplifier network, which takes the output impedance of the amplifier and the internal filter into account. To simplify the analysis, the 12.75 kΩ and 10 pF internal filter is absorbed into the transconductance amplifier. This produces an equivalent $R_{EA}$ = 15 MΩ and $C_{BW}$ = 22 pF for an effective 10 MHz unity gain bandwidth.

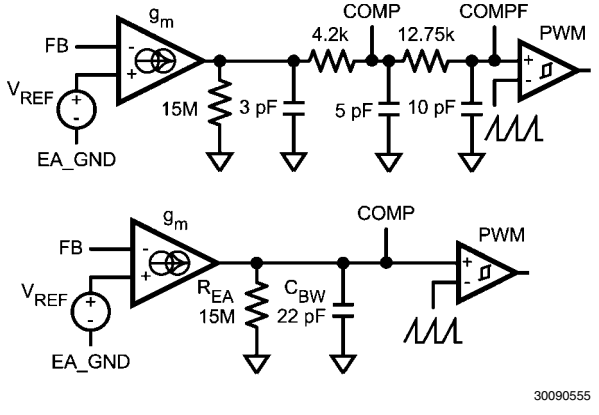



**FIGURE 17. Equivalent Transconductance Amplifier and COMP Filter**

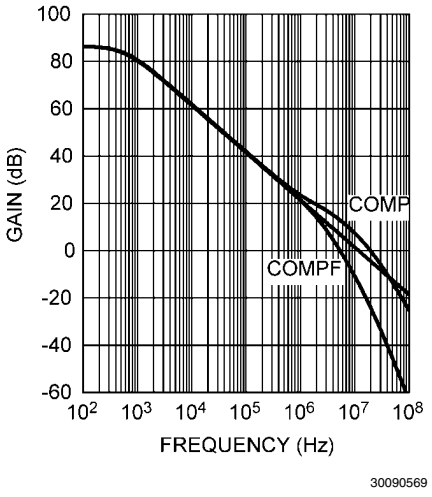



**FIGURE 18. Transconductance Amplifier Open Loop Gain**

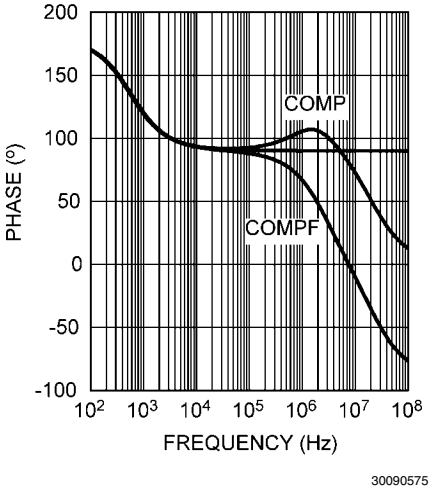



**FIGURE 19. Transconductance Amplifier Open Loop Phase**

Assuming a pole at the origin, the simplified equation for the error amplifier transfer function can be written in terms of the mid-band gain as:

$$\frac{\hat{v}_C}{\hat{v}_O} = -\frac{A_{VM}}{K_{HF}} \times \frac{1 + \frac{\omega_{ZEA}}{s}}{1 + \frac{s}{\omega_{FP}}} \times \frac{1 + \frac{s}{\omega_{FZ}}}{1 + \frac{s}{\omega_{HF}}}$$

Where:

$$A_{VM} = K_{FB} \times g_m \times R_{COMP} \qquad K_{FB} = \frac{R_{FBB}}{R_{FBB} + R_{FBT}}$$

$$K_{HF} = 1 + \frac{C_{HF} + C_{BW}}{C_{COMP}} \qquad \omega_{ZEA} = \frac{1}{C_{COMP} \times R_{COMP}}$$

$$\omega_{FZ} = \frac{1}{C_{FF} \times R_{FBT}} \qquad \omega_{FP} = \frac{1}{C_{FF} \times K_{FB} \times R_{FBT}}$$

$$\omega_{HF} = \frac{C_{HF} + C_{BW} + C_{COMP}}{(C_{HF} + C_{BW}) \times C_{COMP} \times R_{COMP}}$$

In general, the goal of the compensation circuit is to give high dc gain, a bandwidth that is between one-fifth and one-tenth of the switching frequency, and at least 45° of phase margin.

### Control Loop Design Procedure

Once the power stage design is complete, the power stage components are used to determine the proper frequency compensation. By equating the power stage transfer function to the error amplifier transfer function term by term, the control loop design procedure targets an ideal single-pole system response.

The compensation components will scale from the feedback divider ratio and selection of the bottom feedback divider resistor. A maximum value for the divider current is typically set at 1 mA. Using a divider current of 200 µA will allow for a reasonable range of values. For the bottom feedback resistor $R_{FBB} = V_{REF} / 200\ \mu A = 3\ k\Omega$. Choosing a standard 1% value of 2.94 kΩ, the top feedback resistor is found from:

$$R_{FBT} = R_{FBB} \times \left( \frac{V_{OUT}}{V_{REF}} - 1 \right)$$

For $V_{OUT} = 3.3V$ and $V_{REF} = 0.6V$, $R_{FBT} = 13.2\ k\Omega$.

Based on the previously defined power stage values, calculate general terms:

$$D = \frac{V_O}{V_{IN}} \qquad R_i = A \times R_S \qquad T = \frac{1}{f_{SW}}$$

$$K_{SW} = 1 + \frac{f_{SW}}{3400000} \qquad K_{FB} = \frac{R_{FBB}}{R_{FBB} + R_{FBT}}$$

For the design example D = 0.275, $R_i = 0.028\Omega$, T = 2 µs, $K_{SW} = 1.147$ and $K_{FB} = 0.1818$.

Choose a target crossover frequency $f_C$ greater than the minimum control loop bandwidth from the Output Capacitors section. This is typically set between 1/10 and 1/5 of the switching frequency.

$$\omega_C = 2 \times \pi \times f_C \qquad \omega_{SW} = 2 \times \pi \times f_{SW}$$

$$\omega_{BW} = 2 \times \pi \times f_{BW}$$

Choosing $f_C = 100$ kHz for the design example $\omega_C = 628$ krad/sec. The switching frequency $\omega_{SW} = 3.14$ Mrad/sec and the error amplifier bandwidth $\omega_{BW} = 62.8$ Mrad/sec.

Calculate the parallel equivalent $C_O$ and $R_C$ at the target crossover frequency:

$$C1 = C_{O1} \qquad R1 = R_{C1} \qquad C2 = C_{O2} \qquad R2 = R_{C2}$$

$$X1 = \frac{1}{\omega_C \times C1} \qquad X2 = \frac{1}{\omega_C \times C2}$$

$$Z = \frac{\sqrt{R1^2 + X1^2} \times \sqrt{R2^2 + X2^2}}{\sqrt{(R1 + R2)^2 + (X1 + X2)^2}}$$

$$A = TAN^{-1}\left(\frac{X1}{R1}\right) + TAN^{-1}\left(\frac{X2}{R2}\right) - TAN^{-1}\left(\frac{X1 + X2}{R1 + R2}\right)$$

$$C_O = \frac{1}{\omega_C \times Z \times SIN(A)} \qquad R_C = Z \times COS(A)$$

For the design example X1 = 0.00723, X2 = 0.0723, Z = 0.01478 and A = 0.6304. The parallel equivalent $C_O = 183$ µF and $R_C = 11.9\ m\Omega$.

Find the optimal value of the enable current:

$$I_{EN} = I_{SL} \times K_{SW} \times \frac{\frac{L}{C_O} \times \left( \frac{K_{FB}}{R_C} - \frac{1}{R_O} \right) + R_C \times \left( \frac{1}{K_{FB}} - 1 \right)}{R_i \times \left( 1 - \frac{R_C}{R_O \times K_{FB}} \right)}$$

If $I_{EN}$ is not within the range of 40µA to 160µA use either the minimum or maximum limit. Find $R_{EN}$ from:

$$R_{EN} = \frac{V_{EN} - 0.75}{I_{EN}} - 2000$$

For the design example $I_{EN} = 95.5\ \mu A$ and $R_{EN} = 44.7\ k\Omega$. Choosing a standard value of 43 kΩ, $I_{EN} = 94.4\ \mu A$.

Calculate other general terms:

$$K_{SL} = \frac{I_{SL} \times K_{SW}}{I_{EN}} \qquad K_m = \frac{1}{(D - 0.5) \times R_i \times \frac{T}{L} + K_{SL}}$$

$$K_D = 1 + \frac{K_m \times R_i}{R_O}$$

For the design example $K_{SL} = 0.0978$, $K_m = 10.7$ and $K_D = 1.73$.

If the enable resistor has been adjusted from the nominal value to provide more noise immunity or to meet the minimum input voltage limit, calculate the optimal value of $R_C$. The minimum value of $R_C$ to maintain adequate phase margin for stability is about half this value.

$$R_C = \frac{K_{FB} \times L}{K_m \times R_i \times C_O}$$

Checking for the design example $R_C = 9.1\ m\Omega$.

Calculate the compensation components:

$$C_{BW} = \frac{g_m}{\omega_{BW}} \qquad C_{FF} = \frac{C_O \times R_C}{K_{FB} \times R_{FBT}}$$

$$C_{HF} = \frac{g_m \times K_m \times R_C}{\omega_C \times \omega_{SW} \times L} - C_{BW}$$

$$C_{COMP} = \frac{K_{FB} \times g_m \times K_m}{\omega_C \times K_D} - (C_{HF} + C_{BW})$$

$$R_{COMP} = \frac{K_{FB} \times L}{K_D \times R_C \times C_{COMP}}$$

For the design example, the calculated values are $C_{BW}$ = 22 pF, $C_{FF}$ = 904 pF, $C_{HF}$ = 11 pF, $C_{COMP}$ = 2505 pF and $R_{COMP}$ = 9523Ω.

Using standard values of $C_{FF}$ = 820 pF, $C_{HF}$ = 10 pF, $C_{COMP}$ = 2200 pF and $R_{COMP}$ = 10 kΩ, the error amplifier plots of gain and phase are shown in *Figure 20* and *Figure 21*.

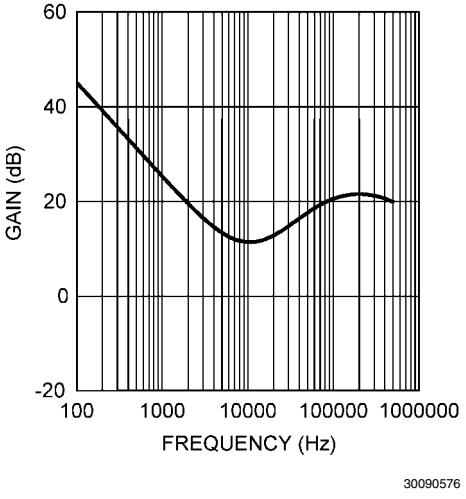



**FIGURE 20. Error Amplifier Gain**

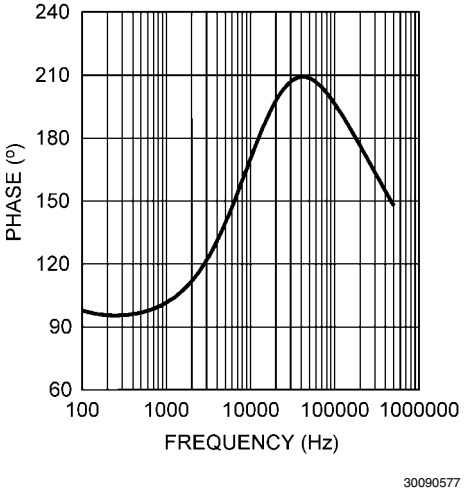



**FIGURE 21. Error Amplifier Phase**

The complete control loop transfer function is equal to the product of the power stage transfer function and error amplifier transfer function. For the Bode plots, the overall loop gain is the equal to the sum in dB and the overall phase is equal to the sum in degrees. Results are shown in *Figure 22* and *Figure 23*. The crossover frequency is 100 kHz with a phase margin of 75°.

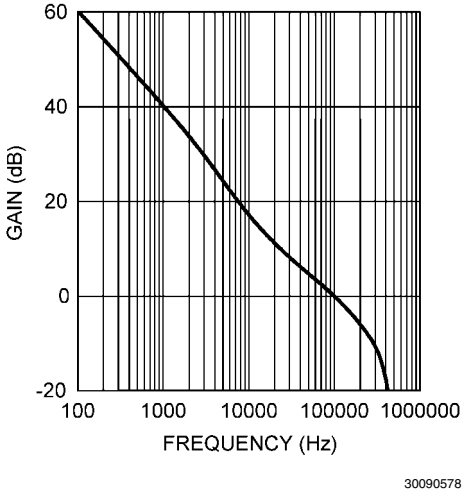



**FIGURE 22. Control Loop Gain**

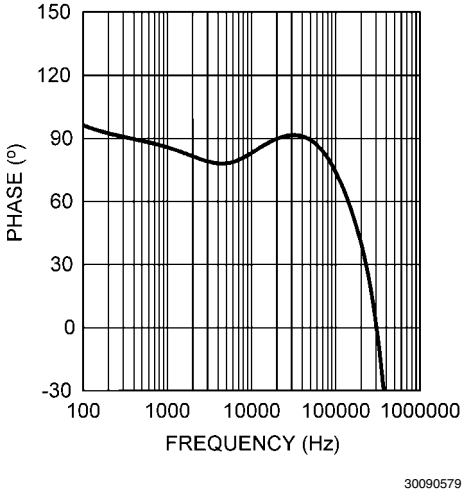



**FIGURE 23. Control Loop Phase**

Compensator design for the 1.2V output is similar. With $V_{REF}$ = 0.6V, the feedback divider resistors are chosen as $R_{FBB}$ = $R_{FBT}$ = 22.6 kΩ. This results in a divider current of about 25 µA, which is considered to be the minimum acceptable level. With $V_{EN}$ = 5V, the nearest standard value to meet the optimal enable current is $R_{EN}$ = 62 kΩ. For a target crossover frequency of 100 kHz, standard values are $C_{FF}$ = 220 pF, $C_{HF}$ = 10 pF, $C_{COMP}$ = 2200 pF and $R_{COMP}$ = 10 kΩ.

For the small-signal analysis, it is assumed that the control voltage at the COMP pin is dc. In practice, the output ripple voltage is amplified by the error amplifier gain at the switching frequency, which appears at the COMP pin adding to the control ramp. This tends to reduce the modulator gain, which may lower the actual control loop crossover frequency.

# Efficiency and Thermal Considerations

The total power dissipated in the power components can be obtained by adding together the loss as mentioned in the MOSFET, input capacitor, output capacitor and output inductor sections.

The efficiency is defined as:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{TOTAL_LOSS}}$$

The highest power dissipating components are the power MOSFETs. The easiest way to determine the power dissipated in the MOSFETs is to measure the total conversion loss ($P_{IN}$ - $P_{OUT}$), then subtract the power loss in the capacitors, inductors and LM3000. The resulting power loss is primarily in the switching MOSFETs. Selecting MOSFETs with exposed pads will aid the power dissipation of these devices. Careful attention to $R_{DS(on)}$ at high temperature should be observed.

### LM3000 OPERATING LOSS

This term accounts for the current drawn at the VIN pin, used for driving the logic circuitry and the power MOSFETs. For the LM3000, this current is equal to the steady state operating current $I_q$ plus the MOSFET gate charge current $I_{GC}$, which is defined as:

$$I_{GC} = (Q_{G_HI} + Q_{G_LO}) \times f_{SW}$$

$$P_D = V_{IN} \times (I_q + I_{GC})$$

Where $P_D$ represents the total power dissipated in the LM3000. $I_q$ is about 5 mA from the Electrical Characteristics table. The LM3000 has an exposed thermal pad to aid power dissipation.

# Layout Considerations

To produce an optimal power solution with a switching converter, as much care must be taken with the layout and design of the printed circuit board as with the component selection. The following are several guidelines to aid in creating a good layout.

### KELVIN TRACES FOR GATE DRIVE AND SENSE LINES

The HG and SW pins provide the gate drive and return for the high-side MOSFET. Likewise the LG and PGND pins provide the gate drive and return for the low-side MOSFET. These lines should run as parallel pairs to each MOSFET, being connected as close as possible to the respective MOSFET gate and source. Although it may be difficult in a compact design, these lines should stay away from the output inductor if possible, to avoid stray coupling.

The EA_GND pins should also be connected with a separate Kelvin trace, running from the output ground sense point. The sense output, which is connecting to the top of the feedback resistor divider, should also run with a dedicated Kelvin trace together with the EA_GND. Keep these lines away from the switch node and output inductor to avoid stray coupling. If possible, the FB and EA_GND traces should be shielded from the switch node by ground planes. If necessary, the feedback divider impedance may be lowered to improve noise immunity.

### SEPARATE PGND AND SGND

Good layout techniques include a dedicated signal ground plane, usually on an internal layer adjacent to the LM3000 and signal component side of the board. Signal level components like the compensation and feedback resistors should be connected to this internal plane. The SGND pin should connect directly to the DAP, with vias from the DAP to the signal ground plane. Separate power ground plane areas for each phase should be made on the power component side of the board, as well as other layers. This allows separate lines for each PGND pin to connect to its respective power ground plane area at each low-side MOSFET source. The signal ground plane is then connected to a quiet point on each power ground plane area. These connections are typically made at the common input/output power terminals or capacitor returns. An equivalent schematic representation is shown in the Typical Application Schematic of *Figure 24*.

### MINIMIZE THE SWITCH NODE

The copper area that connects the power MOSFETs and output inductor together radiates more EMI as it gets larger. Use just enough copper to give low impedance for the switching currents and provide adequate heat spreading for the MOSFETs.

### LOW IMPEDANCE POWER PATH

In a buck regulator the primary switching loop consists of the input capacitor connection to the MOSFETs. Minimizing the area of this loop reduces the stray inductance, which minimizes noise and possible erratic operation. The ceramic input capacitors should be placed as close as possible to the MOSFETs, with the VIN side of the capacitors connected directly to the high-side MOSFET drain, and the PGND side of the capacitors connected as close as possible to the low-side source. The complete power path includes the input capacitors, power MOSFETs, output inductor, and output capacitors. Keep these components on the same side of the board and connect them with thick traces or copper planes. Avoid connecting these components through vias whenever possible, as vias add inductance and resistance. In general, the power components should be kept close together, minimizing the circuit board losses.

## Typical Application

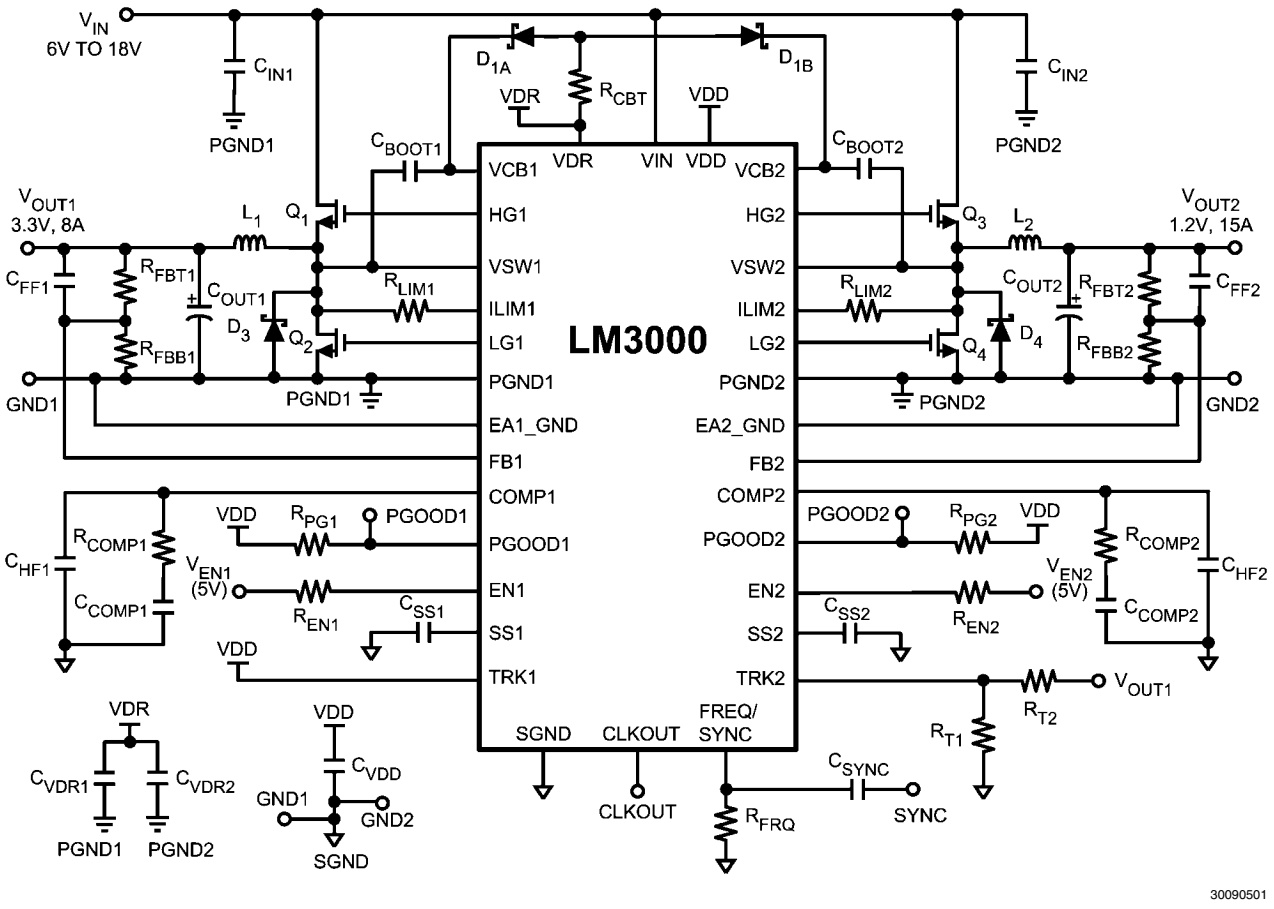
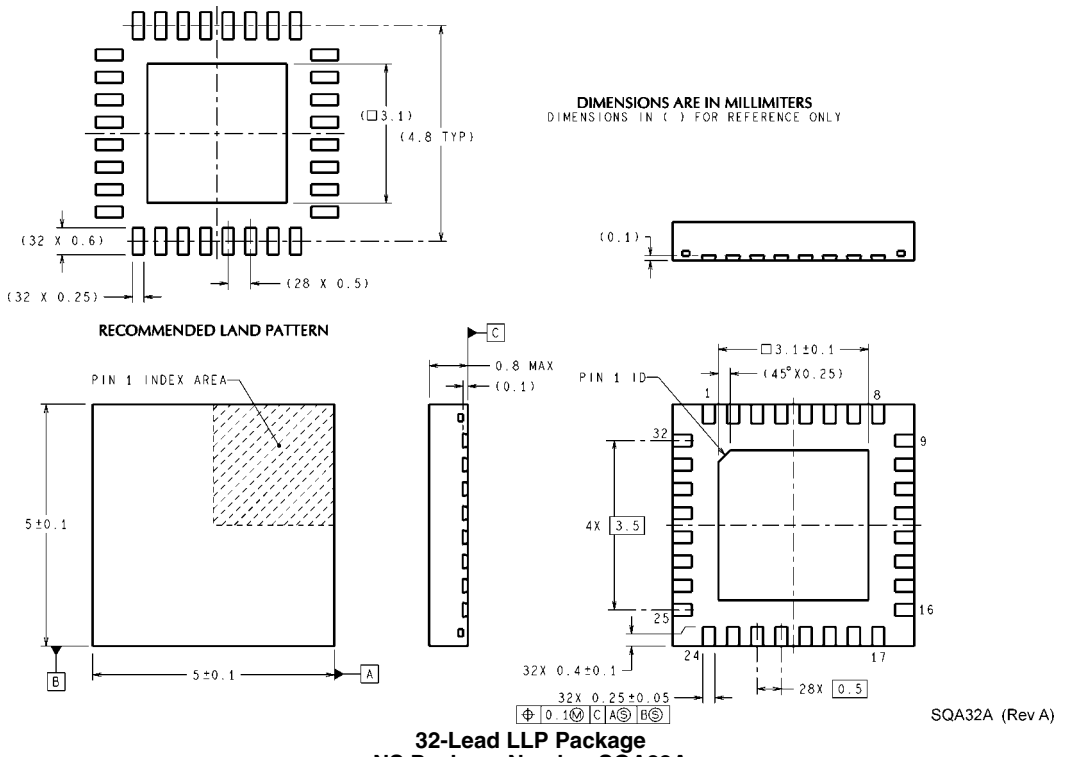



**FIGURE 24. Typical Application Schematic**

## Physical Dimensions inches (millimeters) unless otherwise noted




**32-Lead LLP Package**
**NS Package Number SQA32A**

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