LM27965 Dual Display White LED Driver with I2C Compatible Brightness Control

Check for Samples: LM27965

FEATURES

- **91% Peak LED Drive Efficiency**
- **No Inductor Required**
- **0.3% Current Matching**
- **Drives LEDs with up to 30mA per LED**
- **180mA of total drive current**
- **I^2C Compatible Brightness Control Interface**
- **Adaptive 1× - 3/2× Charge Pump**
- **Resistor-Programmable Current Settings**
- **External Chip $\overline{\text{RESET}}$ Pin**
- **Extended Li-Ion Input: 2.7V to 5.5V**
- **Small low profile industry standard leadless package, WQFN 24 : (4mm x 4mm x 0.8mm)**
- **25mm^2 total solution size**
- **Two I^2C Compatible Chip Address Options: 0x36 for LM27965SQ and 0x38 for LM27965SQ-M**

APPLICATIONS

- **Mobile Phone Display Lighting**
- **PDA Backlighting**
- **General LED Lighting**

DESCRIPTION

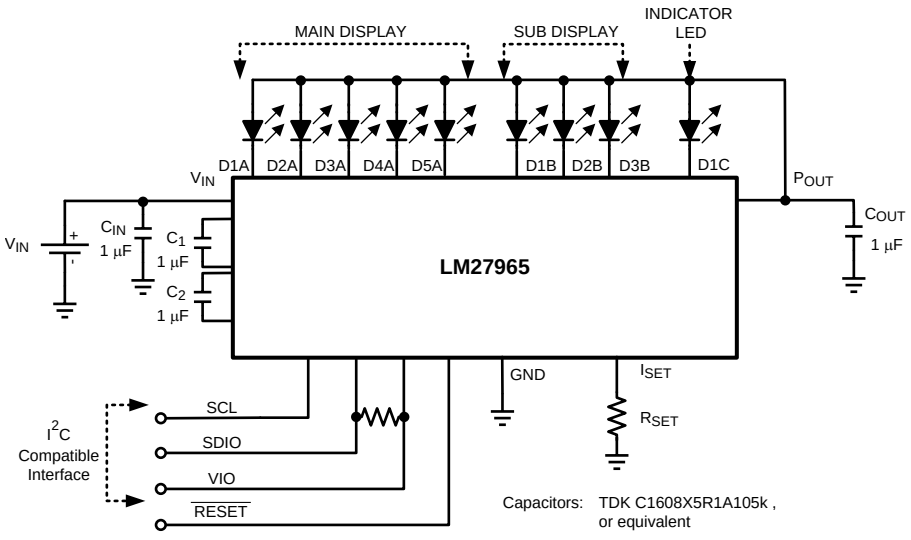
The LM27965 is a highly integrated charge-pump-based dual-display LED driver. The device can drive up to 9 LEDs in parallel with a total output current of 180mA. Regulated internal current sinks deliver excellent current and brightness matching in all LEDs.

The LED driver current sinks are split into three independently controlled groups. The primary group can beconfigurabled with 4 or 5 LEDs, for backlighting a larger main display and the second group can be configured with 2 or 3 LEDs, for backlighing a smaller secondary display. An additional, independently controlled led driver is provided for driving an indicator or general purpose LED. The LM27965 has an I^2C compatible interface that allows the user to independently control the brightness on each bank of LEDs.

The device provides excellent efficiency without the use of an inductor by operating the charge pump in a gain of 3/2, or in Pass-Mode. The proper gain for maintaining current regulation is chosen based on LED forward voltage, so that efficiency is maximized over the input voltage range.

The LM27965 is available in a small 24-pin WQFN-24 package.

TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

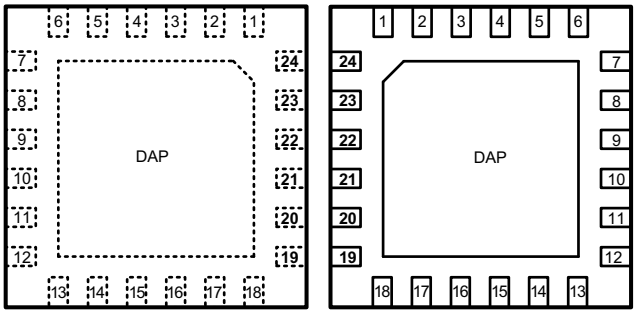
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CONNECTION DIAGRAM

24 Pin WQFN Package
See Package Number RTW0024A



Top View Bottom View

Pin Functions

Pin Descriptions

Pin Name	Pin No.	Pin Descriptions
V_{IN}	24	Input voltage. Input range: 2.7V to 5.5V.
P_{OUT}	23	Charge Pump Output Voltage
C1, C2	19, 22 (C1) 20, 21 (C2)	Flying Capacitor Connections
D5A, D4A, D3A, D2A, D1A	12, 13, 14, 15, 16	LED Drivers - GroupA
D1B, D2B, D3B	4, 5, 6	LED Drivers - GroupB
D1C	3	LED Driver - Indicator LED
I_{SET}	17	Placing a resistor (R_{SET}) between this pin and GND sets the full-scale LED current for DxA , DxB, and D1C LEDs. Full-Scale LED Current = 200 × (1.25V ÷ R_{SET})
SCL	1	Serial Clock Pin
SDIO	2	Serial Data Input/Output Pin
VIO	7	Serial Bus Voltage Level Pin
$\overline{RESET}$	10	Harware Reset Pin. High = Normal Operation, Low = RESET
GND	9, 18, DAP	Ground
NC	8, 11	No Connect

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1) (2) (3)

V_{IN} pin voltage	-0.3V to 6.0V
SCL, SDIO, VIO, $\overline{\text{RESET}}$ pin voltages	-0.3V to (V_{IN}+0.3V) w/ 6.0V max
I_{Dxx} Pin Voltages	-0.3V to (V_{POUT}+0.3V) w/ 6.0V max
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T_{J-MAX})	150ºC
Storage Temperature Range	-65ºC to +150º C
Maximum Lead Temperature (Soldering)	(5)
ESD Rating (6) Human Body Model	2.0kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 170°C (typ.) and disengages at T_J = 165°C (typ.).
(5) For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1187: Leadless Leadframe Package (AN-1187).
(6) The human body model is a 100pF capacitor discharged through 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7)

Operating Rating (1) (2)

Input Voltage Range	2.7V to 5.5V
LED Voltage Range	2.0V to 4.0V
Junction Temperature (T_J) Range	-30°C to +100°C
Ambient Temperature (T_A) Range (3)	-30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 100°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), RTW0024A Package (1)	41.3°C/W

(1) Junction-to-ambient thermal resistance is highly dependent on application and board layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. For more information, please refer to National Semiconductor Application Note 1187: Leadless Leadframe Package (AN-1187).

Electrical Characteristics (1) (2)

Limits in standard typeface are for T_J = 25°C, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 3.6V; $V_{\overline{RESET}} = V_{IN}$; VIO = 1.8V $V_{DxA} = V_{DxB} = V_{DxC}$ = 0.4V; R_{SET} = 12.7kΩ; BankA = BankB = BankC = Fullscale Current; ENA, ENB, ENC, EN5A, EN3B Bits = “1”; C1 = C2 = C_{IN}= C_{OUT}= 1.0µF; Specifications related to output current(s) and current setting pins (I_{Dxx} and I_{SET}) apply to BankA and BankB. (3)

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(3) C_{IN}, C_{POUT}, C_1, and C_2 : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics

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Electrical Characteristics[1] [2] (continued)

Limits in standard typeface are for T_J = 25°C, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 3.6V; $V_{\overline{RESET}}$ = V_{IN}; VIO = 1.8V V_{DxA} = V_{DxB} = V_{DxC} = 0.4V; R_{SET} = 12.7kΩ; BankA = BankB = BankC = Fullscale Current; ENA, ENB, ENC, EN5A, EN3B Bits = "1"; C1 = C2 = C_{IN}= C_{OUT}= 1.0µF; Specifications related to output current(s) and current setting pins (I_{Dxx} and I_{SET}) apply to BankA and BankB. [3]

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{Dxx}	Output Current Regulation BankA or BankB Enabled	3.0V ≤ V_{IN} ≤ 5.5V ENA = '1' or ENB = '1' and ENC= '0'		**18.2 (-9.5%)**	20.1	**22.0 (+9.5%)**	mA (%)
	Output Current Regulation BankC Enabled	3.0V ≤ V_{IN} ≤ 5.5V ENC = '1' and ENA = ENB= '0'		**19.2 (-7.7%)**	20.8	**22.4 (+7.7%)**	mA (%)
	Maximum Diode Current per Dxx Output[4]	R_{SET} = 8.33kΩ			30		mA
	Output Current Regulation BankA, BankB, and BankC Enabled [4]	3.2V ≤ V_{IN} ≤ 5.5V V_{LED} = 3.6V			20 DxA		mA
					20 DxB		
					20 DxC		
$I_{Dxx-MATCH}$	LED Current Matching[5]	3.0V ≤ V_{IN} ≤ 5.5V	BankA		0.3	**1.7**	%
			BankB		0.3	**1.4**	
R_{OUT}	Open-Loop Charge Pump Output Resistance	Gain = 3/2			2.75		Ω
		Gain = 1			1		
V_{DxTH}	V_{Dxx} 1x to 3/2x Gain Transition Threshold	V_{DxA} and/or V_{DxB} Falling R_{SET} = 16.9kΩ			175		mV
V_{HR}	Current sink Headroom Voltage Requirement [6]	I_{Dxx} = 95% ×I_{Dxx} (nom.) (I_{Dxx} (nom) ≈ 15mA) R_{SET} = 16.9kΩ			110		mV
I_Q	Quiescent Supply Current	Gain = 1.5x, No Load			2.90	**3.32**	mA
I_{SD}	Shutdown Supply Current	All ENx bits = "0"			3.4	**5.4**	µA
V_{SET}	I_{SET} Pin Voltage	2.7V ≤ V_{IN} ≤ 5.5V			1.25		V
$I_{DxA-B-C}$ / I_{SET}	Output Current to Current Set Ratio BankA, BankB, BankC				200		
f_{SW}	Switching Frequency			**0.89**	1.27	**1.57**	MHz
t_{START}	Start-up Time	P_{OUT} = 90% steady state			250		µs
f_{PWM}	Internal Diode Current PWM Frequency				20		kHz
$V_{\overline{RESET}}$	Reset Voltage Thresholds	2.7V ≤ V_{IN} ≤ 5.5V	Reset	**0**		**0.45**	V
			Normal Operation	**1.2**		**V_{IN}**	
I^2C Compatible Interface Voltage Specifications (SCL, SDIO, VIO)							
V_{IO}	Serial Bus Voltage Level	2.7V ≤ V_{IN} ≤ 5.5V [7]		**1.4**		**V_{IN}**	V
V_{IL}	Input Logic Low "0"	2.7V ≤ V_{IN} ≤ 5.5V, VIO= 3.0V		**0**		**0.3 × V_{IO}**	V
V_{IH}	Input Logic High "1"	2.7V ≤ V_{IN} ≤ 5.5V, VIO= 3.0V		**0.7 × V_{IO}**		**V_{IO}**	V
V_{OL}	Output Logic Low "0"	I_{LOAD} = 3mA				**400**	mV

(4) The maximum total output current for the LM27965 should be limited to 180mA. The total output current can be split among any of the three banks (I_{DxA} = I_{DxB} = I_{DxC} = 30mA Max.). Under maximum output current conditions, special attention must be given to input voltage and LED forward voltage to ensure proper current regulation. See the Maximum Output Current section of the datasheet for more information.

(5) For the two groups of current sinks on a part (BankA and BankB), the following are determined: the maximum sink current in the group (MAX), the minimum sink current in the group (MIN), and the average sink current of the group (AVG). For each group, two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN)/AVG. The largest number of the two (worst case) is considered the matching figure for the bank. The matching figure for a given part is considered to be the highest matching figure of the two banks. The typical specification provided is the most likely norm of the matching figure for all parts.

(6) For each Dxxpin, headroom voltage is the voltage across the internal current sink connected to that pin. For Group A, B, and C current sinks, V_{HRx} = V_{OUT} -V_{LED}. If headroom voltage requirement is not met, LED current regulation will be compromised.

(7) SCL and SDIO signals are referenced to VIO and GND for minimum VIO voltage testing.

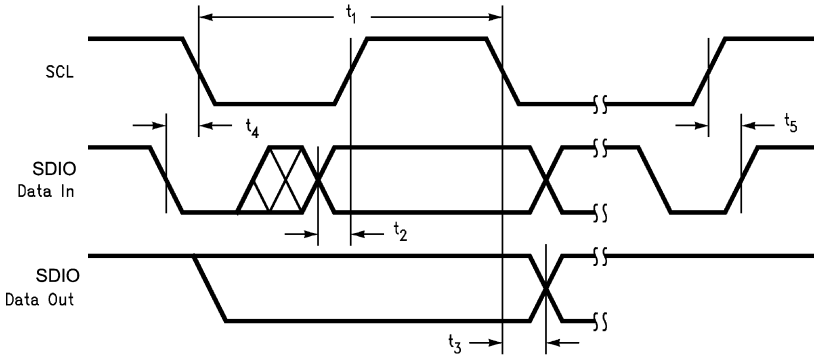
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Electrical Characteristics[1] [2] (continued)

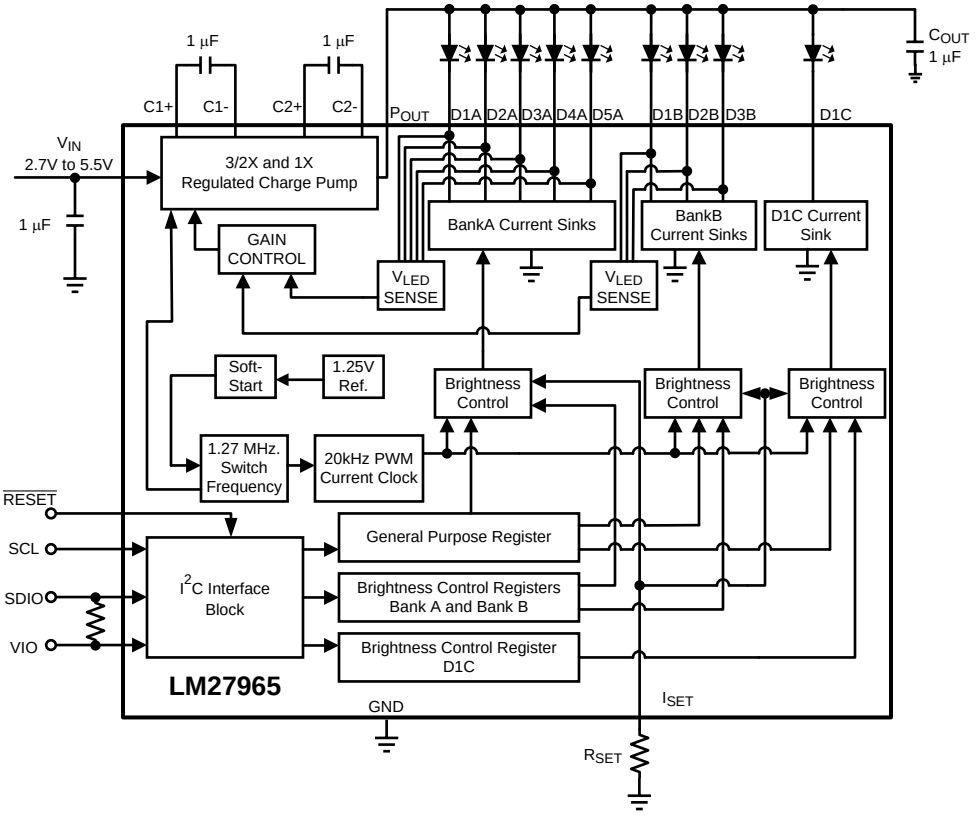
Limits in standard typeface are for T_J = 25°C, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 3.6V; $V_{\overline{RESET}} = V_{IN}$; VIO = 1.8V $V_{DxA} = V_{DxB} = V_{DxC}$ = 0.4V; R_{SET} = 12.7kΩ; BankA = BankB = BankC = Fullscale Current; ENA, ENB, ENC, EN5A, EN3B Bits = "1"; C1 = C2 = C_{IN}= C_{OUT}= 1.0µF; Specifications related to output current(s) and current setting pins (I_{Dxx} and I_{SET}) apply to BankA and BankB. [3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I^2C Compatible Interface Timing Specifications (SCL, SDIO, VIO)[8]						
t_1	SCL (Clock Period)		**2.5**			µs
t_2	Data In Setup Time to SCL High		**100**			ns
t_3	Data Out stable After SCL Low		**0**			ns
t_4	SDIO Low Setup Time to SCL Low (Start)		**100**			ns
t_5	SDIO High Hold Time After SCL High (Stop)		**100**			ns

(8) SCL and SDIO should be glitch-free in order for proper brightness control to be realized.



BLOCK DIAGRAM



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Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; $V_{\overline{RESET}} = V_{IN}$; $V_{LEDxA} = V_{LEDxB} = V_{LED1C}$ = 3.6V; R_{SET} = 16.9kΩ; C_1=C_2= C_{IN} = C_{POUT} = 1µF; ENA = ENB = ENC =EN5A = EN3B = '1'.

LED Drive Efficiency vs Input Voltage

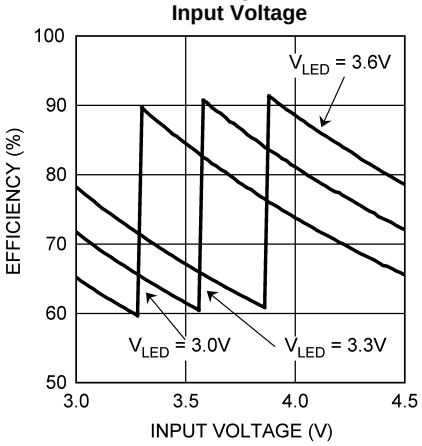


Figure 1.

Input Current vs Input Voltage

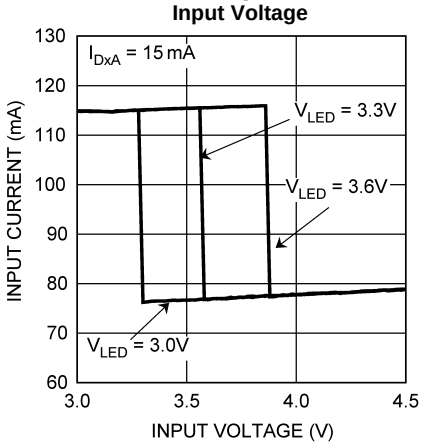


Figure 2.

BankA Current Regulation vs Input Voltage

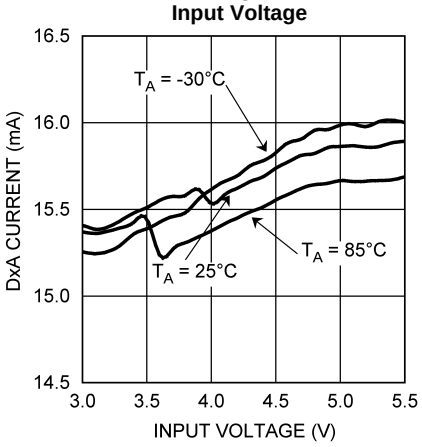


Figure 3.

BankB Current Regulation vs Input Voltage

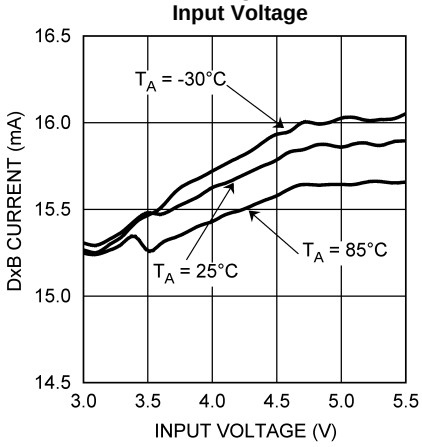


Figure 4.

BankC Current Regulation vs Input Voltage

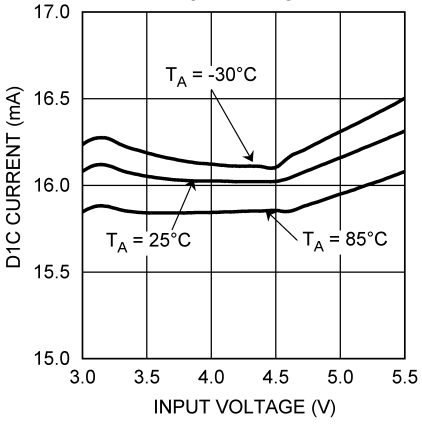


Figure 5.

BankA Current Matching vs Input Voltage

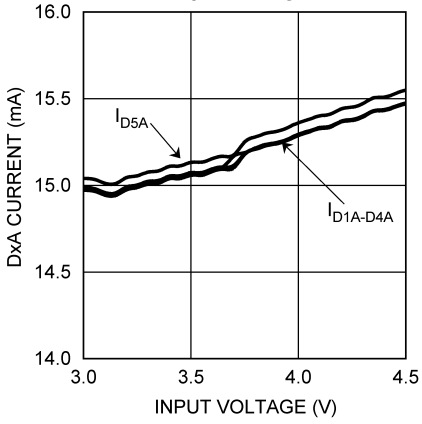


Figure 6.

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Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; $V_{\overline{RESET}}$ = V_{IN}; V_{LEDxA} = V_{LEDxB} = V_{LED1C} = 3.6V; R_{SET} = 16.9kΩ; C_1=C_2= C_{IN} = C_{POUT} = 1µF; ENA = ENB = ENC =EN5A = EN3B = '1'.

BankB Current Matching vs Input Voltage

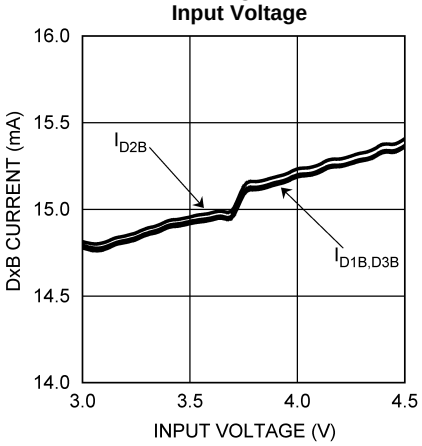


Figure 7.

BankA Diode Current vs Brightness Register Code

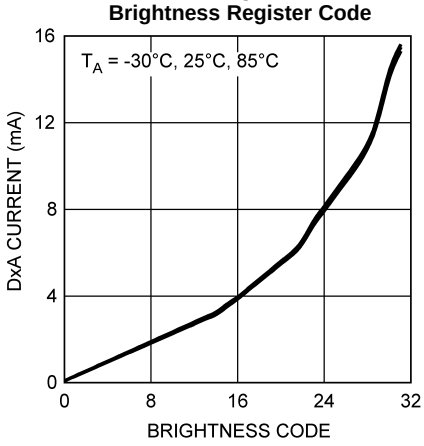


Figure 8.

BankB Diode Current vs Brightness Register Code

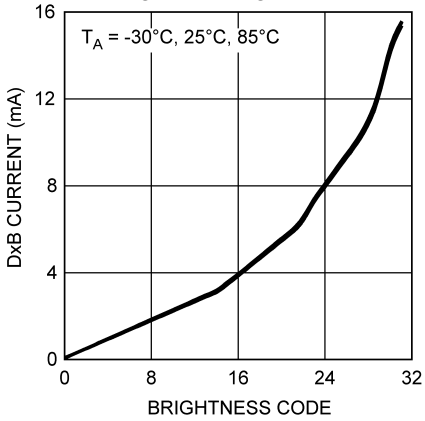


Figure 9.

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CIRCUIT DESCRIPTION

OVERVIEW

The LM27965 is a white LED driver system based upon an adaptive 3/2× - 1× CMOS charge pump capable of supplying up to 180mA of total output current. With three separately controlled banks of constant current sinks, the LM27965 is an ideal solution for platforms requiring a single white LED driver for main display, sub display, and indicator lighting. The tightly matched current sinks ensure uniform brightness from the LEDs across the entire small-format display.

Each LED is configured in a common anode configuration, with the peak drive current being programmed through the use of an external R_{SET} resistor. An I^2C compatible interface is used to enable the device and vary the brightness within the individual current sink banks. For BankA and BankB, 32 levels of brightness control are available. The brightness control is achieved through a mix of analog and pulse width modulated (PWM) methods. BankC has 4 analog brightness levels available.

CIRCUIT COMPONENTS

Charge Pump

The input to the 3/2× - 1x charge pump is connected to the V_{IN} pin, and the regulated output of the charge pump is connected to the V_{OUT} pin. The recommended input voltage range of the LM27965 is 3.0V to 5.5V. The device's regulated charge pump has both open loop and closed loop modes of operation. When the device is in open loop, the voltage at V_{OUT} is equal to the gain times the voltage at the input. When the device is in closed loop, the voltage at V_{OUT} is regulated to 4.6V (typ.). The charge pump gain transitions are actively selected to maintain regulation based on LED forward voltage and load requirements.

LED Forward Voltage Monitoring

The LM27965 has the ability to switch converter gains (1x or 3/2x) based on the forward voltage of the LED load. This ability to switch gains maximizes efficiency for a given load. Forward voltage monitoring occurs on all diode pins within BankA and BankB. At higher input voltages, the LM27965 will operate in pass mode, allowing the P_{OUT} voltage to track the input voltage. As the input voltage drops, the voltage on the DXX pins will also drop ($V_{DXX} = V_{POUT} - V_{LEDx}$). Once any of the active Dxx pins reaches a voltage approximately equal to 175mV, the charge pump will switch to the gain of 3/2. This switch-over ensures that the current through the LEDs never becomes pinched off due to a lack of headroom across the current sinks.

Only active Dxx pins will be monitored. For example, if only BankA is enabled, the LEDs in BankB will not affect the gain transition point. If both banks are enabled, all diodes will be monitored, and the gain transition will be based upon the diode with the highest forward voltage. Diode pins D5A and D3B can have the diode sensing circuity disabled through the general purpose register if those drivers are not going to be used.

BankC (D1C) is not a monitored LED current sink.

$\overline{\text{RESET}}$ Pin

The LM27965 has a hardware reset pin ($\overline{\text{RESET}}$) that allows the device to be disabled by an external controller without requiring an I^2C write command. Under normal operation, the $\overline{\text{RESET}}$ pin should be held high (logic '1') to prevent an unwanted reset. When the $\overline{\text{RESET}}$ is driven low (logic '0'), all internal control registers reset to the default states and the part becomes disabled. Please see the *Electrical Characteristics* section of the datasheet for required voltage thresholds.

I^2C Compatible Interface

DATA VALIDITY

The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

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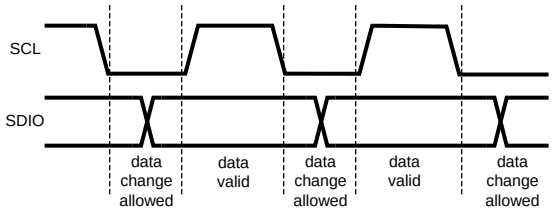


Figure 10. Data Validity Diagram

A pull-up resistor between VIO and SDIO must be greater than [**(VIO-V_{OL}) / 3mA**] to meet the V_{OL} requirement on SDIO. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

START AND STOP CONDITIONS

START and STOP conditions classify the beginning and the end of the I^2C session. A START condition is defined as SDIO signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDIO transitioning from LOW to HIGH while SCL is HIGH. The I^2C master always generates START and STOP conditions. The I^2C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I^2C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

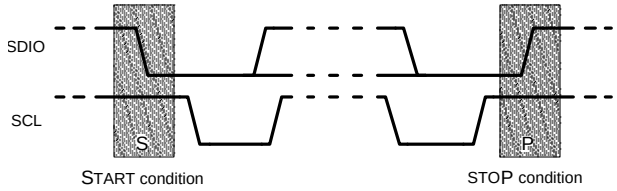


Figure 11. Start and Stop Conditions

TRANSFERING DATA

Every byte put on the SDIO line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDIO line (HIGH) during the acknowledge clock pulse. The LM27965 pulls down the SDIO line during the 9th clock pulse, signifying an acknowledge. The LM27965 generates an acknowledge after each byte is received.

After the START condition, the I^2C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM27965 address is 36h (38h for -M version). For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

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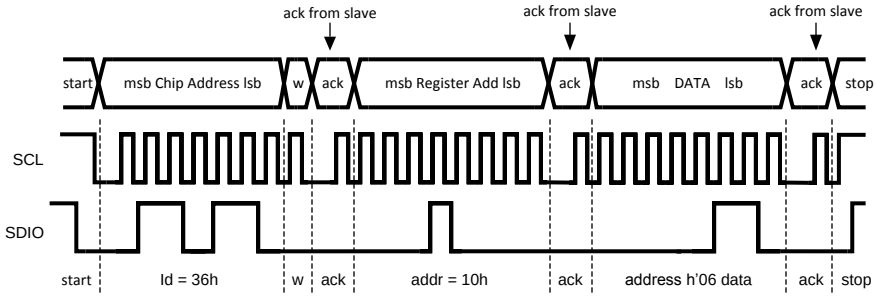


Figure 12. Write Cycle
w = write (SDIO = "0")
r = read (SDIO = "1")
ack = acknowledge (SDIO pulled down by either master or slave)
id = chip address, 36h for LM27965 or 38h for LM27965-M

I²C COMPATIBLE CHIP ADDRESS

The chip address for LM27965 is 0110110, or 36h. The chip address for LM27965-M is 0111000, or 38h.

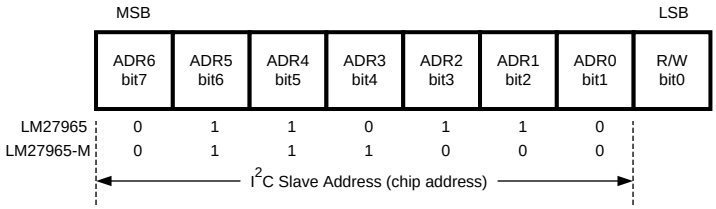


Figure 13. Chip Address

INTERNAL REGISTERS OF LM27965

Register	Internal Hex Address	Power On Value
General Purpose Register	10h	0010 0000
Bank A Brightness Control Register	A0h	1110 0000
Bank B Brightness Control Register	B0h	1110 0000
Bank C Brightness Control Register	C0h	1111 1100

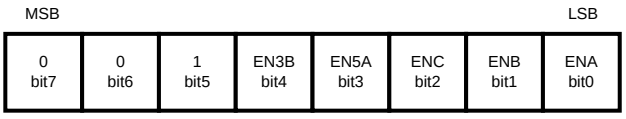


Figure 14. General Purpose Register Description
Internal Hex Address: 10h

NOTE

ENA: Enables DxA LED drivers (Main Display)

ENB: Enables DxB LED drivers (Aux Lighting)

ENC: Enables D1C LED driver (Indicator Lighting)

EN5A: Enables D5A LED voltage sense

EN3B: Enables D3B LED driver and voltage sense

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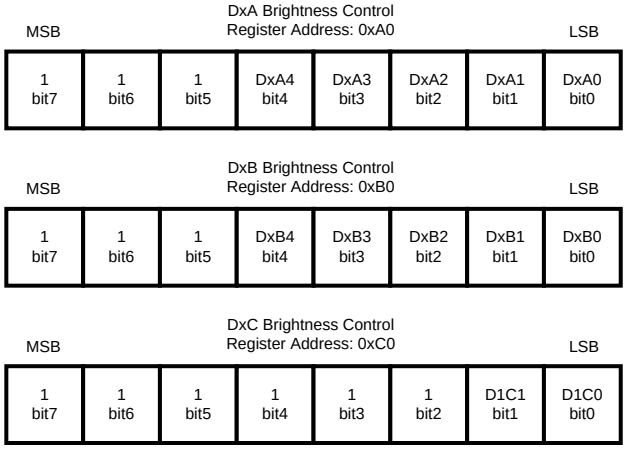


Figure 15. Brightness Control Register Description
Internal Hex Address: 0xA0 (BankA), 0xB0 (BankB), 0xC0 (BankC)

NOTE

DxA4-DxA0: Sets Brightness for DxA pins (BankA). 11111=Fullscale

DxB4-DxB0: Sets Brightness for DxB pins (BankB). 11111=Fullscale

Bit7 to Bit 5: Not Used

DxC1-DxC0: Sets Brightness for DxC pin. 11 = Fullscale

Bit7 to Bit2:Not Used

Full-Scale Current set externally by the following equation:

$$I_{Dxx} = 200 \times 1.25V / R_{SET}$$

Table 1. Brightness Level Control Table (BankA and BankB)

Brightness Code (hex)	Analog Current (% of Full-Scale)	Duty Cycle (%)	Perceived Brightness Level (%)
00	20	1/16	1.25
01	20	2/16	2.5
02	20	3/16	3.75
03	20	4/16	5
04	20	5/16	6.25
05	20	6/16	7.5
06	20	7/16	8.75
07	20	8/16	10
08	20	9/16	11.25
09	20	10/16	12.5
0A	20	11/16	13.75
0B	20	12/16	15
0C	20	13/16	16.25
0D	20	14/16	17.5
0E	20	15/16	18.75
0F	20	16/16	20
10	40	10/16	25
11	40	11/16	27.5
12	40	12/16	30

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Table 1. Brightness Level Control Table (BankA and BankB) (continued)

Brightness Code (hex)	Analog Current (% of Full-Scale)	Duty Cycle (%)	Perceived Brightness Level (%)
13	40	13/16	32.5
14	40	14/16	35
15	40	15/16	37.5
16	40	16/16	40
17	70	11/16	48.125
18	70	12/16	52.5
19	70	13/16	56.875
1A	70	14/16	61.25
1B	70	15/16	65.625
1C	70	16/16	70
1D	100	13/16	81.25
1E	100	15/16	93.75
1F	100	16/16	100

BankC Brightness Levels (%of Full-Scale) = 20%, 40%, 70%, 100%

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APPLICATION INFORMATION

SETTING LED CURRENT

The current through the LEDs connected to DxA and DxB can be set to a desired level simply by connecting an appropriately sized resistor (R_{SET}) between the I_{SET} pin of the LM27965 and GND. The DxA and DxB LED currents are proportional to the current that flows out of the I_{SET} pin and are a factor of 200 times greater than the I_{SET} current. The feedback loops of the internal amplifiers set the voltage of the I_{SET} pin to 1.25V (typ.). The statements above are simplified in the equations below:

$$I_{DxA/B/C}\ (A) = 200 \times (V_{ISET} / R_{SET}) \quad (1)$$

$$R_{SET}\ (\Omega) = 200 \times (1.25V / I_{DxA/B/C}) \quad (2)$$

Once the desired R_{SET} value has been chosen, the LM27965 has the ability to internally dim the LEDs using a mix of Pulse Width Modulation (PWM) and analog current scaling. The PWM duty cycle is set through the I^2C compatible interface. LEDs connected to BankA and BankB current sinks (DxA and DxB) can be dimmed to 32 different levels/duty-cycles. The internal PWM frequency for BankA and BankB is fixed at 20kHz. BankC(D1C) has 4 analog current levels.

Please refer to the I^2C Compatible Interface section of this datasheet for detailed instructions on how to adjust the brightness control registers.

MAXIMUM OUTPUT CURRENT, MAXIMUM LED VOLTAGE, MINIMUM INPUT VOLTAGE

The LM27965 can drive 8 LEDs at 22.5mA each (BankA and BankB) from an input voltage as low as 3.2V, so long as the LEDs have a forward voltage of 3.6V or less (room temperature).

The statement above is a simple example of the LED drive capabilities of the LM27965. The statement contains the key application parameters that are required to validate an LED-drive design using the LM27965: LED current (I_{LEDx}), number of active LEDs (N_x), LED forward voltage (V_{LED}), and minimum input voltage (V_{IN-MIN}).

The equation below can be used to estimate the maximum output current capability of the LM27965:

$$I_{LED_MAX} = [(1.5 \times V_{IN}) - V_{LED} - (I_{ADDITIONAL} \times R_{OUT})] / [(N_x \times R_{OUT}) + k_{HRx}] \quad (3)$$

$$I_{LED_MAX} = [(1.5 \times V_{IN}) - V_{LED} - (I_{ADDITIONAL} \times 2.75\Omega)] / [(N_x \times 2.75\Omega) + k_{HRx}] \quad (4)$$

$I_{ADDITIONAL}$ is the additional current that could be delivered to the other LED banks.

R_{OUT} – Output resistance. This parameter models the internal losses of the charge pump that result in voltage droop at the pump output P_{OUT}. Since the magnitude of the voltage droop is proportional to the total output current of the charge pump, the loss parameter is modeled as a resistance. The output resistance of the LM27965 is typically 2.75Ω (V_{IN} = 3.6V, T_A = 25°C). In equation form:

$$V_{POUT} = (1.5 \times V_{IN}) – [(N_A \times I_{LEDA} + N_B \times I_{LEDB}) \times R_{OUT}] \quad (5)$$

k_{HR} – Headroom constant. This parameter models the minimum voltage required to be present across the current sinks for them to regulate properly. This minimum voltage is proportional to the programmed LED current, so the constant has units of mV/mA. The typical k_{HR} of the LM27965 is 8mV/mA. In equation form:

$$(V_{POUT} – V_{LEDx}) > k_{HRx} \times I_{LEDx} \quad (6)$$

Typical Headroom Constant Values

$$k_{HRA} = 8mV/mA \quad (7)$$

$$k_{HRB} = 8mV/mA \quad (8)$$

Equation 3 is obtained from combining the R_{OUT} Equation 5 with the k_{HRx} Equation 6 and solving for I_{LEDx}. Maximum LED current is highly dependent on minimum input voltage and LED forward voltage. Output current capability can be increased by raising the minimum input voltage of the application, or by selecting an LED with a lower forward voltage. Excessive power dissipation may also limit output current capability of an application.

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Total Output Current Capability

The maximum output current that can be drawn from the LM27965 is 180mA. Each driver bank has a maximum allotted current per Dxx sink that must not be exceeded.

DRIVER TYPE	MAXIMUM Dxx CURRENT
DxA	30mA per DxA Pin
DxB	30mA per DxB Pin
DxC	30mA per DxB Pin

The 180mA load can be distributed in many different configurations. Special care must be taken when running the LM27965 at the maximum output current to ensure proper functionality.

PARALLEL CONNECTED AND UNUSED OUTPUTS

Outputs D1A-5A or D1B-D3B may be connected together to drive one or two LEDs at higher currents. In such a configuration, all five parallel current sinks (BankA) of equal value can drive a single LED. The LED current programmed for BankA should be chosen so that the current through each of the outputs is programmed to 20% of the total desired LED current. For example, if 60mA is the desired drive current for a single LED, R_{SET} should be selected such that the current through each of the current sink inputs is 12mA.

Connecting the outputs in parallel does not affect internal operation of the LM27965 and has no impact on the Electrical Characteristics and limits previously presented. The available diode output current, maximum diode voltage, and all other specifications provided in the Electrical Characteristics table apply to this parallel output configuration, just as they do to the standard 5-LED application circuit.

Both BankA and BankB utilize LED forward voltage sensing circuitry on each Dxx pin to optimize the charge-pump gain for maximum efficiency. Due to the nature of the sensing circuitry, it is not recommended to leave any of the DxA (D1A-D4A) or DxB (D1B-D2B) pins open if either diode bank is going to be used during normal operation. Leaving DxA and/or DxB pins unconnected will force the charge-pump into 3/2× mode over the entire V_{IN} range negating any efficiency gain that could have been achieved by switching to 1× mode at higher input voltages.

If D5A is not used, it is recommended that the driver pin be grounded and the general purpose register bit EN5A be set to 0 to ensure proper gain transitions.

The D3B driver can be completely turned on or off on the fly using the general purpose register. The diode monitoring circuity is enabled and disabled with the driver. If D3B is not used, it is recommended that the driver pin be grounded and the general purpose register bit EN3B be set to 0 to ensure proper gain transitions.

Care must be taken when selecting the proper R_{SET} value. The current on any Dxx pin must not exceed the maximum current rating for any given current sink pin.

POWER EFFICIENCY

Efficiency of LED drivers is commonly taken to be the ratio of power consumed by the LEDs (P_{LED}) to the power drawn at the input of the part (P_{IN}). With a 3/2× - 1× charge pump, the input current is equal to the charge pump gain times the output current (total LED current). The efficiency of the LM27965 can be predicted as follows:

$$P_{LEDTOTAL} = (V_{LEDA} \times N_A \times I_{LEDA}) + (V_{LEDB} \times N_B \times I_{LEDB}) + (V_{LEDC} \times I_{LEDC}) \quad (9)$$

$$P_{IN} = V_{IN} \times I_{IN} \quad (10)$$

$$P_{IN} = V_{IN} \times (GAIN \times I_{LEDTOTAL} + I_Q) \quad (11)$$

$$E = (P_{LEDTOTAL} \div P_{IN}) \quad (12)$$

The LED voltage is the main contributor to the charge-pump gain selection process. Use of low forward-voltage LEDs (3.0V- to 3.5V) will allow the LM27965 to stay in the gain of 1× for a higher percentage of the lithium-ion battery voltage range when compared to the use of higher forward voltage LEDs (3.5V to 4.0V). See the *LED Forward Voltage Monitoring* section of this datasheet for a more detailed description of the gain selection and transition process.

For an advanced analysis, it is recommended that power consumed by the circuit (V_{IN} x I_{IN}) for a given load be evaluated rather than power efficiency.

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POWER DISSIPATION

The power dissipation (P_{DISS}) and junction temperature (T_J) can be approximated with the equations below. P_{IN} is the power generated by the 3/2× - 1× charge pump, P_{LED} is the power consumed by the LEDs, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance for the WQFN-24 package. V_{IN} is the input voltage to the LM27965, V_{LED} is the nominal LED forward voltage, N is the number of LEDs and I_{LED} is the programmed LED current.

$$P_{DISS} = P_{IN} - P_{LEDA} - P_{LEDB} - P_{LEDC} \quad (13)$$

$$P_{DISS} = (GAIN \times V_{IN} \times I_{BANKA + BANKB + BANKC}) - (V_{LEDA} \times N_A \times I_{LEDA}) - (V_{LEDB} \times N_B \times I_{LEDB}) - (V_{LEDC} \times I_{LEDC}) \quad (14)$$

$$T_J = T_A + (P_{DISS} \times \theta_{JA}) \quad (15)$$

The junction temperature rating takes precedence over the ambient temperature rating. The LM27965 may be operated outside the ambient temperature rating, so long as the junction temperature of the device does not exceed the maximum operating rating of 100°C. The maximum ambient temperature rating must be derated in applications where high power dissipation and/or poor thermal resistance causes the junction temperature to exceed 100°C.

THERMAL PROTECTION

Internal thermal protection circuitry disables the LM27965 when the junction temperature exceeds 170°C (typ.). This feature protects the device from being damaged by high die temperatures that might otherwise result from excessive power dissipation. The device will recover and operate normally when the junction temperature falls below 165°C (typ.). It is important that the board layout provide good thermal conduction to keep the junction temperature within the specified operating ratings.

CAPACITOR SELECTION

The LM27965 requires 4 external capacitors for proper operation ($C_1 = C_2 = C_{IN} = C_{OUT} = 1\mu F$). Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR <20mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM27965 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM27965. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over -55°C to 125°C; X5R: ±15% over -55°C to 85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM27965. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, -20%) and vary significantly over temperature (Y5V: +22%, -82% over -30°C to +85°C range; Z5U: +22%, -56% over +10°C to +85°C range). Under some conditions, a nominal 1µF Y5V or Z5U capacitor could have a capacitance of only 0.1µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM27965.

The minimum voltage rating acceptable for all capacitors is 6.3V. The recommended voltage rating for the capacitors is 10V to account for DC bias capacitance losses.

PCB LAYOUT CONSIDERATIONS

The WQFN is a leadframe based Chip Scale Package (CSP) with very good thermal properties. This package has an exposed DAP (die attach pad) at the center of the package measuring 2.6mm x 2.5mm. The main advantage of this exposed DAP is to offer lower thermal resistance when it is soldered to the thermal land on the PCB. For PCB layout, National highly recommends a 1:1 ratio between the package and the PCB thermal land. To further enhance thermal conductivity, the PCB thermal land may include vias to a ground plane. For more detailed instructions on mounting WQFN packages, please refer to Application Note AN-1187 (SNOA401).

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REVISION HISTORY

Changes from Revision A (February 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	16

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM27965SQ-M/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM		27965M	Samples
LM27965SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-30 to 85	L27965S	Samples
LM27965SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-30 to 85	L27965S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

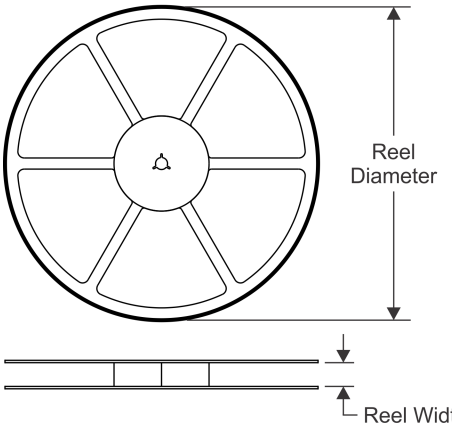
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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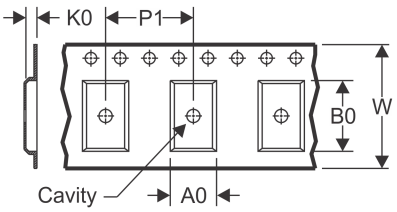
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

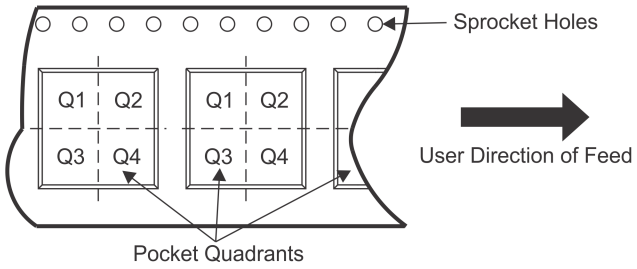


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

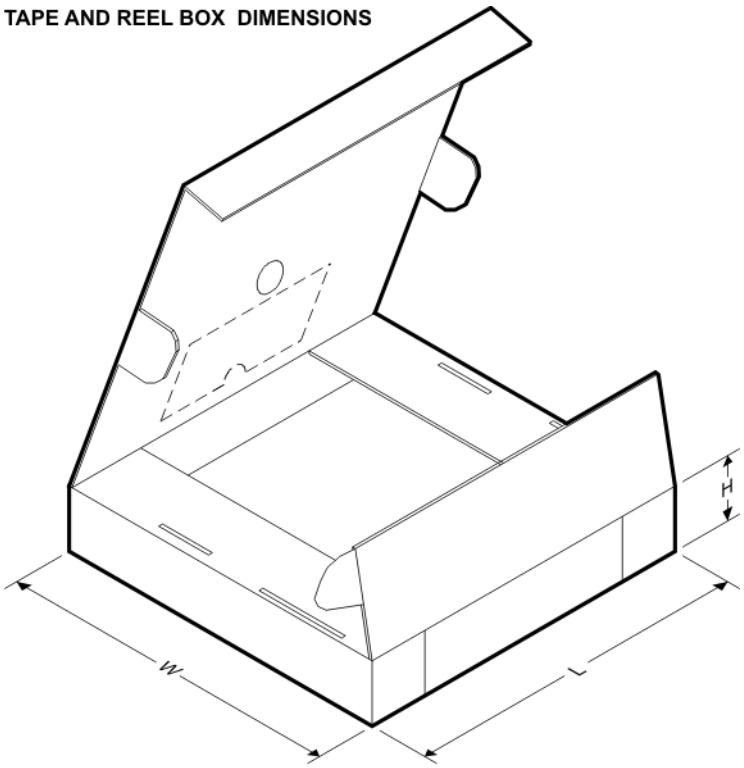
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM27965SQ-M/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM27965SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM27965SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

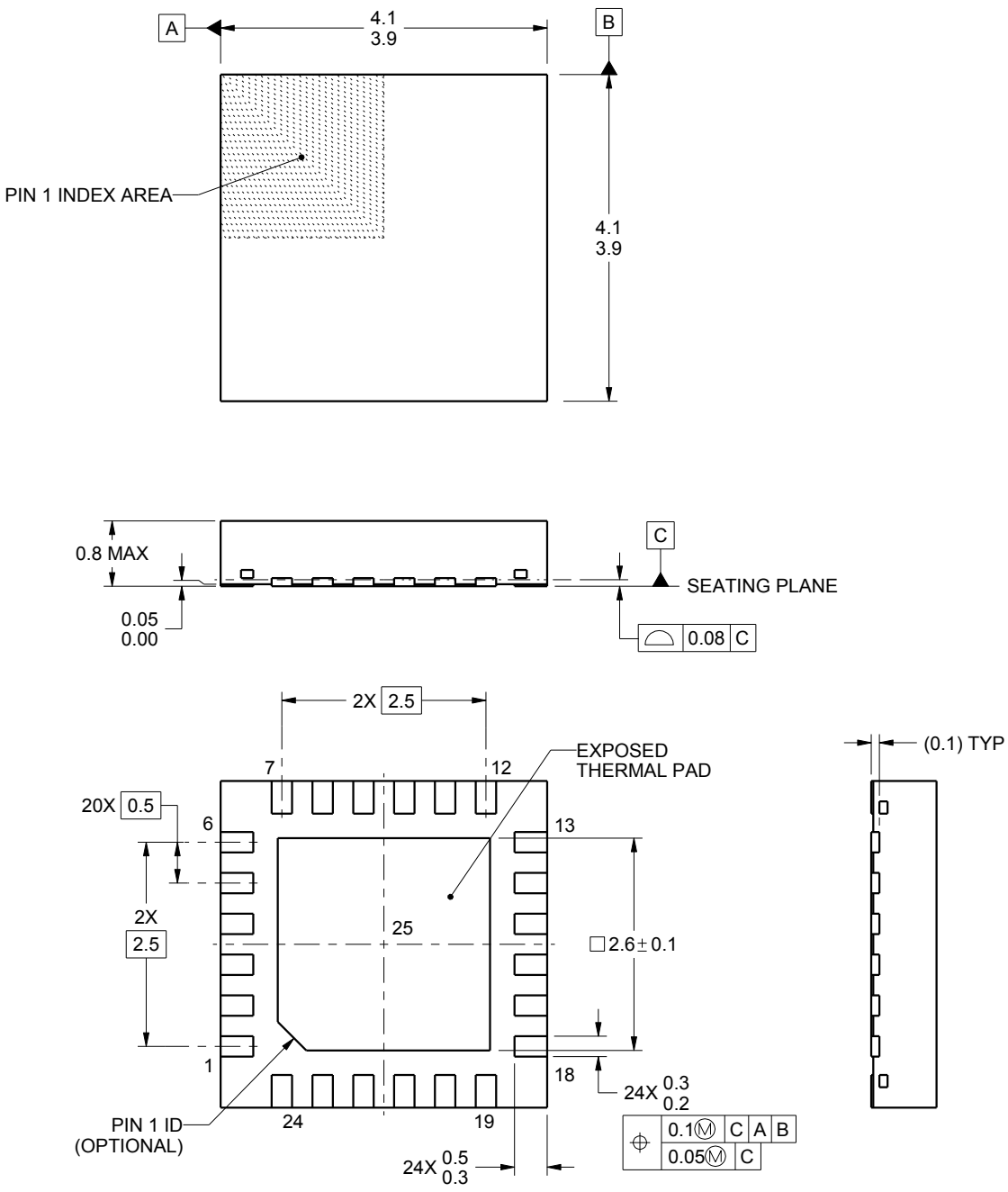
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM27965SQ-M/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LM27965SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LM27965SQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

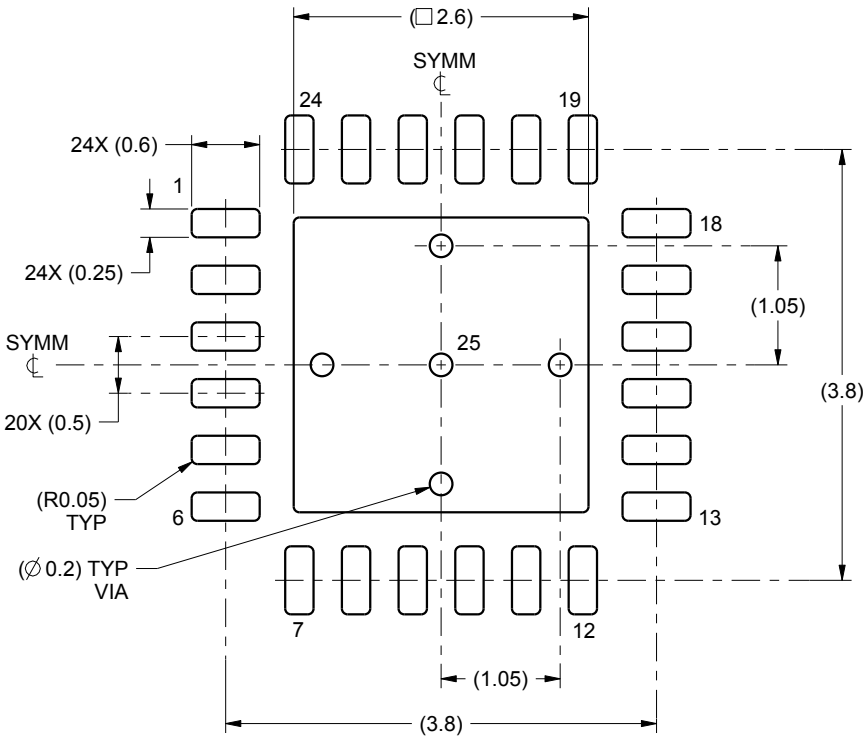
PLASTIC QUAD FLATPACK - NO LEAD



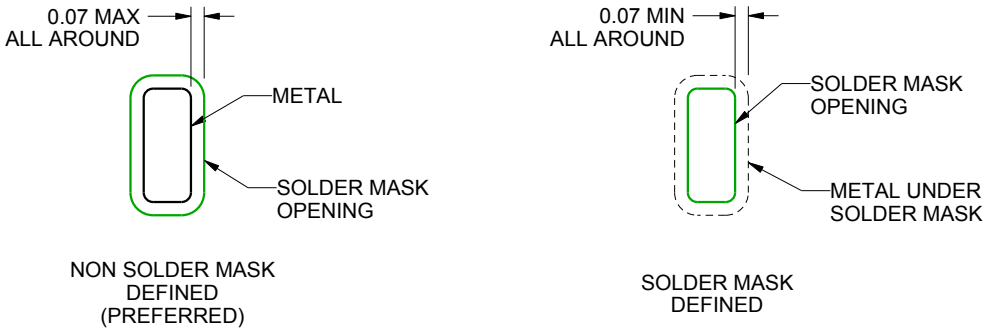
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

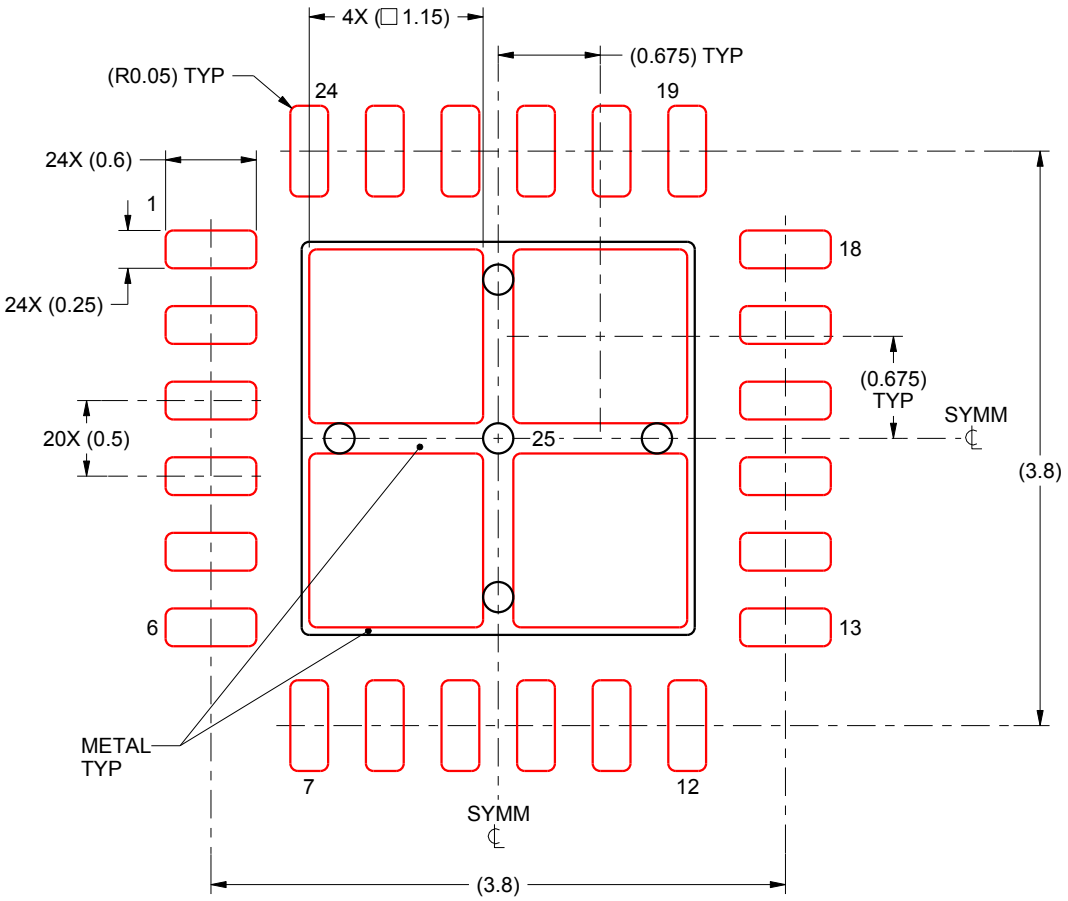


SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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