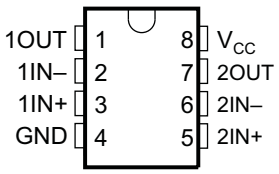
FEATURES

- **Controlled Baseline**
  - **One Assembly/One Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Wide Supply Range:**
  - **Single Supply . . . 3 V to 30 V**
  - **Dual Supplies . . . ±1.5 V to ±15 V**
- **Low Supply-Current Drain, Independent of Supply Voltage . . . 0.7 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground, Allowing Direct Sensing Near Ground**
- **Low Input Bias and Offset Parameters:**
  - **Input Offset Voltage . . . 2 mV Typ**
  - **Input Offset Current . . . 2 nA Typ**
  - **Input Bias Current . . . 15 nA Typ**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 32 V**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The LM258A consists of two independent, high-gain, frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is 3 V to 30 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

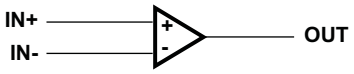
Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, this device can be operated directly from the standard 5-V supply used in digital systems and easily can provide the required interface electronics without additional ±5-V supplies.

ORDERING INFORMATION

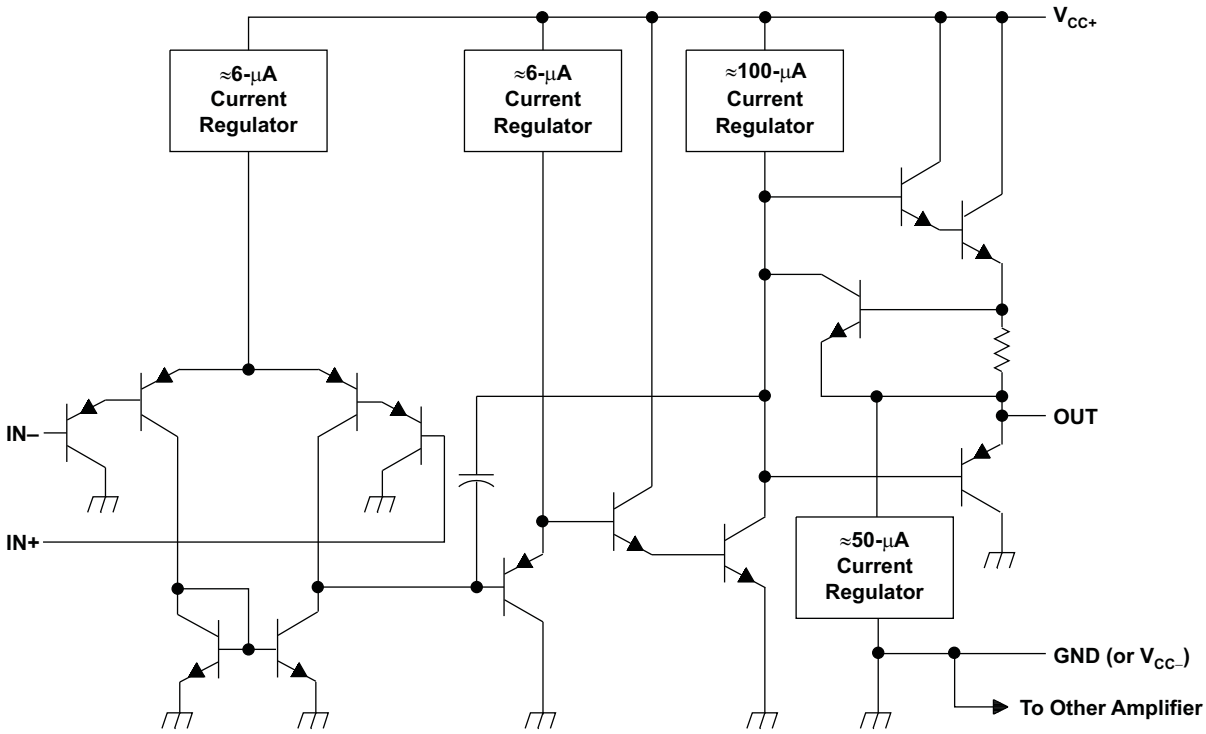
T_A	V_{IO}max AT 25°C	MAX TESTED V_{CC}	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	3mV	30V	SOIC – D	Reel of 2500	LM258AMDREP	258AM

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

SYMBOL (EACH AMPLIFIER)



SCHEMATIC (EACH AMPLIFIER)



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	7
Transistors	51
Capacitors	2

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	Supply voltage(2)	±16 or 32	V
V_{ID}	Differential input voltage(3)	±32	V
V_I	Input voltage (either input)	–0.3 to 32	V
	Duration of output short circuit (one amplifier) to ground at (or below) 25°C free-air temperature ($V_{CC} \le 15$ V)(4)	Unlimited	
θ_{JA}	Package thermal impedance(5)(6)	97	°C/W
T_A	Operating free-air temperature range	–55 to 125	°C
T_J	Operating virtual junction temperature	150	°C
T_{stg}	Storage temperature range(7)	–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages and V_{CC} specified for measurement of I_{OS}, are with respect to the network ground terminal.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
(5) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.
(7) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

Electrical Characteristics

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		T_A(2)	MIN	TYP(3)	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR(min)}$, V_O = 1.4 V		25°C		2	3	mV
				Full range			4	
$\alpha_{I_{IO}}$	Average temperature coefficient of input offset voltage			Full range		7	15	µV/°C
I_{IO}	Input offset current	V_O = 1.4 V		25°C		2	15	nA
				Full range			30	
$\alpha_{I_{IO}}$	Average temperature coefficient of input offset current			Full range		10	200	pA/°C
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–15	–80	nA
				Full range			–100	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to Max		25°C	0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			
V_{OH}	High-level output voltage	$R_L \geq 2\ k\Omega$		25°C	V_{CC} – 1.5			V
		V_{CC} = 30 V	R_L = 2 kΩ	Full range	26			
			$R_L \geq 10\ k\Omega$	Full range	27	28		
V_{OL}	Low-level output voltage	$R_L \leq 10\ k\Omega$		Full range		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \geq 2\ k\Omega$		25°C	50	100		V/mV
				Full range	25			
CMRR	Common-mode rejection ratio	V_{CC} = 5 V to Max, $V_{IC} = V_{ICR(min)}$		25°C	70	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{CC} = 5 V to Max		25°C	65	100		dB
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		25°C		120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	Source	25°C	–20	–30	–60	mA
				Full range	–10			
		V_{CC} = 15 V, V_{ID} = –1 V, V_O = 15 V	Sink	25°C	10	20		
				Full range	5			
		V_{ID} = –1 V, V_O = 200 mV		25°C	12	30		µA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at –5 V, V_O = 0		25°C		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load		Full range		0.7	1.2	mA
		V_{CC} = Max, $V_O = V_{CC}/2$, No load		Full range		1	2	

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. MAX V_{CC} for testing purposes is 30 V.
(2) Full range is –55°C to 125°C.
(3) All typical values are at T_A = 25°C.

Operating Characteristics

V_{CC} = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 30 pF, V_I = ±10 V, See Figure 1	0.3	V/µs
B_1	Unity-gain bandwidth	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	0.7	MHz
V_n	Equivalent input noise voltage	R_S = 100 Ω, V_I = 0 V, f = 1 kHz, See Figure 2	40	nV/√Hz

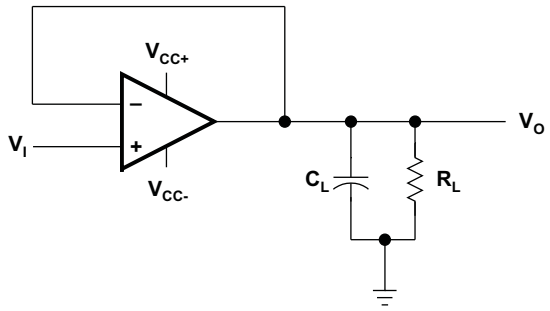


Figure 1. Unity-Gain Amplifier

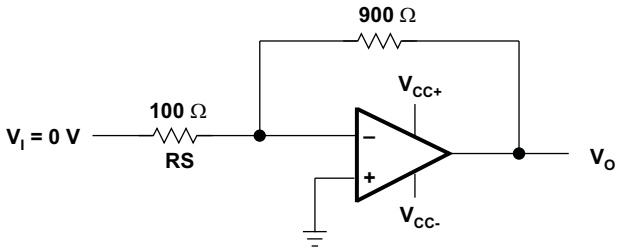


Figure 2. Noise-Test Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM258AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	258AM	Samples
LM258AMDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	258AM	Samples
V62/07605-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	258AM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM258A-EP :

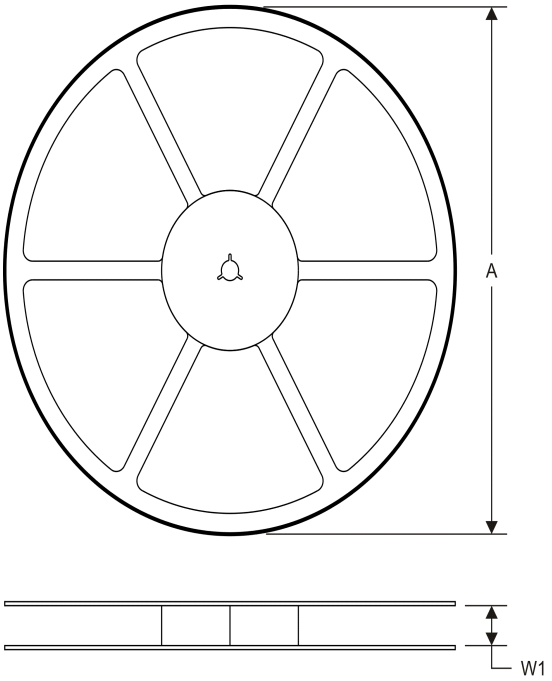
- Catalog: LM258A

NOTE: Qualified Version Definitions:

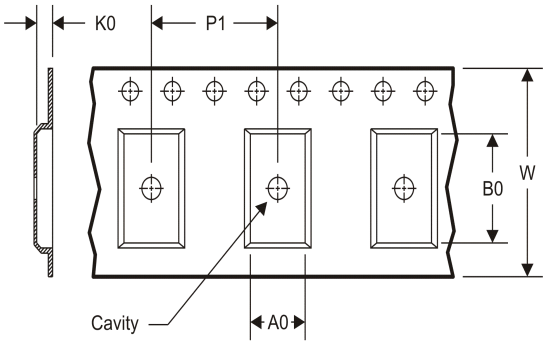
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



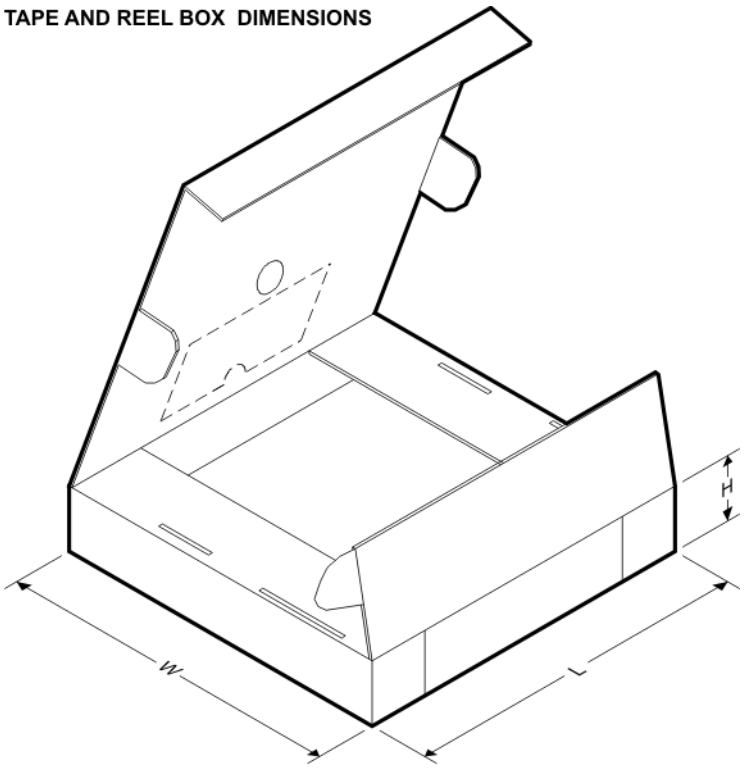
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

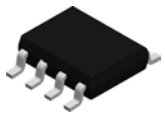
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM258AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258AMDREP	SOIC	D	8	2500	367.0	367.0	35.0

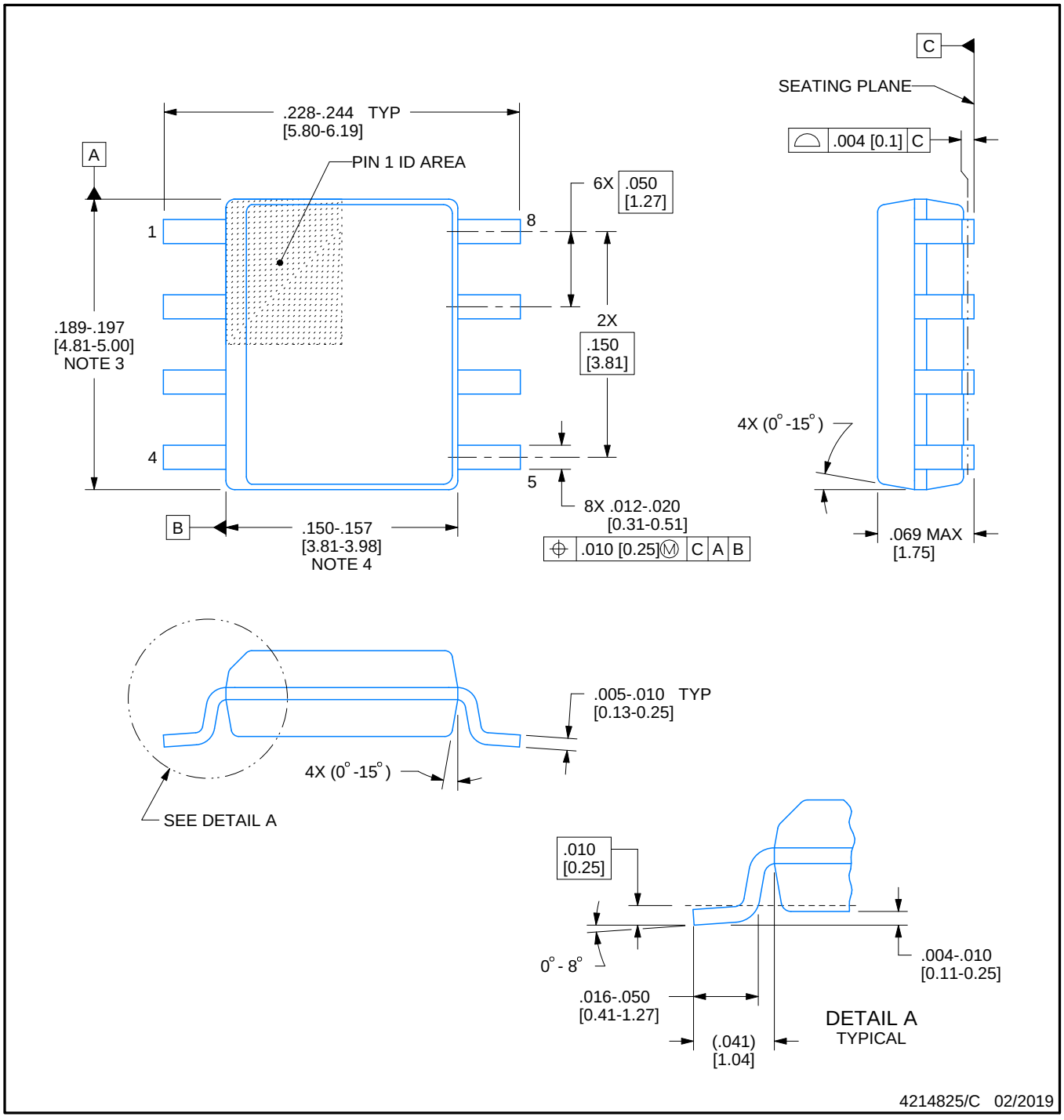


PACKAGE OUTLINE

D0008A

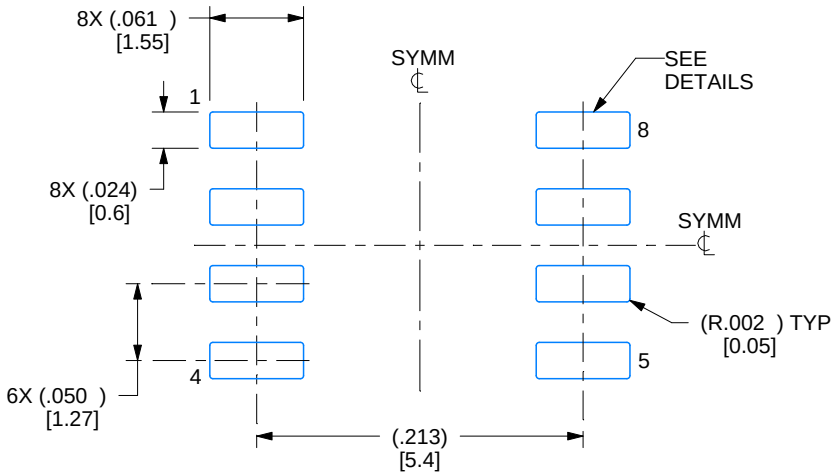
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

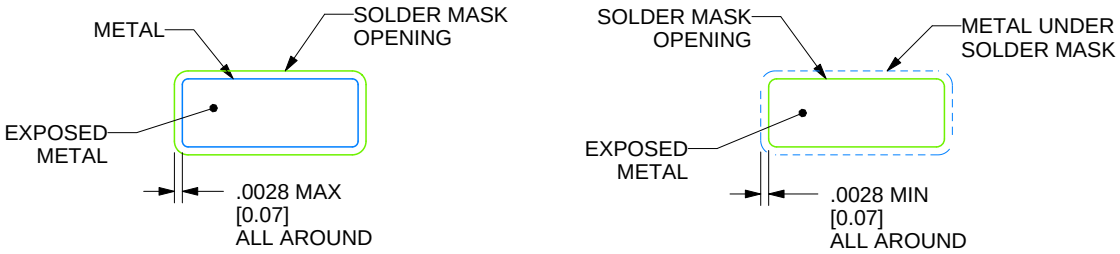


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

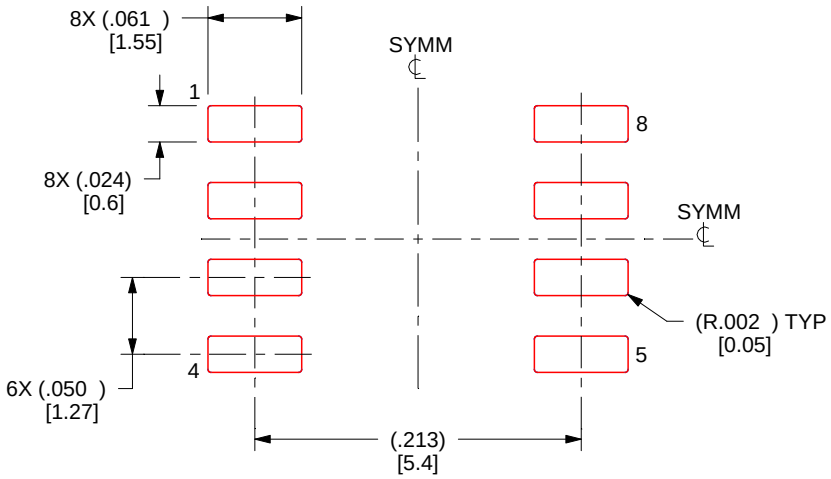
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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