

LM148, LM248, LM348 QUADRUPLE OPERATIONAL AMPLIFIERS

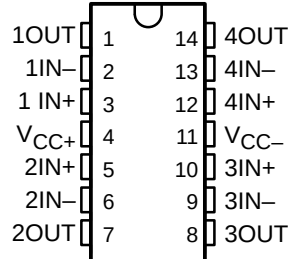
SLOS058C – OCTOBER 1979 – REVISED DECEMBER 2002

- μ A741 Operating Characteristics
- Low Supply-Current Drain . . . 0.6 mA Typ (per amplifier)
- Low Input Offset Voltage
- Low Input Offset Current
- Class AB Output Stage
- Input/Output Overload Protection
- Designed to Be Interchangeable With Industry Standard LM148, LM248, and LM348

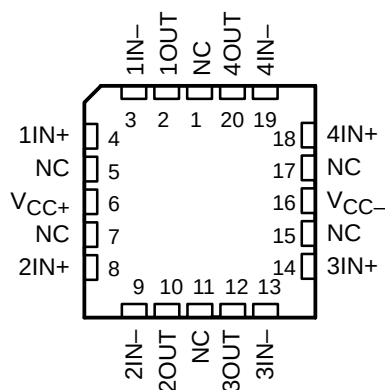
description/ordering information

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the μ A741. These amplifiers exhibit low supply-current drain and input bias and offset currents that are much less than those of the μ A741.

LM148 . . . J PACKAGE
LM248 . . . D OR N PACKAGE
LM348 . . . D, N, OR NS PACKAGE
(TOP VIEW)



LM148 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	V_{IOmax} AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (N)	Tube of 25	LM348N	LM348N
		SOIC (D)	Tube of 50	LM348D	LM348
			Reel of 2500	LM348DR	
		SOP (NS)	Reel of 2000	LM348NSR	LM348
–25°C to 85°C	6 mV	PDIP (N)	Tube of 25	LM248N	LM248N
		SOIC (D)	Tube of 50	LM248D	LM248
			Reel of 2500	LM248DR	
–55°C to 125°C	5 mV	CDIP (J)	Tube of 25	LM148J	LM148J
		LCCC (FK)	Tube of 50	LM148FK	LM148FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

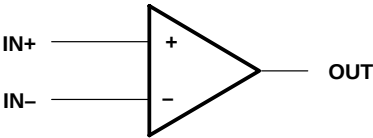
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

LM148, LM248, LM348
QUADRUPLE OPERATIONAL AMPLIFIERS

SLOS058C – OCTOBER 1979 – REVISED DECEMBER 2002

symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Table with 2 columns: Parameter and Rating. Rows include Supply voltage (VCC+), Supply voltage (VCC-), Differential input voltage (VID), Input voltage (VI), Duration of output short circuit, Operating virtual junction temperature (TJ), Package thermal impedance (thetaJA), Package thermal impedance (thetaJC), Case temperature for 60 seconds, Lead temperature, and Storage temperature range.

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

- NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between VCC+ and VCC-.
2. Differential voltages are at IN+ with respect to IN-.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of TJ(max), thetaJA, and TA. The maximum allowable power dissipation at any allowable ambient temperature is PD = (TJ(max) - TA)/thetaJA. Operating at the absolute maximum TJ of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of TJ(max), thetaJC, and TC. The maximum allowable power dissipation at any allowable ambient temperature is PD = (TJ(max) - TC)/thetaJC. Operating at the absolute maximum TJ of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions

Table with 4 columns: Parameter, MIN, MAX, UNIT. Rows include Supply voltage (VCC+) and Supply voltage (VCC-).

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM148			LM248			LM348			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _O = 0	25°C	1	5	1	6	1	6	mV			
			Full range	6	7.5	7.5							
I _{IO}	Input offset current	V _O = 0	25°C	4	25	4	50	4	50	nA			
			Full range	75	125	100							
I _{IB}	Input bias current	V _O = 0	25°C	30	100	30	200	30	200	nA			
			Full range	325	500	400							
V _{ICR}	Common-mode input voltage range		Full range	±12		±12		±12		V			
V _{OM}	Maximum peak output voltage swing	R _L = 10 kΩ	25°C	±12 ±13		±12 ±13		±12 ±13		V			
		R _L ≥ 10 kΩ	Full range	±12		±12		±12					
		R _L = 2 kΩ	25°C	±10 ±12		±10 ±12		±10 ±12					
		R _L ≥ 2 kΩ	Full range	±10		±10		±10					
A _{VD}	Large-signal differential voltage amplification	V _O = ±10 V, R _L = ≥ 2 kΩ	25°C	50	160	25	160	25	160	V/mV			
			Full range	25	15	15							
r _i	Input resistance‡		25°C	0.8	2.5	0.8	2.5	0.8	2.5	MΩ			
B ₁	Unity-gain bandwidth	A _{VD} = 1	25°C	1		1		1		MHz			
φ _m	Phase margin	A _{VD} = 1	25°C	60°		60°		60°					
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin} , V _O = 0	25°C	70	90	70	90	70	90	dB			
			Full range	70	70	70							
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	V _{CC±} = ±9 V to ±15 V, V _O = 0	25°C	77	96	77	96	77	96	dB			
			Full range	77	77	77							
I _{OS}	Short-circuit output current		25°C	±25		±25		±25		mA			
I _{CC}	Supply current (four amplifiers)	No load	25°C			2.4 4.5		2.4 4.5		mA			
		V _O = 0		2.4 3.6									
V _{O1} /V _{O2}	Crosstalk attenuation	f = 1 Hz to 20 kHz	25°C	120		120		120		dB			

[†] All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is -55°C to 125°C for LM148, -25°C to 85°C for LM248, and 0°C to 70°C for LM348.

[‡] This parameter is not production tested.

LM148, LM248, LM348

QUADRUPLE OPERATIONAL AMPLIFIERS

SLOS058C – OCTOBER 1979 – REVISED FEBRUARY 2002

operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Figure 1		0.5		V/ μs

PARAMETER MEASUREMENT INFORMATION

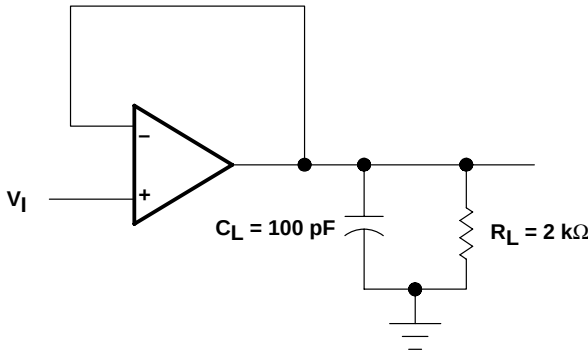


Figure 1. Unity-Gain Amplifier

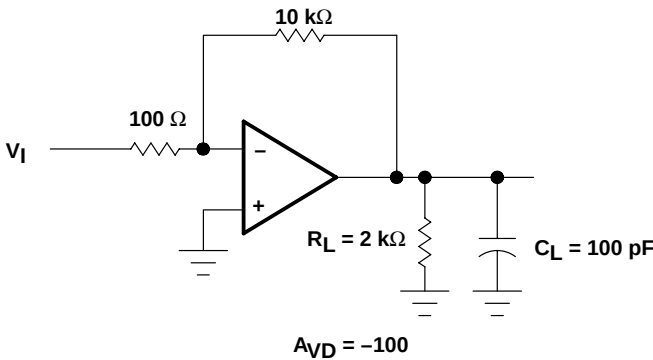


Figure 2. Inverting Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM148 MW8	ACTIVE	WAFERSALE	YS	0	1	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM148FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	LM148FKB	Samples
LM148J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	LM148J	Samples
LM148JB	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	LM148JB	Samples
LM248D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM248	Samples
LM248DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM248	Samples
LM248N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-25 to 85	LM248N	Samples
LM348D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	Samples
LM348DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	Samples
LM348DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	Samples
LM348DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	Samples
LM348DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	Samples
LM348N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	LM348N	Samples
LM348NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM348	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

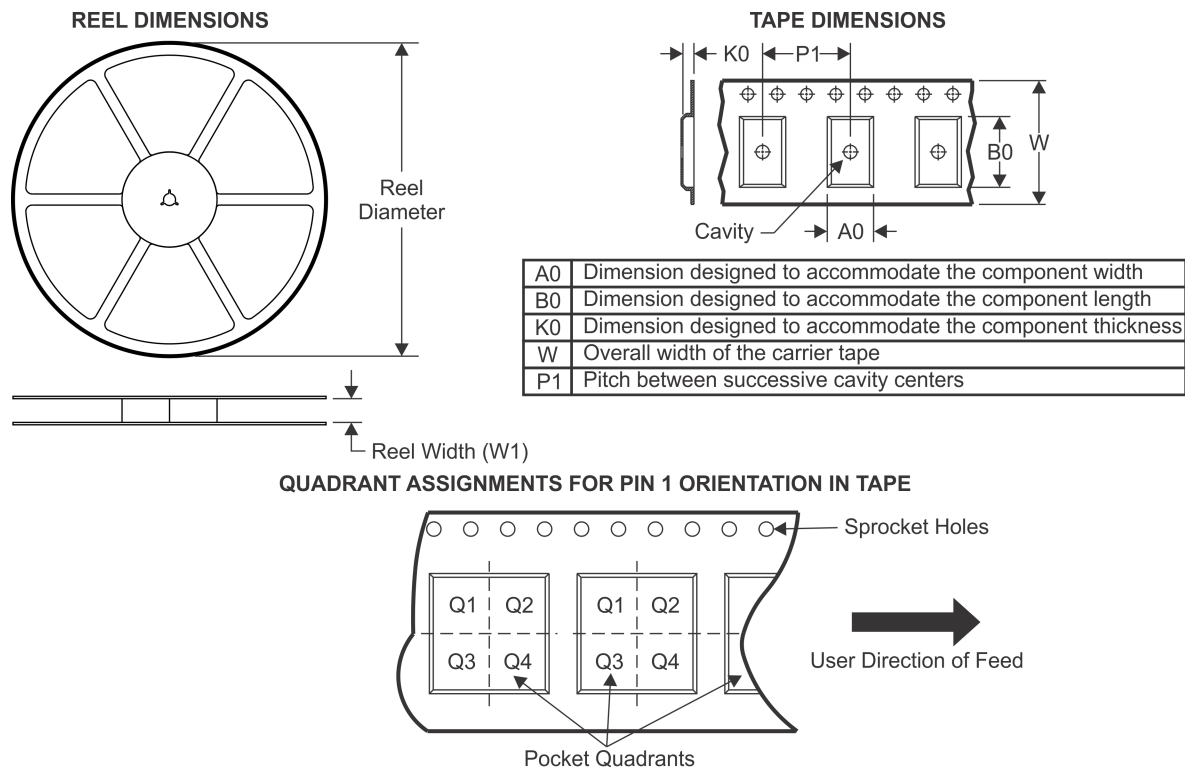
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

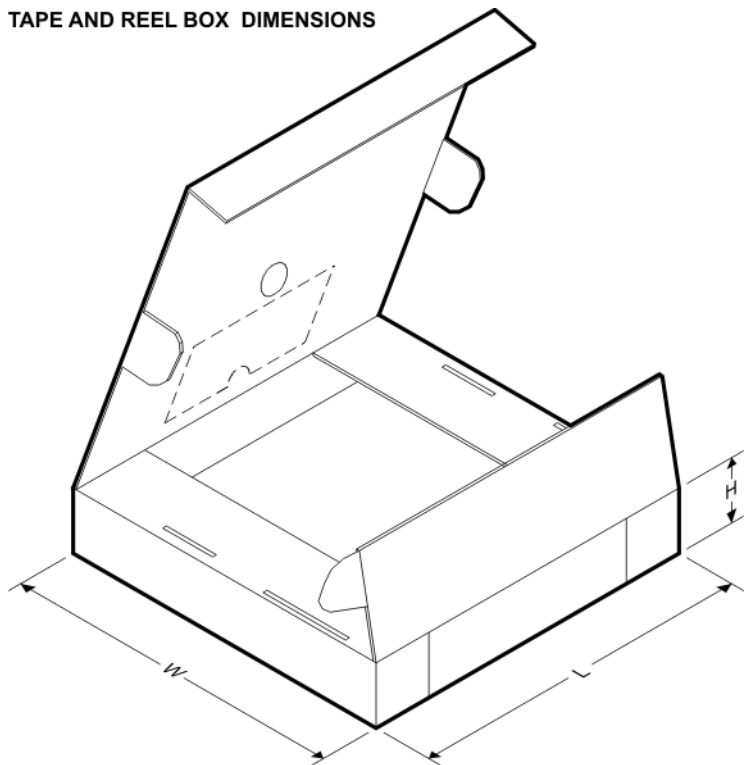
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM248DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM348DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM348DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM348NSR	SO	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

TAPE AND REEL BOX DIMENSIONS



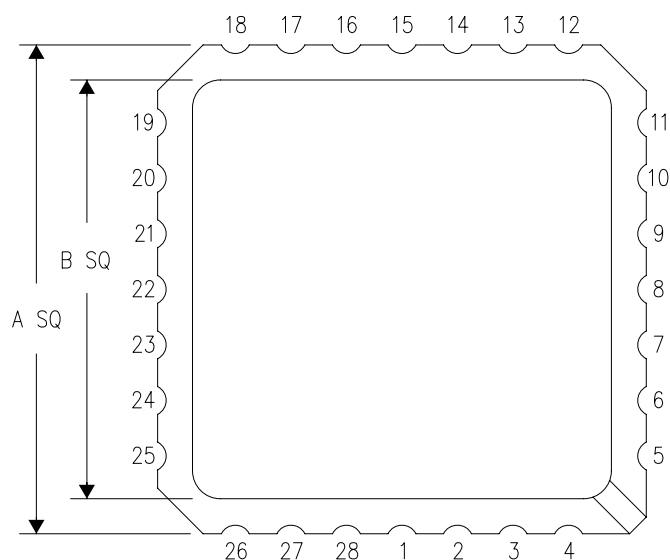
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM248DR	SOIC	D	14	2500	367.0	367.0	38.0
LM348DR	SOIC	D	14	2500	367.0	367.0	38.0
LM348DR	SOIC	D	14	2500	333.2	345.9	28.6
LM348NSR	SO	NS	14	2000	367.0	367.0	38.0

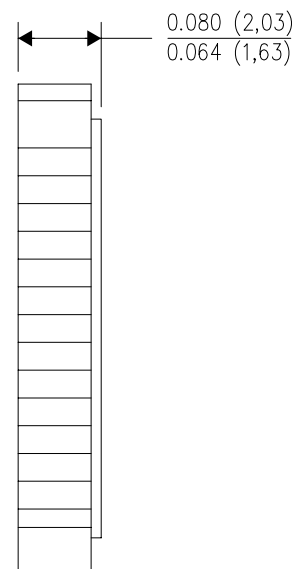
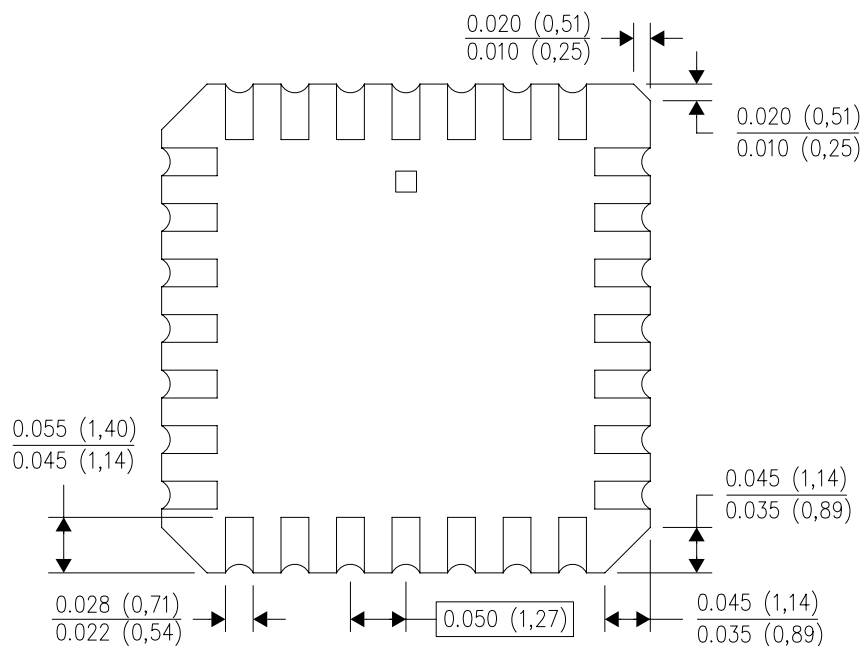
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

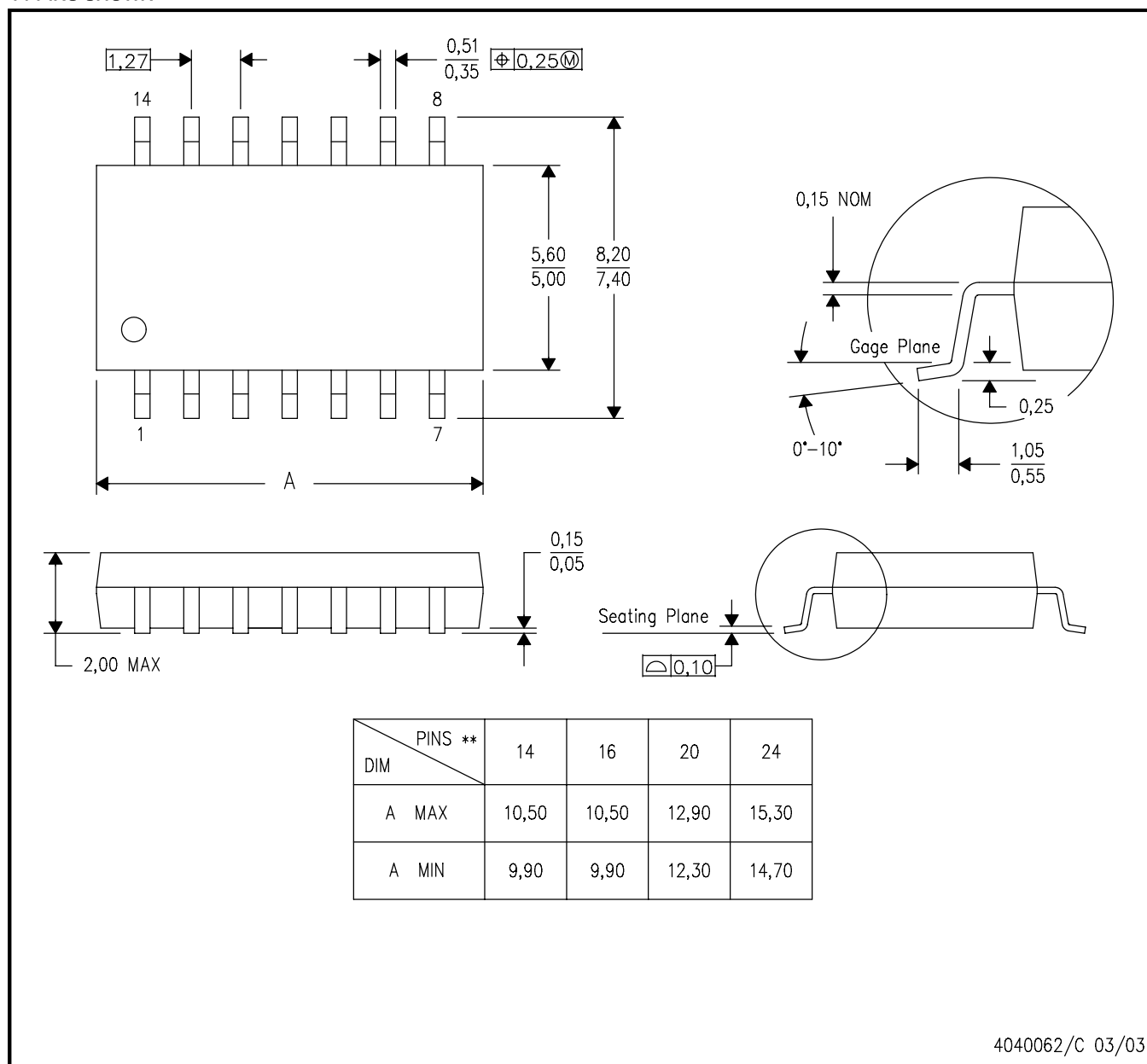
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

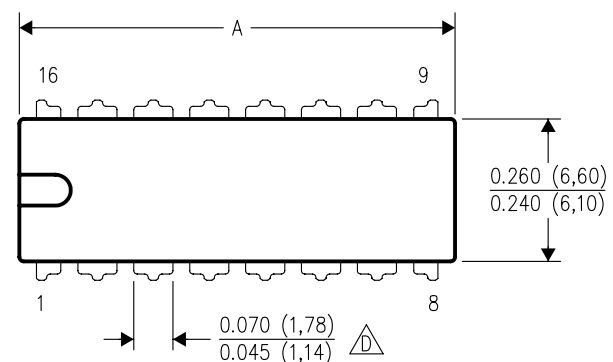


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

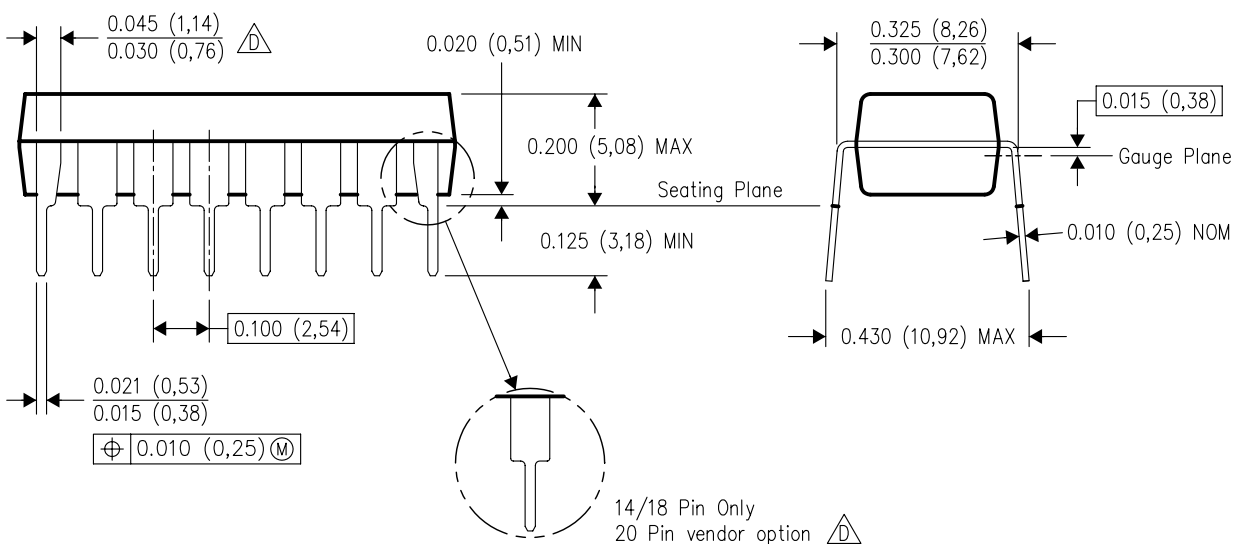
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

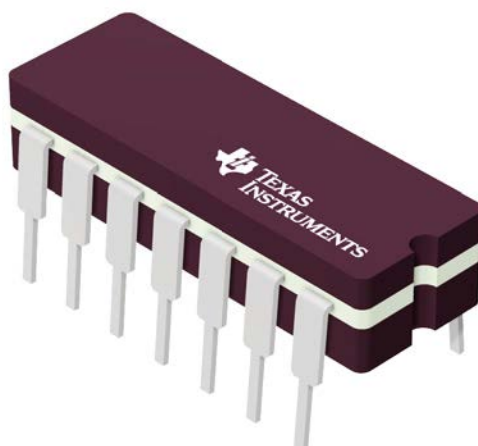
- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

J 14

GENERIC PACKAGE VIEW

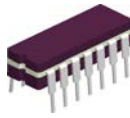
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

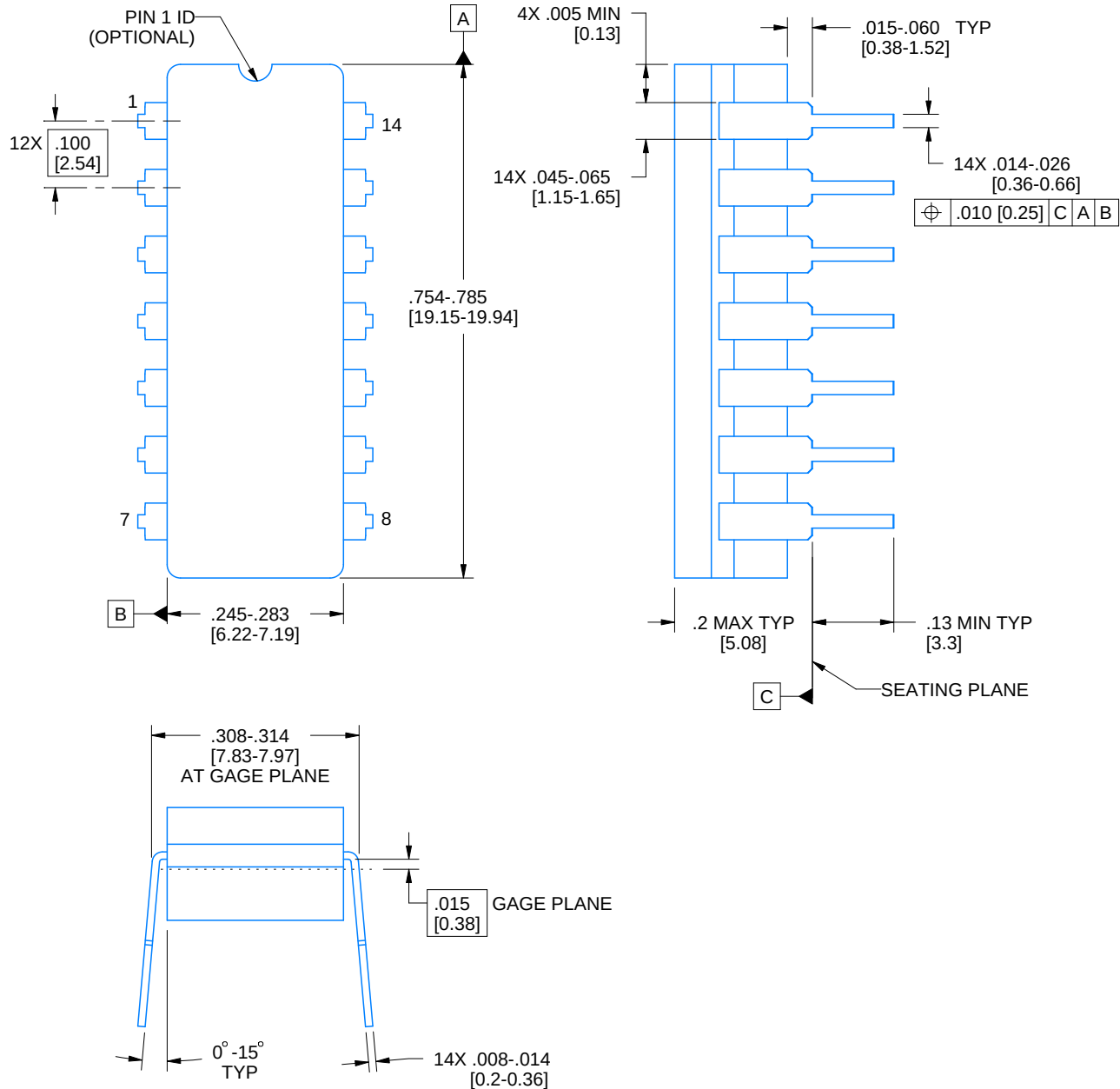


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



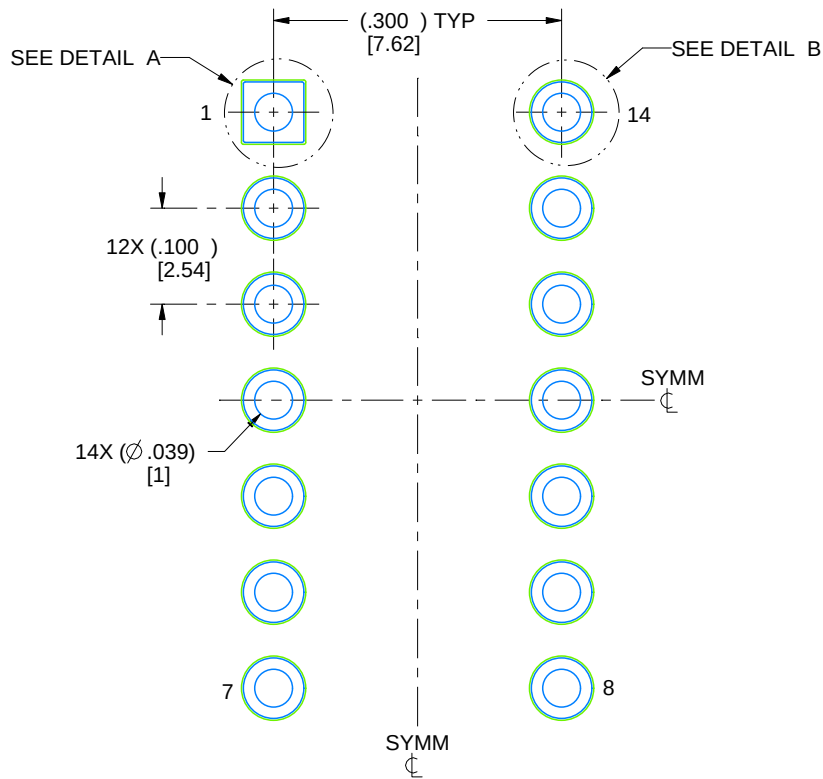
**TEXAS
INSTRUMENTS**
www.ti.com

EXAMPLE BOARD LAYOUT

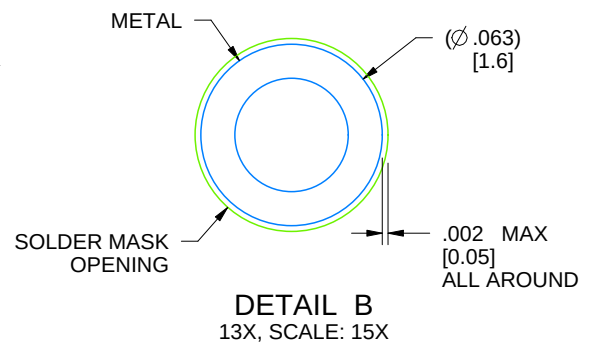
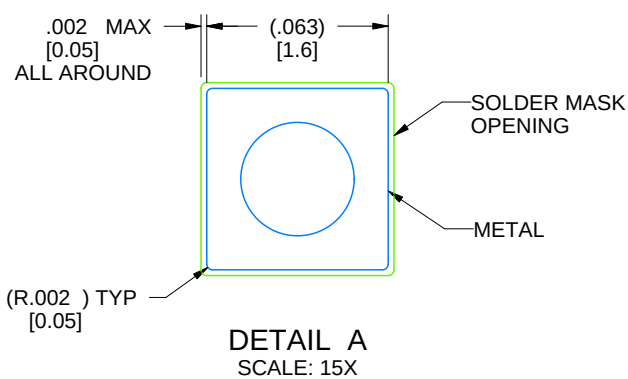
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



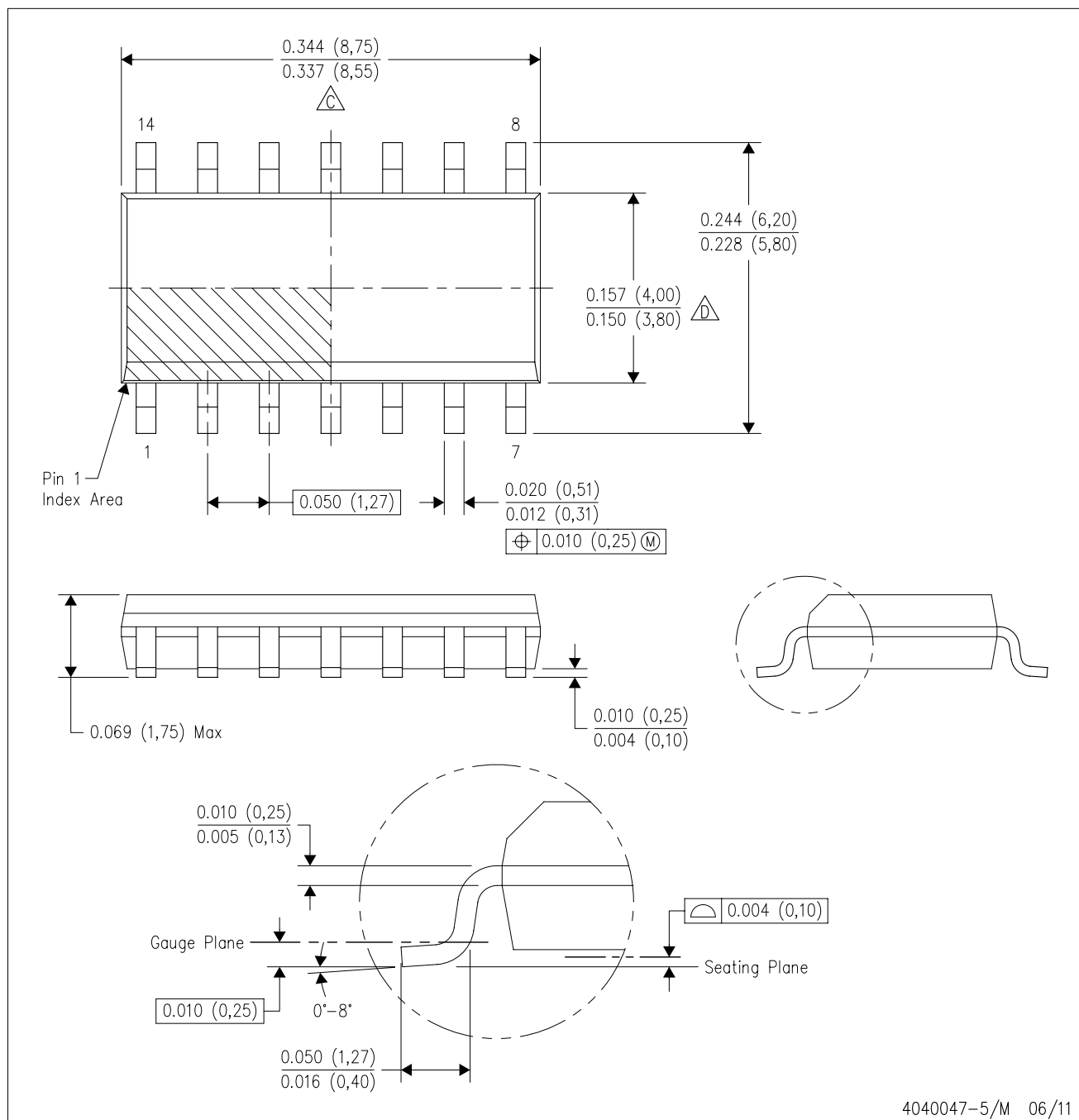
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



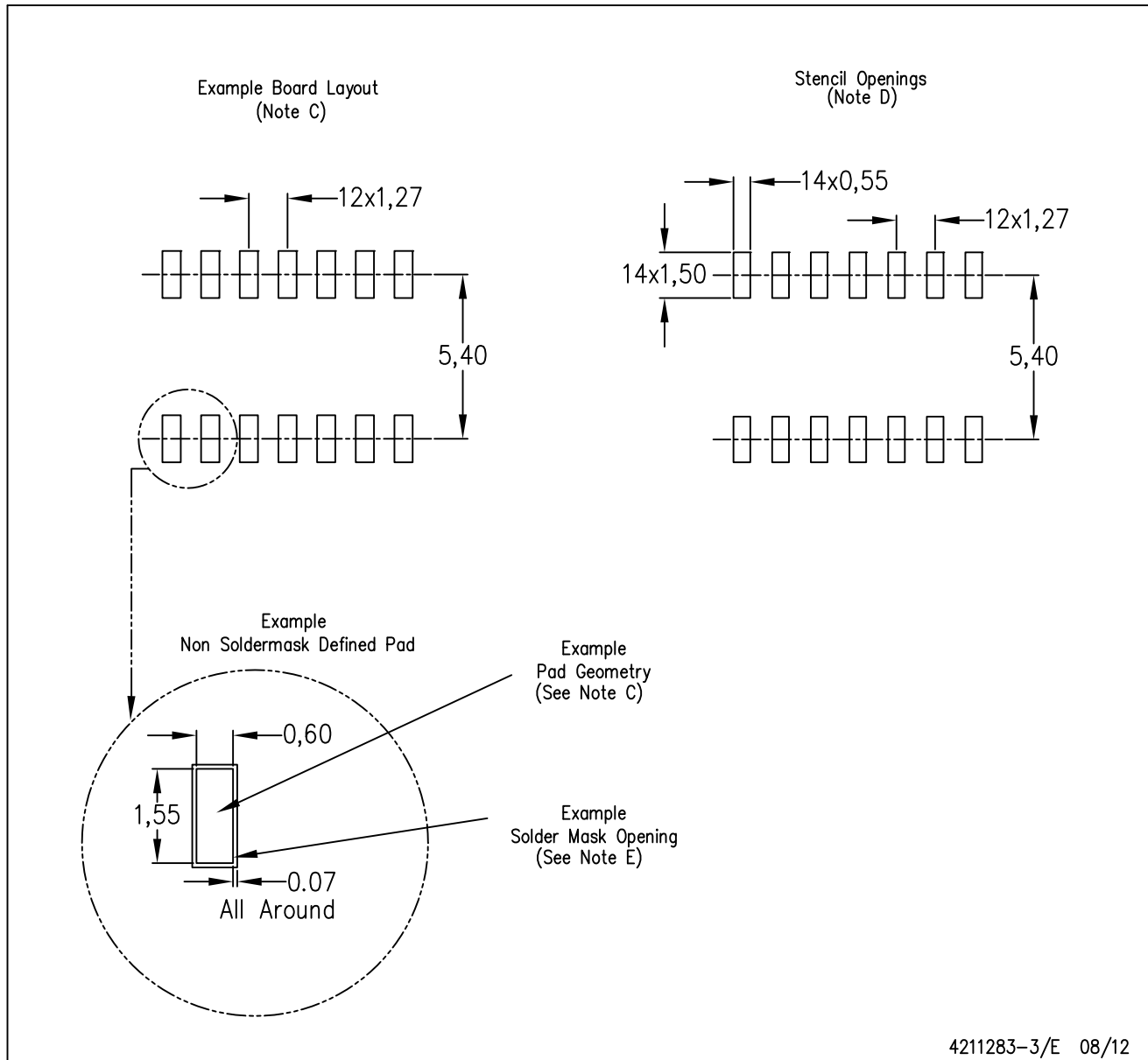
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated