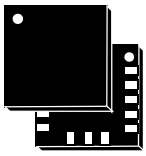
LIS3DSH

MEMS digital output motion sensor: ultra-low-power high-performance three-axis "nano" accelerometer

Datasheet - production data



LGA-16 (3x3x1 mm)

Features

- Wide supply voltage, 1.71 V to 3.6 V
- Independent IOs supply (1.8 V) and supply voltage compatible
- Ultra-low power consumption
- ±2*g*/±4*g*/±6*g*/±8*g*/±16*g* dynamically selectable full scale
- I^2C/SPI digital output interface
- 16-bit data output
- Programmable embedded state machines
- Embedded temperature sensor
- Embedded self-test
- Embedded FIFO
- 10000 *g* high shock survivability
- ECOPACK®, RoHS and “Green” compliant

Applications

- Motion-controlled user interface
- Gaming and virtual reality
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Click/double-click recognition
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LIS3DSH is an ultra-low-power high-performance three-axis linear accelerometer belonging to the “nano” family with an embedded state machine that can be programmed to implement autonomous applications.

The LIS3DSH has dynamically selectable full scales of ±2*g*/±4*g*/±6*g*/±8*g*/±16*g* and is capable of measuring accelerations with output data rates from 3.125 Hz to 1.6 kHz.

The self-test capability allows the user to check the functioning of the sensor in the final application.

The device can be configured to generate interrupt signals activated by user-defined motion patterns.

The LIS3DSH has an integrated first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

The LIS3DSH is available in a small thin plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order codes	Temperature range [°C]	Package	Packaging
LIS3DSHTR	-40 to +85	LGA-16	Tape and reel

This is information on a product in full production. www.st.com

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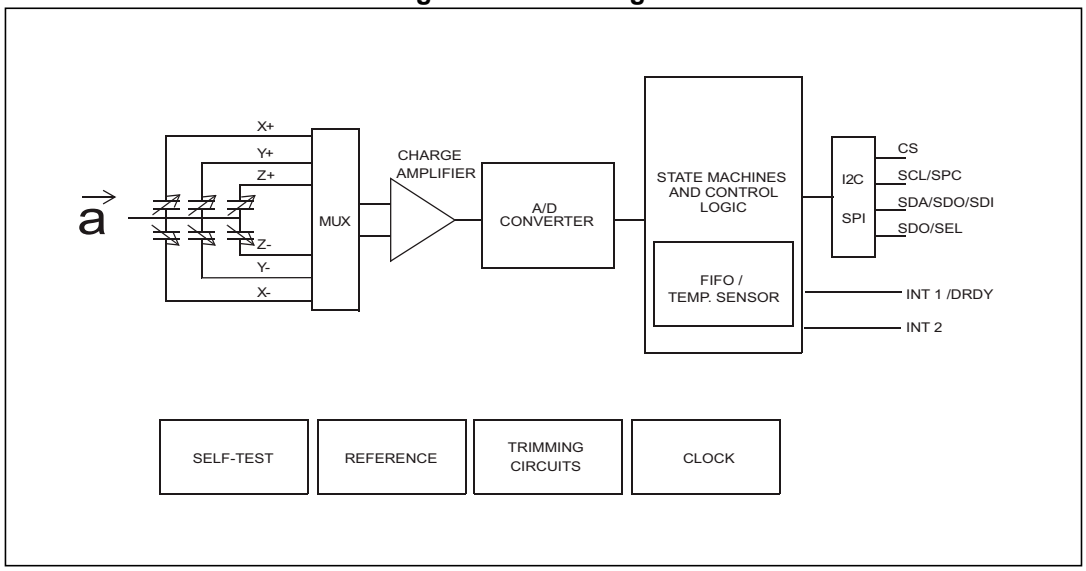
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

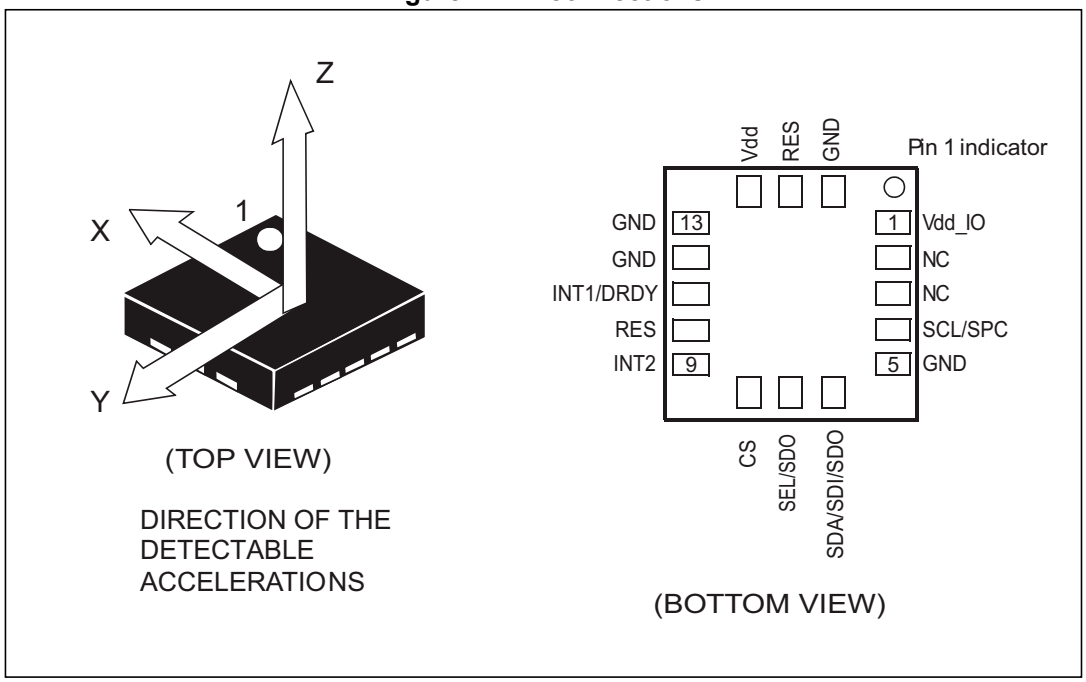


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	NC	Not connected
3	NC	Not connected
4	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
5	GND	0 V supply
6	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SEL SDO	I^2C address selection SPI serial data output (SDO)
8	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	INT 2	Interrupt 2
10	Reserved	Connect to GND
11	INT 1/DRDY	Interrupt 1/ DRDY
12	GND	0 V supply
13	GND	0 V supply
14	Vdd	Power supply
15	Reserved	Connect to Vdd, connect to GND, or leave unconnected
16	GND	0 V supply

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
FS	Measurement range[2]	FS bit set to 000		±2.0		*g*
		FS bit set to 001		±4.0		
		FS bit set to 010		±6.0		
		FS bit set to 011		±8.0		
		FS bit set to 100		±16.0		
So	Sensitivity	FS bit set to 000		0.06		mg/digit
		FS bit set to 001		0.12		
		FS bit set to 010		0.18		
		FS bit set to 011		0.24		
		FS bit set to 100		0.73		
TCSo	Sensitivity change vs. temperature	FS bit set to 00		0.01		%/°C
TyOff	Typical zero-*g* level offset accuracy[3]	FS bit set to 00		±40		mg
TCOff	Zero-*g* level change vs. temperature	Max. delta from 25 °C		±0.5		mg/°C
An	Acceleration noise density	FS bit set to 00, normal mode, ODR = 100 Hz		150		µg/ sqrt(Hz)
ST	Self test positive difference[4]	± 2 *g* range, X, Y-axis ST2,ST1 = [01] see *Figure 55*		140		mg
		± 2 *g* range, Z-axis ST2,ST1 = [01] see *Figure 55*		590		
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Self-test output change" is defined as: $OUTPUT[mg]_{(CNTL5\ ST2,\ ST1\ bits=01)}$ - $OUTPUT[mg]_{(CNTL5\ ST2,\ ST1\ bits=00)}$

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

2.2 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[b].

Table 4. Electrical characteristics (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
Vdd	Supply voltage		1.71	2.5	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.71		Vdd+0.1	V
IddA	Current consumption in active mode	1.6 kHz ODR		225		µA
		3.125 Hz ODR		11		µA
IddPdn	Current consumption in power-down/standby mode			2		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
VOH	High-level output voltage		0.9*Vdd_IO			V
VOL	Low-level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.

b. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

2.3 Communication interface characteristics

2.3.1 SPI - serial peripheral interface

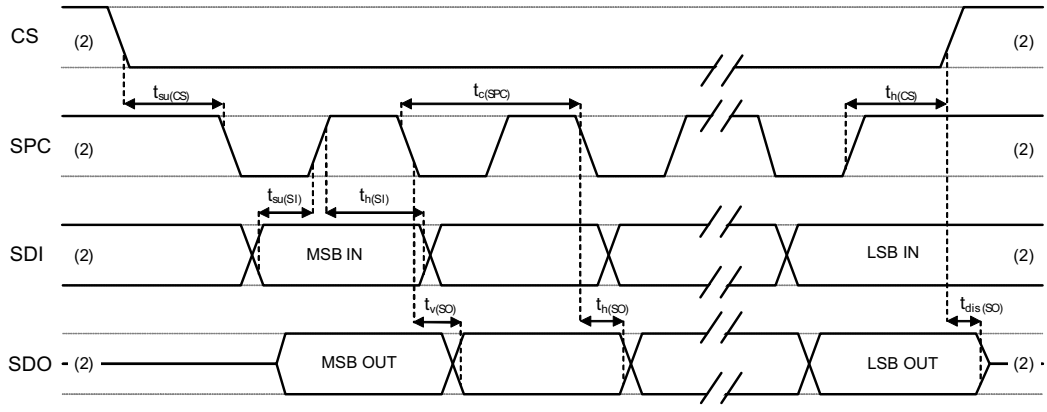
Subject to general operating conditions for Vdd and Top.

Table 5. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min.	Max.	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



2. When no ongoing communication, data on SDO is driven by internal pull-up resistor.

Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.3.2 I²C - inter-IC control interface

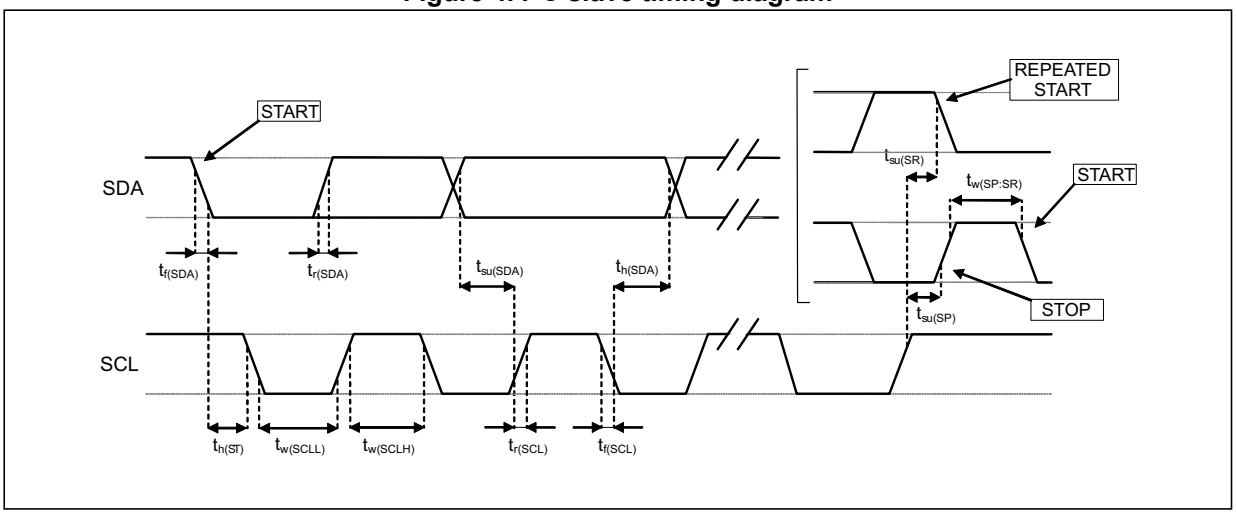
Subject to general operating conditions for Vdd and Top.

Table 6. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. C_b = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SEL)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.1 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.5 Terminology

2.5.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

2.5.2 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* for the X-axis and 0 *g* for the Y-axis, whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor on a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

2.6 Functionality

2.6.1 Self-test

The self-test allows checking the sensor functionality without moving it. The self-test function is off when the self-test bit (ST) is programmed to '0'. When the self-test bit is programmed to '1', an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the chip interface are within the defined specifications.

2.7 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. In order to be compatible with traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation.

When an acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

2.8 IC interface

The complete measurement chain is made up of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage that is available to the user through an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface, therefore making the device particularly suitable for direct interfacing with a microcontroller.

The LIS3DSH features a Data-Ready signal (DRDY) which indicates when a new set of measured acceleration data is available, therefore simplifying data synchronization in the digital system that uses the device.

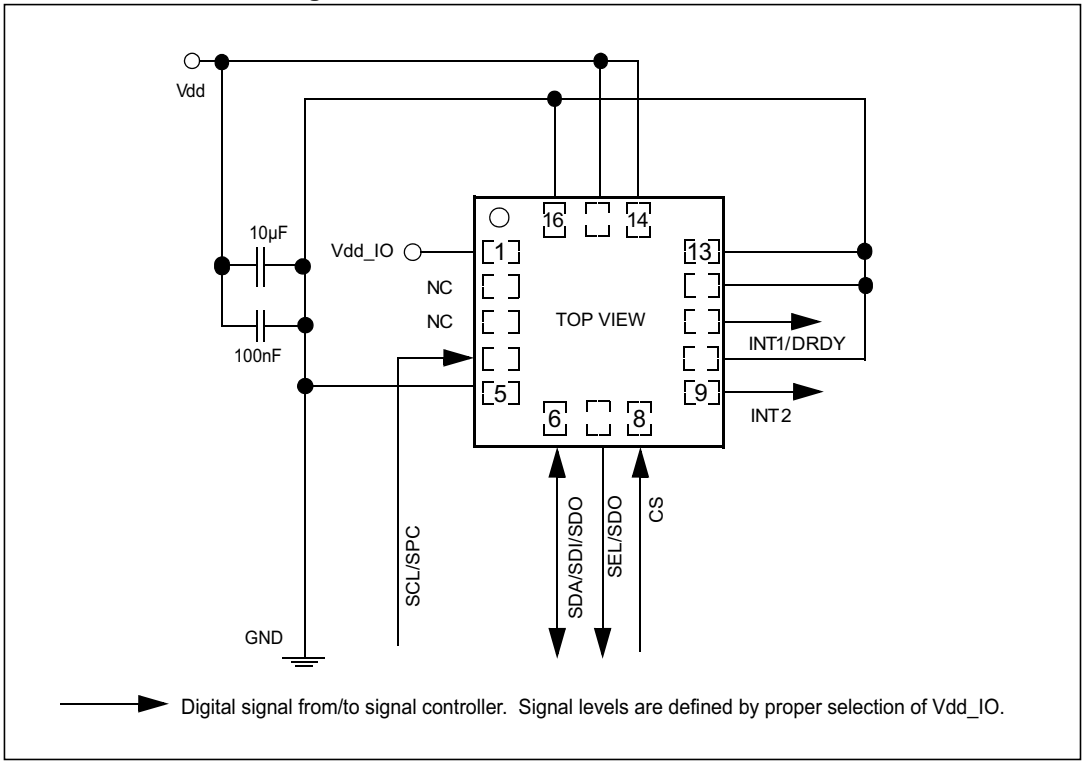
2.9 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff).

The trimming values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the active operation. This allows using the device without further calibration.

3 Application hints

Figure 5. LIS3DSH electrical connections



Note: Pin 15 can be connected to Vdd or GND or left unconnected.

The device core is supplied through the Vdd line while the I/O pins are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF) should be placed as near as possible to pin 14 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high.

3.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

4 Digital main blocks

4.1 State machine

The LIS3DSH embeds two state machines able to run a user-defined program.

The program is made up of a set of instructions that define the transition to successive states. Conditional branches are possible.

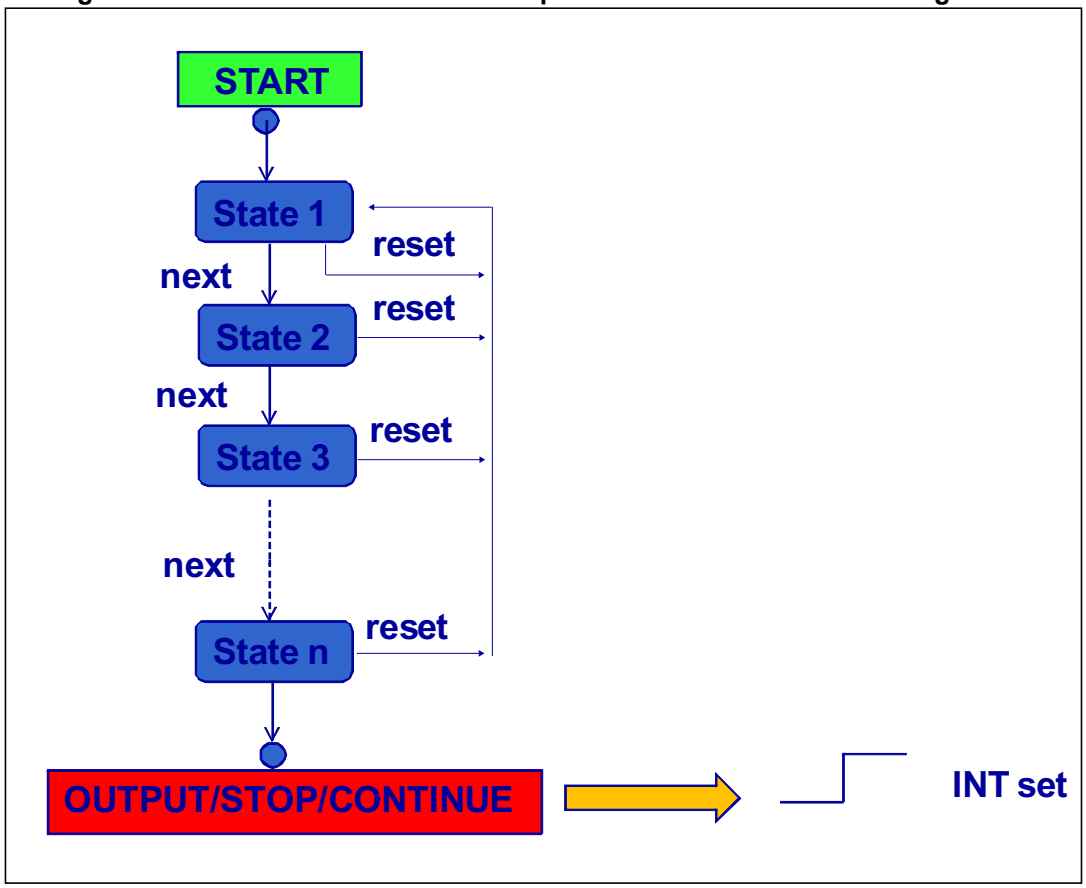
From each state (n) it is possible to have a transition to the next state (n+1) or to a reset state. The transition to the reset point happens when “RESET condition” is true; The transition to the next step happens when “NEXT condition” is true.

An interrupt is triggered when the output/stop/continue state is reached.

Each state machine allows implementing gesture recognition in a flexible way, free-fall, wake-up, 4D/6D orientation, pulse counter and step recognition, click/double-click, shake/double-shake, face-up/face-down, turn/double-turn:

- Code and parameters are loaded by the host into dedicated memory areas for the state program
- State program with timing based on ODR or decimated time
- Possibility of conditional branches

Figure 6. LIS3DSH state machines: sequence of state to execute an algorithm



4.2 FIFO

The LIS3DSH embeds an acceleration data FIFO for each of the three output channels, X, Y, and Z. This allows consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits. Programmable watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT1/2 pins.

4.2.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

4.2.2 FIFO mode

In FIFO mode, data from the X, Y, and Z channels are stored in the FIFO. A watermark interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it is full. When full, the FIFO stops collecting data from the input channels.

4.2.3 Stream mode

In Stream mode, data from the X, Y, and Z measurements are stored in the FIFO. A watermark interrupt can be enabled and set as in the FIFO mode. The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive.

4.2.4 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the X, Y, and Z measurements are stored in the FIFO. A watermark interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

4.2.5 Retrieving data from FIFO

FIFO data is read from the OUT_X, OUT_Y and OUT_Z registers. When the FIFO is in Stream, Bypass or FIFO mode, a read operation to the OUT_X, OUT_Y or OUT_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y, and Z data are placed in the OUT_X, OUT_Y and OUT_Z registers and both single-read and read-burst operations can be used.

5 Digital interfaces

The registers embedded inside the LIS3DSH may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 8. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SEL SDO	I^2C address selection SPI serial data output (SDO)

5.1 I^2C serial interface

The LIS3DSH I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 9. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LIS3DSH is 00111xxb where the xx bits are modified by the SEL/SDO pin in order to modify the device address. If the SEL pin is connected to the voltage supply, the address is 0011101b, otherwise the address is 0011110b if the SEL pin is connected to ground. This solution allows connecting and addressing two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LIS3DSH behaves as a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represents the actual register address while the ADD_INC bit (CTRL_REG6) defines the address increment.

The slave address is completed with a read/write bit. If the bit is '1' (Read), a repeated start (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write), the master transmits to the slave with direction unchanged. *Table 10* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 10. SAD+Read/Write patterns

Command	SAD[6:2]	SAD[1] = $\overline{SEL}$	SAD[0] = SEL	R/W	SAD+R/W
Read	00111	1	0	1	00111101
Write	00111	1	0	0	00111100
Read	00111	0	1	1	00111011
Write	00111	0	1	0	00111010

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DAT A		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW, to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

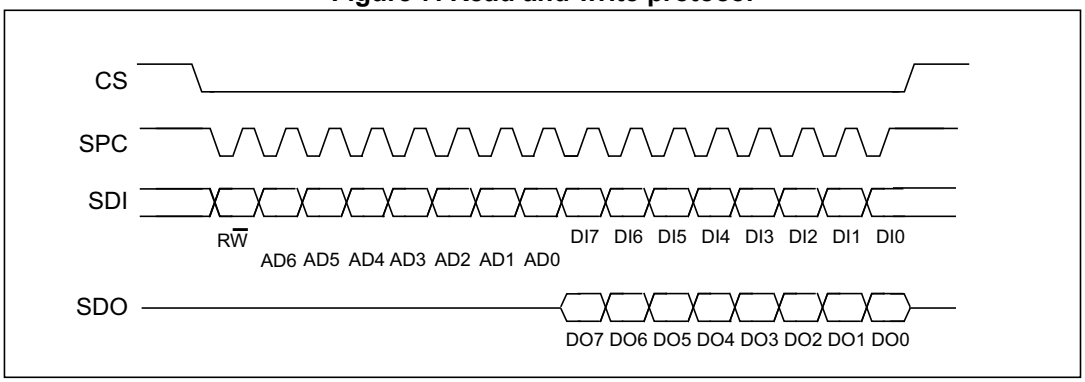
In the communication format presented, MAK is Master acknowledge and NMAK is No Master Acknowledge.

5.2 SPI bus interface

The LIS3DSH SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the outside world with 4 wires: CS, SPC, SDI and SDO.

Figure 7. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. SPC is the serial port clock and it is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI and SDO are respectively the serial port data input and output. Those lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of CS.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

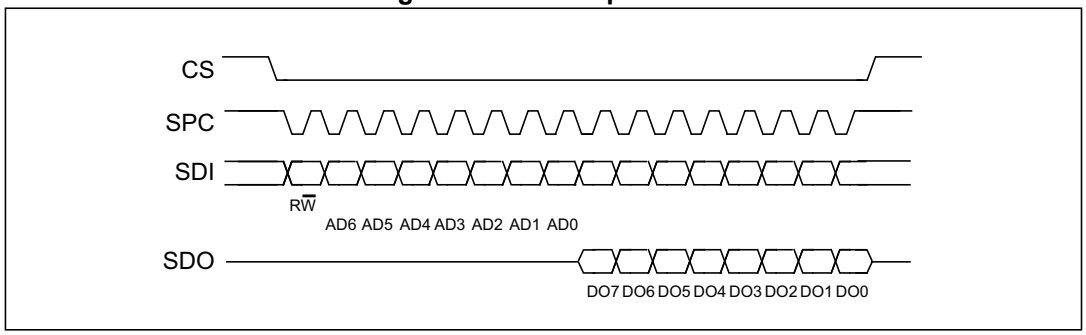
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the ADD_INC *OFF_X (10h)* bit is '0', the address used to read/write data remains the same for every block. When the ADD_INC bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 8. SPI read protocol



The SPI Read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

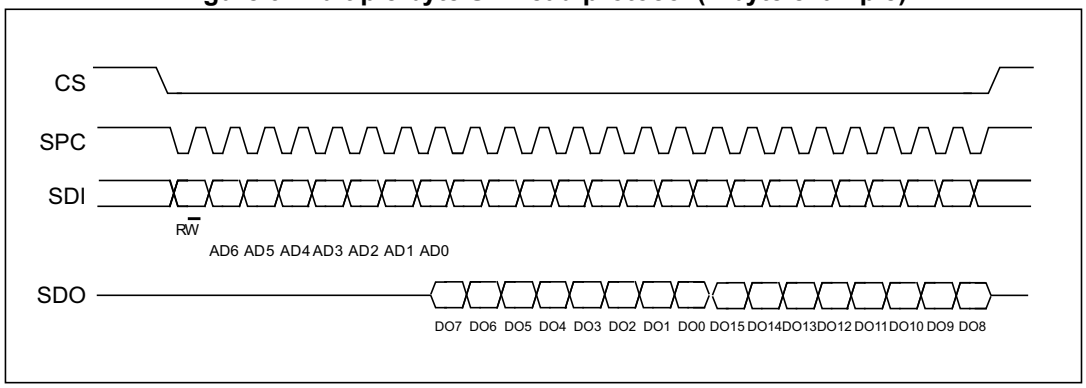
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

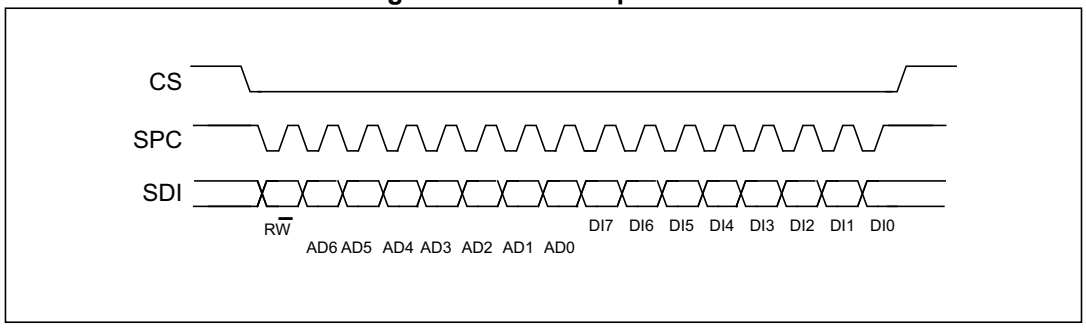
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 9. Multiple byte SPI read protocol (2-byte example)



5.2.2 SPI write

Figure 10. SPI write protocol



The SPI Write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

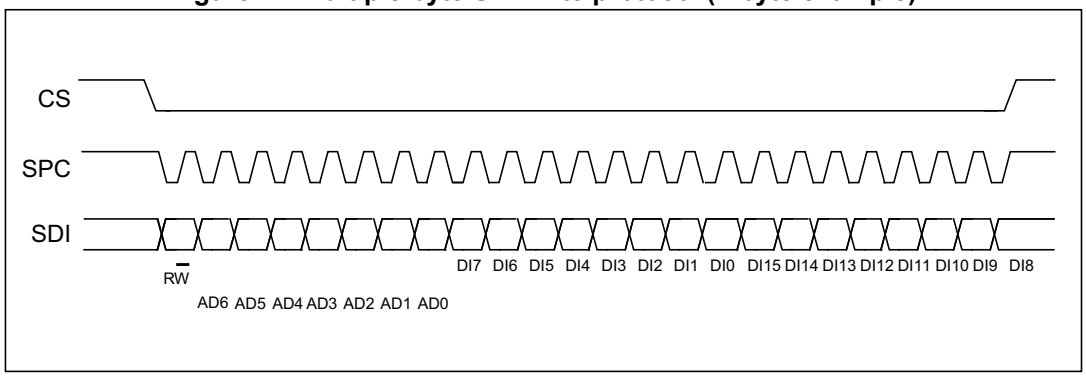
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

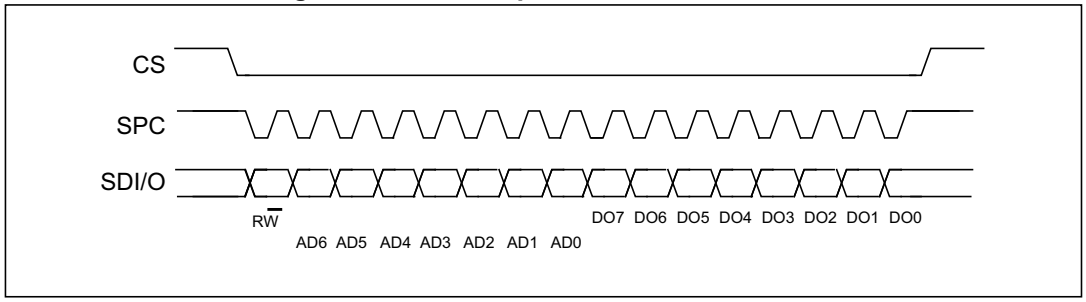
Figure 11. Multiple byte SPI write protocol (2-byte example)



5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM bit to ‘1’ (SPI serial interface mode selection) by internal register.

Figure 12. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

6 Register mapping

Table 15 provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

Table 15. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
OUT_T	r	0C	00001100	-	Temperature output
INFO1	r	0D	00001101	0010 0001	Information register 1
INFO2	r	0E	00001110	0000 0000	Information register 2
WHO_AM_I	r	0F	00001111	0011 1111	Who I am ID
OFF_X	r/w	10	00010000	0000 0000	X-axis offset correction
OFF_Y	r/w	11	00010001	0000 0000	Y-axis offset correction
OFF_Z	r/w	12	00010010	0000 0000	Z-axis offset correction
CS_X	r/w	13	00010011	0000 0000	Constant shift X
CS_Y	r/w	14	00010100	0000 0000	Constant shift Y
CS_Z	r/w	15	00010101	0000 0000	Constant shift Z
LC_L	r/w	16	00010110	0000 0001	Long counter registers
LC_H	r/w	17	00010111	0000 0000	
STAT	r	18	00011000	-	Interrupt synchronization
PEAK1	r	19	00011001	-	Peak value
PEAK2	r	1A	00011010	-	Peak value
VFC_1	r/w	1B	00011011	-	Vector filter coefficient 1
VFC_2	r/w	1C	00011100	-	Vector filter coefficient 2
VFC_3	r/w	1D	00011101	-	Vector filter coefficient 3
VFC_4	r/w	1E	00011110	-	Vector filter coefficient 4
THRS3	r/w	1F	00011111	-	Threshold value 3
CTRL_REG4	r/w	20	00100000	0000 0111	Control register
CTRL_REG1	r/w	21	00100001	0000 0000	SM1 control register
CTRL_REG2	r/w	22	00100010	0000 0000	SM2 control register
CTRL_REG3	r/w	23	00100011	0000 0000	Control registers
CTRL_REG5	r/w	24	00100100	0000 0000	
CTRL_REG6	r/w	25	00100101	0001 0000	
STATUS	r	27	00100111	-	Status data register

Table 15. Register address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
OUT_X_L	r	28	00101000	0000 0000	Output registers
OUT_X_H	r	29	00101001		
OUT_Y_L	r	2A	00101010		
OUT_Y_H	r	2B	00101011		
OUT_Z_L	r	2C	00101100		
OUT_Z_H	r	2D	00101101		
FIFO_CTRL	r/w	2E	00101110	0000 0000	FIFO registers
FIFO_SRC	r	2F	00101111	-	
ST1_X	w	40-4F	01000000 01001111	-	SM1 code register (X =1-16)
TIM4_1	w	50	01010000	-	SM1 general timer
TIM3_1	w	51	01010001	-	
TIM2_1	w	52-53	01010010 01010011	-	
TIM1_1	w	54-55	01010100 01010101	-	
THRS2_1	w	56	01010110	-	SM1 threshold value 1
THRS1_1	w	57	01010111	-	SM1 threshold value 2
MASK1_B	w	59	01011001	-	SM1 axis and sign mask
MASK1_A	w	5A	01011010	-	SM1 axis and sign mask
SETT1	w	5B	01011011	-	SM1 detection settings
PR1	r	5C	01011100	-	Program-reset pointer
TC1	r	5D-5E	01011101 01011110	-	Timer counter
OUTS1	r	5F	01011111	-	Main set flag
ST2_X	w	60-6F	01100000 01101111	-	SM2 code register (X =1-16)
TIM4_2	w	70	01110000	-	SM2 general timer
TIM3_2	w	71	01110001	-	
TIM2_2	w	72-73	01110010 01110011	-	
TIM1_2	w	74-75	01110100 01110101	-	
THRS2_2	w	76	01110110	-	SM2 threshold value 1
THRS1_2	w	77	01110111	-	SM2 threshold value 2

Table 15. Register address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
DES2	w	78	01111000	-	Decimation factor
MASK2_B	w	79	01111001	-	SM2 axis and sign mask
MASK2_A	w	7A	01111010		SM2 axis and sign mask
SETT2	w	7B	01111011	-	SM2 detection settings
PR2	r	7C	01111100	-	Program-reset pointer
TC2	r	7D-7E	01111101 01111110	-	Timer counter
OUTS2	r	7F	01111111		Main set flag

Registers marked as '*Reserved*' must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Register description

7.1 OUT_T (0Ch)

Temperature output register. Temperature data (1LSB/deg - 8-bit resolution). The value is expressed as two's complement.

Table 16. OUT_T register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 17. OUT_T register description

Temp7-Temp0	Temperature data.

7.2 INFO1 (0Dh)

Read-only information register.

Table 18. INFO1 register default values

0	0	1	0	0	0	0	1

7.3 INFO2 (0Eh)

Read-only information register.

Table 19. INFO2 register default values

0	0	0	0	0	0	0	0

7.4 WHO_AM_I (0Fh)

Who_AM_I register.

Table 20. WHO_AM_I register default values

0	0	1	1	1	1	1	1

7.5 OFF_X (10h)

Offset correction X-axis register, signed value.

Table 21. Offset X register

OFFx_7	OFFx_6	OFFx_5	OFFx_4	OFFx_3	OFFx_2	OFFx_1	OFFx_0

Table 22. Offset X register description

OFFx_[7:0]	Offset correction, X-axis. Default value: 0000 0000

7.6 OFF_Y (11h)

Offset correction Y-axis register, signed value.

Table 23. Offset Y register

OFFy_7	OFFy_6	OFFy_5	OFFy_4	OFFy_3	OFFy_2	OFFy_1	OFFy_0

Table 24. Offset Y register description

OFFy_[7:0]	Offset correction, Y-axis. Default value: 0000 0000

7.7 OFF_Z (12h)

Offset correction Z-axis register, signed value.

Table 25. Offset Z register

OFFz_7	OFFz_6	OFFz_5	OFFz_4	OFFz_3	OFFz_2	OFFz_1	OFFz_0

Table 26. Offset Z register description

OFFz_[7:0]	Offset correction, Z-axis. Default value: 0000 0000

7.8 CS_X (13h)

Constant shift, signed value X-axis register - state machine only.

Table 27. Constant shift X-axis register

CS_7	CS_6	CS_5	CS_4	CS_3	CS_2	CS_1	CS_0

Table 28. Constant shift X-axis register description

CS_[7:0]	Constant shift, X-axis. Default value: 0000 0000

7.9 CS_Y (14h)

Constant shift, signed value Y-axis register - state machine only.

Table 29. Constant shift Y-axis register

CS_7	CS_6	CS_5	CS_4	CS_3	CS_2	CS_1	CS_0

Table 30. Constant shift Y-axis register description

CS_[7:0]	Constant shift, Y-axis. Default value: 0000 0000

7.10 CS_Z (15h)

Constant shift, signed value Z-axis register - state machine only.

Table 31. Constant shift Z-axis register

CS_7	CS_6	CS_5	CS_4	CS_3	CS_2	CS_1	CS_0

Table 32. Constant shift Z-axis register description

CS_[7:0]	Constant shift, Z-axis. Default value: 0000 0000

7.11 LC (16h - 17h)

16-bit long-counter register for interrupt state machine program timing.

Table 33. LC_L register

LC_L_7	LC_L_6	LC_L_5	LC_L_4	LC_L_3	LC_L_2	LC_L_1	LC_L_0

Table 34. LC_L register description

LC_L_[7:0]	Long counter for interrupt state machine program timing, low values. Default value: 0000 0000

Table 35. LC_H register

LC_H_7	LC_H_6	LC_H_5	LC_H_4	LC_H_3	LC_H_2	LC_H_1	LC_H_0

Table 36. LC_H register description

LC_H_[7:0]	Long counter for interrupt state machine program timing, high values. Default value: 0000 0000

01h = counting stopped, 00h = counter full: interrupt available and counter is set to default.
Values higher than 00h: counting

7.12 STAT (18h)

Interrupt status - interrupt synchronization register.

Table 37. STAT register

LONG	SYNCW	SYNC1	SYNC2	INT_SM1	INT_SM2	DOR	DRDY

Table 38. STAT register description

LONG	0: no interrupt; 1: long counter (LC) interrupt flag common for both SM
SYNCW	Synchronization for external host controller interrupt based on output data (0: no action waiting from host; 1: action from host based on output data)
SYNC1	0: SM1 running normally; 1: SM1 stopped and await restart request from SM2
SYNC2	0: SM2 running normally; 1: SM2 stopped and await restart request from SM1
INT_SM1	SM1 - Interrupt Selection (1: SM1 interrupt enable; 0: SM1 interrupt disable)
NT_SM2	SM2 - Interrupt Selection (1: SM2 interrupt enable; 0: SM2 interrupt disable)
DOR	Data overrun indicates unread data from output register when next data sample measures start; (0: no overrun; 1: data overrun bit is reset when next sample is ready)
DRDY	Data ready from output register (0: data not ready; 1: data ready)

7.13 PEAK1 (19h)

Peak detection value register for SM1 operation.

Table 39. PEAK1 register

PKx_7	PKx_6	PKx_5	PKx_4	PKx_3	PKx_2	PKx_1	PKx_0

Table 40. PEAK1 register description

PKx_[7:0]	Peak detection for SM1. Default value: 0000 0000

Peak detected value for next condition SM1.

7.14 PEAK2 (1Ah)

Peak detection value register for SM2 operation.

Table 41. PEAK2 register

PKx_7	PKx_6	PKx_5	PKx_4	PKx_3	PKx_2	PKx_1	PKx_0

Table 42. PEAK2 register description

PKx_[7:0]	Peak detection for SM2. Default value: 0000 0000

Peak detected value for next condition SM2.

7.15 VFC_1 (1Bh)

Vector coefficient register 1 for diff. filter.

Table 43. Vector filter coefficient register 1 register

VFC1_7	VFC1_6	VFC1_5	VFC1_4	VFC1_3	VFC1_2	VFC1_1	VFC1_0

Table 44. Vector filter coefficient register 1 description

VFC1_[7:0]	Vector coefficient register 1 for diff. filter. Default value: 0000 0000

7.16 VFC_2 (1Ch)

Vector coefficient register 2 for diff. filter.

Table 45. Vector filter coefficient register 2

VFC2_7	VFC2_6	VFC2_5	VFC2_4	VFC2_3	VFC2_2	VFC2_1	VFC2_0

Table 46. Vector filter coefficient register 2 description

VFC2_[7:0]	Vector coefficient register 2 for diff. filter. Default value: 0000 0000

7.17 VFC_3 (1Dh)

Vector coefficient register 3 for FSM2 filter.

Table 47. Vector filter coefficient register 3

VFC3_7	VFC3_6	VFC3_5	VFC3_4	VFC3_3	VFC3_2	VFC3_1	VFC3_0

Table 48. Vector filter coefficient register 3 description

VFC3_[7:0]	Vector coefficient register 3 for FSM2 filter. Default value: 0000 0000

7.18 VFC_4 (1Eh)

Vector coefficient register 4 for diff filter.

Table 49. Vector filter coefficient register 4

VFC4_7	VFC4_6	VFC4_5	VFC4_4	VFC4_3	VFC4_2	VFC4_1	VFC4_0

Table 50. Vector filter coefficient register 4 description

VFC4_[7:0]	Vector coefficient register 4 for diff. filter. Default value: 0000 0000

7.19 THRS3 (1Fh)

Threshold value register.

Table 51. Threshold value register 3

THRS3_7	THRS3_6	THRS3_5	THRS3_4	THRS3_3	THRS3_2	THRS3_1	THRS3_0

Table 52. Threshold value register 3 description

THRS3_[7:0]	Threshold value, register 3. Default value: 0000 0000

7.20 CTRL_REG4 (20h)

Control register 4.

Table 53. Control register 4

ODR3	ODR2	ODR1	ODR0	BDU	Zen	Yen	Xen

Table 54. CTRL_REG4 register description

ODR 3:0	Output data rate and power mode selection. Default value: 0000 (see *Table 55*)
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

ODR[3:0] is used to set the power mode and ODR selection. In *Table 55* (output data rate selection) all available frequencies are shown.

Table 55. CTRL4 ODR configuration

ODR3	ODR2	ODR1	ODR0	ODR selection
0	0	0	0	Power down
0	0	0	1	3.125 Hz
0	0	1	0	6.25 Hz
0	0	1	1	12.5 Hz
0	1	0	0	25 Hz
0	1	0	1	50 Hz
0	1	1	0	100 Hz
0	1	1	1	400 Hz
1	0	0	0	800 Hz
1	0	0	1	1600 Hz

The **BDU** bit is used to inhibit the update of the output registers until both upper and lower register parts are read. In default mode (BDU = ‘0’) the output register values are updated continuously. When the BDU is activated (BDU = ‘1’), the content of the output registers is not updated until both MSb and LSb are read which avoids reading values related to different sample times.

7.21 CTRL_REG1 (21h)

SM1 control register.

Table 56. SM1 control register

HYST2_1	HYST1_1	HYST0_1	-	SM1_PIN	-	-	SM1_EN

Table 57. SM1 control register structure

HYST2_1 HYST1_1 HYST0_1	Hysteresis unsigned value to be added or subtracted from threshold value in SM1 Default value: 000
SM1_PIN	0: SM1 interrupt routed to INT1; 1: SM1 interrupt routed to INT2 pin Default value: 0
SM1_EN	0: SM1 disabled; 1: SM1 enabled Default value: 0

7.22 CTRL_REG2 (22h)

State program 2 interrupt MNG - SM2 control register.

Table 58. SM2 control register

HYST2_2	HYST1_2	HYST0_2	-	SM2_PIN	-	-	SM2_EN

Table 59. SM2 control register description

HYST2_2 HYST1_2 HYST0_2	Hysteresis unsigned value to be added or subtracted from threshold value in SM2. Default value: 000
SM2_PIN	0: SM2 interrupt routed to INT1; 1: SM2 interrupt routed to INT1 pin. Default value: 0
SM2_EN	0: SM2 disabled; 1: SM2 enabled. Default value: 0

7.23 CTRL_REG3 (23h)

Control register 3.

Table 60. Control register 3

DR_EN	IEA	IEL	INT2_EN	INT1_EN	VFILT	-	STRT

Table 61. CTRL_REG3 register description

DR_EN	DRDY signal enable to INT1. Default value: 0 (0: data ready signal not connected; 1: data ready signal connected to INT1)
IEA	Interrupt signal polarity. Default value: 0 (0: interrupt signals active LOW; 1: interrupt signals active HIGH)
IEL	Interrupt signal latching. Default value: 0 (0: interrupt signal latched; 1: interrupt signal pulsed)
INT2_EN	Interrupt 2 enable/disable. Default value:0 (0: INT2 signal disabled; 1: INT2 signal enabled)
INT1_EN	Interrupt 2 enable/disable. Default value: 0 (0: INT1/DRDY signal disabled; 1: INT1/DRDY signal enabled)
VFILT	Vector filter enable/disable. Default value: 0 (0: vector filter disabled; 1: vector filter enabled)
STRT	Soft reset bit (0: no soft reset; 1: soft reset (POR function)

7.24 CTRL_REG5 (24h)

Control register 5.

Table 62. Control register 5

BW2	BW1	FSCALE2	FSCALE1	FSCALE0	ST2	ST1	SIM

Table 63. Control register 5 description

BW2:BW1	Anti-aliasing filter bandwidth. Default value: 00 (00: 800 Hz; 01: 200 Hz; 10: 400 Hz; 11: 50 Hz)
FSCALE2:0	Full-scale selection. Default value: 00 (000: ±2 *g*; 001: ±4 *g*; 010: ±6 *g*; 011: ±8 *g*; 100: ±16 *g)*
ST2:1	Self-test enable. Default value: 00 (00: self-test disabled)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

Table 64. Self-test mode selection

ST2	ST1	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

7.25 CTRL_REG6 (25h)

Control register 6.

Table 65. Control register 6

BOOT	FIFO_EN	WTM_EN	ADD_ INC	P1_ EMPTY	P1_WTM	P1_OVER RUN	P2_ BOOT

Table 66. Control register 6 description

BOOT	Force reboot, cleared as soon as the reboot is finished. Active high.
FIFO_EN	FIFO enable. Default value: 0 (0: disable; 1: enable)
WTM_EN	Enable FIFO watermark level use. Default value: 0 (0: disable; 1: enable)
ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disable; 1: enable)
P1_EMPTY	Enable FIFO empty indication on Int1. Default value: 0 (0: disable; 1: enable)
P1_WTM	FIFO watermark interrupt on Int1. Default value: 0 (0: disable; 1: enable)
P1_OVERRUN	FIFO overrun interrupt on Int1. Default value: 0 (0: disable; 1: enable)
P2_BOOT	BOOT interrupt on Int2. Default value: 0 (0: disable; 1: enable)

7.26 STATUS (27h)

Status register.

Table 67. Status register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 68. Status register description

ZYXOR	X, Y, and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous)
ZYXDA	X, Y, and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

7.27 OUT_X (28h - 29h)

X-axis output register.

Table 69. OUT_X_L register

XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

Table 70. OUT_X_L register description

XD[7:0]	X-axis output, low values. Default value: 0000 0000

Table 71. OUT_X_H register

XD15	XD14	XD13	XD12	XD11	XD10	XD9	XD8

Table 72. OUT_X_H register description

XD[15:8]	X-axis output, high values. Default value: 0000 0000

7.28 OUT_Y (2Ah - 2Bh)

Y-axis output register.

Table 73. OUT_Y_L register

YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0

Table 74. OUT_Y_L register description

YD[7:0]	Y-axis output, low values. Default value: 0000 0000

Table 75. OUT_Y_H register

YD15	YD14	YD13	YD12	YD11	YD10	YD9	YD8

Table 76. OUT_Y_H register description

YD[15:8]	Y-axis output, high values. Default value: 0000 0000

7.29 OUT_Z (2Ch - 2Dh)

Z-axis output register.

Table 77. OUT_Z_L register

ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0

Table 78. OUT_Z_L register description

ZD[7:0]	Z-axis output, low values. Default value: 0000 0000

Table 79. OUT_Z_H register

ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8

Table 80. OUT_Z_H register description

ZD[15:8]	Z-axis output, high values. Default value: 0000 0000

7.30 FIFO_CTRL (2Eh)

FIFO control register.

Table 81. FIFO control register

FMODE2	FMODE1	FMODE0	WTMP4	WTMP3	WTMP2	WTMP1	WTMP0

Table 82. FIFO control register description

FMODE2:FMODE0	FIFO mode selection
WTMP4:WTMP0	FIFO watermark pointer; FIFO deep if the watermark is enabled.

Table 83. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode. FIFO turned off
0	0	1	FIFO mode. Stops collecting data when FIFO is full.
0	1	0	Stream mode. If the FIFO is full, the new sample overwrites the older one.
0	1	1	Stream mode until trigger is de-asserted, then FIFO mode
1	0	0	Bypass mode until trigger is de-asserted, then Stream mode
1	0	1	Not used
1	1	0	Not used.
1	1	1	Bypass mode until trigger is de-asserted, then FIFO mode

The FIFO trigger is the INT2 source.

7.31 FIFO_SRC (2Fh)

FIFO SRC control register.

Table 84. FIFO_SRC register

WTM	OVRN_ FIFO	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 85. FIFO_SRC register description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level)
OVRN_FIFO	Overrun bit status. (0: FIFO is not completely filled; 1: FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS0	FIFO stored data level

7.32 STx_1 (40h-4Fh)

State machine 1 code register STx_1 (x = 1-16).

State machine 1 system register is made up of 16, 8-bit registers to implement 16-step op-code.

7.33 TIM4_1 (50h)

8-bit general timer (unsigned value) for SM1 operation timing.

Table 86. Timer4 register

TM_7	TM_6	TM_5	TM_4	TM_3	TM_2	TM_1	TM_0

Table 87. Timer4 register description

TM[7:0]	General timer for SM1. Default value: 0000 0000

7.34 TIM3_1 (51h)

8-bit general timer (unsigned value) for SM1 operation timing.

Table 88. Timer3 register

TM_7	TM_6	TM_5	TM_4	TM_3	TM_2	TM_1	TM_0

Table 89. Timer3 register description

TM[7:0]	General timer for SM1. Default value: 0000 0000

7.35 TIM2_1 (52h - 53h)

16-bit general timer (unsigned value) for SM1 operation timing.

Table 90. TIM2_1_L register

TM_7	TM_6	TM_5	TM_4	TM_3	TM_2	TM_1	TM_0

Table 91. TIM2_1_L register description

TM[7:0]	General timer for SM1, low values. Default value: 0000 0000

Table 92. TIM2_1_H register

TM_15	TM_14	TM_13	TM_12	TM_11	TM_10	TM_9	TM_8

Table 93. TIM2_1_H register description

TM[15:8]	General timer for SM1, high values. Default value: 0000 0000

7.36 TIM1_1 (54h - 55h)

16-bit general timer (unsigned value) for SM1 operation timing.

Table 94. TIM1_1_L register

TM_7	TM_6	TM_5	TM_4	TM_3	TM_2	TM_1	TM_0

Table 95. TIM1_1_L register description

TM[7:0]	General timer for SM1, low values. Default value: 0000 0000

Table 96. TIM1_1_H register

TM_15	TM_14	TM_13	TM_12	TM_11	TM_10	TM_9	TM_8

Table 97. TIM1_1_H register description

TM[15:8]	General timer for SM1, high values. Default value: 0000 0000

7.37 THRS2_1 (56h)

Threshold value for SM1 operation.

Table 98. THRS2_1 register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 99. THRS2_1 register description

THS[7:0]	Threshold values for SM1. Default value: 0000 0000

7.38 THRS1_1 (57h)

Threshold value for SM1 operation.

Table 100. THRS1_1 register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 101. THRS1_1 register description

THS[7:0]	Threshold values for SM1. Default value: 0000 0000

7.39 MASK1_B (59h)

Axis and sign mask (swap) for SM1 motion-detection operation.

Table 102. MASK1_B axis and sign mask register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 103. MASK1_B register structure

P_X	0: X + disabled; 1: X + enabled
N_X	0: X - disabled; 1: X – enabled
P_Y	0: Y+ disabled; 1: Y + enabled
N_Y	0: Y- disabled; 1: Y – enabled
P_Z	0: Z + disabled; 1: Z + enabled
N_Z	0: Z - disabled; 1: Z – enabled
P_V	0: V + disabled; 1: V + enabled
N_V	0: V - disabled; 1: V – enabled

7.40 MASK1_A (5Ah)

Axis and sign mask (default) for SM1 motion-detection operation.

Table 104. MASK1_A axis and sign mask register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 105. MASK1_A register structure

P_X	0: X + disabled; 1: X + enabled
N_X	0: X - disabled; 1: X – enabled
P_Y	0: Y + disabled; 1: Y + enabled
N_Y	0: Y - disabled; 1: Y – enabled
P_Z	0: Z + disabled; 1: Z + enabled
N_Z	0: Z - disabled; 1: Z – enabled
P_V	0: V + disabled; 1: V + enabled
N_V	0: V - disabled; 1: V – enabled

7.41 SETT1 (5Bh)

Setting of threshold, peak detection and flags for SM1 motion-detection operation.

Table 106. SETT1 register structure

P_DET	THR3_SA	ABS	-	-	THR3_MA	R_TAM	SITR

Table 107. SETT1 register description

P_DET	SM1 peak detection. Default value: 0 (0: peak detection disabled; 1: peak detection enabled)
THR3_SA	Default value: 0 (0: no action; 1: threshold 3 limit value for axis and sign mask reset (MASKB_1)
ABS	Default value: 0 (0: unsigned thresholds; 1: signed thresholds)
THR3_MA	Default value: 0 (0: no action; 1: threshold 3 limit value for axis and sign mask reset (MASKA_1)
R_TAM	Next condition validation flag. Default value: 0 (0: no valid next condition found; 1: valid next condition found and reset)
SITR	Default value: 0 (0: no actions; 1: program flow can be modified by STOP and CONT commands)

7.42 PR1 (5Ch)

Program and reset pointer for SM1 motion-detection operation.

Table 108. PR1 register

RP3	RP2	RP1	RP0	PP3	PP2	PP1	PP0

Table 109. PR1 register description

RP3-RP0	SM1 reset pointer address
PP3-PP0	SM1 program pointer address

7.43 TC1 (5Dh-5E)

16-bit general timer (unsigned output value) for SM1 operation timing.

Table 110. TC1_L register

TC1_7	TC1_6	TC1_5	TC1_4	TC1_3	TC1_2	TC1_1	TC1_0

Table 111. TC1_L register description

TC1_[7:0]	General timer for SM1, low values. Default value: 0000 0000

Table 112. TC1_H register

TC1_15	TC1_14	TC1_13	TC1_12	TC1_11	TC1_10	TC1_9	TC1_8

Table 113. TC1_H register description

TC1_[15:8]	General timer for SM1, high values. Default value: 0000 0000

7.44 OUTS1 (5Fh)

Output flags on axis for interrupt SM1 management.

Table 114. OUTS1 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Read action of this register, depending on the flag affects SM1 interrupt functions.

Table 115. OUTS1 register description

P_X	0: X + no show; 1: X+ show
N_X	0: X - no show; 1: X – show
P_Y	0: Y + no show; 1: Y + show
N_Y	0: Y - no show; 1: Y – show
P_Z	0: Z + no show; 1: Z + show
N_Z	0: Z - no show; 1: Z – show
P_V	0: V + no show; 1: V + show
N_V	0: V - no show, 1: V – show

7.45 STx_1 (60h-6Fh)

State machine 2 code register STx_1 (x = 1-16).

State machine 2 system register is made up of 16 8-bit registers, to implement 16-step op-code.

7.46 TIM4_2 (70h)

8-bit general timer (unsigned value) for SM2 operation timing.

Table 116. Timer4 register

TM_7	TM_6	TM_5	TM_4	TM_3	TM_2	TM_1	TM_0

Table 117. Timer4 register description

TM_[7:0]	General timer for SM2. Default value: 0000 0000

7.47 TIM3_2 (71h)

8-bit general timer (unsigned value) for SM2 operation timing.

Table 118. Timer3 register

TM_7	TM_6	TM_5	TM_4	TM_3	TM_2	TM_1	TM_0

Table 119. Timer3 register description

TM_[7:0]	General timer for SM2. Default value: 0000 0000

7.48 TIM2_2 (72h - 73h)

16-bit general timer (unsigned value) for SM2 operation timing.

Table 120. TIM2_2_L register

TM_7	TM_6	TM_5	TM_4	TM_3	TM_2	TM_1	TM_0

Table 121. TIM2_2_L register description

TM_[7:0]	General timer for SM2, low values. Default value: 0000 0000

Table 122. TIM2_2_H register

TM_15	TM_14	TM_13	TM_12	TM_11	TM_10	TM_9	TM_8

Table 123. TIM2_2_H register description

TM_[15:8]	General timer for SM2, high values. Default value: 0000 0000

7.49 TIM1_2 (74h - 75h)

16-bit general timer (unsigned value) for SM2 operation timing.

Table 124. TIM1_2_L register

TM_7	TM_6	TM_5	TM_4	TM_3	TM_2	TM_1	TM_0

Table 125. TIM1_2_L register description

TM_[7:0]	General timer for SM2, low values. Default value: 0000 0000

Table 126. TIM1_2_H register

TM_15	TM_14	TM_13	TM_12	TM_11	TM_10	TM_9	TM_8

Table 127. TIM1_2_H register description

TM_[15:8]	General timer for SM2, high values. Default value: 0000 0000

7.50 THRS2_2 (76h)

Threshold signed value for SM2 operation.

Table 128. THRS2_2 register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 129. THRS2_2 register description

THS[7:0]	Threshold values for SM2. Default value: 0000 0000

7.51 THRS1_2 (77h)

Threshold signed value for SM2 operation.

Table 130. THRS1_2 register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 131. THRS1_2 register description

THS[7:0]	Threshold values for SM2. Default value: 0000 0000

7.52 DES2 (78h)

Decimation counter value register for SM2 operation.

Table 132. DES2 register

D7	D6	D5	D4	D3	D2	D1	D0

Table 133. DES2 register description

D[7:0]	Decimation counter values for SM2. Default value: 0000 0000

7.53 MASK2_B (79h)

Axis and sign mask (swap) for SM2 motion-detection operation.

Table 134. MASK2_B axis and sign mask register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 135. MASK2_B register description

P_X	0: X + disabled; 1: X + enabled
N_X	0: X - disabled; 1: X – enabled
P_Y	0: Y + disabled; 1: Y + enabled
N_Y	0: Y - disabled; 1: Y – enabled
P_Z	0: Z + disabled; 1: Z + enabled
N_Z	0: Z - disabled; 1: Z – enabled
P_V	0: V + disabled; 1: V + enabled
N_V	0: V - disabled; 1: V – enabled

7.54 MASK2_A (7Ah)

Axis and sign mask (default) for SM2 motion-detection operation.

Table 136. MASK2_A axis and sign mask register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 137. MASK2_A register description

P_X	0: X + disabled; 1: X + enabled
N_X	0: X - disabled; 1: X – enabled
P_Y	0: Y + disabled; 1: Y + enabled
N_Y	0: Y - disabled; 1: Y – enabled
P_Z	0: Z + disabled; 1: Z + enabled
N_Z	0: Z - disabled; 1: Z – enabled
P_V	0: V + disabled; 1: V + enabled
N_V	0: V - disabled; 1: V – enabled

7.55 SETT2 (7Bh)

Setting of threshold, peak detection and flags for SM2 motion-detection operation.

Table 138. SETT2 register

P_DET	THR3_SA	ABS	RADI	D_CS	THR3_MA	R_TAM	SITR

Table 139. SETT2 register description

P_DET	SM2 peak detection. Default value: 0 (0: peak detection disabled; 1: peak detection enabled)
THR3_SA	Default value: 0 (0: no action; 1: threshold 3 limit value for axis and sign mask reset (MASK2_B)
ABS	Default value: 0 (0: unsigned thresholds; 1: signed thresholds)
RADI	0: raw data; 1: diff. data for State Machine 2
D_CS	0: DIFF2 enabled (difference between current data and previous data); 1: constant shift enabled (difference between current data and constant values)
THR3_MA	Default value: 0 (0: no action; 1: threshold 3 limit value for axis and sign mask reset (MASK2_A)
R_TAM	Next condition validation flag. Default value: 0 (0: no valid next condition found; 1: valid next condition found and reset)
SITR	Default value: 0 (0: no actions; 1: program flow can be modified by STOP and CONT commands)

7.56 PR2 (7Ch)

Program and reset pointer for SM2 motion-detection operation.

Table 140. PR2 register

RP3	RP2	RP1	RP0	PP3	PP2	PP1	PP0

Table 141. PR2 register description

RP3-RP0	SM2 reset pointer address
PP3-PP0	SM2 program pointer address

7.57 TC2 (7Dh-7E)

16-bit general timer (unsigned output value) for SM2 operation timing.

Table 142. TC2_L register

TC2_7	TC2_6	TC2_5	TC2_4	TC2_3	TC2_2	TC2_1	TC2_0

Table 143. TC2_L register description

TC2_[7:0]	General timer for SM2, low values. Default value: 0000 0000

Table 144. TC2_H register

TC2_15	TC2_14	TC2_13	TC2_12	TC2_11	TC2_10	TC2_9	TC2_8

Table 145. TC2_H register description

TC2_[15:8]	General timer for SM2, high values. Default value: 0000 0000

7.58 OUTS2 (7Fh)

Output flags on axis for interrupt SM2 management.

Table 146. OUTS2 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Read action of this register, depending on the flag affects SM2 interrupt functions.

Table 147. OUTS2 register description

P_X	0: X + no show; 1: X + show
N_X	0: X - no show; 1: X – show
P_Y	0: Y + no show; 1: Y + show
N_Y	0: Y - no show; 1: Y – show
P_Z	0: Z + no show; 1: Z + show
N_Z	0: Z - no show; 1: Z – show
P_V	0: V + no show; 1: V + show
N_V	0: V - no show; 1: V – show

8 Package information

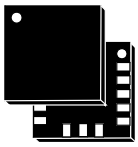
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 LGA-16 package information

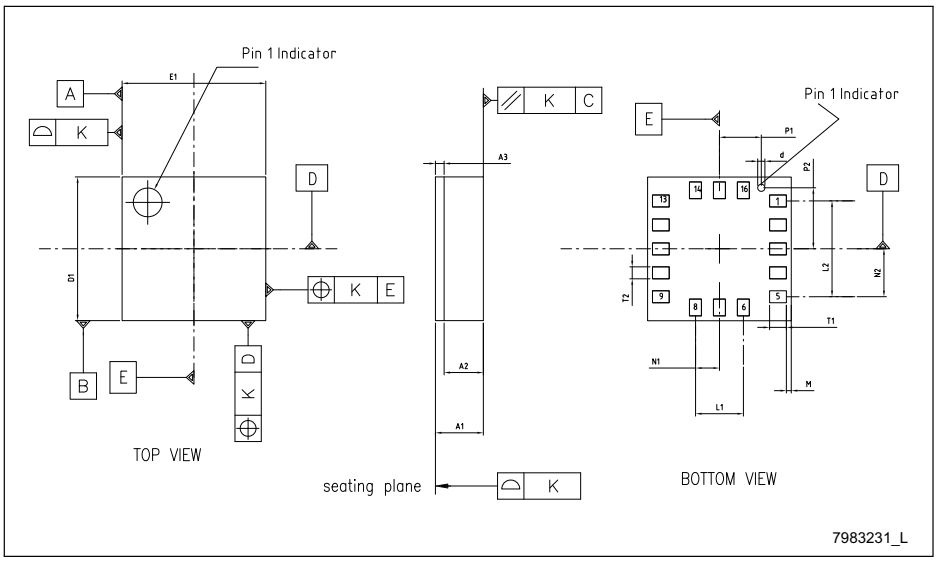
Figure 13. LGA-16: package outline and mechanical data

Ref.	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1			1.000			0.0394
A2		0.785			0 .0309	
A3		0.200			0 .0079	
D1	2.850	3.000	3 .150	0.1122	0.1181	0.1240
E1	2.850	3.000	3 .150	0.1122	0.1181	0.1240
L1		1.000	1 .060		0.0394	0.0417
L2		2.000	2 .060		0.0787	0.0811
N1		0.500			0 .0197	
N2		1.000			0 .0394	
M	0 .040	0.100	0 .160	0.0016	0.0039	0.0063
P1		0.875			0 .0344	
P2		1.275			0 .0502	
T1	0.290	0.350	0 .410	0.0114	0.0138	0.0161
T2	0.190	0.250	0 .310	0.0075	0.0098	0.0122
d		0 .150			0.0059	
k		0 .050			0.0020	

Outline and mechanical data



LGA-16 (3x3x1.0mm)
Land Grid Array Package



9 Revision history

Table 148. Document revision history

Date	Revision	Changes
26-Oct-2011	1	Initial release
15-Oct-2015	2	Document status promoted to production data Updated *Table 1: Device summary* Updated description of pin 15 in *Table 2: Pin description* Added Note concerning pin 15 below *Figure 5: LIS3DSH electrical connections* Updated description of BW bits in *Table 48: Control register 5 description* Updated package outline in *Figure 13: LGA-16: package outline and mechanical data* Minor textual updates
01-Sep-2017	3	Updated *Figure 7* through *Figure 12* in *Section 5: Digital interfaces* Added default values for CTRL_REGx registers and changed order of registers in *Table 15* and *Section 7: Register description* Added default value for ADD_INC bit in *Table 66* Updated bits 3 and 4 in *SETT2 (7Bh)* Updated *PR1 (5Ch)* and *PR2 (7Ch)* Updated registers *OFF_X (10h)* through *LC (16h - 17h)* Updated registers *PEAK1 (19h)* through *THRS3 (1Fh)* Updated registers *OUT_X (28h - 29h)* through *OUT_Z (2Ch - 2Dh)* Updated registers *TIM4_1 (50h)* through *THRS1_1 (57h)* and *TC1 (5Dh-5E)* Updated registers *TIM4_2 (70h)* through *DES2 (78h)* and *TC2 (7Dh-7E)*

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