LH7A404
32-Bit System-on-Chip

Preliminary data sheet

FEATURES

- 32-bit ARM9TDMI™ RISC Core
  - 16 kB Cache: 8 kB Instruction and 8 kB Data Cache
  - MMU (Windows CE™ Enabled)
  - Up to 266 MHz; See Table 1 for speed options
- 80 kB On-Chip Static RAM
- Vectored Interrupt Controller
- External Bus Interface
  - Up to 133 MHz; See Table 1 for bus speed options
  - Asynchronous and Synchronous interface RAM, Flash, PC Card and CompactFlash
- Clock and Power Management
  - 32.768 kHz and 14.7456 MHz Oscillators
  - Programmable PLL
- Programmable LCD Controller
  - Up to 1,024 × 768 Resolution
  - Supports STN, Color STN, AD-TFT, HR-TFT, TFT
  - Up to 64 K-Colors and 15 Gray Shades
- 9 Channel, 10-bit A/D Converter
  - Touch Screen Controller
  - Brownout Detector
- DMA (12 Channels)
  - External DMA Channels
  - AC97
  - MMC
  - USB
- USB 2.0 Full Speed Host (two downstream ports)
- USB 2.0 Full Speed Device
- Synchronous Serial Port (SSP)
  - Motorola SPI™, Texas Instruments SSI, National Semiconductor MICROWIRE™
- On-board Boot ROM
  - Variety of Boot Modes: external ROM, NAND Flash, Serial EEPROM, or XMODEM
- PS/2 Keyboard/Mouse Interface (KMI)
- Three Programmable Timers
- Three UARTs, one with Classic IrDA (115 kbit/s)
- Smart Card Interface (ISO7816)
- Four Pulse Width Modulators (PWMs)
- MultiMediaCard Interface with Secure Digital (MMC 2.11/SD 1.0)
- AC97 Codec Interface
- Smart Battery Monitor Interface
- Real Time Clock (RTC)
- Up to 64 General Purpose I/O Channels
- Watchdog Timer
- JTAG Debug Interface and Boundary Scan
- Operating Voltage
  - 1.8 V (200 MHz), 2.1 V (266 MHz) Core
  - 3.3 V Input/Output (Except XTALIN is 1.8 V)
- 5 V Tolerant Digital Inputs (excludes oscillator pins)
  - Oscillator pins T19, T20, Y18, Y19: 1.8 V ± 10 %
- Operating Temperature: –40°C to +85°C
- 324-Ball LFBGA Package

DESCRIPTION

The advent of 3G technology opens up a wide range of multimedia applications in mobile information appliances. The LH7A404 is designed from the ground up with a 32-bit ARM922 Core to provide high processing performance, low power consumption, and a high level of integration. Features include 80 kB on-chip SRAM, fully static design, power management unit, low voltage (1.8 V Core, 3.3 V I/O) and on-chip PLL.

NOTE: Devices containing lead-free solder formulations have different reflow temperatures than leaded-solder formulations. When using both solder formulations on the same PC board, designers should consider the effect of different reflow temperatures on the overall PCB assembly process. (Refer to www.nxp.com for an application note on recommended soldering practices).

Table 1. LH7A404 Versions

PART NUMBER[1]	CORE CLOCK	BUS CLOCK	LOW POWER CURRENT BY MODE	VERSION
LH7A404-N0F-092-xx[2]	266 MHz	133 MHz	Run = 228 mA (Typ.); Halt = 60 mA (Typ.); Standby = 200 µA (Typ.)	SOT1021-1
LH7A404-N0F-000-xx[2]	200 MHz	100 MHz	Run = 147 mA (Typ.); Halt = 41 mA (Typ.); Standby = 70 µA (Typ.)	SOT1021-1

NOTES:
1. Where 'xx' is a two digit revision number, e.g. B2; refer to www.NXP.com for a list of all the active revisions
2. Lead-free part.

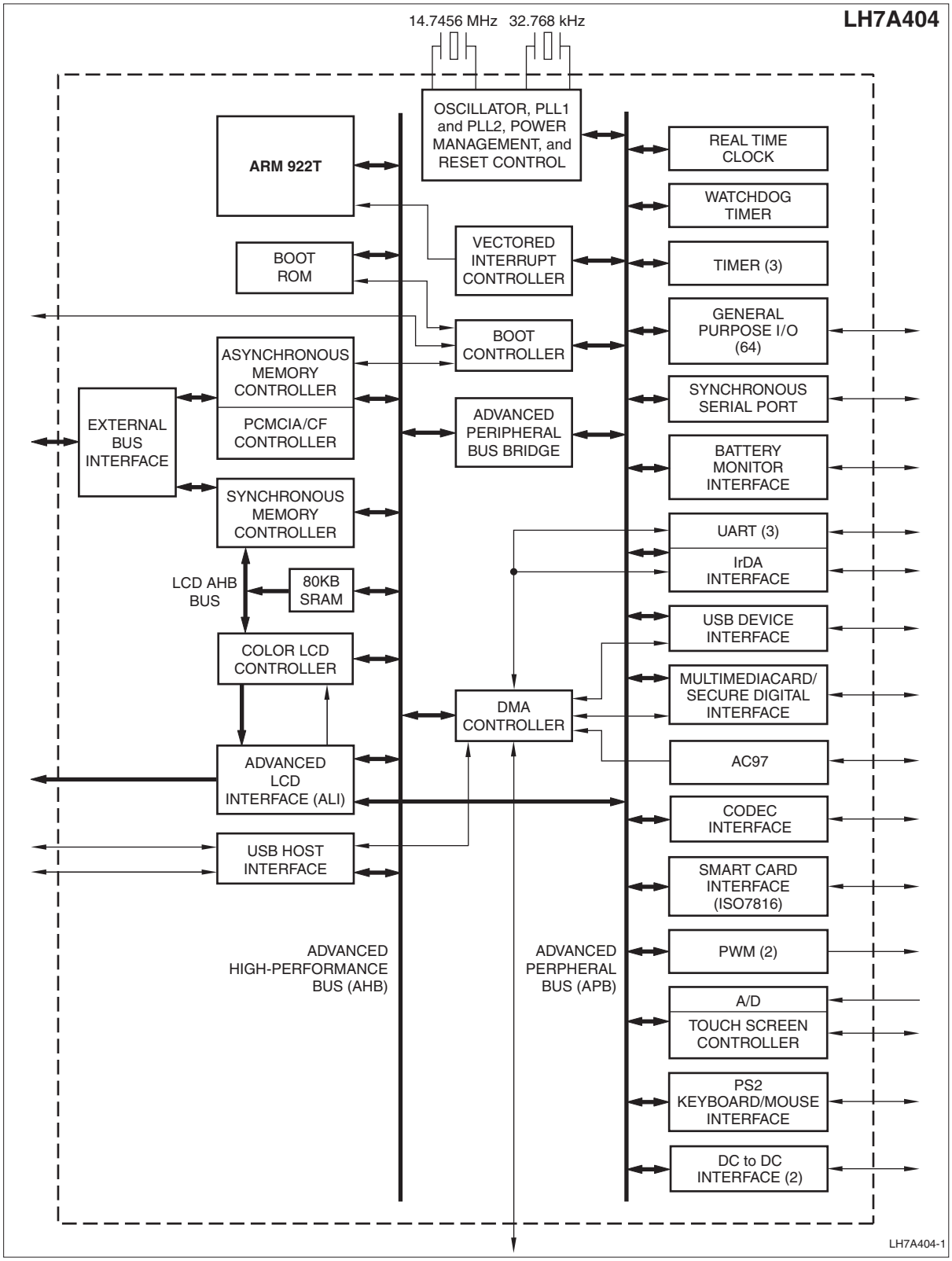


Figure 1. LH7A404 Block Diagram

Table 2. LH7A404 Functional Pin List

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
E10	VDD	I/O Ring Power					
E11							
H10							
H11							
K5							
K8							
K13							
K16							
L5							
L8							
L13							
L16							
N10							
N11							
T10							
T11							
U18							
J9	VSS	I/O Ring Ground					
J10							
J11							
J12							
K9							
K10							
K11							
K12							
L9							
L10							
L11							
L12							
M9							
M10							
M11							
M12							
T18							
E7	VDDC	Core Power					
E9							
E14							
G5							
G16							
P5							
P16							
T7							
T12							
T14							

Table 2. LH7A404 Functional Pin List (Cont'd)

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
E6	VSSC	Core Ground					
E15							
F5							
F16							
J16							
M5							
R5							
R16							
T6							
T15							
Y17	VDDA	Analog Power for PLL1 and PLL2					
W17							
V16	VSSA	Analog Ground for PLL1 and PLL2					
U15							
W16	VDDAD	Analog Power for A/D, Touch Screen Controller					
V13	VSSAD	Analog Ground for A/D, Touch Screen Controller					
D2	nPOR	Power on Reset	Input	Input		I	3
E1	nURESET	User Reset	Input	Input		I	3
F3	WAKEUP	Wake Up	Input	Input		I	3
F4	nPWRFL	Power Fail Signal	Input	Input		I	3
C1	nEXTPWR	External Power	Input	Input		I	3
C5	nRESETOUT	Reset Output to external devices. This pin carries the same state as the internal SoC reset signal.	LOW		12 mA	O	
Y18	XTALIN	14.7456 MHz Crystal Oscillator pins. For an external clock source, XTALIN can be used while XTALOUT is left unconnected. XTALIN voltage is 1.8 V nominal.					
Y19	XTALOUT						
T19	XTAL32IN	32.768 kHz Real Time Clock, Crystal Oscillator pins. To drive the device from an external clock source, XTAL32IN can be used while XTAL32OUT is left unconnected.					
T20	XTAL32OUT						
L2	PGMCLK	Programmable Clock (14.7456 MHz MAX.)	LOW	LOW	8 mA	O	
T16	CLKEN	External Oscillator Enable Output	LOW	LOW	8 mA	I/O	
Y13	WIDTH0	Boot Width Pins. Used with the MEDCHG and INTBOOT bits for internal Boot ROM. On power up, the values on these pins are latched to determine the width and type of Boot device. Boot width can be 8-, 16-, or 32-bit. The pins must be pulled HIGH with a 33 kΩ resistor.	Input	Input		I	3
W13	WIDTH1						
E4	MEDCHG	Media Change bit; used at power on with INTBOOT and WIDTHx pins to determine boot device.	Input	No Change		I	3
Y20	INTBOOT	When LOW, boot device is selected according to the MEDCHG bit. When HIGH, the lower 64 kB addresses are mapped to the internal Boot ROM.	Input	No Change		I	

Table 2. LH7A404 Functional Pin List (Cont'd)

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
N19	D0	Data Bus	LOW	LOW	12 mA	I/O	
P20	D1						
N18	D2						
N20	D3						
M16	D4						
M18	D5						
L18	D6						
L17	D7						
L19	D8						
J19	D9						
K17	D10						
J18	D11						
H19	D12						
G20	D13						
G19	D14						
H17	D15						
F19	D16						
E20	D17						
E19	D18						
D20	D19						
E18	D20						
C20	D21						
D18	D22						
B20	D23						
C18	D24						
A20	D25						
B18	D26						
C16	D27						
B17	D28						
A18	D29						
A17	D30						
B15	D31						
P17	A0	Asynchronous Address Bus	HIGH	LOW	12 mA	O	
N16	A1						

Table 2. LH7A404 Functional Pin List (Cont'd)

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
N17	A2/SA0	Asynchronous Address Bus and Synchronous Address Bus	LOW	LOW	12 mA	O	
M19	A3/SA1						
M20	A4/SA2						
L20	A5/SA3						
M17	A6/SA4						
K18	A7/SA5						
K20	A8/SA6						
K19	A9/SA7						
J20	A10/SA8						
H20	A11/SA9						
J17	A12/SA10						
H18	A13/SA11						
F20	A14/SA12						
G18	A15/SA13						
H16	A16/SB0	• Asynchronous Address Bus • Synchronous Device Bank Address 0	LOW	LOW	12 mA	O	
F18	A17/SB1	• Asynchronous Address Bus • Synchronous Device Bank Address 1	LOW	LOW	12 mA	O	
G17	A18	Asynchronous Address Bus	LOW	LOW	12 mA	O	
F17	A19						
D19	A20	Asynchronous Address Bus	LOW	LOW	12 mA	O	4
E17	A21						
C19	A22	Asynchronous Address Bus	LOW	LOW	12 mA	O	
D17	A23						
B19	A24						
A16	A25						
D15	A26						
B14	A27						
V18	nCS0	Asynchronous Memory Chip Select 0	HIGH	HIGH	12 mA	O	
R19	nCS1	Asynchronous Memory Chip Select 1	HIGH	HIGH	12 mA	O	
R18	nCS2	Asynchronous Memory Chip Select 2	HIGH	HIGH	12 mA	O	
P19	nCS3	Asynchronous Memory Chip Select 3	HIGH	HIGH	12 mA	O	
R20	nCS6	Asynchronous Memory Chip Select 6	HIGH	No Change	12 mA	O	
R17	nCS7	Asynchronous Memory Chip Select 7	HIGH	No Change	12 mA	O	
C12	nOE	Asynchronous Memory Output Enable	HIGH	HIGH	12 mA	O	4
D12	nWE	Asynchronous Memory Write Enable	HIGH	HIGH	12 mA	O	4
P18	nWAIT	Asynchronous Memory Wait; pull HIGH if unused	Input	No Change		I	5
C17	nSCS0	Synchronous Memory Chip Select 0	HIGH	HIGH	12 mA	I/O	
A19	nSCS1	Synchronous Memory Chip Select 1	HIGH	HIGH	12 mA	I/O	
D16	nSCS2	Synchronous Memory Chip Select 2	HIGH	HIGH	12 mA	I/O	
E16	nSCS3	Synchronous Memory Chip Select 3	HIGH	HIGH	12 mA	I/O	
B16	nSWE	Synchronous Memory Write Enable	HIGH	HIGH	12 mA	O	
A14	SCKE0	Clock Enable 0 for Synchronous Memory	HIGH	No Change	12 mA	O	
B13	SCKE1_2	Clock Enable 1 OR 2 for Synchronous Memory	HIGH	No Change	12 mA	O	

Table 2. LH7A404 Functional Pin List (Cont'd)

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
C14	SCKE3	Clock Enable 3 for Synchronous Memory	Depends on MEDCHG	LOW	12 mA	I/O	
D14	SCLK	Synchronous Memory Clock	LOW	No Change	20 mA	I/O	2
A13	nBLE0	Byte Lane Enable 0	HIGH	HIGH	12 mA	I/O	
U9	nBLE1	Byte Lane Enable 1	HIGH	HIGH	12 mA	O	
Y7	nBLE2	Byte Lane Enable 2	HIGH	HIGH	12 mA	O	
C13	nBLE3	Byte Lane Enable 3	HIGH	HIGH	8 mA	O	
C15	nCAS	Synchronous Memory Column Address Strobe	HIGH	HIGH	12 mA	I/O	
A15	nRAS	Synchronous Memory Row Address Strobe	HIGH	HIGH	12 mA	I/O	
D13	DQM0	Data Mask for Synchronous Memories	HIGH	No Change	12 mA	O	
E13	DQM1						
B12	DQM2						
A12	DQM3						
M2	PA0/ LCDVD16	• GPIO Port A0 • LCD Data pin 16	PA0: Input	No Change	8 mA	I/O	
L4	PA1/ LCDVD17	• GPIO Port A1 • LCD Data pin 17	PA1: Input	No Change	8 mA	I/O	
M3	PA2	GPIO Port A[6:2]	PAx: Input	No Change	8 mA	I/O	
M4	PA3						
M1	PA4						
N3	PA5						
N2	PA6						
N1	PA7	• GPIO Port A7 • Boot Width Selection (See Table 6)	PA7: Input	No Change	8 mA	I/O	4
N4	PB0/UARTRX1	• GPIO Port B0 • UART1 Receive Data Input	PB0: Input	No Change	8 mA	I/O	
P3	PB1/UARTTX3	• GPIO Port B1 • UART3 Transmit Data Out	PB1: Input	No Change	8 mA	I/O	
P2	PB2/UARTRX3	• GPIO Port B2 • UART3 Receive Data In	PB2: Input	No Change	8 mA	I/O	
P1	PB3/UARTCTS3	• GPIO Port B3 • UART3 Clear to Send	PB3: Input	No Change	8 mA	I/O	
R3	PB4/UARTDCD3	• GPIO Port B4 • UART3 Data Carrier Detect	PB4: Input	No Change	8 mA	I/O	
N5	PB5/UARTDSR3	• GPIO Port B5 • UART3 Data Set Ready	PB5: Input	No Change	8 mA	I/O	
R2	PB6/SWID/SMBD	• GPIO Port B6 • Single Wire Data • Smart Battery Data	PB6: Input	No Change	8 mA	I/O	
R1	PB7/SMBCLK	• GPIO Port B7 • Smart Battery Clock	PB7: Input	No Change	8 mA	I/O	
P4	PC0/UARTTX1	• GPIO Port C0 • UART1 Transmit Data Output	PC0: LOW	No Change	12 mA	I/O	
T1	PC1	GPIO Port C[5:1]	PCx: LOW	No Change	12 mA	I/O	
T2	PC2						
T3	PC3						
R4	PC4						
U1	PC5						
U2	PC6	GPIO Port C6	PC6: LOW	No Change	12 mA	I/O	4

Table 2. LH7A404 Functional Pin List (Cont'd)

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
V1	PC7	GPIO Port C7	PC7: LOW	No Change	12 mA	I/O	
Y11	PD0/LCDVD8	• GPIO Port D[7:0] • LCD Video Data Interface	PDx: LOW	LOW if 8-bit LCD enabled; else No Change	12 mA	I/O	
U10	PD1/LCDVD9						
W12	PD2/LCDVD10						
V11	PD3/LCDVD11						
W11	PD4/LCDVD12						
U11	PD5/LCDVD13						
V12	PD6/LCDVD14						
Y12	PD7/LCDVD15						
Y9	PE0/LCDVD4	• GPIO Port E[3:0] • LCD Video Data Interface	PEx: Output	LOW if 8-bit LCD enabled; else No Change	12 mA	I/O	
W10	PE1/LCDVD5						
V10	PE2/LCDVD6						
T9	PE3/LCDVD7						
D4	PE4/SCCLKIN	• GPIO Port E4 • Smart Card Push-Pull Mode Clock Input	PE4: Output	No Change	12 mA	I/O	
C3	PE5/SCCLKEN	• GPIO Port E5 • Smart Card Push-Pull Mode External Clock Buffer Enable	PE5: Output	No Change	12 mA	I/O	
B2	PE6/SCIN	• GPIO Port E6 • Smart Card Push-Pull Mode Data Input	PE6: Output	No Change	12 mA	I/O	
A1	PE7/SCDATEN	• GPIO Port E7 • Smart Card Push-Pull Mode Data Out External Buffer Enable	PE7: Output	No Change	12 mA	I/O	
A9	PF0/INT0	• GPIO Port F0 • Interrupt 0	PF0: Input	No Change	8 mA	I/O	3
D9	PF1/INT1	• GPIO Port F1 • Interrupt 1	PF1: Input	No Change	8 mA	I/O	3
A8	PF2/INT2	• GPIO Port F2 • Interrupt 2	PF2: Input	No Change	8 mA	I/O	3
C8	PF3/INT3	• GPIO Port F3 • Interrupt 3	PF3: Input	No Change	8 mA	I/O	3
B8	PF4/INT4	• GPIO Port F4 • Interrupt 4	PF4: Input	No Change	8 mA	I/O	3
D8	PF5/INT5/ SCDETECT	• GPIO Port F5 • Interrupt 5 • Smart Card Interface Card Detect Signal	PF5: Input	No Change	8 mA	I/O	3
A7	PF6/INT6/ PCRDY1	• GPIO Port F6 • Interrupt 6 • Ready for Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PF6: Input	No Change	8 mA	I/O	3
E8	PF7/INT7/PCRDY2	• GPIO Port F7 • Interrupt 7 • Ready for Card 2 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PF7: Input	No Change	8 mA	I/O	3
Y2	PG0/nPCOE	• GPIO Port G0 • Output Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
W4	PG1/nPCWE	• GPIO Port G1 • Write Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	

Table 2. LH7A404 Functional Pin List (Cont'd)

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
Y3	PG2/nPCIOR	• GPIO Port G2 • I/O Read Strobe for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
U5	PG3/nPCIOW	• GPIO Port G3 • I/O Write Strobe for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
T5	PG4/nPCREG	• GPIO Port G4 • Register Memory Access for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
W5	PG5/nPCCE1	• GPIO Port G5 • Card Enable 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode. This signal and nPCCE2 are used by the PC Card for decoding low and high byte accesses.	LOW	No Change	8 mA	I/O	
Y4	PG6/nPCCE2	• GPIO Port G6 • Card Enable 2 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode. This signal and nPCCE1 are used by the PC Card for decoding low and high byte accesses.	LOW	No Change	8 mA	I/O	
W6	PG7/PCDIR	• GPIO Port G7 • Direction for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	LOW	No Change	8 mA	I/O	
V6	PH0/PCRESET1	• GPIO Port H0 • Reset Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PHx: Input	No Change	8 mA	I/O	
Y5	PH1/CFA8/ PCRESET2	• GPIO Port H1 • Address Bit 8 for PC Card (CompactFlash) in Single Card mode • Reset Card 2 for PC Card (PCMCIA or CompactFlash) in Dual Card mode	PHx: Input	No Change	8 mA	I/O	
W7	PH2/nPCSLOTE1	• GPIO Port H2 • Enable Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode. This signal is used for gating other control signals to the appropriate PC Card.	PHx: Input	No Change	8 mA	I/O	
U6	PH3/CFA9/ PCMCIAA25/ nPCSLOTE2	• GPIO Port H3 • Address Bit 9 for PC Card (CompactFlash) in Single Card mode • Address Bit 25 for PC Card (PCMCIA) in Single Card mode • Enable Card 2 for PC Card (PCMCIA or CompactFlash) in Dual Card mode. Used for gating other control signals to the appropriate PC Card.	PHx: Input	No Change	8 mA	I/O	
W8	PH4/nPCWAIT1	• GPIO Port H4 • WAIT Signal for Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PHx: Input	No Change	8 mA	I/O	
Y6	PH5/CFA10/ PCMCIAA24/ nPCWAIT2	• GPIO Port H5 • Address Bit 10 for PC Card (CompactFlash) in Single Card mode • Address Bit 24 for PC Card (PCMCIA) in Single Card mode • WAIT Signal for Card 2 for PC Card (PCMCIA or CompactFlash) in Dual Card mode	PHx: Input	No Change	8 mA	I/O	
V7	PH6/nAC97RESET	• GPIO Port H6 • AC97 Reset	PHx: Input	No Change	8 mA	I/O	

Table 2. LH7A404 Functional Pin List (Cont'd)

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
U7	PH7/ nPCSTATRE	• GPIO Port H7 • Status Read Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	PHx: Input	No Change	8 mA	I/O	
T4	LCDFP/LCDSPS	• LCD Frame Pulse • ALI Reset Row Driver Counter	LOW	LOW if not in ALI mode	12 mA	O	
V2	LCDLP/ LCDHRLP	• LCD Linepulse • ALI Latch Pulse	LOW	LOW if not in ALI mode	12 mA	O	
U3	LCDCLS	ALI Clock for Row Drivers	LOW	No Change	12 mA	O	
V3	LCDSPL	ALI Start Pulse Left for reverse scanning	LOW	No Change	12 mA	O	
U4	LCDUBL	ALI Up, Down signal for reverse scanning	LOW	No Change	12 mA	O	
W1	LCDSPR	ALI Start Pulse Right for normal scanning	LOW	No Change	12 mA	O	
V4	LCDLBR	ALI Output for reverse scanning	HIGH	No Change	12 mA	O	
W2	LCDMOD	ALI MOD Signal used by the row driver	LOW	No Change	12 mA	O	
V5	LCDPS	ALI Power Save	HIGH	No Change	12 mA	O	
Y1	LCDVDDEN	ALI Power Sequence Control	LOW	No Change	12 mA	O	
W3	LCDREV	ALI Reverse	HIGH	No Change	12 mA	O	
U8	LCDCLKIN	External Clock Input for LCD controller	Input	No Change		I	
V8	LCDVD0	LCD Video Data Interface	LOW	LOW	12 mA	O	
T8	LCDVD1						
W9	LCDVD2						
Y8	LCDVD3						
V9	LCDENAB/ LCDM	• LCD TFT Data Enable • LCD STN AC Bias	LOW	LOW	12 mA	O	
Y10	LCDDCLK	LCD Pixel Clock	LOW	LOW	12 mA	O	
U17	USBDCP	USB Device Full Speed Pull-up Resistor Control	Input	Input	12 mA	I	
U20	USBDP	USB Device Data Positive (Differential Pair)	Input	Input	12 mA	I/O	
U19	USBDN	USB Device Data Negative (Differential Pair)	Input	Input	12 mA	I/O	
W19	USBHDP0	USB Data Host Positive 0 (Differential Pair)	Input	HIGH	12 mA	I/O	
W20	USBHDN0	USB Data Host Negative 0 (Differential Pair)	Input	LOW	12 mA	I/O	
V19	USBHDP1	USB Data Host Positive 1 (Differential Pair)	Input	Input	12 mA	I/O	
V20	USBHDN1	USB Data Host Negative 1 (Differential Pair)	Input	Input	12 mA	I/O	
T17	USBHPWR	USB Host Power; This pin is connected to the remote USB Host Power Switch's Enable pin. In response to a fault condition, signalled on the nUSBHOVRCURR pin, the LH7A404 can assert this pin, which causes the power switch shut down.	LOW	No Change	12 mA	O	
V17	nUSBHOVRCURR	USB Host Overcurrent; The overcurrent input is used to indicate to the host a fault has occurred, resulting in current limiting. The LH7A404 can be programmed to cause the remote power switch to shut off by asserting USBHPWR in response to an nUSBHOVRCURR assertion.	Input	Input	12 mA	I	
D11	nPWME0	DC-DC Converter 0 PWM 0 Enable	Input	Input	8 mA	I/O	
A10	nPWME1	DC-DC Converter 1 PWM 1 Enable	Input	Input	8 mA	I/O	
C11	PWM0	DC-DC Converter 0 Output (Pulse Width Modulated)	LOW	Input	8 mA	I/O	
C10	PWM1	DC-DC Converter 1 Output (Pulse Width Modulated)	LOW	Input	8 mA	I/O	
B9	PWM2	PWM Output 2	LOW	No Change	8 mA	O	
D10	PWM3	PWM Output 3	LOW	No Change		O	
C9	PWMSYNC	PWM Synchronizing Input for PWM2	Input	No Change	8 mA	I	

Table 2. LH7A404 Functional Pin List (Cont'd)

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
C7	ACBITCLK	• Audio Codec (AC97) Clock • Audio Codec (ACI) Clock	Input	No Change	8 mA	I/O	
B7	ACOUT	• Audio Codec (AC97) Output • Audio Codec (ACI) Output	LOW	LOW	8 mA	O	
A6	ACSYNC	• Audio Codec (AC97) Synchronization • Audio Codec (ACI) Synchronization	LOW	LOW	8 mA	O	
B6	ACIN	• Audio Codec (AC97) Input • Audio Codec (ACI) Input	Input	No Change	8 mA	I/O	
A5	MMCCLK	MultiMediaCard Clock (20 MHz MAX.)	LOW	LOW	8 mA	I/O	
D7	MMCCMD	MultiMediaCard Command	Input	Input	8 mA	I/O	
C6	MMCDATA0	MultiMediaCard Data 0	Input	Input	8 mA	I/O	
B5	MMCDATA1	MultiMediaCard Data 1	Input	Input	8 mA	I/O	
A4	MMCDATA2	MultiMediaCard Data 2	Input	Input	8 mA	I/O	
B4	MMCDATA3	MultiMediaCard Data 3	Input	Input	8 mA	I/O	
F2	UARTCTS2	UART2 Clear to Send Signal	Input	Input	8 mA	I/O	
F1	UARTDCD2	UART2 Data Carrier Detect Signal	Input	Input	8 mA	I/O	
G2	UARTDSR2	UART2 Data Set Ready Signal	Input	Input	8 mA	I/O	
G3	UARTIRTX1	IrDA Transmit	LOW	No Change	8 mA	I/O	
G1	UARTIRRX1	IrDA Receive	Input	Input	8 mA	I/O	
H2	UARTTX2	UART2 Transmit Data Output	HIGH	No Change	8 mA	I/O	
G4	UARTRX2	UART2 Receive Data Input	Input	Input	8 mA	I/O	
K3	SSPCLK	Synchronous Serial Port Clock	LOW	LOW	8 mA	O	
L1	SSPRX	Synchronous Serial Port Receive	Input	Input	8 mA	I/O	
L3	SSPTX	Synchronous Serial Port Transmit	Input	Input	8 mA	I/O	
K4	SSPFRM	Synchronous Serial Port Frame Sync	HIGH	HIGH	8 mA	O	
J2	COL0	Keyboard Interface	HIGH	HIGH	8 mA	I/O	
H4	COL1						
H5	COL2						
J1	COL3						
J3	COL4						
J4	COL5						
J5	COL6						
K2	COL7						
E2	BATOK	Battery OK	Input	Input		I	3
D1	nBATCHG	Battery Change	Input	Input		I	3
U12	BATCNTL	Battery Control for A/D controller battery monitor	LOW	No Change	12 mA	O	
H1	KMIDAT	Keyboard/Mouse Data	Input	No Change	12 mA	I/O	
H3	KMICLK	Keyboard/Mouse Clock	Input	No Change	12 mA	I/O	
K1	TBUZ	Timer Buzzer Output (254 kHz MAX.)	LOW	LOW	8 mA	I/O	
Y16	AN0/UL/X+	• ADC channel 0 • Touch Screen Controller Upper Left • Touch Screen Controller X-plus	Input	Input		I	
Y15	AN1/UR/X-	• ADC channel 1 • Touch Screen Controller Upper Right • Touch Screen Controller X-minus	Input	Input		I	
W14	AN2/LL/Y+	• ADC channel 2 • Touch Screen Controller Lower Left • Touch Screen Controller Y-plus	Input	Input		I	

Table 2. LH7A404 Functional Pin List (Cont'd)

LFBGA	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE	I/O	NOTES
U13	AN3/LR/Y-	• ADC channel 3 • Touch Screen Controller Lower Right • Touch Screen Controller Y-minus	Input	Input		I	
V14	AN4/WIPER	• ADC channel 4 • Wiper input from 5-wire Touch Screen	Input	Input		I	
U14	VSS or VSSA	Connect pin to either VSS or VSSA	Input	Input		I	
V15	AN6	ADC channel 6	Input	Input		I	
W15	AN7	ADC channel 7	Input	Input		I	
T13	AN8	ADC channel 8	Input	Input		I	
Y14	AN9	ADC channel 9	Input	Input		I	
E12	SCIO	Smart Card Interface I/O	LOW	LOW	12 mA	I/O	
A11	SCCLK	Smart Card Interface Clock	LOW	LOW	12 mA	I/O	
B11	nSCRESET	Smart Card Interface Reset	LOW	LOW	12 mA	O	
B10	SCVCCEN	Smart Card Interface VCC Enable	LOW	No Change	12 mA	O	
D6	CTCLKIN	Counter Timer Clock Input	Input	No Change		I	
A3	DREQ0	DMA Request 0	Input	No Change		I	
D5	DACK0	DMA Acknowledge 0	Input	No Change	12 mA	I/O	
C4	DEOT0	DMA End of Transfer 0	Input	No Change	12 mA	I/O	
B3	DREQ1	DMA Request 1	Input	No Change		I	
A2	DACK1	DMA Acknowledge 1	Input	No Change	12 mA	I/O	
E5	DEOT1	DMA End of Transfer 1	Input	No Change	12 mA	I/O	
U16	nTEST0	Test Pin 0. Internal weak pull up to VDD. Status latched at nPOR going HIGH. Pull LOW for JTAG mode. Pull HIGH (or leave open) for Normal mode. See Table 3.	Input with pull-up	Input with pull-up		I	
W18	nTEST1	Test Pin 1. Internal weak pull up to VDD. Status latched at nPOR going HIGH. Pull HIGH (or leave open) for both JTAG and Normal mode. See Table 3.	Input with pull-up	Input with pull-up		I	
D3	TDI	JTAG Data In. Internal weak pull up to VDD.	Input	No Change		I	
C2	TCK	JTAG Clock. Internal weak pull up to VDD.	Input	No Change		I	3
B1	TDO	JTAG Data Out	High Z	No Change	4 mA	O	
E3	TMS	JTAG Test Mode Select. Internal weak pull up to VDD.	Input	No Change		I	

NOTES:
1. Signals beginning with 'n' are Active LOW.
2. The SCLK pin can source up to 12 mA and sink up to 20 mA. See 'DC Characteristics'.
3. Schmitt trigger input; see 'DC Specifications', page 31 for triggers points and hysteresis.
4. These pins have alternate NAND Flash functions during boot-up when using the internal Boot ROM. Consult the Boot ROM Chapter of the User's Guide for more information.
5. The nWAIT pin must be pulled HIGH with a 33 kΩ resistor to avoid the possibility of the SMC inadvertently going into WAIT.
6. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ.

Table 3. nTEST Pin Function

MODE	nTEST0	nTEST1	nURESET
JTAG	0	1	1
Normal	1	1	x

Table 4. LCD Controller Pins

LFBGA PIN	RESET STATE	LCD SIGNAL	STN						TFT	AD-TFT/ HR-TFT
			MONO 4-BIT		MONO 8-BIT		COLOR			
			SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL		
L4	PA1	LCDVD17								LOW
M2	PA0	LCDVD16								LOW
Y12	PD7	LCDVD15				MLSTN7		CLSTN7	Intensity	Intensity
V12	PD6	LCDVD14				MLSTN6		CLSTN6	BLUE4	BLUE4
U11	PD5	LCDVD13				MLSTN5		CLSTN5	BLUE3	BLUE3
W11	PD4	LCDVD12				MLSTN4		CLSTN4	BLUE2	BLUE2
V11	PD3	LCDVD11				MLSTN3		CLSTN3	BLUE1	BLUE1
W12	PD2	LCDVD10				MLSTN2		CLSTN2	BLUE0	BLUE0
U10	PD1	LCDVD9				MLSTN1		CLSTN1	GREEN4	GREEN4
Y11	PD0	LCDVD8				MLSTN0		CLSTN0	GREEN3	GREEN3
T9	PE3	LCDVD7		MLSTN3	MUSTN7	MUSTN7	CUSTN7	CUSTN7	GREEN2	GREEN2
V10	PE2	LCDVD6		MLSTN2	MUSTN6	MUSTN6	CUSTN6	CUSTN6	GREEN1	GREEN1
W10	PE1	LCDVD5		MLSTN1	MUSTN5	MUSTN5	CUSTN5	CUSTN5	GREEN0	GREEN0
Y9	PE0	LCDVD4		MLSTN0	MUSTN4	MUSTN4	CUSTN4	CUSTN4	RED4	RED4
Y8	LCDVD3	LCDVD3	MUSTN3	MUSTN3	MUSTN3	MUSTN3	CUSTN3	CUSTN3	RED3	RED3
W9	LCDVD2	LCDVD2	MUSTN2	MUSTN2	MUSTN2	MUSTN2	CUSTN2	CUSTN2	RED2	RED2
T8	LCDVD1	LCDVD1	MUSTN1	MUSTN1	MUSTN1	MUSTN1	CUSTN1	CUSTN1	RED1	RED1
V8	LCDVD0	LCDVD0	MUSTN0	MUSTN0	MUSTN0	MUSTN0	CUSTN0	CUSTN0	RED0	RED0
U3	LCDCLS	LCDCLS								LCDCLS
Y10	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK	LCDDCLK
T4	LCDFP	LCDFP/ LCDSPS	LCDFP	LCDFP	LCDFP	LCDFP	LCDFP	LCDFP	LCDFP	LCDSPS
V2	LCDLP	LCDLP/ LCDHRLP	LCDLP	LCDLP	LCDLP	LCDLP	LCDLP	LCDLP	LCDLP	LCDHRLP
W2	LCDMOD	LCDMOD								LCDMOD
V5	LCDPS	LCDPS								LCDPS
W3	LCDREV	LCDREV								LCDREV
V3	LCDSPL	LCDSPL								LCDSPL
V4	LCDLBR	LCDLBR								LCDLBR
W1	LCDSPR	LCDSPR								LCDSPR
U4	LCDUBL	LCDUBL								LCDUBL
Y1	LCDVDDEN	LCDVDDEN								LCDVDDEN
U8	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN	LCDCLKIN
V9	LCDENAB	LCDENAB/ LCDM	LCDM	LCDM	LCDM	LCDM	LCDM	LCDM	LCDENAB	

NOTES:
1. The Intensity bit is identically generated for all three colors.
2. MUSTN = Monochrome Upper Panel
   MLSTN = Monochrome Lower Panel
   CUSTN = Color Upper Panel
   CLSTN = Color Lower Panel

Table 5. LFBGA Numerical Pin List

LFBGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
A1	PE7/SCDATEN	95 mV/ns	12 mA
A2	DACK1	95 mV/ns	12 mA
A3	DREQ0		
A4	MMCDATA2	110 mV/ns	8 mA
A5	MMCCLK	110 mV/ns	8 mA
A6	ACSYNC	110 mV/ns	8 mA
A7	PF6/INT6/PCRDY1	110 mV/ns	8 mA
A8	PF2/INT2	110 mV/ns	8 mA
A9	PF0/INT0	110 mV/ns	8 mA
A10	nPWME1	95 mV/ns	12 mA
A11	SCCLK	95 mV/ns	12 mA
A12	DQM3	110 mV/ns	8 mA
A13	nBLE0	95 mV/ns	12 mA
A14	SCKE0	95 mV/ns	12 mA
A15	nRAS	95 mV/ns	12 mA
A16	A25	95 mV/ns	12 mA
A17	D30	95 mV/ns	12 mA
A18	D29	95 mV/ns	12 mA
A19	nSCS1	95 mV/ns	12 mA
A20	D25	95 mV/ns	12 mA
B1	TDO	100 mV/ns	4 mA
B2	PE6/SCIN	95 mV/ns	12 mA
B3	DREQ1		
B4	MMCDATA3	110 mV/ns	8 mA
B5	MMCDATA1	110 mV/ns	8 mA
B6	ACIN	110 mV/ns	8 mA
B7	ACOUT	110 mV/ns	8 mA
B8	PF4/INT4	110 mV/ns	8 mA
B9	PWM2	110 mV/ns	8 mA
B10	SCVCCEN	95 mV/ns	12 mA
B11	nSCRESET	95 mV/ns	12 mA
B12	DQM2	95 mV/ns	12 mA
B13	SCKE1_2	95 mV/ns	12 mA
B14	A27	95 mV/ns	12 mA
B15	D31	95 mV/ns	12 mA
B16	nSWE	95 mV/ns	12 mA
B17	D28	95 mV/ns	12 mA
B18	D26	95 mV/ns	12 mA
B19	A24	95 mV/ns	12 mA
B20	D23	95 mV/ns	12 mA
C1	nEXTPWR		
C2	TCK		
C3	PE5/SCCLKEN	95 mV/ns	12 mA
C4	DEOT0	95 mV/ns	12 mA
C5	nRESETOUT		

Table 5. LFBGA Numerical Pin List (Cont'd)

LFBGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
C6	MMCDATA	110 mV/ns	8 mA
C7	ACBITCLK	110 mV/ns	8 mA
C8	PF3/INT3	110 mV/ns	8 mA
C9	PWMSYNC		
C10	PWM1	110 mV/ns	8 mA
C11	PWM0	110 mV/ns	8 mA
C12	nOE	95 mV/ns	12 mA
C13	nBLE3	110 mV/ns	8 mA
C14	SCKE3	95 mV/ns	12 mA
C15	nCAS	95 mV/ns	12 mA
C16	D27	95 mV/ns	12 mA
C17	nSCS0	95 mV/ns	12 mA
C18	D24	95 mV/ns	12 mA
C19	A22	95 mV/ns	12 mA
C20	D21	95 mV/ns	12 mA
D1	nBATCHG		
D2	nPOR		
D3	TDI		
D4	PE4/SCCLKIN	95 mV/ns	12 mA
D5	DACK0	95 mV/ns	12 mA
D6	CTCLKIN		
D7	MMCCMD	110 mV/ns	8 mA
D8	PF5/INT5/SCDETECT	110 mV/ns	8 mA
D9	PF1/INT1	110 mV/ns	8 mA
D10	PWM3	110 mV/ns	8 mA
D11	nPWME0	110 mV/ns	8 mA
D12	nWE	95 mV/ns	12 mA
D13	DQM0	95 mV/ns	12 mA
D14	SCLK	190 mV/ns	20 mA
D15	A26	95 mV/ns	12 mA
D16	nSCS2	95 mV/ns	12 mA
D17	A23	95 mV/ns	12 mA
D18	D22	95 mV/ns	12 mA
D19	A20	95 mV/ns	12 mA
D20	D19	95 mV/ns	12 mA
E1	nURESET		
E2	BATOK		
E3	TMS		
E4	MEDCHG		
E5	DEOT1	95 mV/ns	12 mA
E6	VSSC		
E7	VDDC		
E8	PF7/INT7/PCRDY2	110 mV/ns	8 mA
E9	VDDC		
E10	VDD		

Table 5. LFBGA Numerical Pin List (Cont'd)

LFBGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
E11	VDD		
E12	SCIO	95 mV/ns	12 mA
E13	DQM1	95 mV/ns	12 mA
E14	VDDC		
E15	VSSC		
E16	nSCS3	95 mV/ns	12 mA
E17	A21	95 mV/ns	12 mA
E18	D20	95 mV/ns	12 mA
E19	D18	95 mV/ns	12 mA
E20	D17	95 mV/ns	12 mA
F1	UARTDCD2	110 mV/ns	8 mA
F2	UARTCTS2	110 mV/ns	8 mA
F3	WAKEUP		
F4	nPWRFL		
F5	VSSC		
F16	VSSC		
F17	A19	95 mV/ns	12 mA
F18	A17/SBANK1	95 mV/ns	12 mA
F19	D16	95 mV/ns	12 mA
F20	A14/SA12	95 mV/ns	12 mA
G1	UARTIRRX1	110 mV/ns	8 mA
G2	UARTDSR2	110 mV/ns	8 mA
G3	UARTIRTX1	110 mV/ns	8 mA
G4	UARTRX2	110 mV/ns	8 mA
G5	VDDC		
G16	VDDC		
G17	A18	95 mV/ns	12 mA
G18	A15/SA13	95 mV/ns	12 mA
G19	D14	95 mV/ns	12 mA
G20	D13	95 mV/ns	12 mA
H1	KMIDAT	95 mV/ns	12 mA
H2	UARTTX2	110 mV/ns	8 mA
H3	KMICLK	95 mV/ns	12 mA
H4	COL1	100 mV/ns	8 mA
H5	COL2	100 mV/ns	8 mA
H10	VDD		
H11	VDD		
H16	A16/SBANK0	95 mV/ns	12 mA
H17	D15	95 mV/ns	12 mA
H18	A13/SA11	95 mV/ns	12 mA
H19	D12	95 mV/ns	12 mA
H20	A11/SA9	95 mV/ns	12 mA
J1	COL3	100 mV/ns	8 mA
J2	COL0	100 mV/ns	8 mA
J3	COL4	100 mV/ns	8 mA

Table 5. LFBGA Numerical Pin List (Cont'd)

LFBGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
J4	COL5	100 mV/ns	8 mA
J5	COL6	100 mV/ns	8 mA
J9	VSS		
J10	VSS		
J11	VSS		
J12	VSS		
J16	VSSC		
J17	A12/SA10	95 mV/ns	12 mA
J18	D11	95 mV/ns	12 mA
J19	D9	95 mV/ns	12 mA
J20	A10/SA8	95 mV/ns	12 mA
K1	TBUZ	110 mV/ns	8 mA
K2	COL7	100 mV/ns	8 mA
K3	SSPCLK	110 mV/ns	8 mA
K4	SSPFRM	110 mV/ns	8 mA
K5	VDD		
K8	VDD		
K9	VSS		
K10	VSS		
K11	VSS		
K12	VSS		
K13	VDD		
K16	VDD		
K17	D10	95 mV/ns	12 mA
K18	A7/SA5	95 mV/ns	12 mA
K19	A9/SA7	95 mV/ns	12 mA
K20	A8/SA6	95 mV/ns	12 mA
L1	SSPRX	110 mV/ns	8 mA
L2	PGMCLK	110 mV/ns	8 mA
L3	SSPTX	110 mV/ns	8 mA
L4	PA1/LCDVD17	110 mV/ns	8 mA
L5	VDD		
L8	VDD		
L9	VSS		
L10	VSS		
L11	VSS		
L12	VSS		
L13	VDD		
L16	VDD		
L17	D7	95 mV/ns	12 mA
L18	D6	95 mV/ns	12 mA
L19	D8	95 mV/ns	12 mA
L20	A5/SA3	95 mV/ns	12 mA
M1	PA4	110 mV/ns	8 mA
M2	PA0/LCDVD16	110 mV/ns	8 mA

Table 5. LFBGA Numerical Pin List (Cont'd)

LFBGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
M3	PA2	110 mV/ns	8 mA
M4	PA3	110 mV/ns	8 mA
M5	VSSC		
M9	VSS		
M10	VSS		
M11	VSS		
M12	VSS		
M16	D4	95 mV/ns	12 mA
M17	A6/SA4	95 mV/ns	12 mA
M18	D5	95 mV/ns	12 mA
M19	A3/SA1	95 mV/ns	12 mA
M20	A4/SA2	95 mV/ns	12 mA
N1	PA7	110 mV/ns	8 mA
N2	PA6	110 mV/ns	8 mA
N3	PA5	110 mV/ns	8 mA
N4	PB0/UARTRX1	110 mV/ns	8 mA
N5	PB5/UARTDSR3	110 mV/ns	8 mA
N10	VDD		
N11	VDD		
N16	A1	95 mV/ns	12 mA
N17	A2/SA0	95 mV/ns	12 mA
N18	D2	95 mV/ns	12 mA
N19	D0	95 mV/ns	12 mA
N20	D3	95 mV/ns	12 mA
P1	PB3/UARTCTS3	110 mV/ns	8 mA
P2	PB2/UARTRX3	110 mV/ns	8 mA
P3	PB1/UARTTX3	110 mV/ns	8 mA
P4	PC0/UARTTX1	95 mV/ns	12 mA
P5	VDDC		
P16	VDDC		
P17	A0	95 mV/ns	12 mA
P18	nWAIT		
P19	nCS3	95 mV/ns	12 mA
P20	D1	95 mV/ns	12 mA
R1	PB7/SMBCLK	110 mV/ns	8 mA
R2	PB6/SWID/SMBD	110 mV/ns	8 mA
R3	PB4/UARTDCD3	110 mV/ns	8 mA
R4	PC4	95 mV/ns	12 mA
R5	VSSC		
R16	VSSC		
R17	nCS7	95 mV/ns	12 mA
R18	nCS2	95 mV/ns	12 mA
R19	nCS1	95 mV/ns	12 mA
R20	nCS6	95 mV/ns	12 mA
T1	PC1	95 mV/ns	12 mA

Table 5. LFBGA Numerical Pin List (Cont'd)

LFBGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
T2	PC2	95 mV/ns	12 mA
T3	PC3	95 mV/ns	12 mA
T4	LCDFP/LCDSPS	95 mV/ns	12 mA
T5	PG4/nPCREG	110 mV/ns	8 mA
T6	VSSC		
T7	VDDC		
T8	LCDVD1	95 mV/ns	12 mA
T9	PE3/LCDVD7	95 mV/ns	12 mA
T10	VDD		
T11	VDD		
T12	VDDC		
T13	AN8		
T14	VDDC		
T15	VSSC		
T16	CLKEN	110 mV/ns	8 mA
T17	USBHPWR	95 mV/ns	12 mA
T18	VSS		
T19	XTAL32IN		
T20	XTAL32OUT		
U1	PC5	95 mV/ns	12 mA
U2	PC6	95 mV/ns	12 mA
U3	LCDCLS	95 mV/ns	12 mA
U4	LCDUBL	95 mV/ns	12 mA
U5	PG3/nPCIOW	110 mV/ns	8 mA
U6	PH3/CFA9/PCMCIAA25/ nPCSLOTE2	110 mV/ns	8 mA
U7	PH7/nPCSTATRE	110 mV/ns	8 mA
U8	LCDCLKIN		
U9	nBLE1	95 mV/ns	12 mA
U10	PD1/LCDVD9	95 mV/ns	12 mA
U11	PD5/LCDVD13	95 mV/ns	12 mA
U12	BATCTL	95 mV/ns	12 mA
U13	AN3/LR/Y-		
U14	VSS or VSSA		
U15	VSSA		
U16	nTEST0		
U17	USBDCP		
U18	VDD		
U19	USBDN		
U20	USBDP		
V1	PC7	95 mV/ns	12 mA
V2	LCDLP/LCDHRLP	95 mV/ns	12 mA
V3	LCDSPL	95 mV/ns	12 mA
V4	LCDLBR	95 mV/ns	12 mA
V5	LCDPS	95 mV/ns	12 mA

Table 5. LFBGA Numerical Pin List (Cont'd)

LFBGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
V6	PH0/PCRESET1	110 mV/ns	8 mA
V7	PH6/nAC97RESET	110 mV/ns	8 mA
V8	LCDVD0	95 mV/ns	12 mA
V9	LCDENAB/LCDM	95 mV/ns	12 mA
V10	PE2/LCDVD6	95 mV/ns	12 mA
V11	PD3/LCDVD11	95 mV/ns	12 mA
V12	PD6/LCDVD14	95 mV/ns	12 mA
V13	VSSAD		
V14	AN4/WIPER		
V15	AN6		
V16	VSSA		
V17	nUSBHOVRCURR		
V18	nCS0	95 mV/ns	12 mA
V19	USBHDP1		
V20	USBHDN1		
W1	LCDSPR	95 mV/ns	12 mA
W2	LCDMOD	95 mV/ns	12 mA
W3	LCDREV	95 mV/ns	12 mA
W4	PG1/nPCWE	110 mV/ns	8 mA
W5	PG5/nPCCE1	110 mV/ns	8 mA
W6	PG7/PCDIR	110 mV/ns	8 mA
W7	PH2/nPCSLOTE1	110 mV/ns	8 mA
W8	PH4/nPCWAIT1	110 mV/ns	8 mA
W9	LCDVD2	95 mV/ns	12 mA
W10	PE1/LCDVD5	95 mV/ns	12 mA
W11	PD4/LCDVD12	95 mV/ns	12 mA
W12	PD2/LCDVD10	95 mV/ns	12 mA

Table 5. LFBGA Numerical Pin List (Cont'd)

LFBGA	SIGNAL	SLEW RATE	OUTPUT DRIVE
W13	WIDTH1		
W14	AN2/LL/Y+		
W15	AN7		
W16	VDDAD		
W17	VDDA		
W18	nTEST1		
W19	USBHDP0		
W20	USBHDN0		
Y1	LCDVDDEN	95 mV/ns	12 mA
Y2	PG0/nPCOE	110 mV/ns	8 mA
Y3	PG2/nPCIOR	110 mV/ns	8 mA
Y4	PG6/nPCCE2	110 mV/ns	8 mA
Y5	PH1/CFA8/PCRESET2	110 mV/ns	8 mA
Y6	PH5/CFA10/PCMCIAA24/ nPCWAIT2	110 mV/ns	8 mA
Y7	nBLE2	95 mV/ns	12 mA
Y8	LCDVD3	95 mV/ns	12 mA
Y9	PE0/LCDVD4	95 mV/ns	12 mA
Y10	LCDDCLK	95 mV/ns	12 mA
Y11	PD0/LCDVD8	95 mV/ns	12 mA
Y12	PD7/LCDVD15	95 mV/ns	12 mA
Y13	WIDTH0		
Y14	AN9		
Y15	AN1/UR/X-		
Y16	AN0/UL/X+		
Y17	VDDA		
Y18	XTALIN		
Y19	XTALOUT		
Y20	INTBOOT		

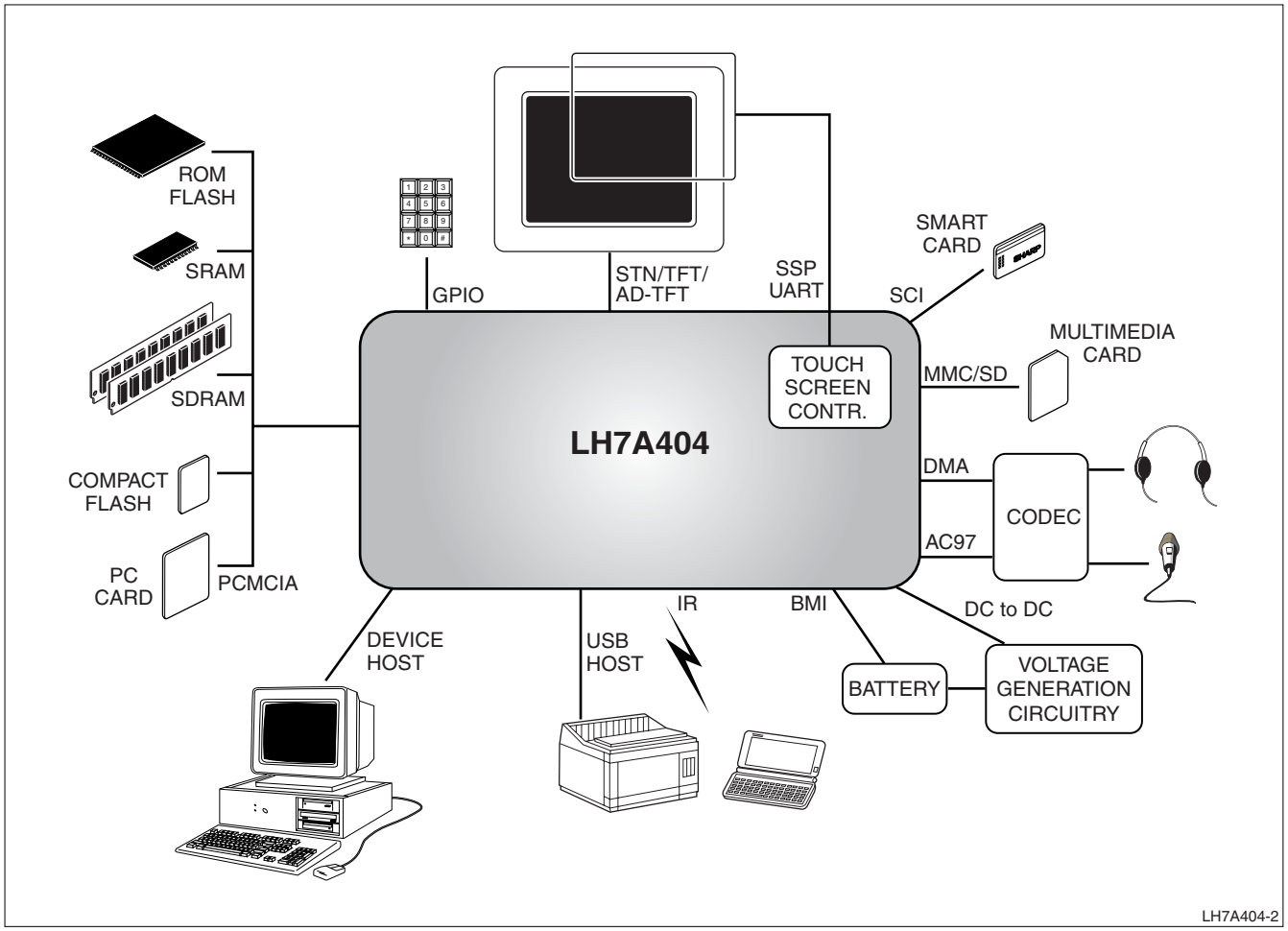


Figure 2. Application Diagram

SYSTEM DESCRIPTIONS

ARM922T Processor

The LH7A404 microcontroller features the ARM922T cached core with an Advanced High-performance Bus (AHB) interface. The processor is a member of the ARM9T family of processors. For more information, see the ARM document, 'ARM922T Technical Reference Manual', available on ARM's website at www.arm.com.

Clock and State Controller

The clocking scheme in the LH7A404 is based around two primary oscillator inputs. These are the 14.7456 MHz input crystal and the 32.768 kHz real time clock oscillator; see Figure 3. The 14.7456 MHz oscillator supplies the main system clock domains for the LH7A404. The 32.768 kHz oscillator controls the power-down operations and real time clock peripheral. The clock and state controller provides the clock gating and frequency division necessary, and then supplies the clocks to the processor and rest of the system. The amount of clock gating that actually takes place depends on the power saving mode selected.

The 32.768 kHz clock provides the source for the Real Time Clock tree and power-down logic. This clock is used for the power state control and is the only clock in the LH7A404 that runs continuously. The 32.768 kHz clock is divided down to 1 Hz for the Real Time Clock counter using a ripple divider to save power.

The 14.7456 MHz source is used to generate the main system clocks for the LH7A404. It is the source for PLL1 and PLL2, the primary clock for the peripherals, and the source clock to the programmable clock (PGM) divider.

PLL1 provides the main clock tree for the chip. It generates the following clocks: FCLK, HCLK, and PCLK. FCLK is the clock that drives the ARM922T core.

HCLK is the main bus (AHB) clock, as such it clocks all memory interfaces, bus arbitrators and the AHB peripherals. HCLK is generated by dividing FCLK by 1, 2, 3, or 4. HCLK can be gated by the system to enable low power operation.

PCLK is the peripheral bus (APB) clock. It is generated by dividing HCLK by either 2, 4, or 8.

PLL2 generates a fixed 48 MHz clock signal for the USB peripheral.

Power Modes

The LH7A404 has three operational states: Run, Halt, and Standby. During Run all clocks are hardware enabled and the processor is clocked. In the Halt mode the device is functioning, but the processor clock is halted while it waits for an event such as a key press. Standby equates to the computer being switched ‘off’, i.e. no display (LCD disabled) and the main oscillator is shut down.

Reset Modes

Three external signals can generate resets to the LH7A404: nPOR (power on reset), nPWRFL (power failure) and nURESET (user reset). If any of these are active, a system reset is internally generated. An nPOR reset performs a full system reset. The nPWRFL and nURESET resets perform a full system reset except for the SDRAM refresh control, SDRAM Global Configuration, SDRAM Device Configuration, and the RTC peripheral registers. The SDRAM controller issues a self-refresh command to external SDRAM before the system enters an nPWRFL and nURESET reset. This allows the system to maintain its Real Time Clock and SDRAM contents. Upon release of Reset, the chip enters Standby mode. Once in the Run mode the PWRSR register can be interrogated to determine the nature of the reset and the trigger source, after which software can then take appropriate actions.

Data Paths

The data paths in the LH7A404 are:

- The AMBA AHB bus
- The AMBA APB bus
- The External Bus Interface
- The LCD AHB bus
- The DMA busses.

AMBA AHB BUS

The Advanced Microprocessor Bus Architecture AHB (AMBA AHB) is a high speed 32-bit-wide data bus. The AMBA AHB is for high-performance, high-clock-frequency system modules.

LH7A404 peripherals and memory with high bandwidth requirements are connected to the ARM922T processor and other bus masters using a multi-master AHB bus. These peripherals include the external memory interfaces, on-chip SRAM, LCD Controller (bus master), DMA Controller (bus master), and USB Host (bus master). Remaining peripherals reside on the lower bandwidth Advanced Peripheral Bus (APB), which is accessed from the AHB via the APB Bridge. The APB Bridge is the only master on the APB, and its operation is transparent to the user as it converts AHB accesses into slower APB accesses automatically.

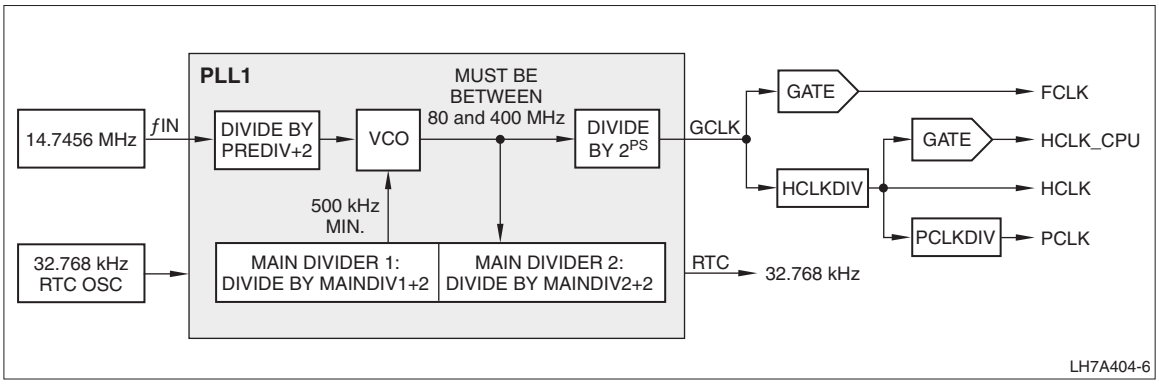


Figure 3. Clock and State Controller Block Diagram

AMBA APB BUS

The AMBA APB provides a lower-bandwidth bus for peripherals accessed less frequently. This reduces the loading on the AHB, allowing it to run faster to maximize system performance, while the APB can operate at a lower clock rate to conserve power. The APB Bridge is the only master on the APB. All AHB masters can access APB peripherals via the ABP Bridge. The APB clock frequency can be selected by software to divide the clock speed of the AHB bus by 2, 4, or 8.

EXTERNAL BUS INTERFACE (EBI)

The External Bus Interface (EBI) provides a 32-bit-wide, high speed gateway to external memory devices. The supported memory devices include:

- Asynchronous RAM/ROM/Flash
- Synchronous DRAM/Flash
- PCMCIA interfaces
- CompactFlash interfaces.

The EBI can be controlled by either the Asynchronous Memory Controller or Synchronous Memory Controller. There is an arbiter on the EBI input, with priority given to the Synchronous Memory Controller interface.

LCD BUS

The LCD controller has its own local memory bus that connects it to the system's embedded memory and external SDRAM. The function of this local data bus is to allow the LCD controller to perform its video refresh function without congesting the main AHB bus. This leads to better system performance and lower power consumption. There is an arbiter on both the embedded memory and the synchronous memory controller. In both cases the LCD bus is given priority.

DMA BUSES

The LH7A404 has a DMA system that connects the higher speed/higher data volume APB peripherals (MMC, USB Device and AC97) to the AHB bus. This enables the efficient transfer of data between these peripherals and external memory without the intervention of the ARM922T core.

USB HOST CONTROLLER DMA BUS

The USB Host Controller has its own DMA controller. It acts as another bus master on the AHB bus. It does not interact with the non-USB DMA controller except in bus arbitration.

Memory Map

The LH7A404 system has a 32-bit-wide address bus, allowing addressing up to 4GB of memory. This memory space is subdivided into a number of memory banks, shown in Figure 4. Four of these banks (each 256MB) are allocated to the Synchronous Memory Controller. Eight banks (each 256MB) are allocated to the Asynchronous Memory Controller. Two of these eight banks are designed for PCMCIA systems. Part of the remaining memory space is allocated to the embedded SRAM, and to the control registers of the AHB and APB. The rest of the memory space is not used.

The LH7A404 can boot from both internal and external devices. The selection is determined by the value of five pins at power-on reset as shown in Table 6. If booting is from an external device (with INTBOOT = 0), refer to Table 7. When booting from external synchronous memory, bank 4 (nSCS3) is mapped into memory location zero. When booting from external asynchronous memory, memory bank 0 (nSCS0) is mapped into memory location zero.

Figure 4 shows the memory map of the LH7A404 system for the two boot modes.

Once the LH7A404 has booted, the boot code can configure the ARM922T MMU to remap the low memory space to a location in RAM. This allows the user to set the interrupt vector table.

Table 6. Internal Boot Modes

BOOT DEVICE	GPIO PA7	LATCHED MEDCHG	LATCHED WIDTH1	LATCHED WIDTH0	LATCHED INTBOOT
External device	See Table 7				0
8-bit interface, 3-byte address NAND Flash	0	0	0	0	1
8-bit interface, 4-byte address NAND Flash	0	0	0	1	1
8-bit interface, 5-byte address NAND Flash	0	0	1	0	1
16-bit interface, 3-byte address NAND Flash	1	0	0	0	1
16-bit interface, 4-byte address NAND Flash	1	0	0	1	1
16-bit interface, 5-byte address NAND Flash	1	0	1	0	1
XMODEM using UART2	0	1	0	0	1
I^2C EEPROM	0	1	0	1	1
Undefined	0	0	1	1	1
	0	1	1	1	1
	1	0	1	1	1
	1	1	x	x	1

Table 7. External Boot Modes

BOOT MODE	MEDCHG	WIDTH1	WIDTH0	INTBOOT
8-bit ROM	0	0	0	0
16-bit ROM	0	0	1	0
32-bit ROM	0	1	0	0
Invalid: Do not allow this condition.	0	1	1	0
16-bit SynchFlash (Initializes device MODE Register)	1	0	0	0
16-bit SROM (Initializes device MODE Register)	1	0	1	0
32-bit SynchFlash (Initializes device MODE Register)	1	1	0	0
32-bit SROM (Initializes device MODE Register)	1	1	1	0
Boot from internal Boot ROM; see Table 6	x	x	x	1

Vectored Interrupt Controller (VIC)

The LH7A404 has two VICs working together to manage interrupt requests from on-chip and off-chip sources. Each VIC performs these primary functions:

- Determine if an interrupt source is disabled or can generate an FIQ or IRQ to the ARM core
- Prioritize up to 16 separate interrupt sources for simultaneous and nested processing
- Obtain the address of the interrupt handler (vector) for up to 16 interrupt sources
- Provide a default vector and a set of status registers for up to 16 non-vectored sources. Software determines the priority of these interrupts.

Two VICs are daisy-chained together to support up to 64 different interrupts, 32 of which are vectored. The VIC supports both FIQ and IRQ interrupts. FIQ interrupts have a higher priority than IRQ interrupts. If two interrupts with the same priority become active at the same time, the priority must be resolved in software. When an interrupt becomes active, the VIC generates an FIQ or IRQ if the corresponding mask bit is set. Interrupts are not latched in the VIC, but may latch on a particular peripheral when applicable.

After a power-on reset, all mask register bits are cleared, masking all interrupts. They must be set by software after power-on reset to enable interrupts.

A vectored interrupt has improved latency as it provides direct information about where its service routine is located and eliminates software arbitration needed with a simple interrupt controller.

The VICs continue to operate in Halt and Standby modes, so external interrupts may bring the chip out of these low power modes.

External Bus Interface

The ARM922T, LCD controller, and DMA engine have access to an external memory system. The LCD controller has access to an internal frame buffer in embedded SRAM and an extension buffer in Synchronous Memory for large displays. The processor and DMA engine share the main system bus, providing access to all external memory devices and the embedded SRAM frame buffer.

An arbitration unit ensures that control over the External Bus Interface (EBI) is only granted when an existing access has been completed. See Figure 4.

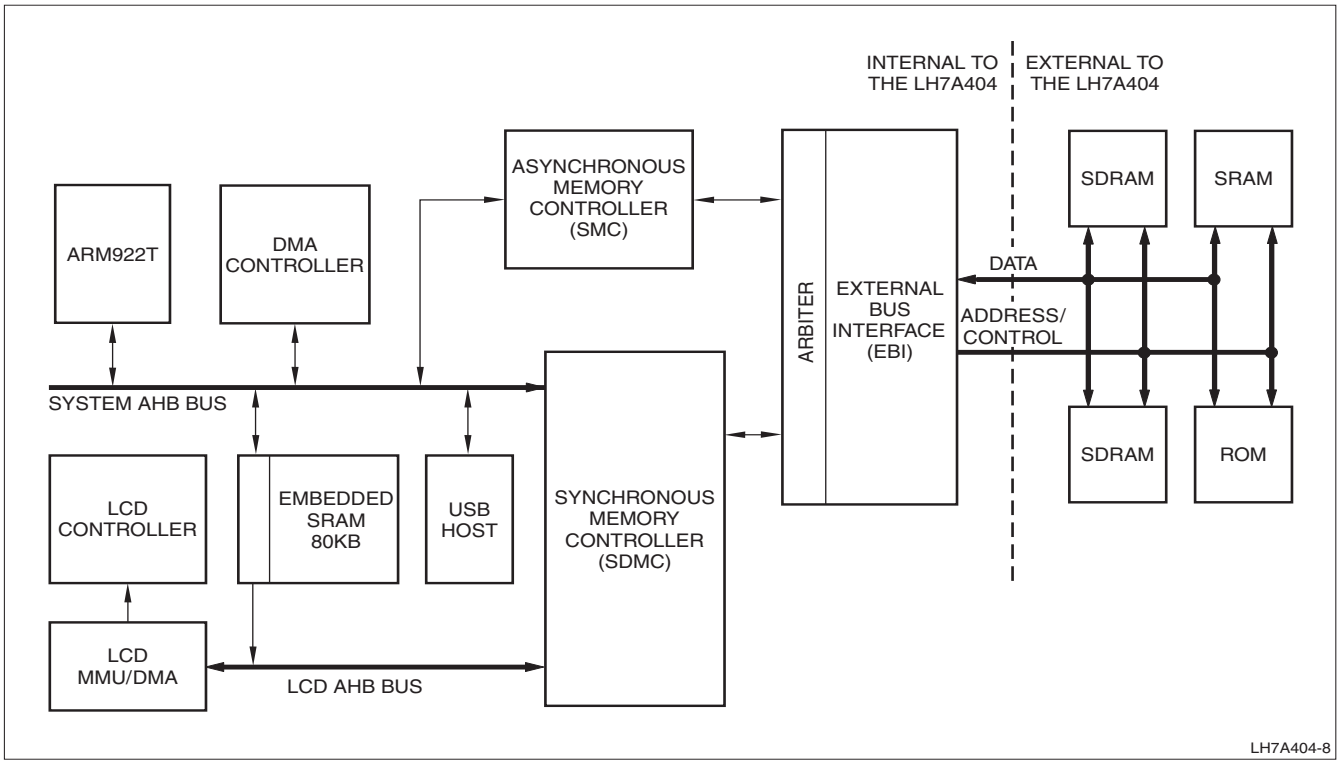


Figure 4. External Bus Interface Block Diagram

Embedded SRAM

The LH7A404 incorporates 80 kB of embedded SRAM. This embedded memory is used for storing code, data, or LCD frame data and is contiguous with external SDRAM. The 80 kB is large enough to store a QVGA frame (320 × 240) at 8 bits per pixel, equivalent to 70 kB of information.

Locating the frame buffer on chip reduces the overall power consumed by LH7A404 applications. Normally, the system performs external accesses to acquire this data. The LCD controller automatically uses an overflow frame buffer in SDRAM if a larger screen size is required. This overflow buffer can be located on any 4 kB page boundary in SDRAM, allowing software to set the MMU (in the LCD controller) page tables so the two memory areas appear contiguous, allowing byte, half-word, and word accesses.

Static Memory Controller (SMC)

The asynchronous Static Memory Controller (SMC) provides an interface between the AMBA AHB system bus and external (off-chip) memory devices.

The SMC simultaneously supports up to eight independently configurable memory banks. Each memory bank can support:

- SRAM
- ROM
- Flash EPROM
- Burst ROM memory.

Each memory bank may use devices with either 8-, 16-, or 32-bit external memory data paths. The memory controller is configured to support little-endian operation only.

The memory banks can be configured to support:

- Non-burst read and write accesses only to high-speed CMOS static RAM
- Non-burst write accesses, nonburst read accesses and asynchronous page mode read accesses to fast-boot block flash memory.

The SMC has six main functions:

- Memory bank select
- Access sequencing
- Wait state generation
- Byte lane write control
- External bus interface
- CompactFlash or PCMCIA interfacing.

SDRAM (Synchronous) Memory Controller

The SDRAM (Synchronous) Memory Controller provides a high speed memory interface to a wide variety of synchronous memory devices, including Synchronous DRAM, Synchronous Flash and Synchronous ROMs.

The key features of the controller are:

- LCD DMA port for high bandwidth
- Up to four Synchronous Memory banks can be independently set up
- Includes special configuration bits for Synchronous ROM operation
- Includes ability to program Synchronous Flash devices using write and erase commands
- On booting from Synchronous ROM, (and optionally with Synchronous Flash), a configuration sequence is performed before releasing the processor from reset
- Data is transferred between the controller and the Synchronous DRAM in four-word bursts. Longer transfers within the same page are concatenated, forming a seamless burst
- Programmable for 16- or 32-bit data bus size
- Two reset domains enable Synchronous DRAM contents to be preserved over a ‘soft’ reset
- Power saving Synchronous Memory SCKE and external clock modes provided.

Secure Digital/MultiMediaCard (MMC)

The SD Memory Card is a flash-based memory card that meets the security, capacity, performance, and environment requirements inherent in electronic devices. The SD Memory Card host supports MultiMediaCard (MMC) operation as well, and is compatible with MMC Cards.

The SD/MMC controller can be used as an MMC card controller or as an SD Card controller, and supports the full SD/MMC bus protocol as defined in the MMC system specification 2.11 provided by the MMC Association and the ‘SD Memory Card Spec v1.0’ from the SD Association.

SD/MMC INTERFACE DESCRIPTION

The SD/MMC controller uses the three-wire signal bus (clock, command, and data) to input and output data to and from the MMC, and to configure and acquire status information from the card. The SD controller differs in that it has four data lines instead of one.

The SD/MMC bus lines can be divided into three groups:

- Power supply: VSS1, VSS2, and VDD
- Data transfer group: MMCCMD, MMCDATA0, MMCDATA1, MMCDATA2, MMCDATA3 (for MMC, do not use MMCDATA1, MMCDATA2, MMCDATA3)
- Clock: MMCCLK

MMC CONTROLLER

The MMC controller implements MMC-specific functions, serves as the bus master for the MMC Bus and implements the standard interface to the MMC (card initialization, CRC generation and validation, command/response transactions, etc.).

Smart Card Interface (SCI)

The SCI (ISO7816) connects to an external Smart Card reader. The SCI can autonomously control data transfer to and from the Smart Card. Transmit and receive data FIFOs are provided to reduce the required interaction between the CPU core and the peripheral.

SCI FEATURES

- Supports asynchronous T0 and T1 transmission protocols
- Supports clock rate conversion factor F = 372, with bit rate adjustment factors of D = 1, 2, or 4
- Eight-character-deep buffered Tx and Rx paths
- Direct interrupts for Tx and Rx FIFO level monitoring
- Interrupt status register
- Hardware-initiated card deactivation sequence on detection of card removal
- Software-initiated card deactivation sequence on transaction complete
- Limited support for synchronous smart cards via registered input/output.

PROGRAMMABLE PARAMETERS

- Smart Card clock frequency
- Communication baud rate
- Protocol convention
- Card activation/deactivation time
- Maximum time for first character of Answer to Reset (ATR) reception checking
- Maximum ATR character stream duration checking
- Maximum time of receipt of first character of data stream checking
- Maximum time allowed between characters checking
- Character guard time
- Block guard time
-
- Transmit/receive character retry.

Direct Memory Access Controller (DMA)

The DMA Controller can be used to interface streams from 20 internal peripherals to the system memory using 10 fully-independent programmable channels which consist of five M2P (transmit) channels and five P2M (receive) channels.

The following peripherals may be allocated to the 10 channels:

- USB Device
- USB Host
- SD/MMC
- AC97
- UART1
- UART2
- UART3

Each of the above peripherals contain one Tx and one Rx channel, except the AC97, which contains three Tx and Rx channels. These peripherals also have their own bi-directional DMA bus, capable of simultaneously transferring data in both directions. All memory transfers take place via the main system AHB bus.

The DMA Controller can also be used to interface streams from memory-to-memory (M2M) or memory-to-external peripheral (M2P) using two dedicated M2M channels. External handshake signals are available to support memory-to-/from-external peripheral (M2P/P2M) transfers. A software trigger is available for M2M transfers only.

The DMA Controller features:

- Two dedicated channels for M2M and external M2P/P2M
- Ten fully independent, programmable DMA controller internal M2P/P2M channels (5 Tx and 5 Rx)
- Channels assignable to one of a number of different peripherals
- Independent source and destination address registers. Source and destination can be programmed to auto-increment or not auto-increment for M2M channels
- Two buffer descriptors per M2P and M2M channel to avoid potential data under/over-flow due to software introduced latency. A buffer refers to the area in system memory that is characterized by a buffer descriptor, i.e., a start address and the length of the buffer in bytes
- No AMBA wrapping bursts for DMA channels; only incrementing bursts are supported
- Buffer size independent of the peripheral's packet size for the internal M2P channels. Transfers can automatically switch between buffers
- Maskable interrupt generation
- Internal arbitration between DMA channels, plus support for an AHB bus arbiter
- DMA data transfer sizes, byte, word and quad-word data transfers are supported using a 16-byte data. Maximum data transfer size per M2M channel is programmable
- Per-channel clock gating reducing power in channels that have not been enabled by software. See the 'Clock and State Controller' section.

A set of control and status registers are available to the system processor for setting up DMA operations and monitoring their status. System interrupts are generated when any/all of the DMA channels wish to inform the processor to update the buffer descriptor. The DMA controller can service 10 out of 20 possible peripherals using the ten DMA channels, each with its own peripheral DMA bus capable of simultaneously transferring data in both directions.

The SD/MMC, UART[3:1], USB Device, and USB Host peripherals can each use two DMA channels, one for transmit and one for receive. The AC97 peripheral can use six DMA channels (three transmit and three receive) to allow different sample frequency data queues to be handled with low software overhead.

The DMA controller includes an M2M transfer feature allowing block moves of data from one memory address space to another with minimum of program effort and time. An M2M software trigger capability is provided. The DMA controller can also fill a block of memory with data from a single location.

The DMA controller's M2M channels can also be used in M2P/P2M mode. A set of external handshake signals, DREQ, DACK and TC/DEOT are provided for each of two M2M channels.

DREQ (input) can be programmed edge or level active, and active HIGH or LOW. The peripheral may hold DREQ active for the duration of the block transfers or may assert/deassert on each transfer.

DACK (output) can be programmed active HIGH or LOW. DACK will assert and return to de-asserted with each Read or Write, the timing coinciding with nOE or nWE from the EBI.

TC/DEOT is a bidirectional signal with programmable direction and active polarity. When configured as an Output, the DMA will assert Terminal Count (TC) on the final transfer to coincide with the DACK, typically when the byte count has expired. When configured as an Input, the peripheral must assert DEOT concurrent with DREQ for the final transfer in the block.

Transfer is terminated when DEOT is asserted by the external peripheral or when the byte count expires, whichever occurs first. Status bits indicate if the actual byte count is equal to the programmed limit, and if the count was terminated by peripheral asserting DEOT. Terminating the transfer causes a DMA interrupt on that channel and rollover to the 'other' buffer if so configured.

USB Device

The features of the USB are:

- Compliant with USB 2.0 Full Speed specification
- Provides a high-level interface that removes the USB protocol details from firmware
- Compatible with both OpenHCI and Intel UHCI standards
- Supports full-speed (12 Mbit/s) functions
- Supports Suspend and Resume signalling.

USB Host Controller

The features of the USB Host Controller are:

- Open Host Controller Interface Specification (OpenHCI) Rev. 1.0 Compliant
- Universal Serial Bus Specification 2.0 Full Speed compatible
- Supports Low Speed and High Speed USB devices
- Root Hub has two Downstream Ports
- DMA functionality.

Color LCD Controller

The LH7A404's LCD Controller is programmable to support up to 1,024 × 768, 16-bit color LCD panels. It interfaces directly to STN, color STN, TFT, AD-TFT, and HR-TFT panels. Unlike other LCD controllers, the LH7A404's LCD Controller saves an external timing ASIC by incorporating the timing conversion logic for thin LCD modules such as AD-TFT and HR-TFT.

The Color LCD Controller features support for:

- Up to 1,024 × 768 Resolution
- 16-bit Video Bus
- 16 bits-per-pixel (bpp) 5:5:5:1 or 5:6:5 direct color or on-chip color palette for 1, 2, 4, and 8 bpp resolution
- STN, Color STN, AD-TFT, HR-TFT, TFT panels
  - Single and Dual Scan STN panels
  - Up to 15 Gray Shades (mono STN)
  - Up to 3375 colors (color STN)
  - Up to 64 k-Colors
  - An on-chip SRAM frame buffer conserves bus bandwidth and saves active power.

AC97 Codec Controller

The AC97 Codec controller includes a 5-pin serial interface to an external audio codec. The AC97 link is a bi-directional, fixed rate, serial Pulse Code Modulated (PCM) digital stream, dividing each audio frame into 12 outgoing and 12 incoming data streams (slots), each with 20-bit resolution per sample.

The AC97 controller contains logic that controls the AC97 link to the audio codec and an interface to the AMBA APB.

Its main features include:

- Serial-to-parallel conversion for data received from the external codec
- Parallel-to-serial conversion for data transmitted to the external codec
- Reception/transmission of control and status information via the AMBA APB interface
- Support for up to 4 simultaneous codec sampling rates with its 4 transmit and 4 receive channels. The transmit and receive paths are buffered with internal FIFO memories, allowing data to be stored independently in both transmit and receive modes. Three of the outgoing FIFOs can be written via either the APB interface or with DMA channels 1-3.

Audio Codec Interface (ACI)

The ACI provides:

- A digital serial interface to an off-chip 8-bit codec
- All the necessary clocks and timing pulses to perform serialization or de-serialization of the data stream to, or from the codec device.

The interface supports full duplex operation and the transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes.

The ACI includes a programmable frequency divider that generates a common transmit and receive bit clock output from the on-chip ACI clock input (ACBITCLK). Transmit data values are output synchronous with the rising edge of the bit clock output. Receive data values are sampled on the falling edge of the bit clock output. The start of a data frame is indicated by a synchronization output signal that is coincident with the bit clock.

Pulse Width Modulator (PWM)

The Pulse Width Modulator features:

- Configurable dual output
- Separate input clocks for each PWM output
- 16-bit resolution
- Programmable synchronous mode support allows external input to start PWM
- Programmable pulse width (duty cycle), interval (frequency), and polarity
  - Static programming: when the PWM is stopped
  - Dynamic programming: when the PWM is running
  - Updates duty cycle, frequency, and polarity at end of a PWM cycle

The PWM is a configurable dual-output, dual-clock-input AMBA slave module, and connects to the APB.

Synchronous Serial Port (SSP)

The SSP is a master-only interface for synchronous serial communication with peripheral devices that have either Motorola SPI, National Semiconductor MICROWIRE, or Texas Instruments Synchronous Serial Interfaces.

The SSP performs serial-to-parallel conversion on data received from a peripheral. The transmit and receive paths are buffered with internal FIFO memories allowing up to eight 16-bit values to be stored independently in both transmit and receive modes. Serial data is transmitted on SSPTXD and received on SSPRXD.

The LH7A404 SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SCLK from the input clock SSPCLK. Bit rates are supported to 2 MHz and beyond, subject to choice of frequency for SSPCLK; the maximum bit rate will usually be determined by peripheral device's capability.

UART/IrDA

The LH7A404 contains three UARTs; UART1, UART2, and UART3.

The UART performs:

- Serial-to-Parallel conversion on data received from the peripheral device
- Parallel-to-Serial conversion on data transmitted to the peripheral device.

The transmit and receive paths can both be routed through the DMA separately or simultaneously, and are buffered with internal FIFO memories. This allows up to 16 bytes to be stored independently in both transmit and receive modes. The UART can generate:

- Four individually maskable interrupts from the receive, transmit, and modem status logic blocks
- A single combined interrupt so that the output is asserted if any of the individual interrupts are asserted and unmasked.

If a framing, parity or break error occurs during reception, the appropriate error bit is set and stored in the FIFO. If an overrun condition occurs, the overrun register bit is set immediately and the FIFO data is prevented from being overwritten. UART1 also supports IrDA 1.0 (15.2 kbit/s).

The modem status input signals Clear to Send (CTS), Data Carrier Detect (DCD) and Data Set Ready (DSR) are supported on UART2 and UART3.

Timers

The LH7A404 includes three programmable timers. Each of the timers can operate in two modes: free running and pre-scale. The timers are programmed using four registers; Load, Value, Control, and Clear.

Two identical timers, Timer 1 (TC1) and Timer 2 (TC2), use clock sources of either 508 kHz or 2 kHz. The clock source and mode are selectable by writing to the appropriate bits in the system control register. Each timer has a 16-bit read/write data register and a control register. The timer is immediately loaded with the value written to the data register. This value is then decremented on the next active clock edge to arrive after the write. When the timer underflows, it immediately asserts its appropriate interrupt.

Timer 3 (TC3) has the same basic operation, but is clocked from a single 7.3728 MHz source. Once the timer has been enabled and written to, it decrements on the next rising edge of the 7.3728 MHz clock after the data register has been updated.

FREE-RUNNING MODE

In free-running mode, the timer wraps around to 0xFFFF when it underflows and continues counting down.

PRE-SCALE MODE

In pre-scale (periodic) mode, the value written to each timer is automatically re-loaded when the timer underflows. This mode can be used to produce a programmable frequency to drive the buzzer or generate a periodic interrupt.

Real Time Clock (RTC)

The RTC provides a basic alarm function or long time-base counter. This is achieved by generating an interrupt signal after counting for a programmed number of cycles of a real-time clock input. Counting in one-second intervals is achieved by use of a 1 Hz clock input to the RTC.

Keyboard and Mouse Interface (KMI)

The Keyboard and Mouse Interface has the following features:

- IBM PS/2 or AT-compatible keyboard or mouse interface
- Half-duplex, bidirectional synchronous serial interface using open-drain outputs for clock and data.
- Programmable 4-bit reference clock divider
- Polled or interrupt-driven mode
- Separately maskable transmit and receive interrupts
- Single combined interrupt output
- Odd parity generation and checking
- Register bits for override of keyboard clock and data lines.

Additional test registers and modes are implemented for functional verification and manufacturing test.

A/D Converter with Brownout Detector and Touch Screen Controller

The LH7A404 includes an A/D Converter (ADC) with integrated Touch Screen Controller (TSC) and brownout detector. The TSC is a complete interface to a Touch Screen for portable personal devices. It combines the front-end biasing and control circuitry with A/D conversion, reference generation, and digital interface functions to completely replace external ICs used to implement this interface. The ADC features:

- A 10-bit A/D converter with integrated sample-and-hold, fully differential, high impedance signal and reference inputs
- Active matrix for bias and control circuits necessary for connection to external 4-, 5-, 7-, and 8-wire touch panels, including pen pressure implementation

- Battery voltage sense in addition to normal direct voltage inputs
- A 9-channel multiplexer for routing user-selected inputs to A/D
- A 16 × 16 FIFO for 10-bit digital output of A/D
- A pen-down sensor to generate interrupts to the host
- Low-power circuitry and power control modes to minimize on-chip power dissipation
- Conversion automation for flexibility while minimizing CPU management and interrupt overhead
- A brownout detector with separate interrupt

Battery Monitor Interface (BMI)

The BMI is a serial communication interface specified for two types of battery monitors/gas gauges. The first type employs a single wire interface. The second interface employs a two-wire multi-master bus, implementing the Smart Battery System Specification. If both interfaces are enabled at the same time, the Single Wire Interface has priority.

SINGLE WIRE INTERFACE

The Single Wire Interface performs:

- Serial-to-parallel conversion on data received from the peripheral device
- Parallel-to-serial conversion on data transmitted to the peripheral device
- Data packet coding/decoding on data transfers (incorporating Start/Data/Stop data packets)

The Single Wire interface uses a command-based protocol in which the host initiates a data transfer by sending a WriteData/Command word to the battery monitor.

SMART BATTERY INTERFACE

The Smart Battery Interface performs:

- Serial-to-parallel conversion on data received from the peripheral device
- Parallel-to-serial conversion of data transmitted to the peripheral device.

The Smart Battery Interface uses a two-wire multi-master bus (the SMBus), allowing multiple bus masters to be connected to it. A master device initiates a bus transfer and provides the clock signals. A slave device can receive data provided by the master or it can provide data to the master. Since more than one device may attempt to take control of the bus as a master, SMBus provides an arbitration mechanism by relying on the wired-AND connection of all SMBus interfaces to the SMBus.

DC-to-DC Converter

The features of the DC-DC Converter interface are:

- Dual-drive PWM outputs with independent closed loop feedback
- Software programmable configuration of one of 8 output frequencies (each being a fixed division of the input clock).
- Software programmable configuration of duty cycle from 0 to 15/16, in intervals of 1/16.
- Hardware-configured output polarity (for positive or negative voltage generation) during power-on reset via the polarity select inputs
- Dynamically switched PWM outputs to one of a pair of preprogrammed frequency/duty cycle combinations via external pins.

Watchdog Timer (WDT)

The Watchdog Timer provides hardware protection against malfunctions. It is a programmable timer that is reset by software at regular intervals. Failure to reset the timer will cause an FIQ interrupt. Failure to service the FIQ interrupt generates a system reset.

Features of the WDT:

- Timing derived from the system clock
- 16 programmable time-out periods: 2^{16} through 2^{31} clock cycles
- Generates a system reset (resets LH7A404) or a FIQ interrupt whenever a time-out period is reached
- Software enable, lockout, and counter-reset mechanisms add security against inadvertent writes
- Protection mechanism guards against interrupt-service-failure:
  - The first WDT time-out triggers FIQ and asserts nWDFIQ status flag
  - If FIQ service routine fails to clear nWDFIQ, then the next WDT time-out triggers a system reset.

General Purpose I/O (GPIO)

The GPIO has eight ports, each with a data register and a data direction register. It also has added registers including Keyboard Scan, PINMUX, GPIO Interrupt Enable, INTYPE1/2, GPIOFEOI and PGHCON.

The data direction register determines whether a port is configured as an input or an output while the data register is used to read the value of the GPIO pins.

The GPIO Interrupt Enable, INTYPE[2:1], and the GPIOFEOI registers control edge-triggered Interrupts on Port F. The PINMUX register controls which signals are from Port D and Port E when they are set as outputs, while the PGHCON controls the operations of Port G and Port H.

ELECTRICAL SPECIFICATIONS

IMPORTANT: The LH7A404 is an electrostatic discharge (ESD) sensitive device. ESD protection circuitry internal to the LH7A404 has been added to reduce ESD susceptibility. Appropriate ESD precautions are still required during handling to prevent degradation or failure due to high electrostatic discharges. System design practices should be evaluated to prevent LH7A404 ESD voltages from exceeding the maximum rated voltage as specified in this data sheet.

Absolute maximum ratings

PARAMETER	MINIMUM	MAXIMUM
DC Core Supply Voltage (VDDC)	–0.3 V	2.4 V
DC I/O Supply Voltage (VDD)	–0.3 V	4.6 V
DC Analog Supply Voltage (VDDA)	–0.3 V	2.4 V
DC Analog Supply Voltage (VDDAD)	–0.3 V	4.6 V
5 V Tolerant Digital Input Pin Voltage	–0.5 V	5.5 V
ESD, Human Body Model (Analog pins AN0 - AN9 rated at 500 V)		2 kV
ESD, Charged Device Model		1 kV
Storage Temperature	–55°C	125°C

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the device.

Recommended operating conditions for LH7A404-N0E-000-xx/LH7A404-N0F-000-xx

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	NOTES
DC Core Supply Voltage (VDDC)	1.71 V	1.8 V	1.89 V	1
DC I/O Supply Voltage (VDD)	3.0 V	3.3 V	3.6 V	
DC Analog Supply Voltage (VDDA)	1.71 V	1.8 V	1.89 V	
DC A/D and TSC Supply Voltage (VDDAD)	3.0 V	3.3 V	3.6 V	
Clock Frequency	10 MHz		200 MHz	
Bus Clock Frequency			100 MHz	
External Clock Input (XTALIN)	14 MHz	14.7456 MHz	20 MHz	2
External Clock Input (XTALIN) Voltage	1.71 V	1.8 V	1.89 V	
Operating Temperature	–40°C	25°C	+85°C	

NOTES:
1. Core Voltage should never exceed I/O Voltage after initial power up. See “Power Supply Sequencing” on page 31.
2. Many of the peripherals do not operate properly at clock speeds other than 14.7456 MHz. Some (such as USB) function only at 14.7456 MHz.

Recommended Operating Conditions for LH7A404-N0E-092-xx/LH7A404-N0F-092-xx

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	NOTES
DC Core Supply Voltage (VDDC)	2.0 V	2.1 V	2.2 V	1
DC I/O Supply Voltage (VDD)	3.14 V	3.3 V	3.6 V	
DC Analog Supply Voltage (VDDA)	2.0 V	2.1 V	2.2 V	
DC A/D and TSC Supply Voltage (VDDAD)	3.0 V	3.3 V	3.6 V	
Clock Frequency	10 MHz		266 MHz	
Bus Clock Frequency			133 MHz	
External Clock Input (XTALIN)	14 MHz	14.7456 MHz	20 MHz	2
External Clock Input (XTALIN) Voltage	1.71 V	1.8 V	1.89 V	
Operating Temperature	−40°C	25°C	+85°C	

NOTES:
1. Core Voltage should never exceed I/O Voltage after initial power up. See “Power Supply Sequencing” on page 31.
2. Many blocks do not operate properly at speeds other than 14.7456 MHz. Some (such as USB) function only at 14.7456 MHz.

Table 8. Clock Frequency vs. Voltages (VDD) vs. Temperature*

PARAMETER		1.71 V	1.80 V	1.89 V
25°C	Clock Frequency (FCLK)	213 MHz	227 MHz	253 MHz
	Clock Period (1/FCLK)	4.69 ns	4.41 ns	3.95 ns
70°C	Clock Frequency (FCLK)	205 MHz	220 MHz	236 MHz
	Clock Period (1/FCLK)	4.88 ns	4.46 ns	2.36 ns
85°C	Clock Frequency (FCLK)	200 MHz	212 MHz	232 MHz
	Clock Period (1/FCLK)	5.00 ns	4.72 ns	4.24 ns

NOTE: *LH7A404-N0E-000-xx and LH7A404-N0F-000-xx only. Table 8 is representative of a typical device. Guaranteed values are in the Recommended Operating Conditions table.

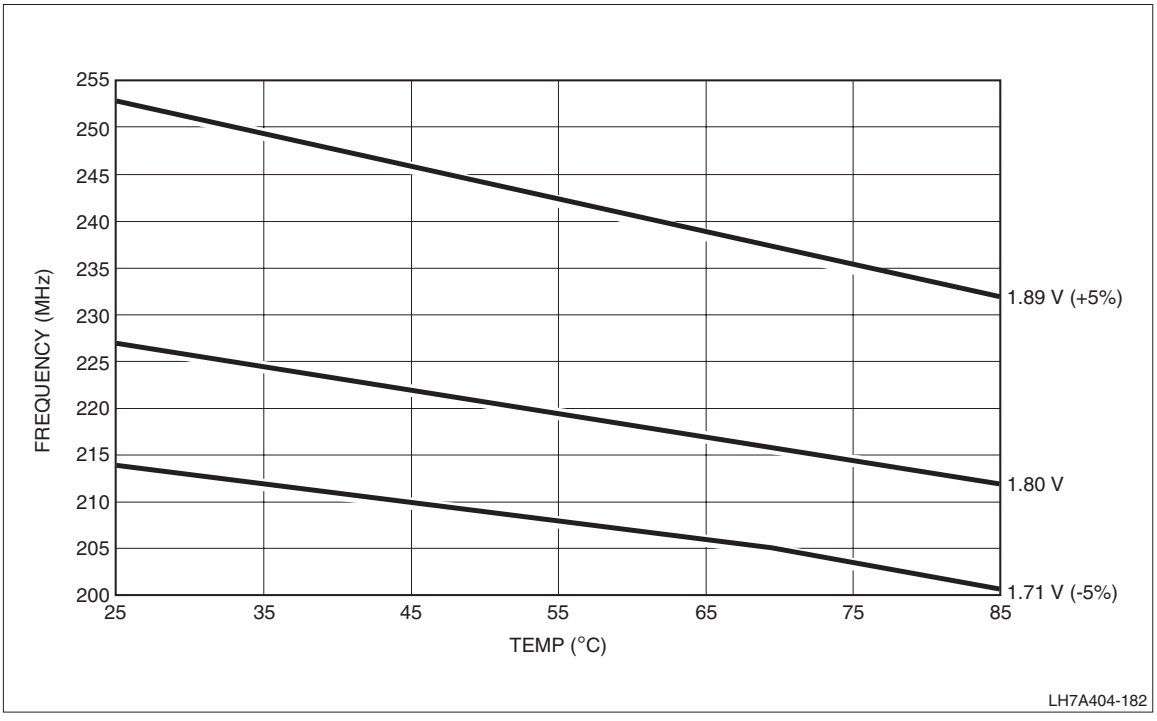


Figure 5. Temperature/Voltage/Speed Chart (LH7A404-N0E-000-xx and LH7A404-N0F-000-xx Only)

Power Supply Sequencing

NXP recommends that the 1.8 V power supply be energized before the 3.3 V supply. If this is not possible, the 1.8 V supply may not lag the 3.3 V supply by more than 100 μs. If longer delay time is needed, it is recommended that the voltage difference between the two power supplies be within 1.5 V during power supply ramp up.

To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

DC/AC SPECIFICATIONS

The DC and AC specifications appears in the table below. Parameters apply to all part numbers except where noted.

DC Specifications

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS	NOTE
VIH	CMOS/Schmitt Trigger Input HIGH Voltage	2.0			V		
VIL	CMOS/Schmitt Trigger Input LOW Voltage			0.8	V		
VHST	Schmitt Trigger Hysteresis	0.25			V	VIL to VIH	
VOH	CMOS Output HIGH Voltage, Output Drive 1	2.6			V	IOH = -2 mA	
	Output Drive 2	2.6			V	IOH = -4 mA	
	Output Drive 3	2.6			V	IOH = -8 mA	
	Output Drive 4 and 5	2.6			V	IOH = -12 mA	1
VOL	CMOS Output LOW Voltage, Output Drive 1			0.4	V	IOL = 2 mA	
	Output Drive 2			0.4	V	IOL = 4 mA	
	Output Drive 3			0.4	V	IOL = 8 mA	
	Output Drive 4			0.4	V	IOL = 12 mA	
	Output Drive 5			0.4	V	IOL = 20 mA	1
IIN	Input Leakage Current	-10		10	μA	VIN = VDD or GND	
	Input Leakage Current, with pullup resistors	-95		10	μA		
IOZ	Output Tri-state Leakage Current	-10		10	μA	VOUT = VDD or GND	
ISTARTUP	Startup Current			50	μA		2
CIN	Input Capacitance			4	pF		
COUT	Output Capacitance			4	pF		
LH7A404-N0E-000-XX AND LH7A404-N0F-000-XX ONLY							
IACTIVE	Active Current (Operating Current)		147	238	mA		3
IHALT	Halt Current		41	45	mA		4
ISTANDBY	Standby Current		70		μA		5
LH7A404-N0E-092-XX AND LH7A404-N0F-092-XX ONLY							
IACTIVE	Active Current (Operating Current)		228	370	mA		3
IHALT	Halt Current		60		mA		4
IHALT	Standby Current		200		μA		5

NOTES:

1. Output Drive 5 can sink 20 mA of current, but sources 12 mA of current.
2. Current consumption until oscillators are stabilized.
3. See 'Current Consumption by Operating Mode', page 34 for operating conditions.
4. Both oscillators running, LCD Active; all other peripherals stopped.
5. 32 kHz oscillator running; all other peripherals stopped.

Analog-To-Digital Converter Electrical Characteristics

Table 9 shows the derated specifications for extended temperature operation. See Figure 6 for the ADC transfer characteristics.

Table 9. ADC Electrical Characteristics

PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
A/D Resolution	10		10	Bits	
Throughput Conversion	17			CLK Cycles	1
Acquisition Time	3			CLK Cycles	
Data Format		binary			2
Clk Frequency	500		5,000	ns	
Differential Non-Linearity (DNL)	-0.99		+4.5	LSB	3
Integral Non-Linearity (INL)	-4.5		+4.5	LSB	4
Offset Error	+35		+50	mV	5
Gain Error	-4.0		4.0	LSB	
Reference Voltage Output	1.85	2.0	2.15	V	
VREF-	VSSA	VSSA	(VREF+) -1.0	V	6
VREF+	(VREF-) +1.0	VREF	VDDAD	V	6
Crosstalk between channels		-60		dB	
Analog Input Voltage Range	0		VDDAD	V	7
Analog Input Current			5	μA	
Reference Input Current			5	μA	
Analog Input capacitance			15	pF	
Operating Supply Voltage	3.0		3.6	V	
Operating Current, VDDAD		590	1000	μA	
Standby Current, VDDAD		180		μA	8
Stop Current, VDDAD		1		μA	
Brownout Trip Point (falling point)	2.36	2.63	2.9	V	
Brownout Hysteresis		120		mV	
Operating Temperature	–40		85	°C	

NOTES:

1. The analog section of the ADC takes 16 × A2DCLK cycles per conversion, plus 1 × A2DCLK cycles to be made available in the PCLK domain. An additional 3 × PCLK cycles are required before being available on the APB.
2. Data out = 0000000000 when the analog input equals the negative reference. Data out = 1111111111 when the analog input equals the positive reference.
3. Guaranteed monotonic.
4. INL calculated as deviation from 'best fit' line after subtracting offset/gain errors over the center 90 % of full scale output range.
5. DC voltage error for the transition voltage from code 511 (0x1FF) to 512 (0x200)
6. The internal voltage reference is driven to nominal value VREF = 2.0 V. Using the Reference Multiplexer, alternative low impedance (RS < 500) voltages can be selected as reference voltages. The range of voltages allowed are specified above.
7. The analog input pins can be driven anywhere between the power supply rails. If the voltage at the input to the ADC exceeds VREF+ or is below VREF-, the A/D result will saturate appropriately at positive or negative full scale. Trying to pull the analog input pins above or below the power supply rails will cause protection diodes to be forward-biased, resulting in large current source/sink and possible damage to the ADC.
8. Bandgap and other low-bandwidth circuitry operating. All other ADC blocks shut down.

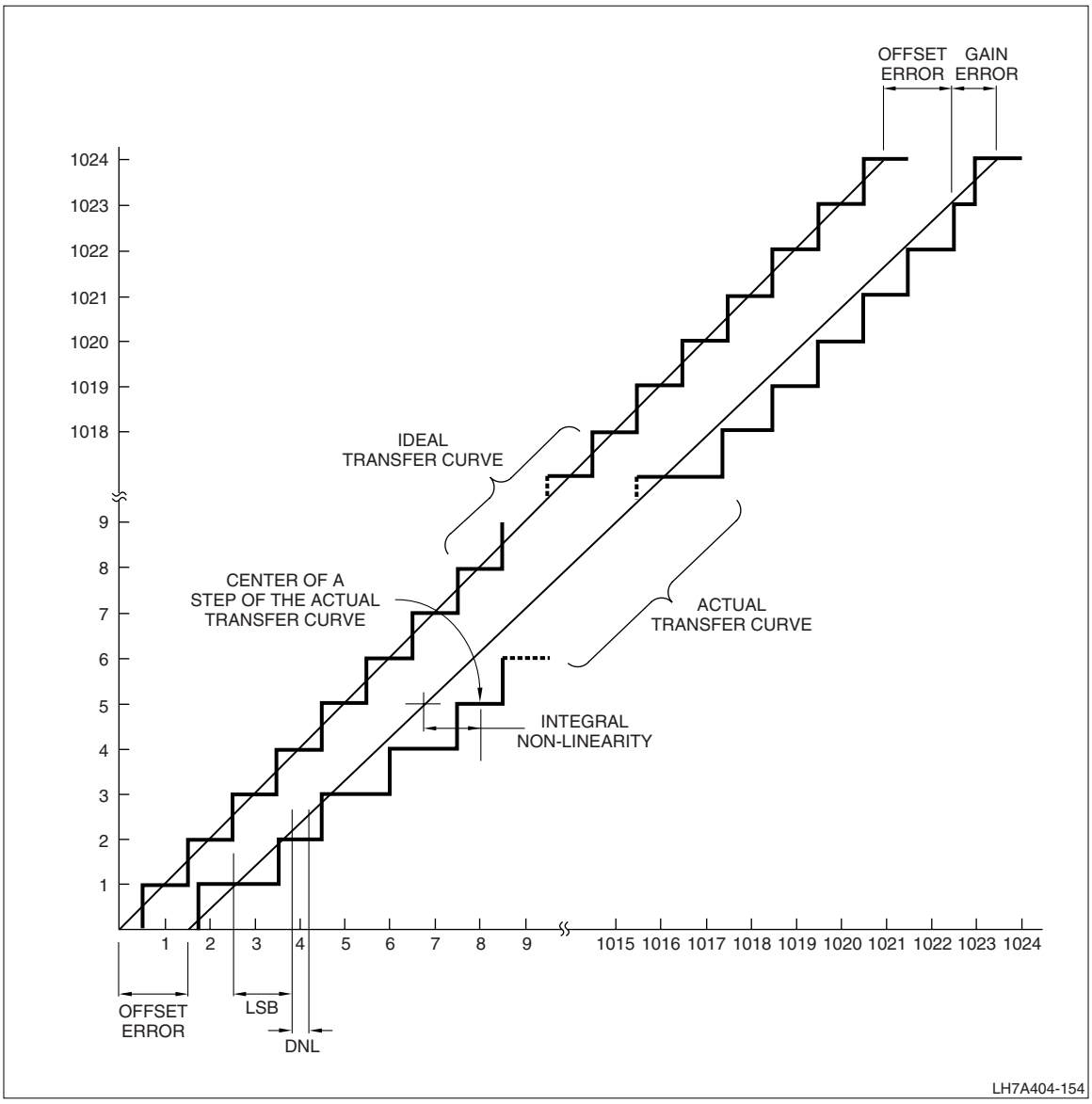


Figure 6. ADC Transfer Characteristics

AC Test Conditions

PARAMETER	RATING	UNIT
DC I/O Supply Voltage (VDD)	3.0 to 3.6	V
DC Core Supply Voltage (VDDC)	1.7 to 1.9	V
Input Pulse Levels	VSS to 3	V
Input Rise and Fall Times	2	ns
Input and Output Timing Reference Levels	VDD/2	V

CURRENT CONSUMPTION BY OPERATING MODE

Current consumption can depend on a number of parameters. To make these data more usable, the values presented in Table 11 were derived under the conditions described here.

Maximum Specified Value

The values specified in the MAXIMUM column were determined using these operating characteristics:

- All IP blocks either operating or enabled at maximum frequency and size configuration
- Core operating at maximum power configuration
- All voltages at maximum specified values
- Nominal specified ambient temperature.

Typical

The values in the TYPICAL column were determined using a 'typical' application under 'typical' environmental conditions and the following operating characteristics:

- LINUX operating system running from SDRAM
- UART and AC97 peripherals operating; all other peripherals as needed by the OS
- LCD enabled with 320 × 240 × 16-bit color, 60 Hz refresh rate, data in SDRAM
- I/O loads at nominal
- Cache enabled
- FCLK = 200; HCLK = 100; PCLK = 50 MHz
- All voltages at typical values
- Nominal case temperature.

PERIPHERAL CURRENT CONSUMPTION

In addition to the modal current consumption, Table 10 shows the typical current consumption for each of the on-board peripheral blocks. The values were determined with the peripheral clock running at 200 MHz, typical conditions, and no I/O loads. This current is supplied by the 1.8 V power supply.

Table 10. Peripheral Current Consumption

PERIPHERAL	TYPICAL	UNITS
AC97	1.3	mA
UART (each)	1.0	mA
RTC	0.005	mA
Timers (each)	0.1	mA
LCD (+I/O)	5.4 (+1.0)	mA
MMC	0.6	mA
SCI	23	mA
PWM (each)	45	µA
BMI-SWI	1.0	mA
BMI-SBus	1.0	mA
SDRAM (+I/O)	1.5 (+14.8)	mA
USB Device (+PLL)	5.6 (+3.3)	mA
ACI	0.8	mA
VIC	610	µA
KMI	38	µA
USB Host	715	µA
ADC/TSC	590	µA

Table 11. Current Consumption by Mode

SYMBOL	PARAMETER	FCLK = 200 MHz (TYP.)	FCLK = 266 MHz (TYP.)	UNITS
RUN MODE				
ICORE	Core Current	132	199	mA
IIO	I/O Current	15	29	mA
HALT MODE (All Peripherals Disabled)				
ICORE	Core Current	40	58	mA
IIO	I/O Current	1	2	mA
STANDBY MODE (Typical Conditions Only)				
ICORE	Core Current	66	200	µA
IIO	I/O Current	4	4	µA

NOTES:
1. FCLK = 200 MHZ pertains to LH7A404-N0E-000-xx and LH7A404-N0F-000-xx
2. FCLK = 266 MHz pertains to LH7A404-N0E-092-xx and LH7A404-N0F-092-xx.

AC Specifications

All signals described in Table 12 relate to transitions following an internal reference clock signal. The illustration in Figure 7 represents all cases of these sets of measurement parameters.

The reference clock signals in this design are:

- HCLK, internal System Bus clock ('C' in timing data)
- PCLK, the Peripheral Bus clock
- SSPCLK, the Synchronous Serial Port clock
- UARTCLK, the UART Interface clock
- LCDDCLK, the LCD Data clock from the LCD Controller
- ACBITCLK, the AC97 and ACI clock
- SCLK, the Synchronous Memory clock.

All signal transitions are measured from the 50 % point of the clock to the 50 % point of the signal.

For outputs from the LH7A404, tOVXXX (e.g. tOVA) represents the amount of time for the output to become valid from the rising edge of the reference clock signal. Maximum requirements for tOVXXX are shown in Table 12.

The signal tOHXXX (e.g. tOHA) represents the amount of time the output must be held valid after the rising edge of the reference clock signal. Minimum requirements for tOHXXX are listed in Table 12.

For inputs, tISXXX (e.g. tISD) represents the amount of setup time the input signal must be valid after a valid address bus, or rising edge of the peripheral clock. Maximum requirements for tISXXX are shown in Table 12.

The signal tIHXXX (e.g. tIHD) represents the amount of time the output must be held valid following the rising edge of the reference clock signal. Minimum requirements are shown in Table 12.

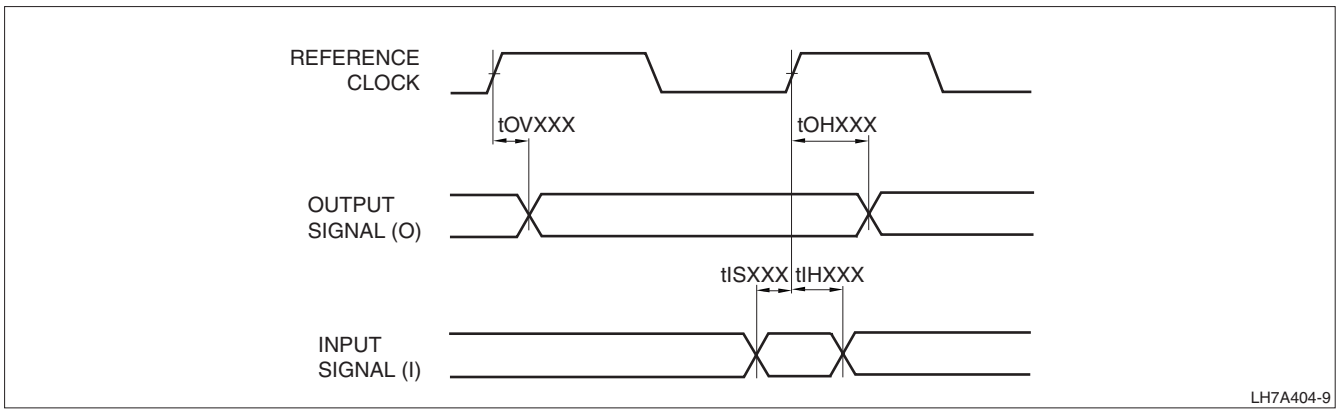


Figure 7. LH7A404 Signal Timing

Table 12. AC Signal Characteristics

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION	NOTES
ASYNCHRONOUS MEMORY INTERFACE SIGNALS (+ [wait states × HCLK period])							
A[27:0]	Output	50 pF	tRC	4 × tHCLK – 7.0 ns	4 × tHCLK + 7.5 ns	Read Cycle Time	1
	Output	50 pF	tWC	4 × tHCLK – 7.0 ns	4 × tHCLK + 7.5 ns	Write Cycle Time	1
	—	—	tWS	tHCLK ns	tHCLK ns	Wait State Width	1
D[31:0]	Output	50 pF	tDVWE	tHCLK – 6.0 ns	tHCLK – 2.0 ns	Data Valid to Write Edge (nWE invalid)	1
			tDHWE	tHCLK – 7.0 ns	tHCLK + 2.0 ns	Data Hold after Write Edge (nWE invalid)	1
			tDVBE	tHCLK – 5.0 ns	tHCLK – 1.0 ns	Data Valid to nBLE Invalid	1
			tDHBE	tHCLK – 7.0 ns	tHCLK + 3.0 ns	Data Hold after nBLE Invalid	1
	Input	—	tDSCS	15 ns	—	Data Setup to nCSx Invalid	1
			tDHCS	0 ns	—	Data Hold to nCSx Invalid	1
			tDSOE	15 ns	—	Data Setup to nOE Invalid	1
			tDHOE	0 ns	—	Data Hold to nOE Invalid	1
			tDSBE	15 ns	—	Data Setup to nBLE Invalid	1
			tDHBE	0 ns	—	Data Hold to nBLE Invalid	1
nCS[7:0]	Output	50 pF	tCS	2 × tHCLK – 3.0 ns	2 × tHCLK + 3.0 ns	nCSx Width	1
			tAVCS	tHCLK – 4.0 ns	tHCLK	Address Valid to nCSx Valid	1
			tAHCS	tHCLK	tHCLK + 4.5 ns	Address Hold after nCSx Invalid	1
nWE	Output	50 pF	tWE	tHCLK – 2.0 ns	tHCLK + 1.0 ns	nWE Width	1
			tAVWE	tHCLK – 4.0 ns	tHCLK ns	Address Valid to nWE Valid	1
			tCSHWE	tHCLK – 1.0 ns	tHCLK + 2.0 ns	nCSx Hold after nWE Invalid	1
nOE	Output	50 pF	tOE	2 × tHCLK – 3.0 ns	2 × tHCLK + 3.0 ns	nOE Width	1
			tAVOE	tHCLK – 4.0 ns	tHCLK	Address Valid to nOE Valid	1
			tAHOE	tHCLK	tHCLK + 4.5 ns	Address Hold after nOE Invalid	1
nBLE (Write)	Output	50 pF	tBEW	tHCLK – 5.0 ns	tHCLK	nBLE Width	1
			tAVBE	tHCLK – 2.0 ns	tHCLK	Address Valid to nBLE Valid	1
			tCSHBE	tHCLK	tHCLK + 3.0 ns	nCSx Hold after nBLE Invalid	1
nBLE (Read)	Output	50 pF	tBER	2 × tHCLK – 5.0 ns	2 × tHCLK + 3.0 ns	nBLE Width	1
			tAVBE	tHCLK – 2.0 ns	tHCLK	Address Valid to nBLE Valid	1
			tAHBE	tHCLK	tHCLK + 4.5 ns	Address Hold after nBLE Invalid	1
SYNCHRONOUS MEMORY INTERFACE SIGNALS (‘-092’ parts/’-000’ parts)							
SA[13:0]	Output	50 pF	tOVA	—	5.5/7.5 ns	Address Valid	2
			tOHA	1.5/1.5 ns	—	Address Hold	2
A[17:16]/ SB[1:0]	Output	50 pF	tOVB	—	5.5/7.5 ns	Bank Select Valid	2
D[31:0]	Output	50 pF	tOHD	1.5ns	—	Data Hold	2
			tOVD	2 ns	5.5/7.5 ns	Data Valid	2
	Input	—	tISD	1.5/2.5 ns	—	Data Setup	2
			tIHD	1.0/1.5 ns	—	Data Hold	2
nCAS	Output	50 pF	tOVCA	2 ns	5.5/7.5 ns	CAS Valid	2
			tOHCA	1.5/2 ns	—	CAS Hold	2
nRAS	Output	50 pF	tOVRA	2 ns	5.5/7.5 ns	RAS Valid	2
			tOHRA	1.5/2 ns	—	RAS Hold	2
nSWE	Output	50 pF	tOVSDW	2 ns	5.5/7.5 ns	Write Enable Valid	2
			tOHSDW	1.5/2 ns	—	Write Enable Hold	2
SCKE[1:0]	Output	50 pF	tOVC0	2 ns	5.5/7.5 ns	Clock Enable Valid	2
DQM[3:0]	Output	50 pF	tOVDQ	2 ns	5.5/7.5 ns	Data Mask Valid	2
nSCS[3:0]	Output	50 pF	tOVSC	2 ns	5.5/7.5 ns	Synchronous Chip Select Valid	2
			tOHSC	1.5/2 ns	—	Synchronous Chip Select Hold	2
PCMCIA INTERFACE SIGNALS (+ [wait states × HCLK period])							
nPCREG	Output	50 pF	tOVDREG	—	tHCLK + 5 ns	nREG Valid	
			tOHDREG	4 × tHCLK – 5 ns	—	nREG Hold	

Table 12. AC Signal Characteristics (Cont'd)

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION	NOTES
D[31:0]	Output	50 pF	tOVD	—	tHCLK + 5 ns	Data Valid	
			tOHD	4 × tHCLK – 6 ns	—	Data Hold	
	Input	—	tISD	—	tHCLK - 10 ns	Data Setup Time	
			tIHD	4 × tHCLK – 5 ns	—	Data Hold Time	
nPCCE1	Output	50 pF	tOVCE1	—	tHCLK + 5 ns	Chip Enable 1 Valid	
			tOHCE1	4 × tHCLK – 5 ns	—	Chip Enable 1 Hold	
nPCCE2	Output	50 pF	tOVCE2	—	tHCLK + 5 ns	Chip Enable 2 Valid	
			tOHCE2	4 × tHCLK – 5 ns	—	Chip Enable 2 Hold	
nPCOE	Output	50 pF	tOVOE	—	tHCLK + 5 ns	Output Enable Valid	
			tOHOE	3 × tHCLK – 5 ns	—	Output Enable Hold	
nPCWE	Output	50 pF	tOVWE	—	n × tHCLK + 5 ns	Write Enable Valid	
			tOHWE	3 × tHCLK – 5 ns	—	Write Enable Hold	
PCDIR	Output	50 pF	tOVPCD	—	tHCLK + 5 ns	Card Direction Valid	
			tOHPCD	4 × tHCLK – 5 ns	—	Card Direction Hold	
MMC INTERFACE SIGNALS							
MMCCMD	Output	50 pF	tOVCMD	—	½tcyc – 3 ns	MMC Command Valid	3
			tOHCMD	½tcyc + 3 ns	—	MMC Command Hold	3
MMCDATA	Output	50 pF	tOVDAT	—	½tcyc – 3 ns	MMC Data Valid	3
			tOHDAT	½tcyc + 3 ns	—	MMC Data Hold	3
MMCDATA	Input	—	tISDAT	5 ns	—	MMC Data Setup	
			tIHDAT	5 ns	—	MMC Data Hold	
MMCCMD	Input	—	tISCMD	5 ns	—	MMC Command Setup	
			tIHCMD	5 ns	—	MMC Command Hold	
AC97 INTERFACE SIGNALS							
ACOUT	Output	50 pF	tOVAC97	—	½tcyc – 10 ns	AC97 Output Valid	4
			tOHAC97	½tcyc + 10 ns	—	AC97 Output Hold	4
ACIN	Input	—	tISAC97	2.5 ns	—	AC97 Input Setup	
			tIHAC97	2.5 ns	—	AC97 Input Hold	
ACSYNC	Output	50 pF	tOVAC97	—	½tcyc – 10 ns	AC97 Synchronization Valid	4
			tOHAC97	½tcyc + 10 ns	—	AC97 Synchronization Hold	4
SYNCHRONOUS SERIAL PORT (SSP)							
SSPFRM	Output	50 pF	tOVFRM	—	10 ns	SSP Frame Output Valid	
			tOHFRM	5 ns	—	SSP Frame Output Hold	
SSPTX	Output	50 pF	tOVTX		10 ns	SSP Transmit Valid	
			tOHTX	5 ns	—	SSP Transmit Hold	
SSPRX	Input	—	tISRX	14 ns	—	SSP Receive Setup	
			tIHRX	14 ns	—	SSP Receive Hold	
SSPCLK	Output	50 pF	tCLK	8.819 ms	271 ns	SSP Clock Period	
AUDIO CODEC INTERFACE (ACI)							
ACOUT	Output	50 pF	tOVD	—	15 ns	ACOUT delay from rising clock edge	
			tOHD	10 ns	—	ACOUT Hold	
ACIN	Input		tIS	10 ns	—	ACIN Setup	
			tIH	2.5 ns	—	ACIN Hold	
COLOR LCD CONTROLLER							
LCDVD [17:0]	Output	50 pF	tOV	—	3 ns	LCD Data Clock to Data Valid	

NOTES:
1. Register BCRx:WST1 = 0b000
2. The 'x/x' in the MIN./MAX. indicates (LH7A404-N0E-092-xx and H7A404-N0F-092-xx)/ (LH7A404-N0E-000-xx and LH7A404-N0F-000-xx), respectively.
3. 'tcyc' is the period of one MMC Clock
4. 'tcyc' is the period of one AC97 Clock
5. 'nC' in the MIN./MAX. columns indicates the number of system clock (HCLK) periods after valid address
6. For Output Drive strength specifications, refer to Table 2

SMC Waveforms

Figure 8 and Figure 9 show waveforms and timing for an external asynchronous memory Write. Figure 10 and Figure 11 show the waveforms and timing for an external asynchronous memory Read.

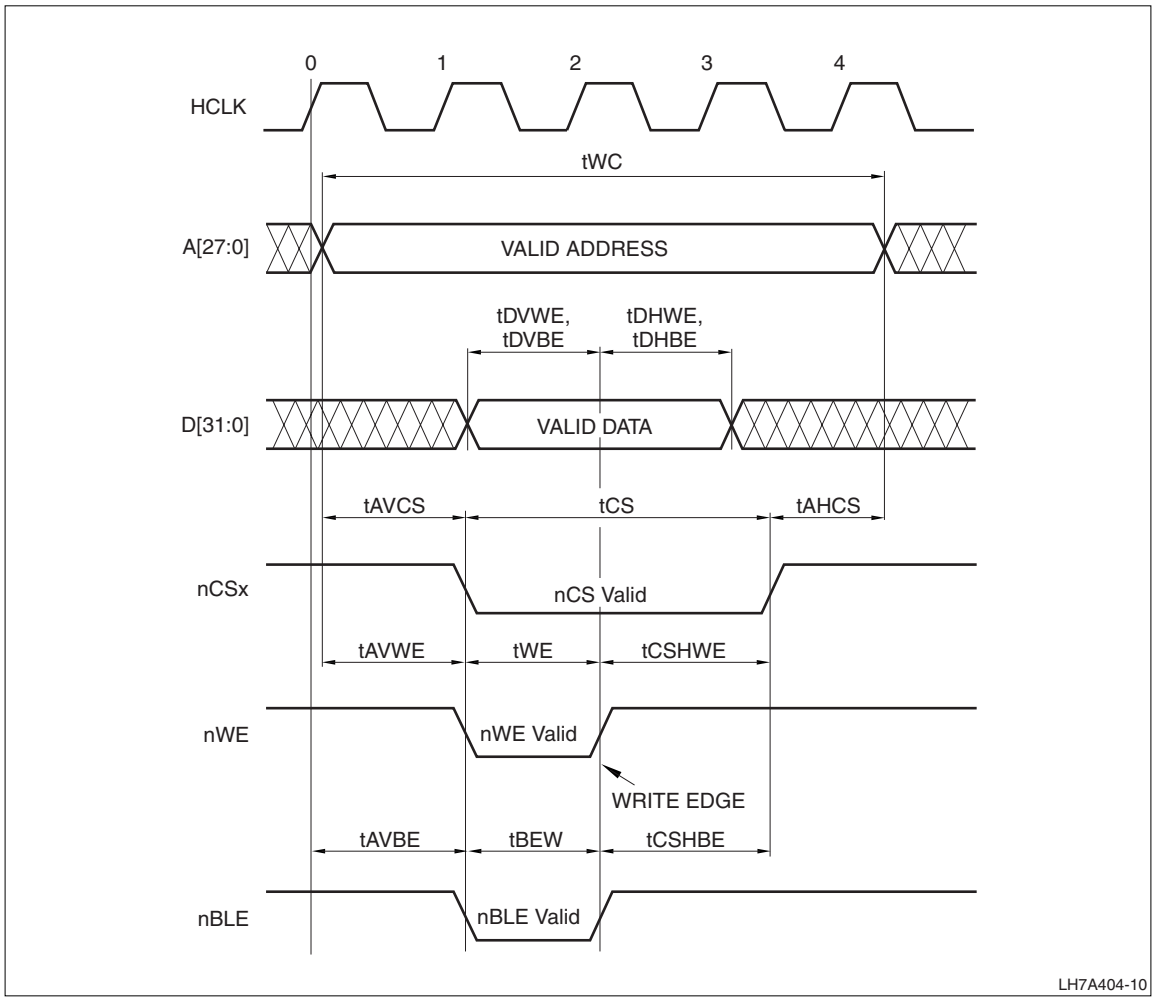


Figure 8. External Asynchronous Memory Write, Zero Wait States (BCRx:WST1 = 0b000)

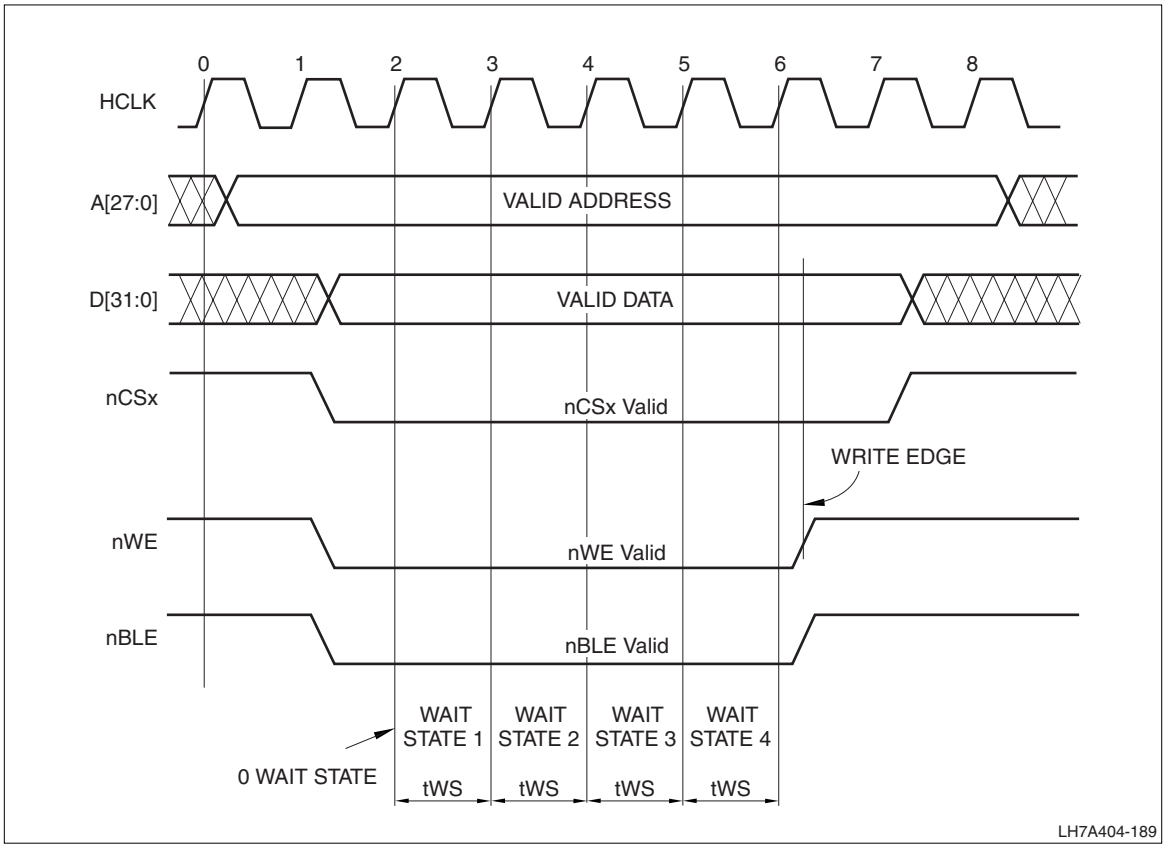


Figure 9. External Asynchronous Memory Write, Four Wait States (BCRx:WST1 = 0b100)

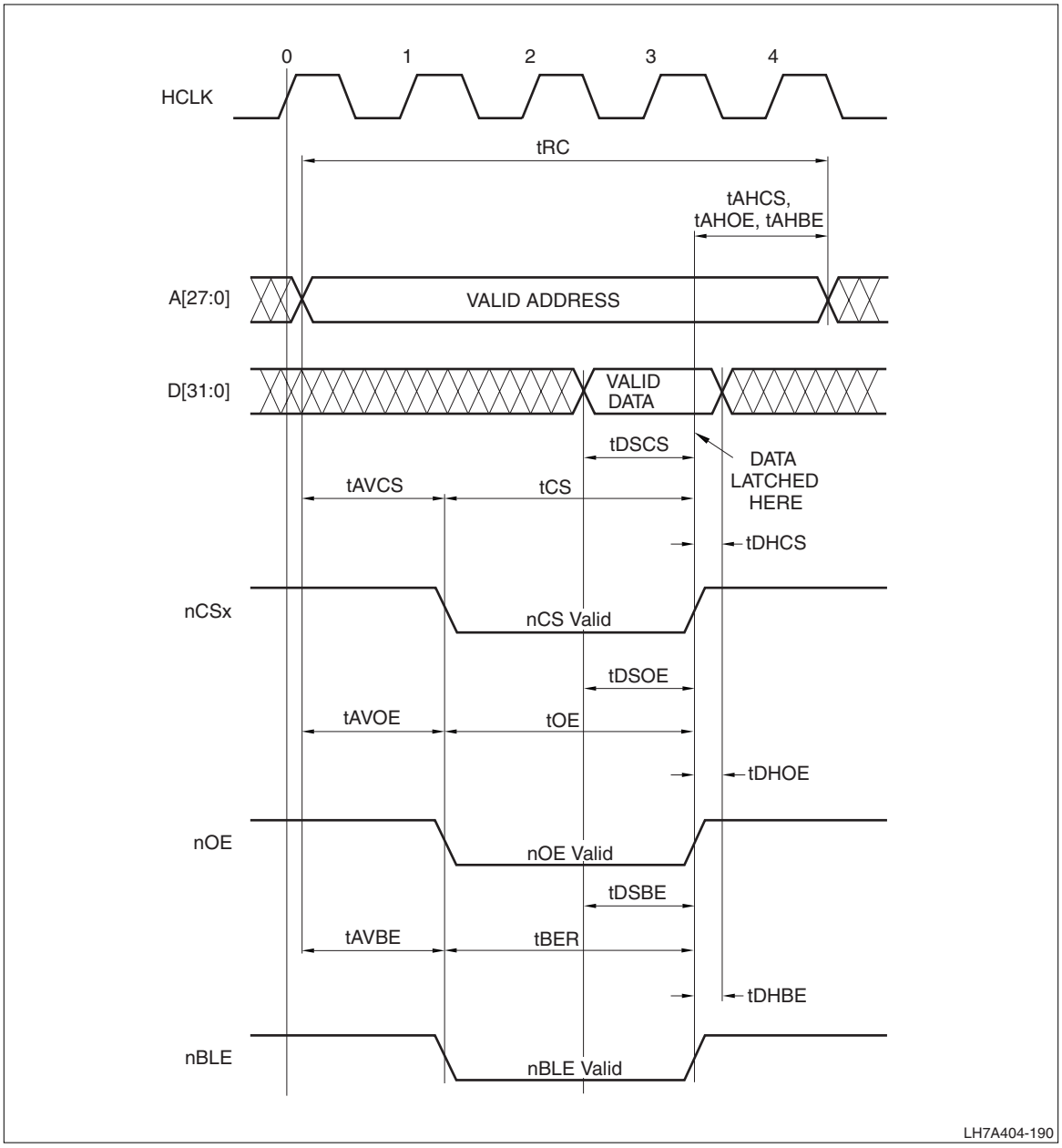


Figure 10. External Asynchronous Memory Read, Zero Wait States (BCRx:WST1 = 0b000)

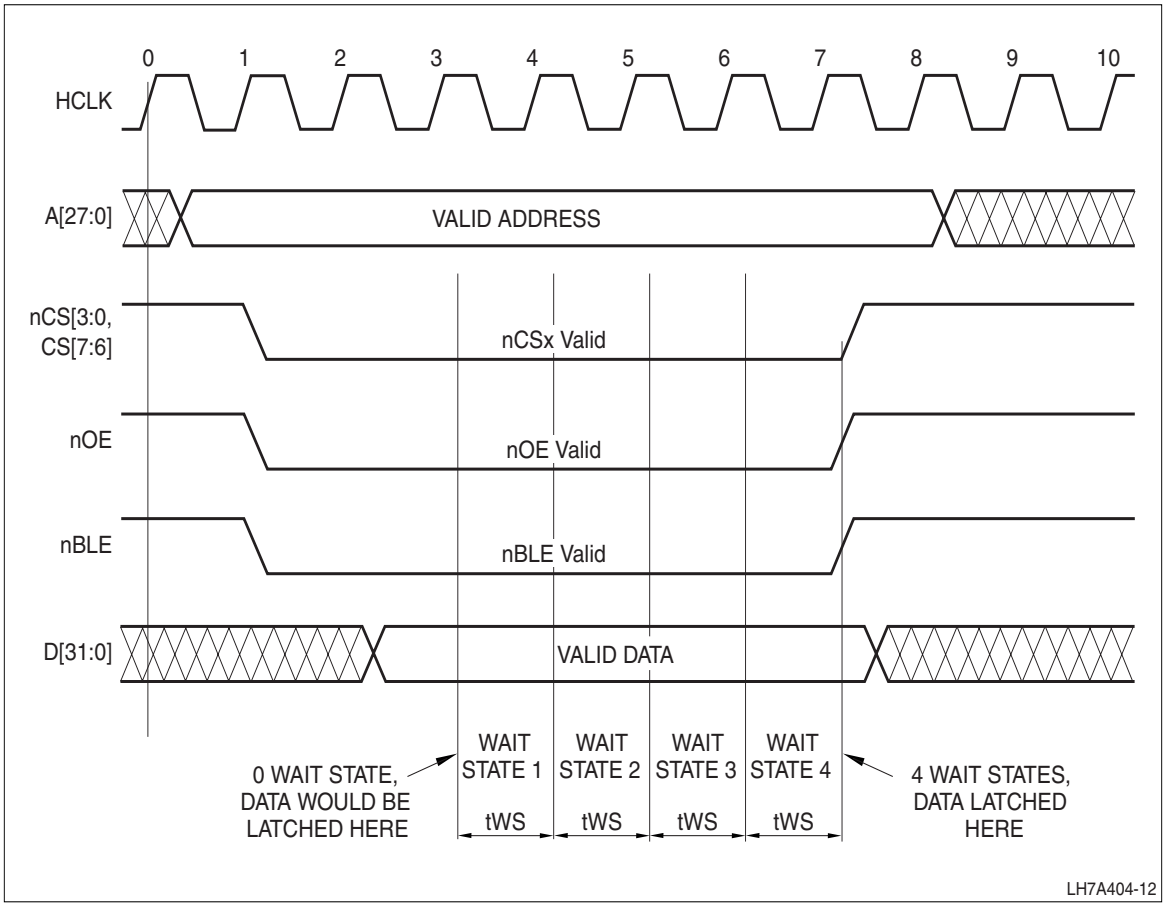


Figure 11. External Asynchronous Memory Read, Four Wait States (BCRx:WST1 = 0b100)

TIMING FOR nWAIT SIGNALLING

In addition to being able to program the number of Wait States, the SMC also can use nWAIT signalling to extend transactions. When the nWAIT input is asserted, the current transaction is held in suspense until nWAIT is released, allowing slow memory or memory-mapped peripherals time to complete the action.

Figure 12 through Figure 17 illustrate nWAIT timing using different WST register settings and circumstances.

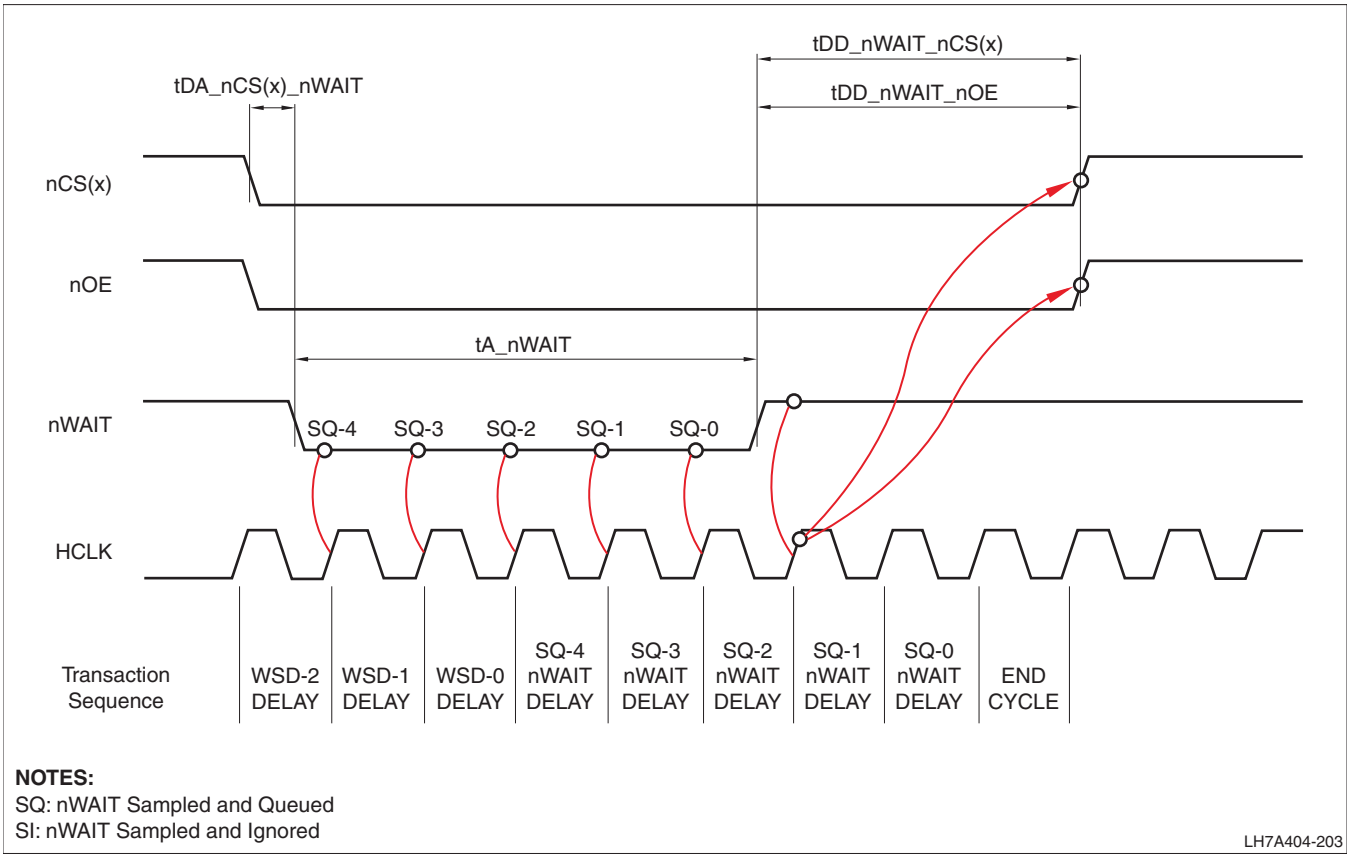


Figure 12. nWAIT Read Sequence (BCRx:WST1 = 2); Minimum Wait State Example

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT [1]
tDA_nCS(x)_nWAIT	Delay from nCS(x) assertion to nWAIT assertion	0	29	HCLK periods
tDD_nWAIT_nCS(x)	Delay from nWAIT deassertion to nCS(x) deassertion		4	HCLK periods
tDD_nWAIT_nOE	Delay from nWAIT deassertion to nOE deassertion		4	HCLK periods
tA_nWAIT	Assertion time of nWAIT	2		HCLK periods

NOTES:

1. The timing relationship is specified as a cycle-based timing. Variations caused by clock jitter, power rail noise, and I/O conditioning will cause these timings to vary nominally. It is recommended that designers add a small margin to avoid possible corner-case conditions.
2. The Bank Configuration Register (BCRx:WST1) must have Read Wait States set to a minimum of 2.
3. The number of HCLK periods that nWAIT lags assertion of nCSx must be added to the minimum value for BCRx:WST1. For example, if nWAIT lags nCSx by 3 HCLK periods, the minimum setting of BCRx:WST1 is 2 + 3, or a total of 5 as the minimum value for BCRx:WST1.
4. No nWAIT delay cycles are added for any nWAIT assertions that occur prior to the beginning of the WSD-2 delay. These nWAIT assertions are ignored.
5. Once the WSD-2 delay begins, one HCLK cycle is added to the transaction each time nWAIT is sampled and queued (SQ-x). The nWAIT cycles begin being added after the Wait State Countdown reaches WSD-0.
6. Once nWAIT is sampled HIGH (de-asserted), the current memory transaction is queued to complete.
7. Since static and dynamic memory cannot be accessed at the same time, prolonged extension of an SMC transaction by either Wait States or nWAIT delays can cause refresh failure for the SDRAM, and may cause SDRAM data loss.

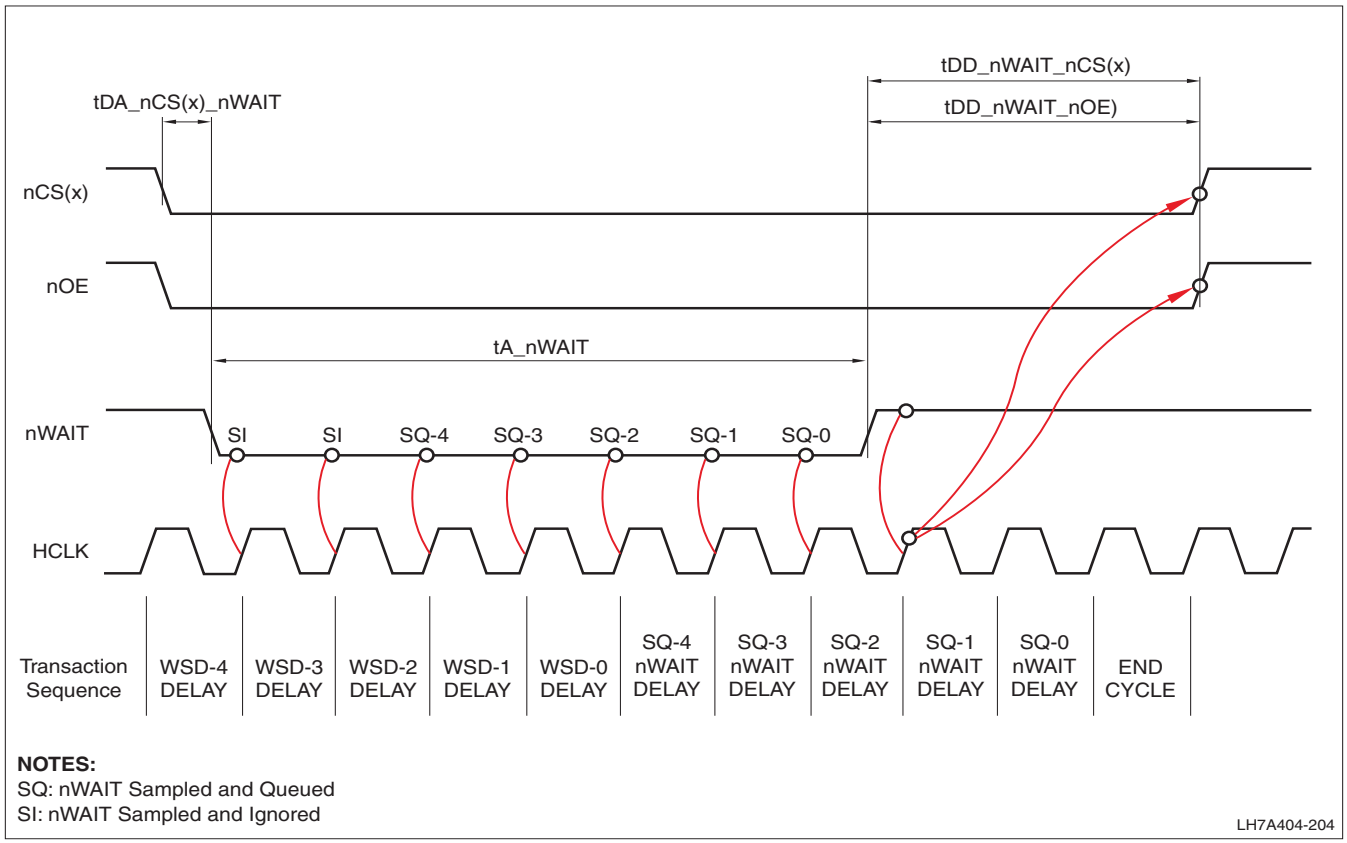


Figure 13. nWAIT Read Sequence (BCRx:WST1 = 4); Ignored and Queued nWAIT Delays

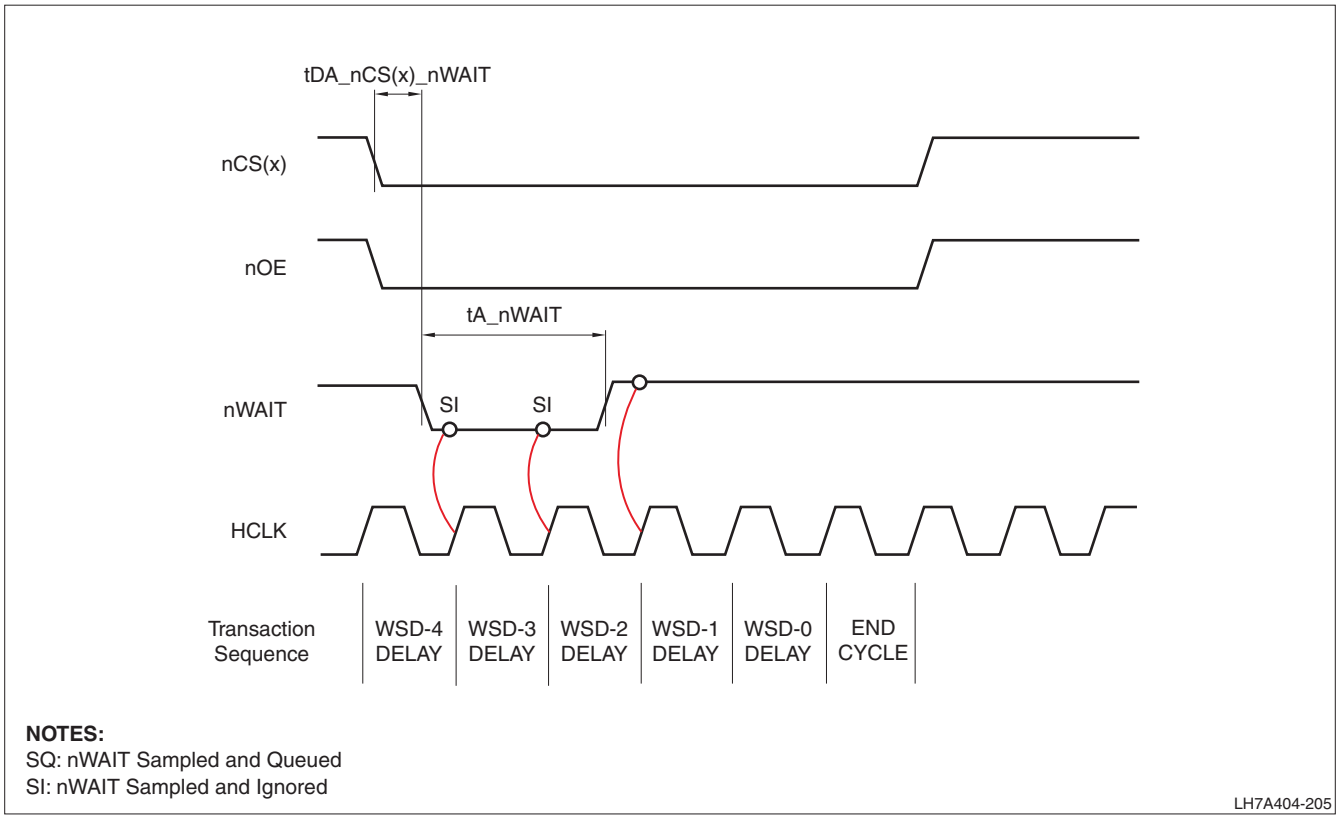


Figure 14. nWAIT Read Sequence (BCRx:WST1 = 4); nWAIT Has No Effect On Current Transaction

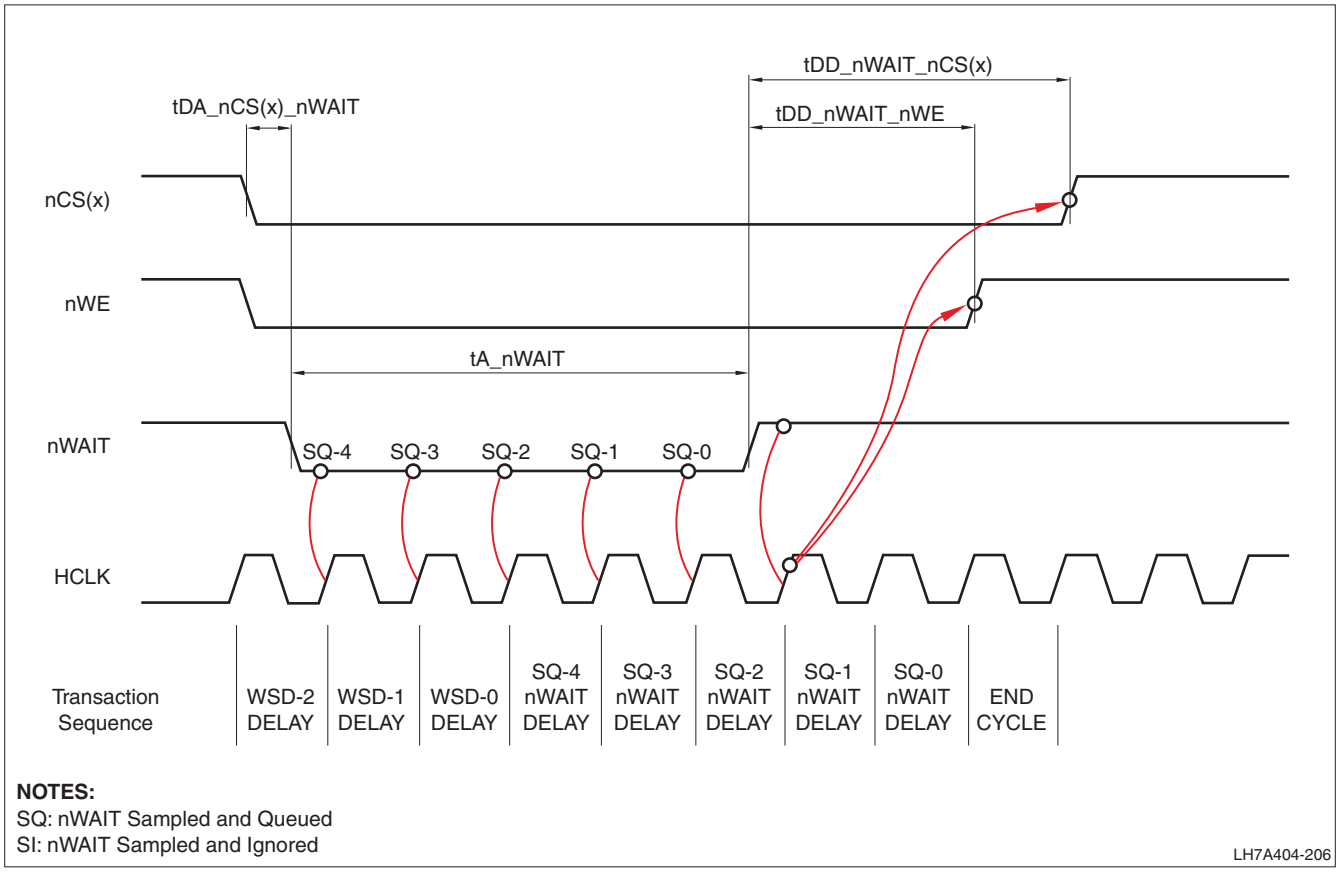


Figure 15. nWAIT Write Sequence (BCRx:WST1 = 2); Minimum Wait State Example

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT[1]
tIDA_nCS(x)_nWAIT	Delay from nCS(x) assertion to nWAIT assertion	0	29	HCLK periods
tDD_nWAIT_nCS(x)	Delay from nWAIT deassertion to nCS(x) deassertion		4	HCLK periods
tDD_nWAIT_nWE	Delay from nWAIT deassertion to nWE deassertion		3	HCLK periods
tA_nWAIT	Assertion time of nWAIT	2		HCLK periods

NOTES:
1. The timing relationship is specified as a cycle-based timing. Variations caused by clock jitter, power rail noise, and I/O condtioning will cause these timings to vary nominally. It is recommended that designers add a small margin to avoid possible corner-case conditions.
2. The Bank Configuration Register (BCRx:WST1) must have Write Wait States set to a minimum of 2.
3. The number of HCLK periods that nWAIT lags assertion of nCSx must be added to the minimum value for BCRx:WST1. For example, if nWAIT lags nCSx by 3 HCLK periods, the minimum setting of BCRx:WST1 is 2 + 3, or a total of 5 as the minimum value for BCRx:WST1.
4. No nWAIT delay cycles are added for any nWAIT assertions that occur prior to the beginning of the WSD-2 delay. These nWAIT assertions are ignored.
5. Once the WSD-2 delay begins, one HCLK cycle is added to the transaction each time nWAIT is sampled and queued (SQ-x). The nWAIT cycles begin being added after the Wait State Countdown reaches WSD-0.
6. Once nWAIT is sampled HIGH (de-asserted), the current memory transaction is queued to complete.
7. Since static and dynamic memory cannot be accessed at the same time, prolonged extension of an SMC transaction by either Wait States or nWAIT delays can cause refresh failure for the SDRAM, and may cause SDRAM data loss.

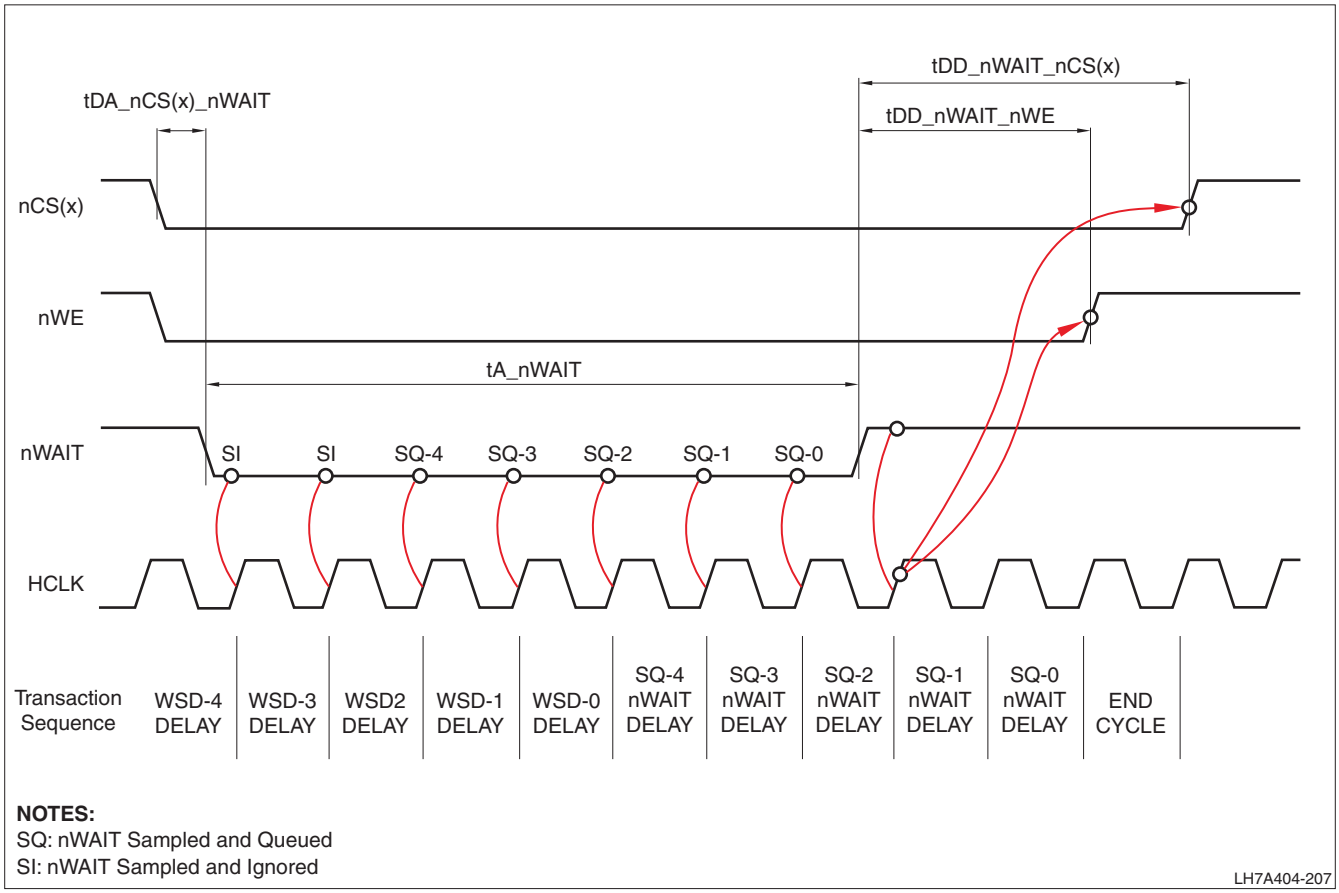
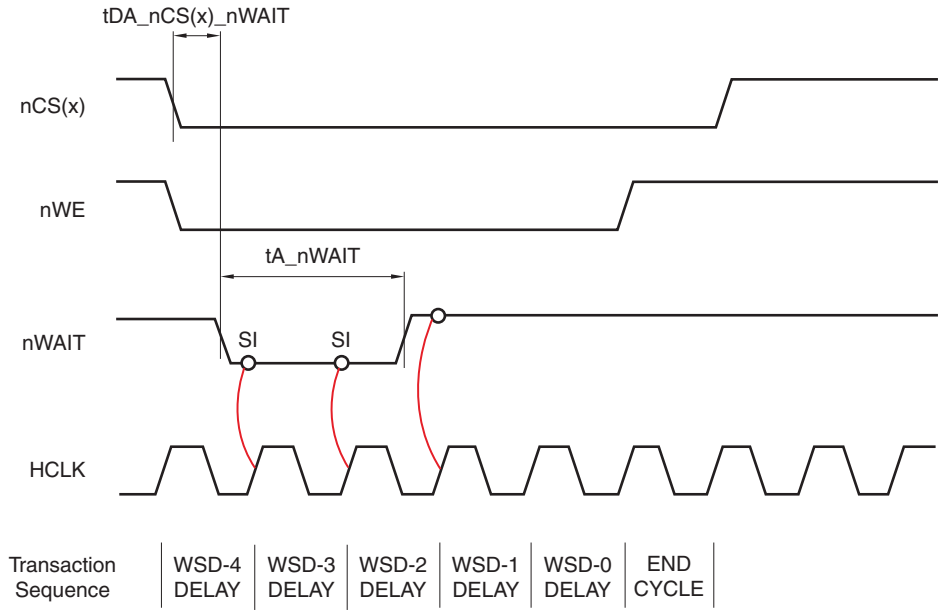


Figure 16. nWAIT Write Sequence (BCRx:WST1 = 4); Ignored and Queued nWAIT Delays



NOTES:
SQ: nWAIT Sampled and Queued
SI: nWAIT Sampled and Ignored

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Figure 17. nWAIT Write Sequence (BCRx:WST1 = 4); nWAIT Has No Effect On Current Transaction

Synchronous Memory Controller Waveforms

Figure 18 shows the waveform and timing for a Synchronous Burst Read (page already open). Figure 19 shows the waveform and timing for synchronous memory to activate a bank and Write.

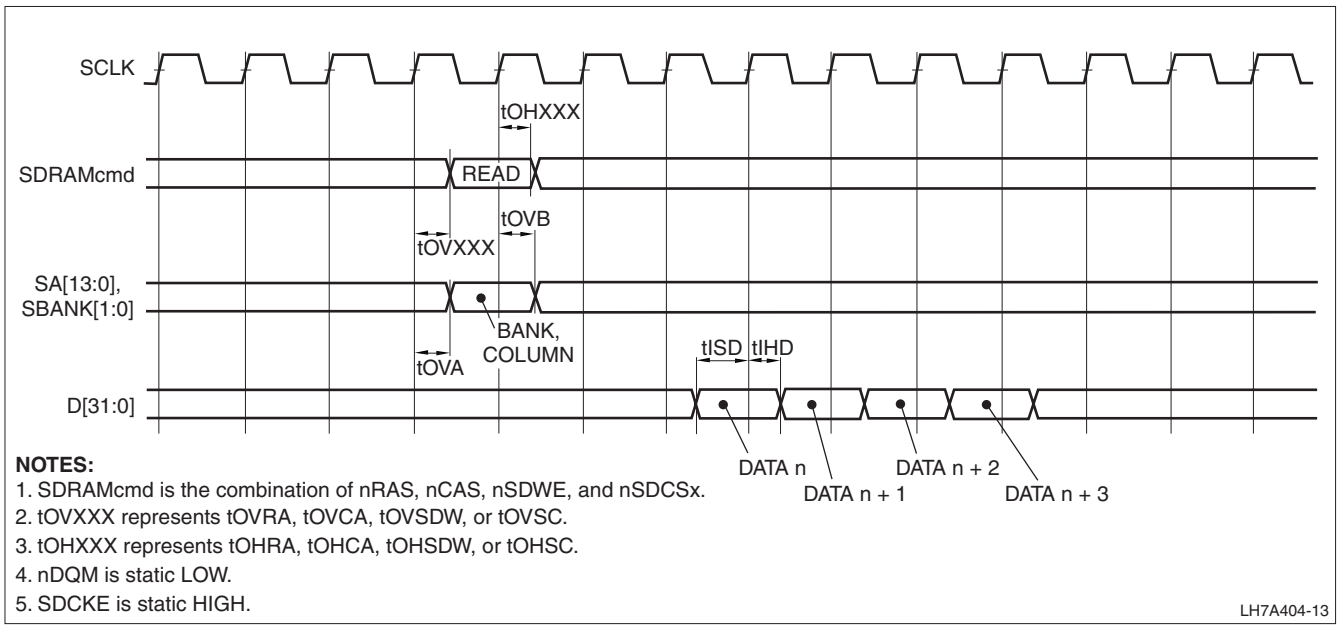


Figure 18. Synchronous Burst Read

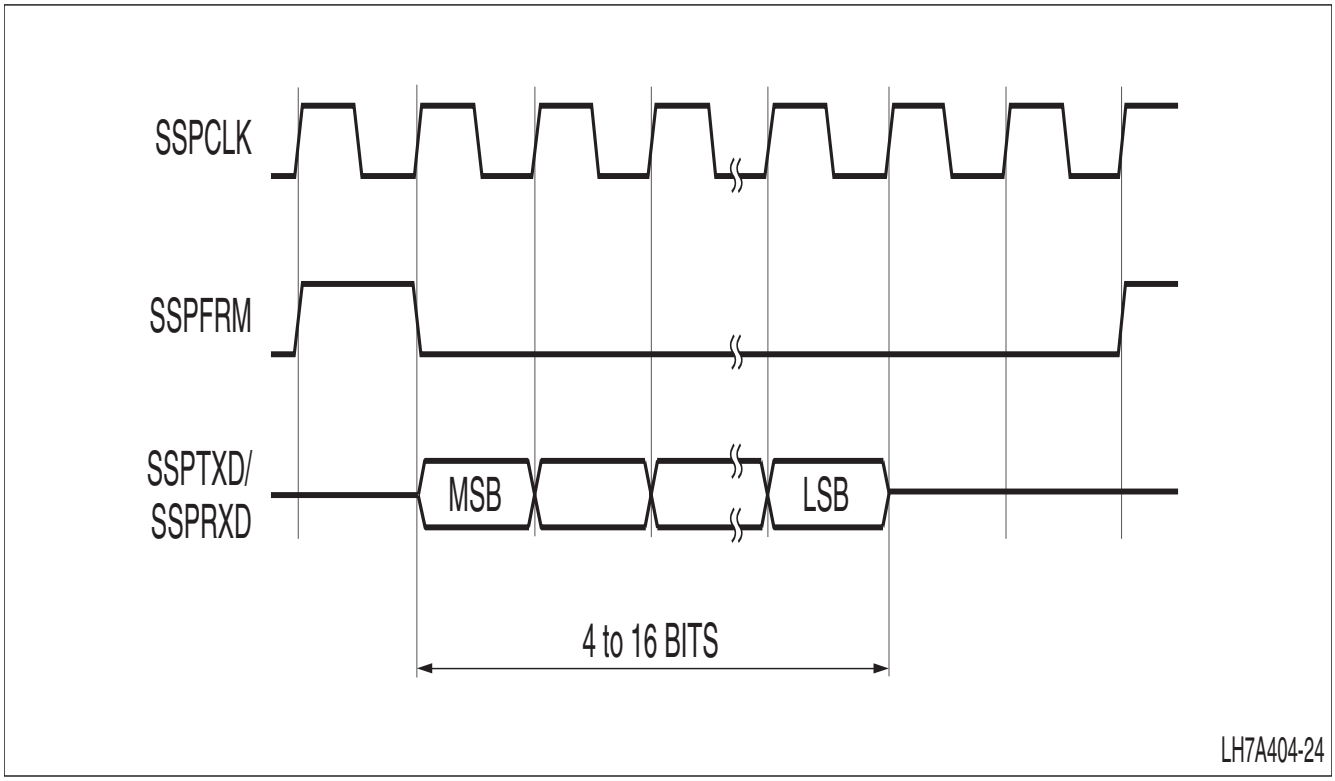


Figure 19. Synchronous Bank Activate and Write

SSP Waveforms

The Synchronous Serial Port (SSP) supports three data frame formats:

- Texas Instruments SSI
- Motorola SPI
- National Semiconductor MICROWIRE

Each frame format is between 4 and 16 bits in length, depending upon the programmed data size. Each data frame is transmitted beginning with the Most Significant Bit (MSB) i.e. 'big endian'. For all three formats, the SSP serial clock is held LOW (inactive) while the SSP is idle. The SSP serial clock transitions only during active transmission of data. The SSPFRM signal marks the beginning and end of a frame.

Figure 20 and Figure 21 show Texas Instruments synchronous serial frame format, Figure 22 through Figure 29 show the Motorola SPI format, and Figure 30 and Figure 31 show National Semiconductor's MICROWIRE data frame format.

For Texas Instruments SSI format, the SSPFRM pin is pulsed prior to each frame's transmission for one serial clock period beginning at its rising edge. For this frame format, both the SSP and the external slave device drive their output data on the rising edge of the clock and latch data from the other device on the falling edge. See Figure 20 and Figure 21.

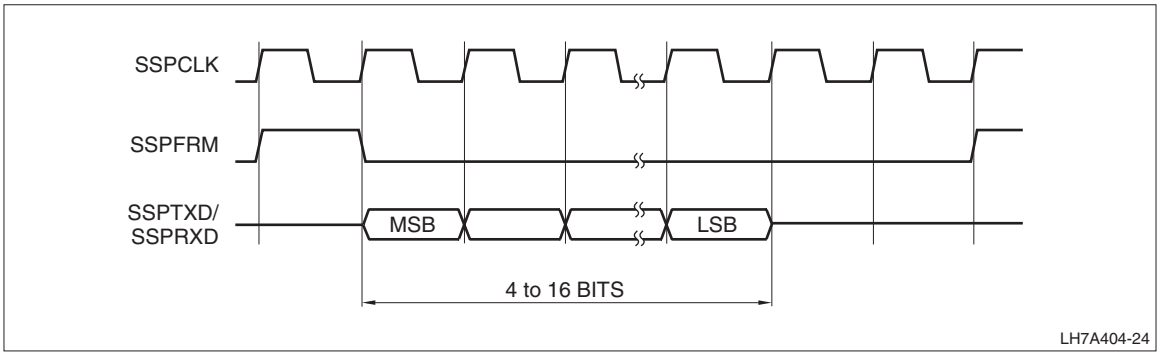


Figure 20. Texas Instruments Synchronous Serial Frame Format (Single Transfer)

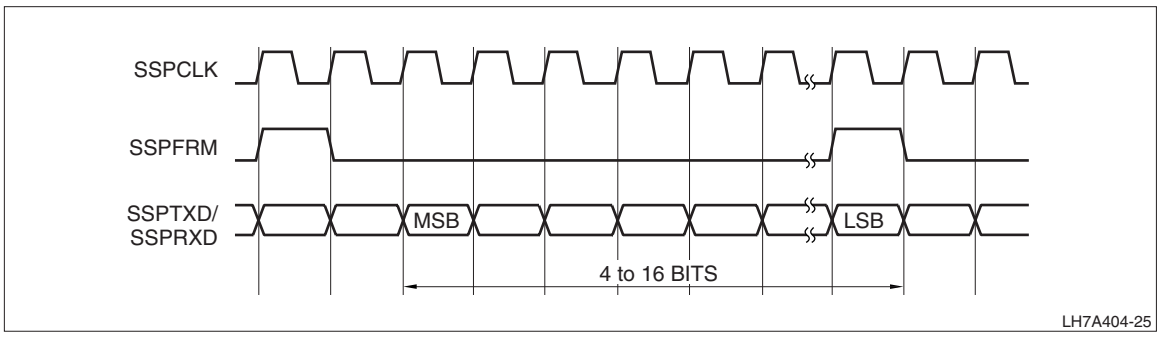


Figure 21. Texas Instruments Synchronous Serial Frame Format (Continuous Transfer)

For Motorola SPI, the serial frame pin (SSPFRM) is active LOW. The SPO and SPH bits in SSP Control Register 0 determine SSPCLK and SSPFRM operation in single and continuous modes. See Figures 22 through 29.

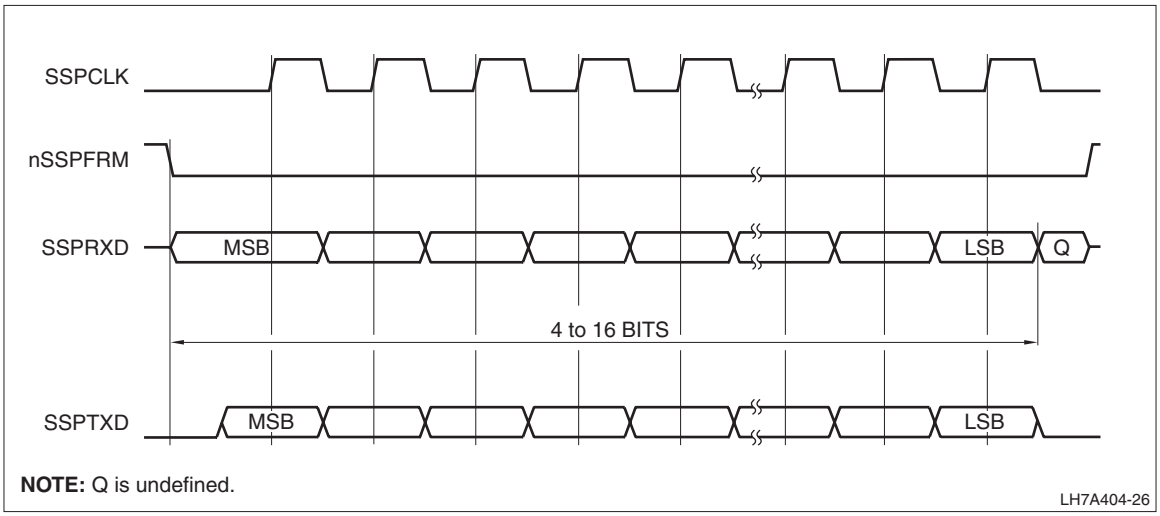


Figure 22. Motorola SPI Frame Format (Single Transfer) with SPO = 0 and SPH = 0

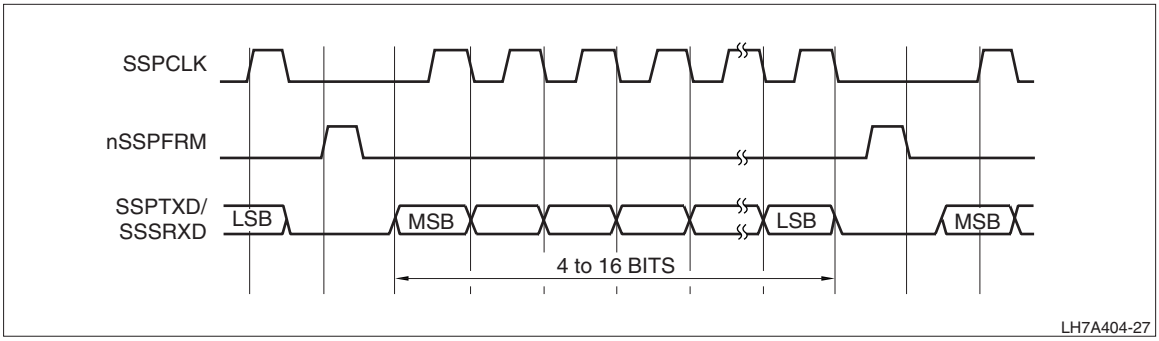


Figure 23. Motorola SPI Frame Format (Continuous Transfer) with SPO = 0 and SPH = 0

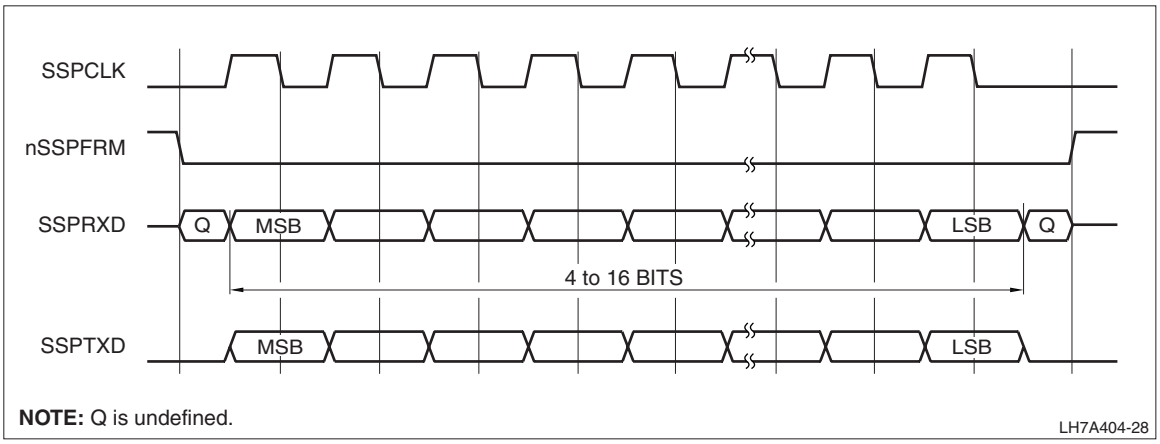


Figure 24. Motorola SPI Frame Format (Single Transfer) with SPO = 0 and SPH = 1

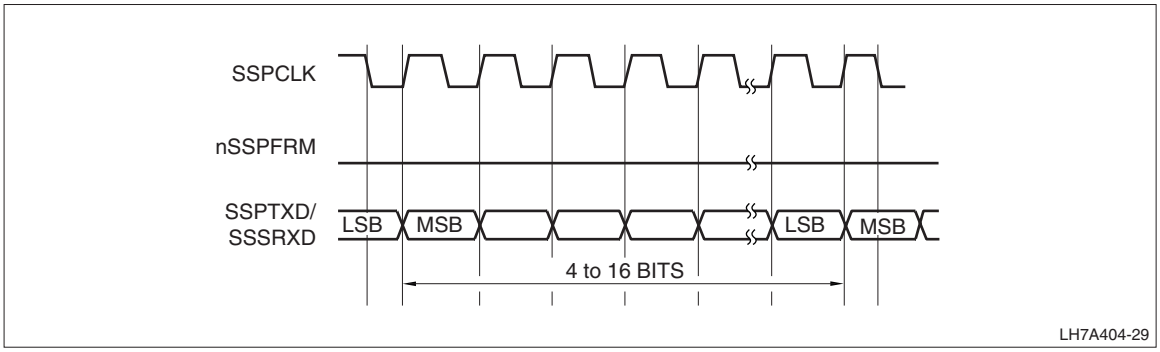


Figure 25. Motorola SPI Frame Format (Continuous Transfer) with SPO = 0 and SPH = 1

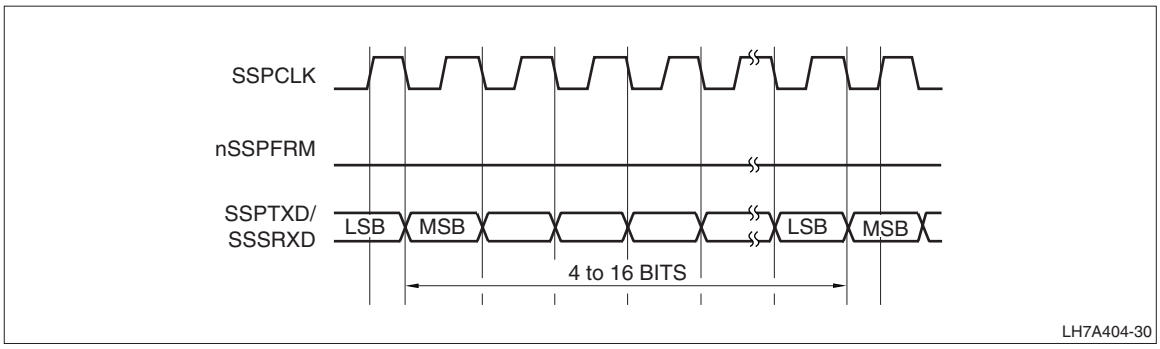


Figure 26. Motorola SPI Frame Format (Continuous Transfer) with SPO = 1 and SPH = 1

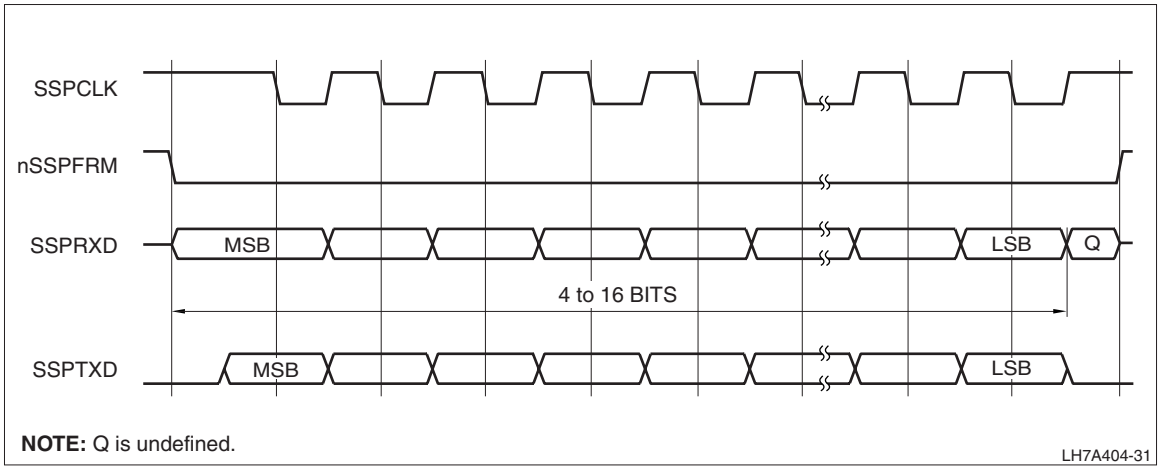


Figure 27. Motorola SPI Frame Format (Single Transfer) with SPO = 1 and SPH = 0

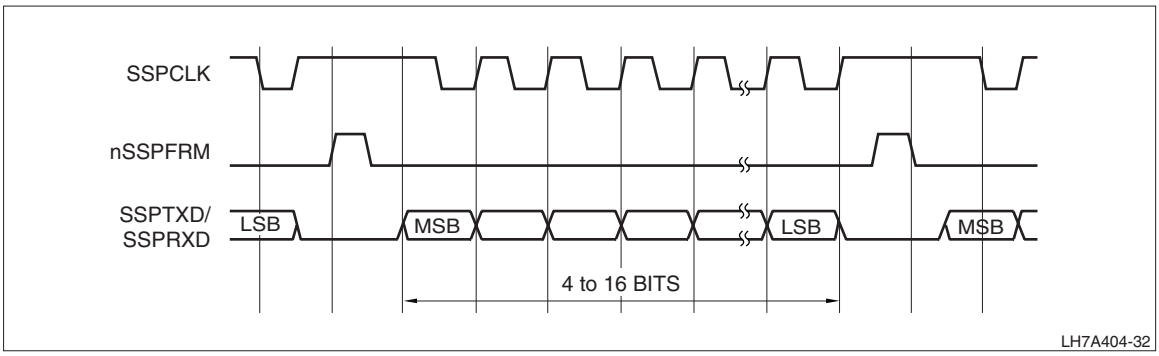


Figure 28. Motorola SPI Frame Format (Continuous Transfer) with SPO = 1 and SPH = 0

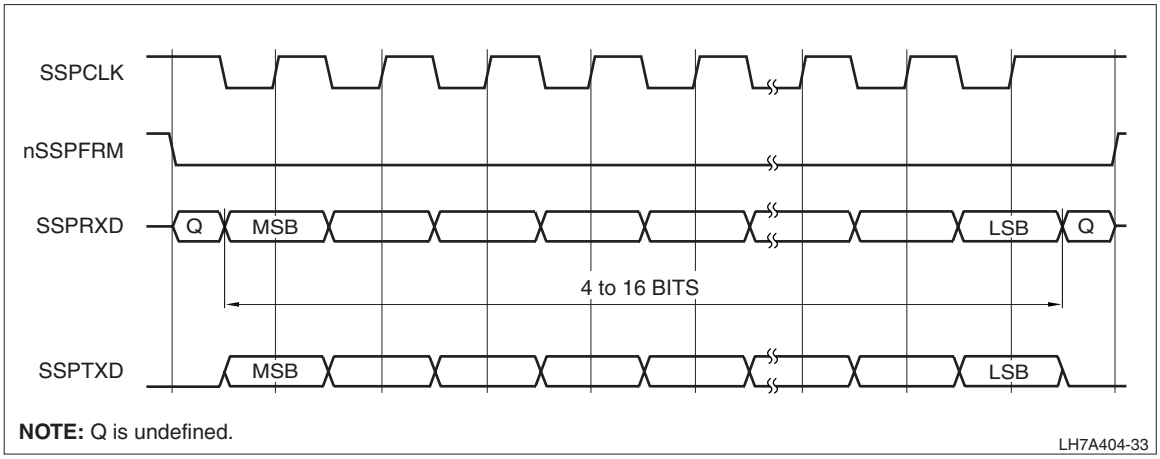


Figure 29. Motorola SPI Frame Format (Single Transfer) with SPO = 1 and SPH = 1

For National Semiconductor MICROWIRE format, the serial frame pin (SSPFRM) is active LOW. Both the SSP and external slave device drive their output data on the falling edge of the clock, and latch data from the other device on the rising edge of the clock. Unlike the full-duplex transmission of the other two frame formats, the National Semiconductor MICROWIRE format utilizes a master-slave messaging technique that operates in half-duplex. When a frame begins in this mode, an 8-bit control message is transmitted to the off-chip slave. During this transmission no incoming data is received by the SSP. After the message has been sent, the external slave device decodes the message. After waiting one serial clock period after the last bit of the 8-bit control message was received it responds by returning the requested data. The returned data can be 4 to 16 bits in length, making the total frame length between 13 to 25 bits. See Figure 30 and Figure 31.

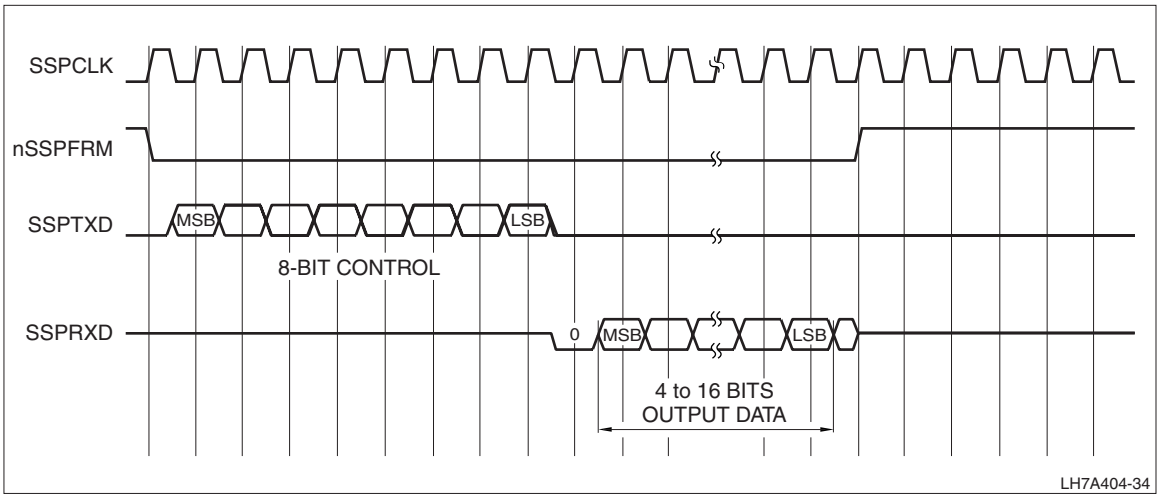


Figure 30. MICROWIRE Frame Format (Single Transfer)

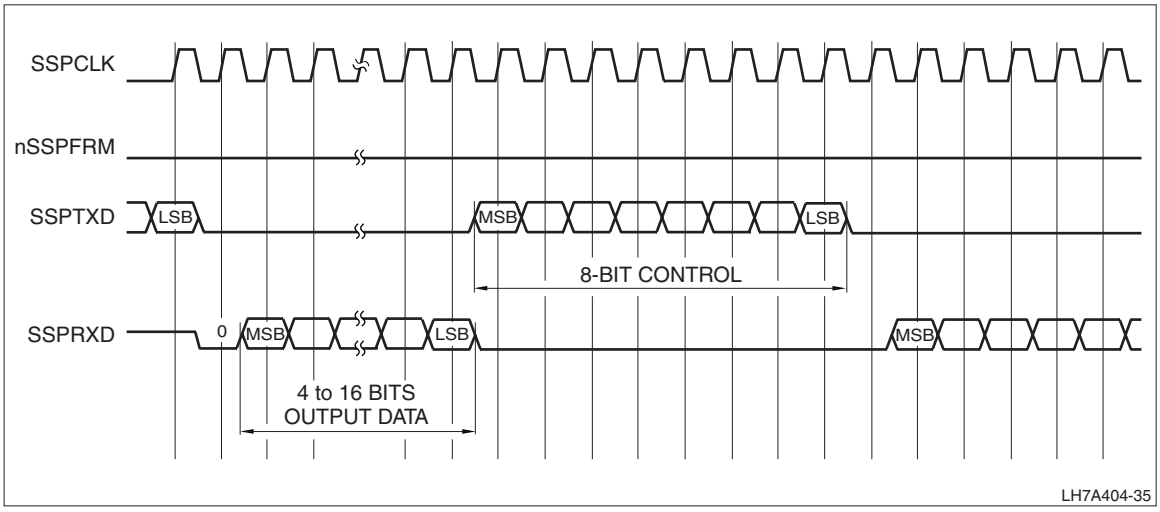


Figure 31. MICROWIRE Frame Format (Continuous Transfers)

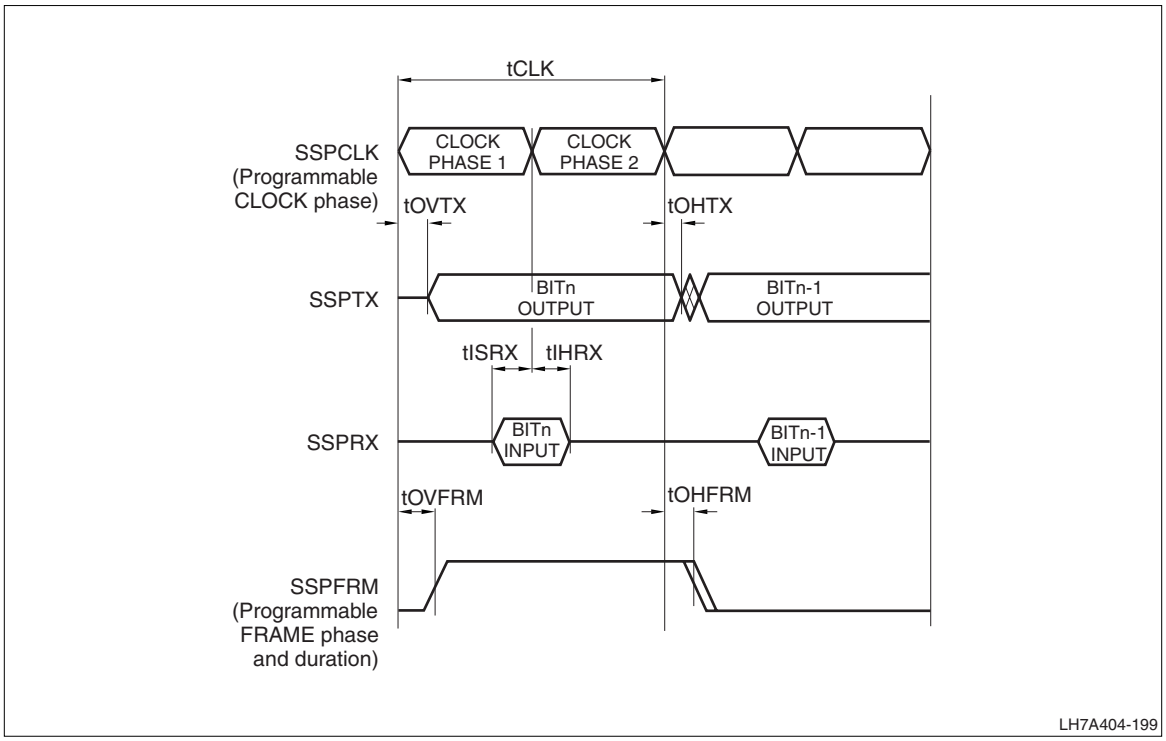
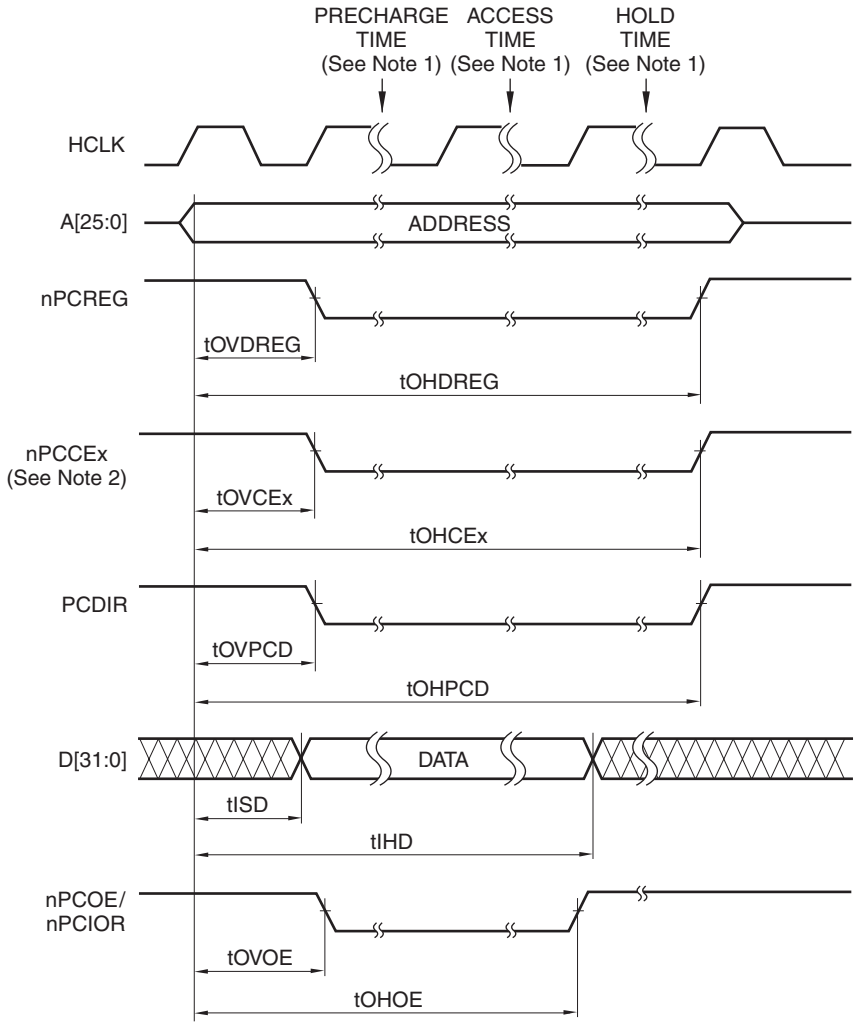


Figure 32. General SSP Timing

PC Card (PCMCIA) Waveforms

Figure 33 shows the waveforms for PCMCIA Read transactions and Figure 34 shows the waveforms and timing for Write transactions. Figure 35 shows the pre-charge, access, and hold timing relationships.



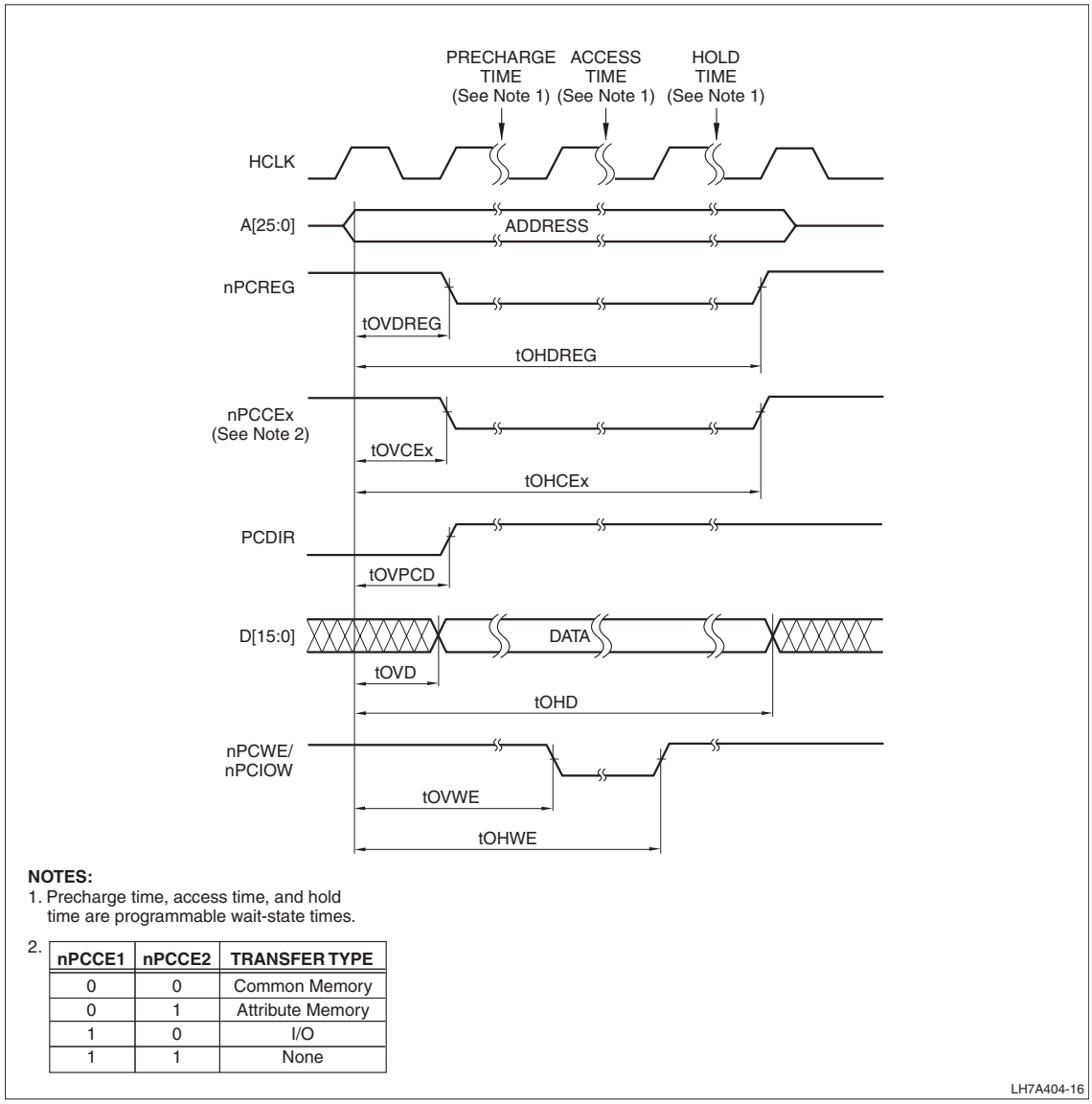
NOTES:

1. Precharge time, access time, and hold time are programmable wait-state times.
2.

nPCCE1	nPCCE2	TRANSFER TYPE
0	0	Common Memory
0	1	Attribute Memory
1	0	I/O
1	1	None

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Figure 33. PCMCIA Read Transfer



NOTES:
1. Precharge time, access time, and hold time are programmable wait-state times.
2.

nPCCE1	nPCCE2	TRANSFER TYPE
0	0	Common Memory
0	1	Attribute Memory
1	0	I/O
1	1	None

Figure 34. PCMCIA Write Transfer

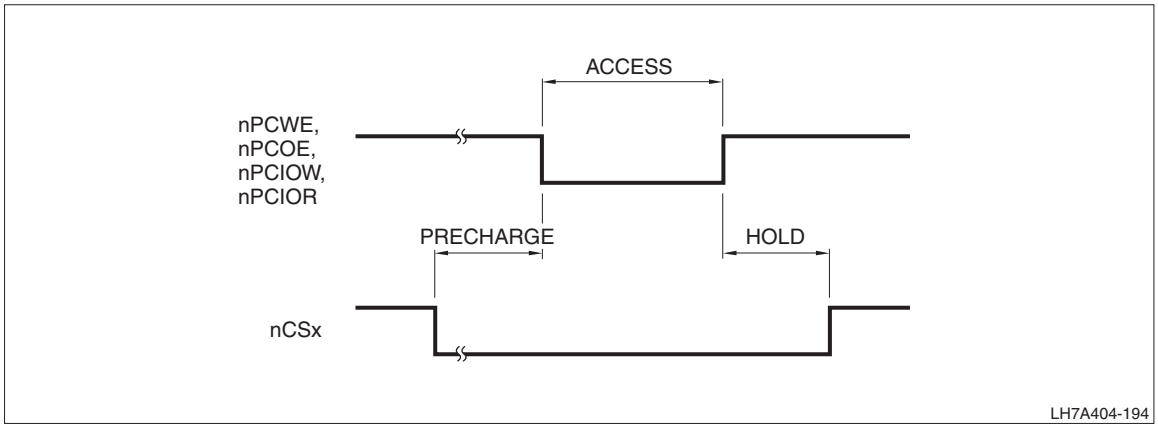


Figure 35. PCMCIA Precharge, Access, and Hold Waveform

MMC Interface Waveforms

Figure 36 shows the waveforms and timing for an MMC command or data Write. Figure 37 shows the waveforms and timing for an MMC command or data Read.

AC97 Interface Waveforms

Figure 38 shows the waveforms and timing for the AC97 interface Data Setup and Hold.

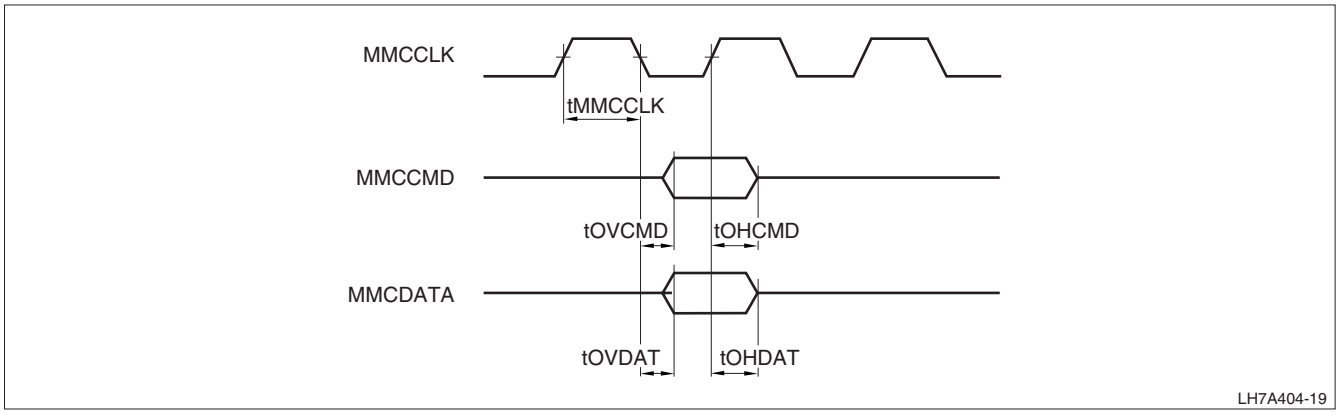


Figure 36. MMC Command/Data Write

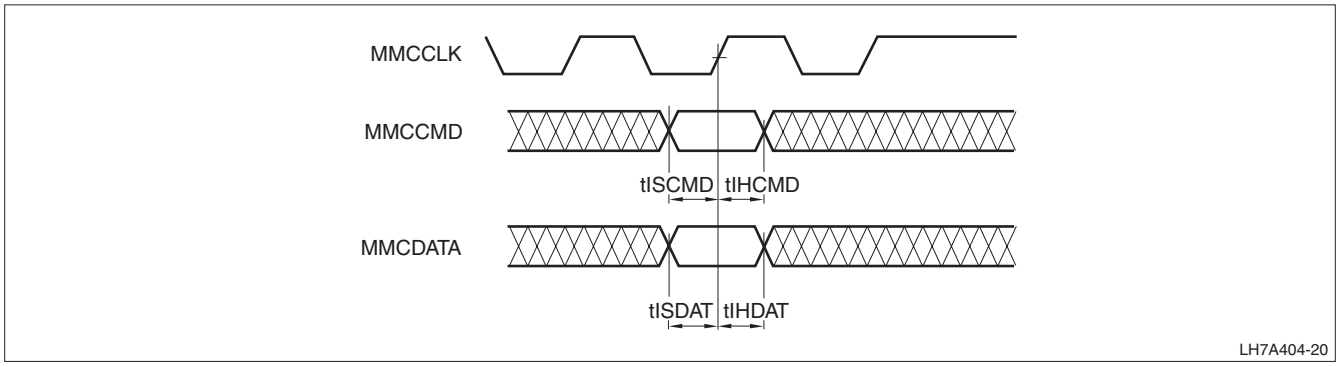


Figure 37. MMC Command/Data Read

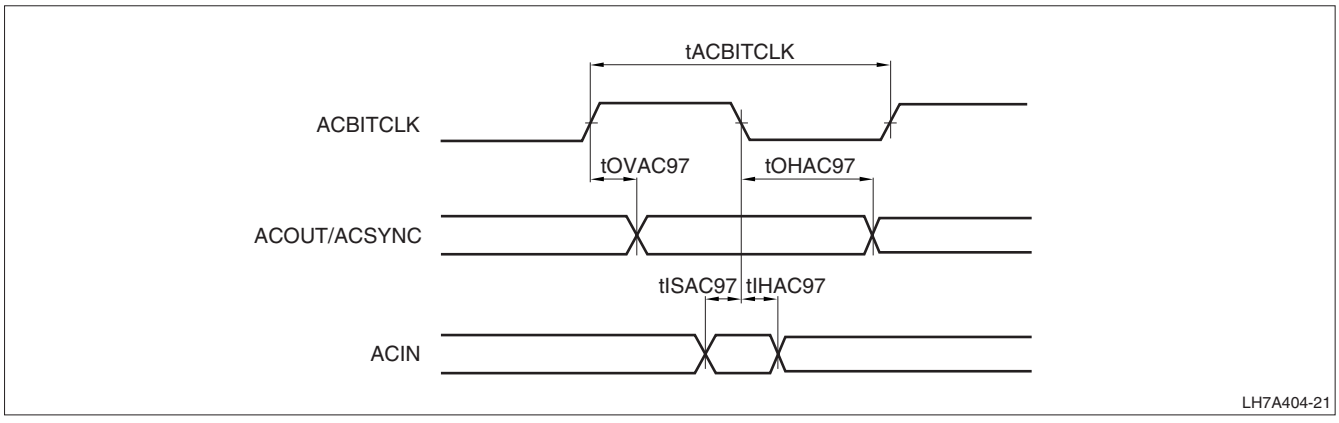


Figure 38. AC97 Data Setup and Hold

Audio Codec Interface (ACI) Timing

The timing for the Audio Codec Interface are shown in Figure 39 and Figure 40. Transmit data is clocked on the rising edge of ACBITCLK (whether transmitted by the LH7A404 ACI or by the external codec chip); receive data is clocked on the falling edge. This allows full-speed, full duplex operation.

Color LCD Controller Waveforms

Figure 41 shows the Valid Output Setup Time for LCD data. Timing diagrams for each CLCDC mode are represented in Figure 42 through Figure 47.

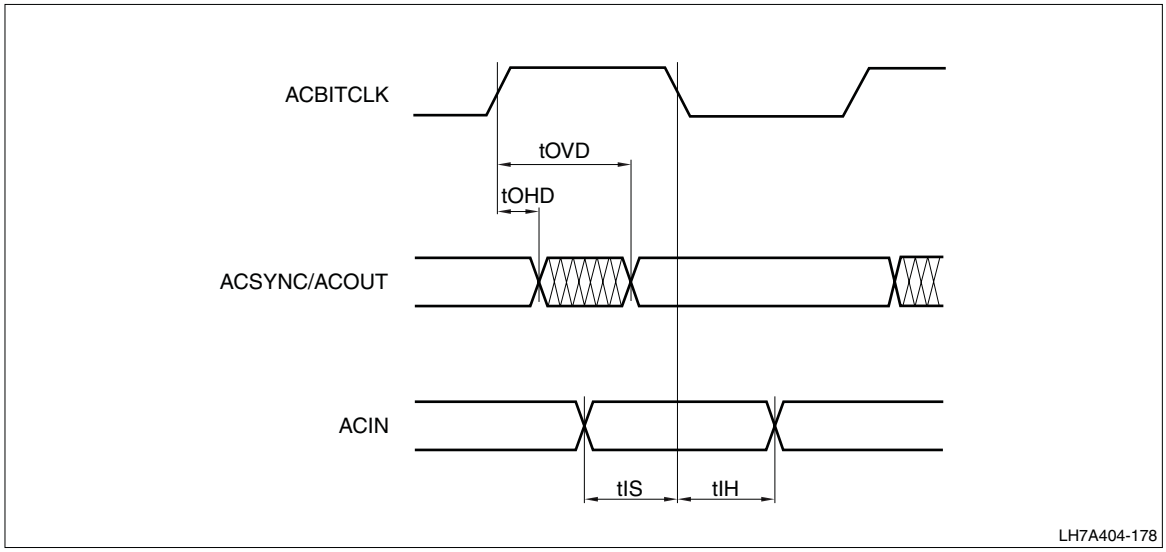


Figure 39. ACI Signal Timing

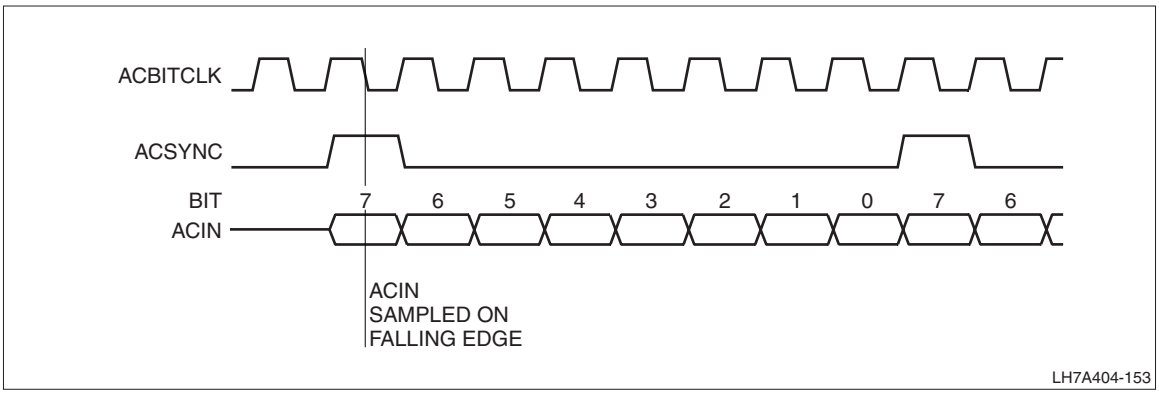


Figure 40. ACI Data Stream

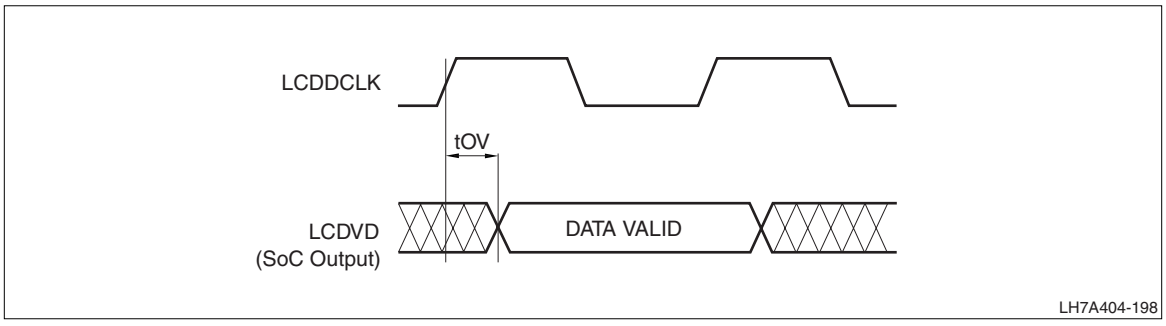


Figure 41. CLCDC Valid Output Data Time

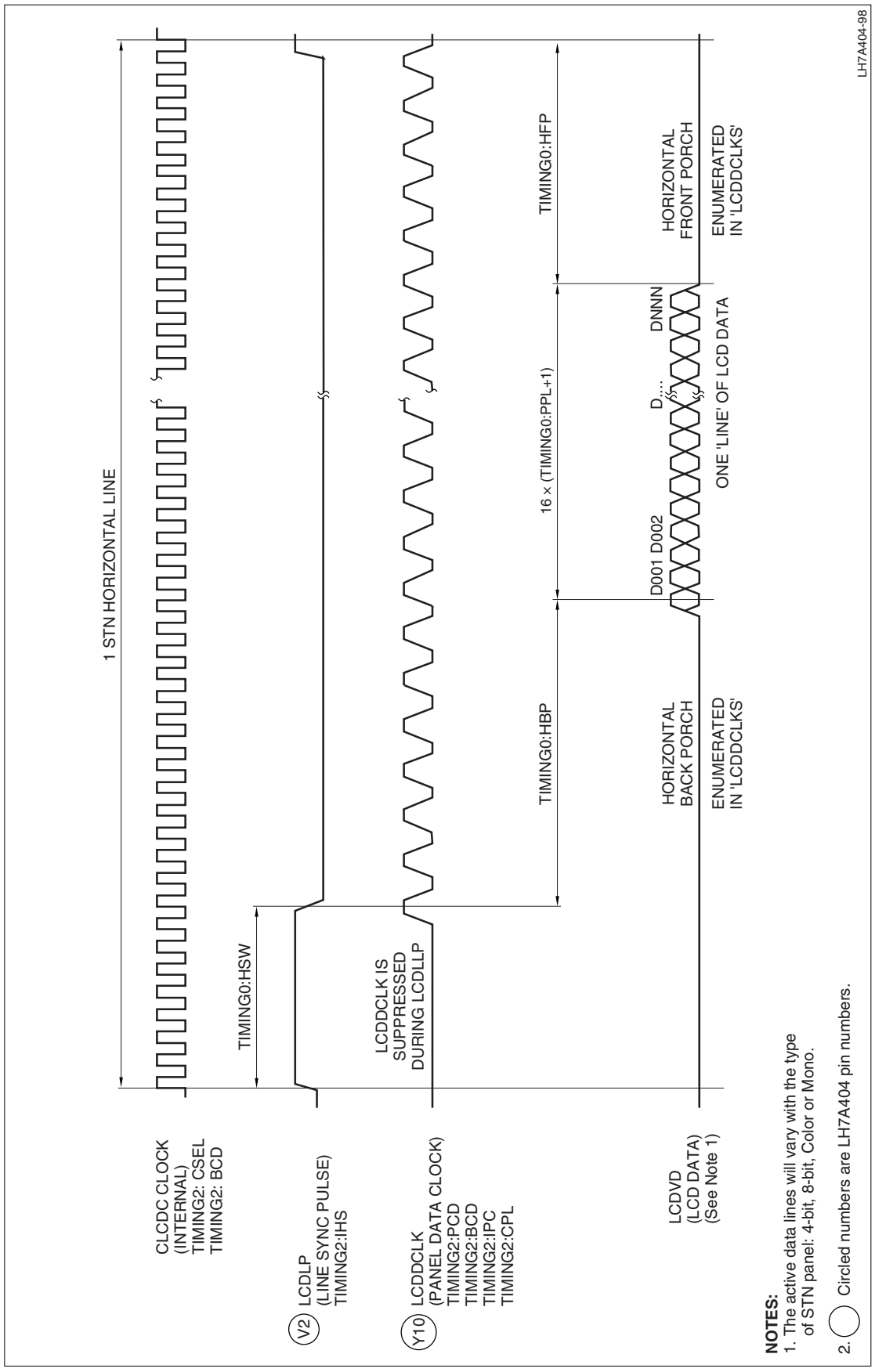


Figure 42. STN Horizontal Timing

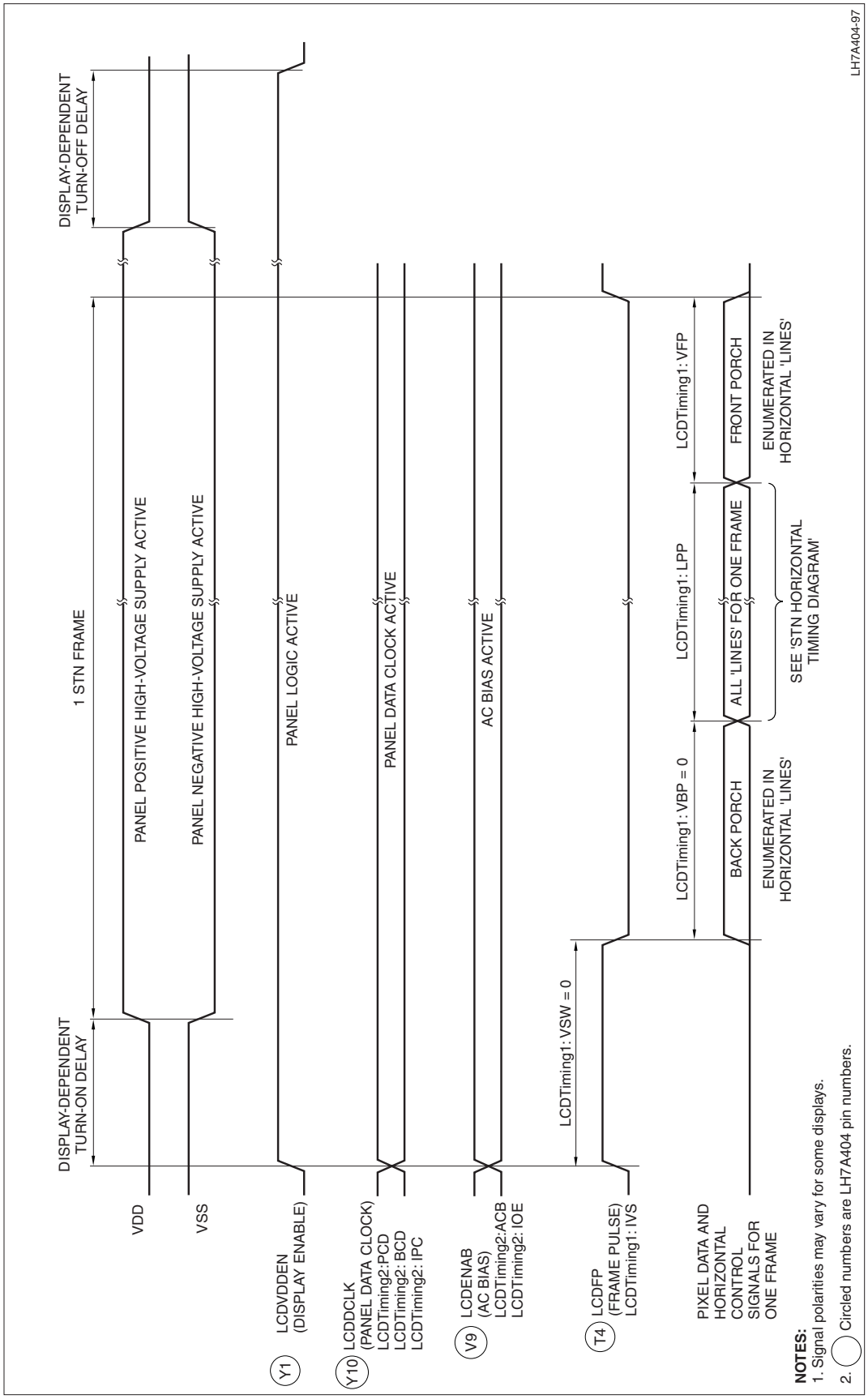


Figure 43. STN Vertical Timing

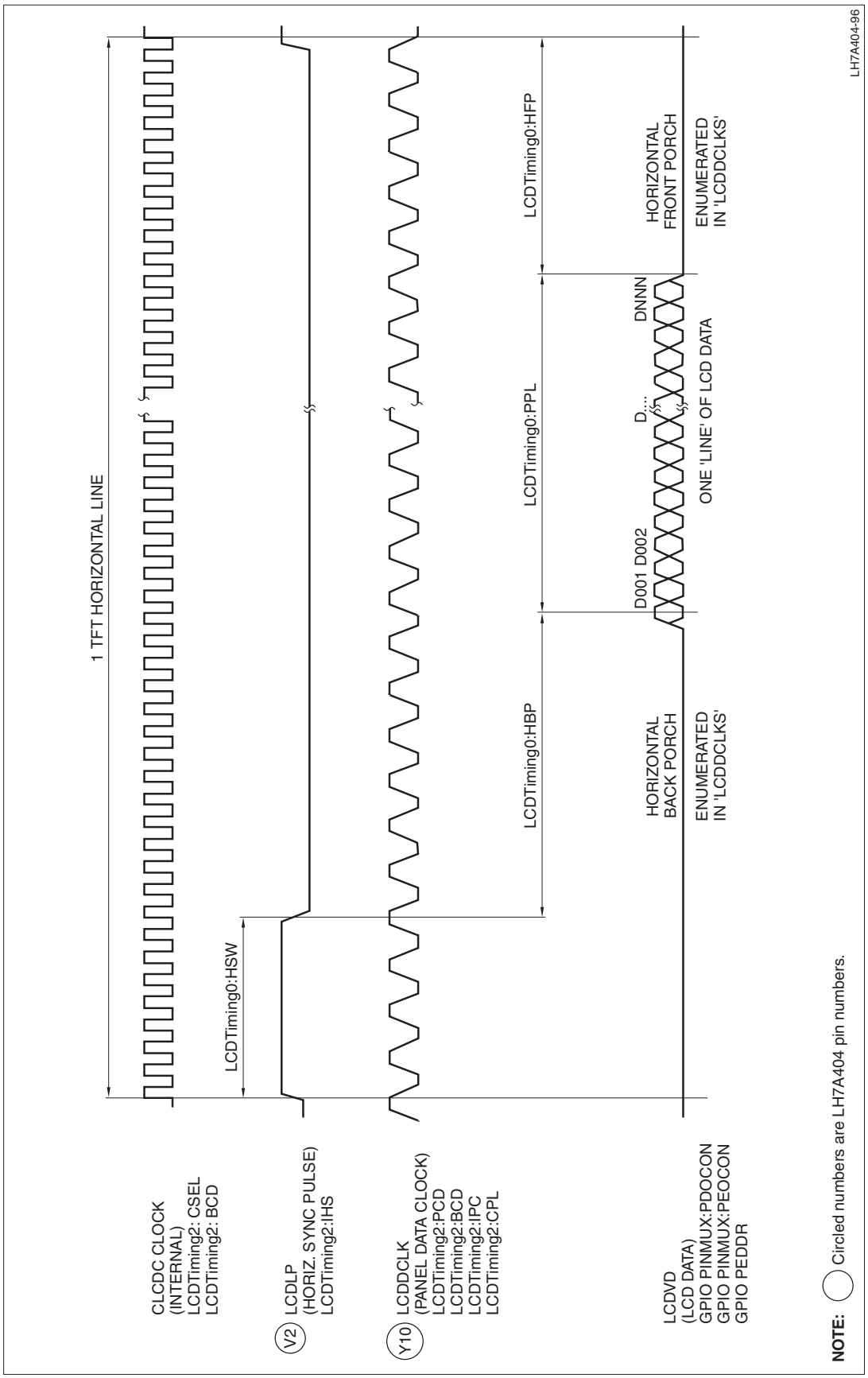


Figure 44. TFT Horizontal Timing

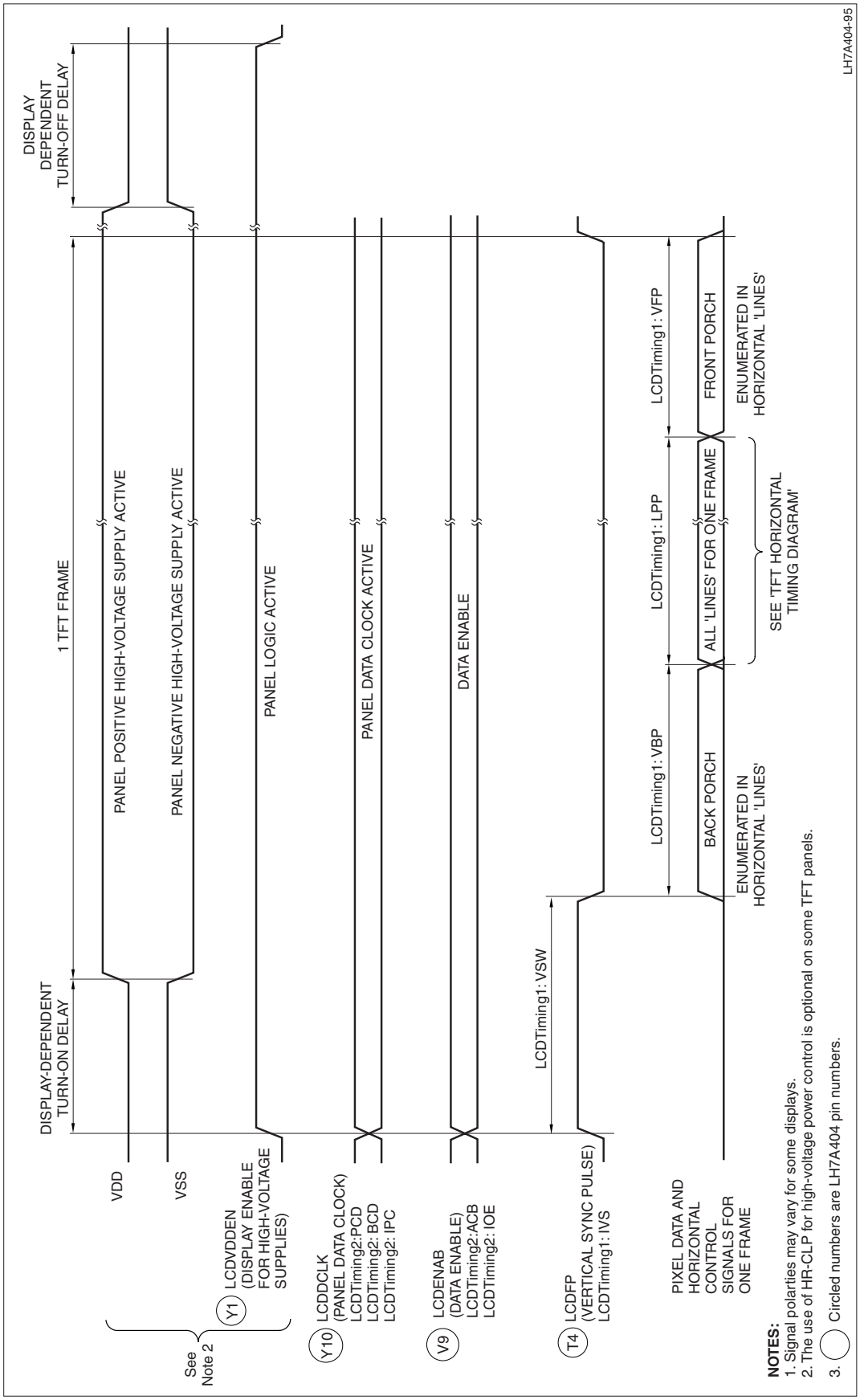


Figure 45. TFT Vertical Timing

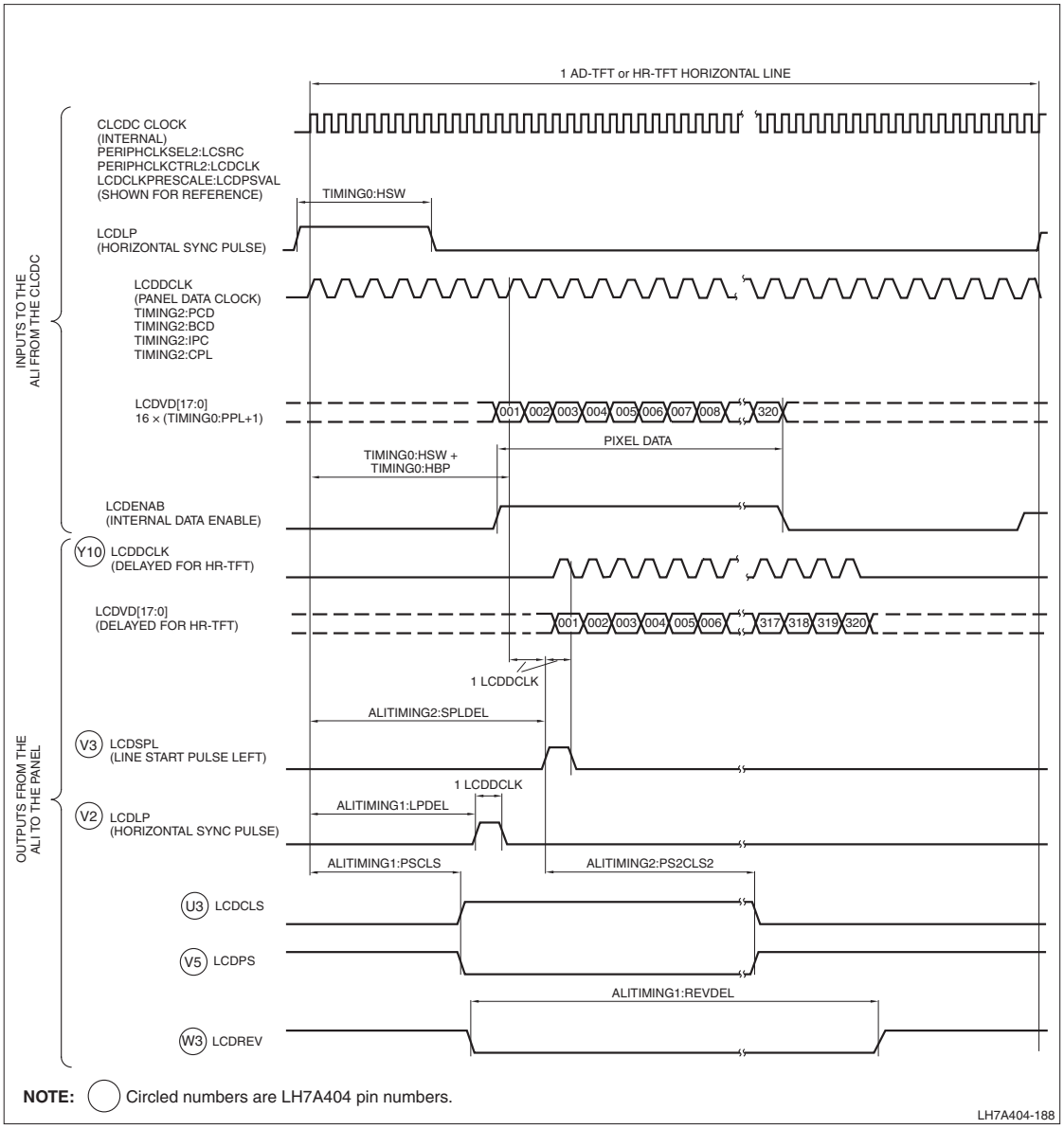


Figure 46. AD-TFT and HR-TFT Horizontal Timing

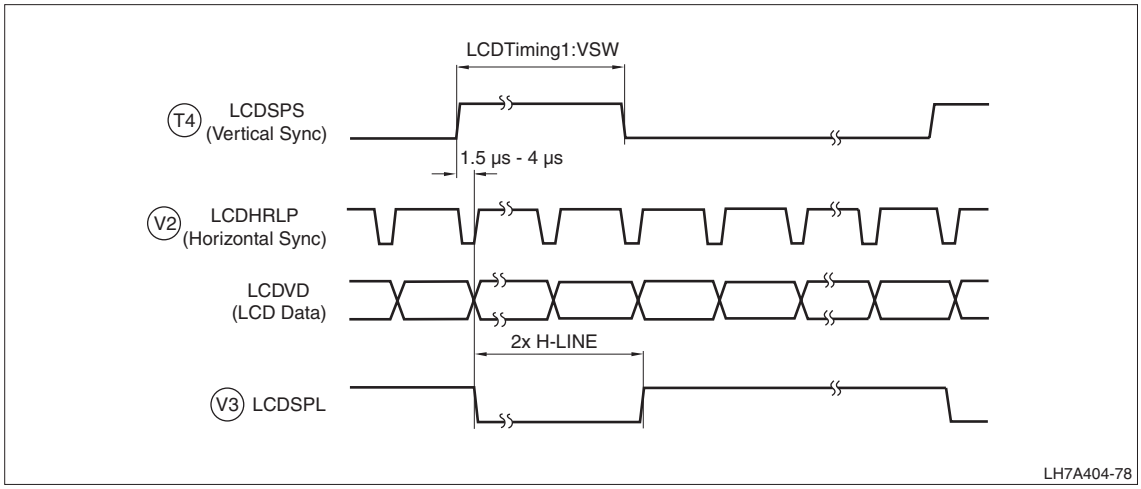


Figure 47. AD-TFT and HR-TFT Timing

Clock and State Controller (CSC) Waveforms

Figure 48 shows the behavior of the LH7A404 when coming out of Reset or Power-On. Table 13 gives the timing parameters.

At Power-On, nPOR must be held LOW until the 32.768 kHz oscillator is stable, and must be deasserted at least two 1 Hz clock periods before the WAKEUP signal is asserted. Once the 14.7456 MHz oscillator is stable, the PLLs require 250 µs to lock.

On transition from Standby to Run (including a Cold Boot), the Wakeup pin must not be asserted for two 1 Hz clock periods after assertion of nPOR to allow time for sampling BATOK and nEXTPWR. The delay prevents a false 'battery good' indication caused by alkaline battery recovery that can immediately follow a battery-low switch off.

nRESETOUT Timing Sequence

Timing for the nRESETOUT sequence is shown for each of the three reset triggers (nPOR, nURESET, and nPWRFL) in Figure 49 through Figure 51, and timing values are presented in Table 14 through Table 16.

Table 13. Reset AC Timing

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT
tOSC32 (32 kHz)	32.768 kHz Oscillator Stabilization Time after Power On*		550	ms
tOSC14 (14 MHz)	14.7456 MHz Oscillator Stabilization Time after WAKEUP		2.5	ms

NOTE: *VDDC = VDDCmin

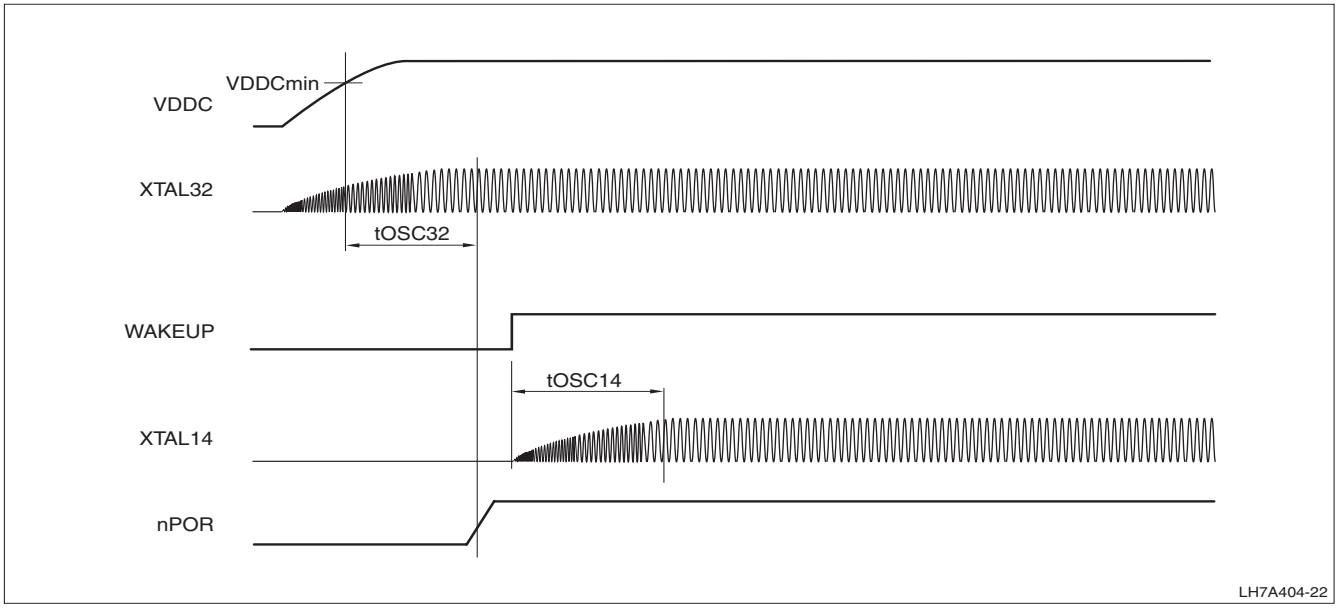


Figure 48. PLL Start-up

NOTE: *The timing relationship is specified as a cycle-based timing. Due to variations in crystal input clock jitter, power rail noise and I/O conditioning these timings will vary marginally. It is recommended that designers

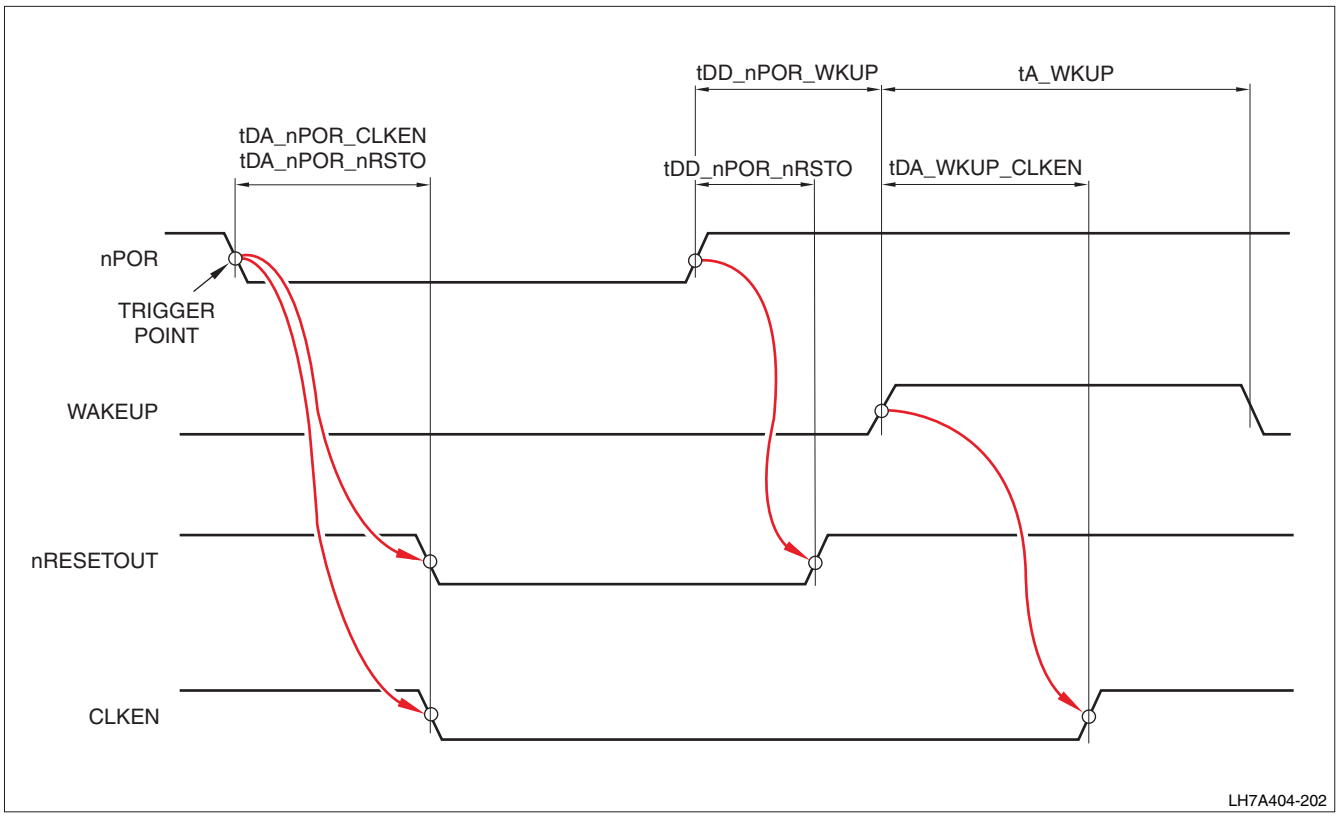


Figure 49. nRESETOUT Timing for nPOR Trigger

Table 14. nRESETOUT Timing Values for nPOR Trigger

SIGNAL	MIN.	TYP.	MAX.	UNITS	DESCRIPTION
tDA_nPOR_nRSTO			30	ns	nPOR to nRESETOUT assertion delay
tDD_nPOR_nRSTO			30	ns	nPOR to nRESETOUT deassertion delay
tDD_nPOR_WKUP	2			1 Hz Periods*	nPOR deassertion to WAKEUP assert delay
tA_WKUP	4			XTAL32 Periods*	WAKEUP assertion time
tDA_nPOR_CLKEN			30	ns	nURESET assertion to CLKEN deassertion delay
tDA_WKUP_CLKEN	2		4	XTAL32 Periods*	WAKEUP to CLKEN assertion delay

add some timing margin to avoid any possible corner case condition.

NOTE: ***The timing relationship is specified as a cycle-based timing. Due to variations in crystal input clock jitter, power rail noise and I/O conditioning these timings will vary marginally. It is recommended that designers

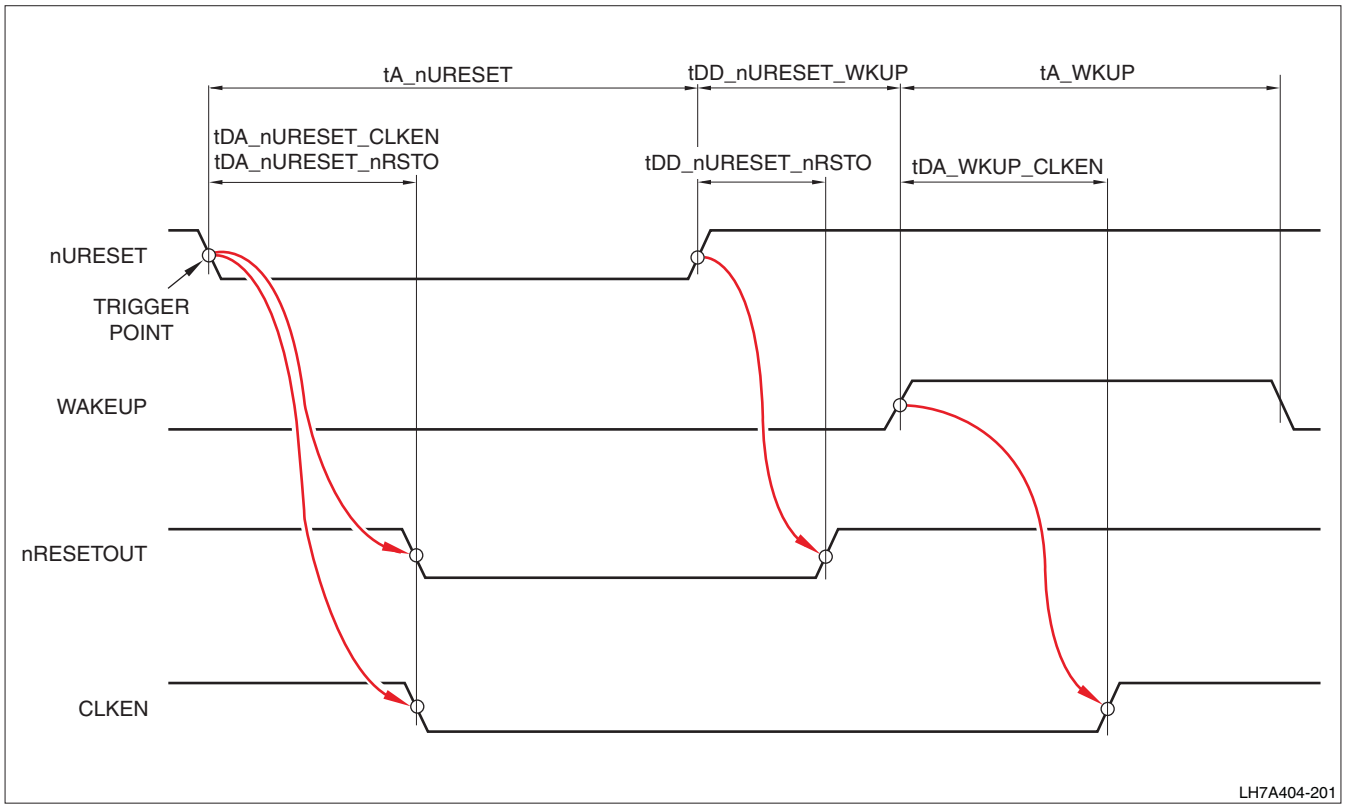


Figure 50. nRESETOUT Timing for nURESET Trigger

Table 15. nRESETOUT Timing Values for nURESET Trigger

SIGNAL	MIN.	TYP.	MAX.	UNITS	DESCRIPTION
tDA_nURESET_nRSTO	2		4	XTAL32 Periods*	nURESET to nRESETOUT assertion delay
tDD_nURESET_nRSTO	0		2	XTAL32 Periods*	nURESET to nRESETOUT deassertion delay
tA_nURESET	4			XTAL32 Periods*	nURESET assertion time
tDD_nURESET_WKUP	2			XTAL32 Periods*	nURESET deassertion to WAKEUP assertion delay
tA_WKUP	4			XTAL32 Periods*	WAKEUP assertion time
tDA_nURESET_CLKEN	2		4	XTAL32 Periods*	nURESET assertion to CLKEN deassertion delay
tDA_WKUP_CLKEN	2		4	XTAL32 Periods*	WAKEUP to CLKEN assertion delay

add some timing margin to avoid any possible corner case condition.

NOTE: *The timing relationship is specified as a cycle-based timing. Due to variations in crystal input clock jitter, power rail noise and I/O conditioning these timings will vary marginally. It is recommended that designers

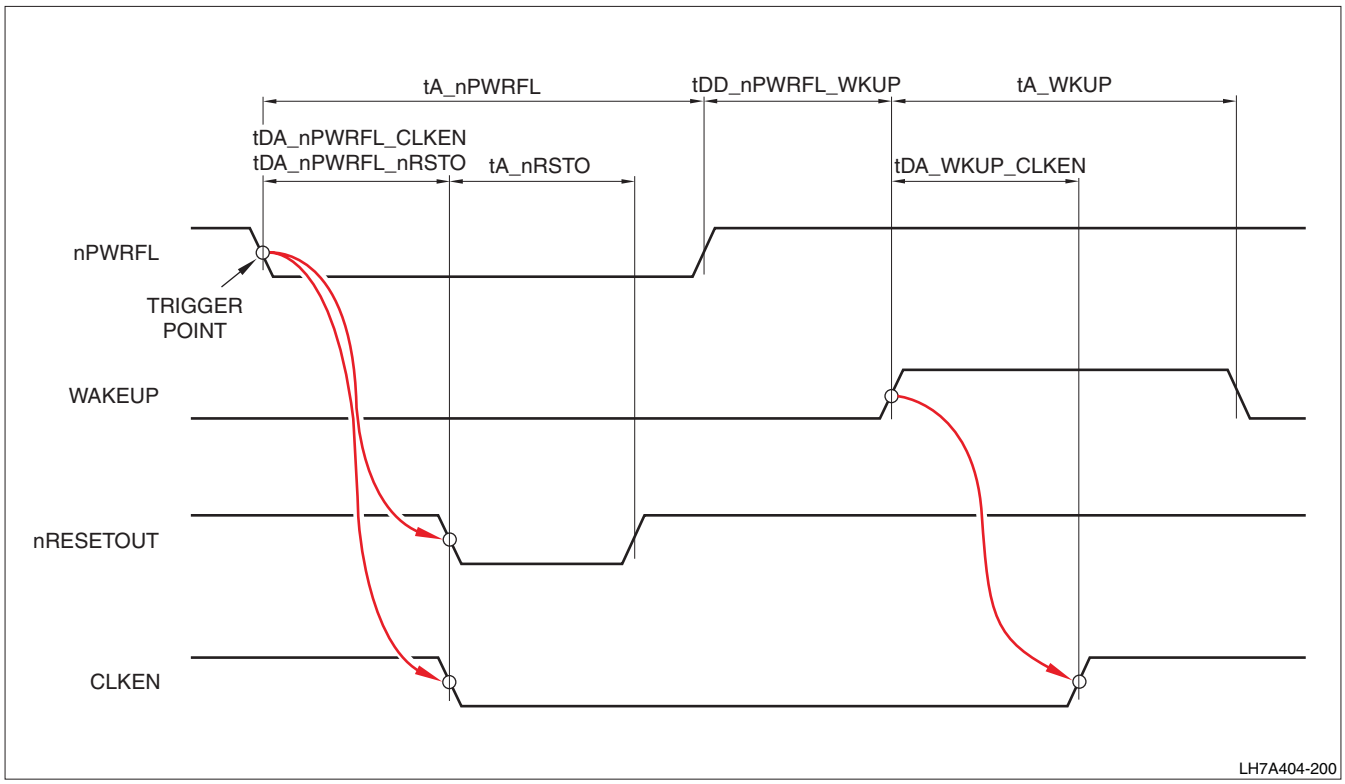


Figure 51. nRESETOUT Timing for nPWRFL Trigger

Table 16. nRESETOUT Timing Values for nPWRFL Trigger

SIGNAL	MIN.	TYP.	MAX.	UNITS*	DESCRIPTION
tDA_nPWRFL_nRSTO	2		4	XTAL32 Periods	nPWRFL to nRESETOUT assertion delay
tA_nRSTO		2		XTAL32 Periods	nRESETOUT assertion time
tA_nPWRFL	4			XTAL32 Periods	nPWRFL assertion time
tDD_nPWRFL_WKUP	2			1 Hz Periods	nPWRFL deassertion to WAKEUP assertion delay
tA_WKUP	4			XTAL32 Periods	WAKEUP assertion time
tDA_nPWRFL_CLKEN	2		4	XTAL32 Periods	nPWRFL assertion to CLKEN deassertion delay
tDA_WKUP_CLKEN	2		4	XTAL32 Periods	WAKEUP to CLKEN assertion delay

add some timing margin to avoid any possible corner case condition.

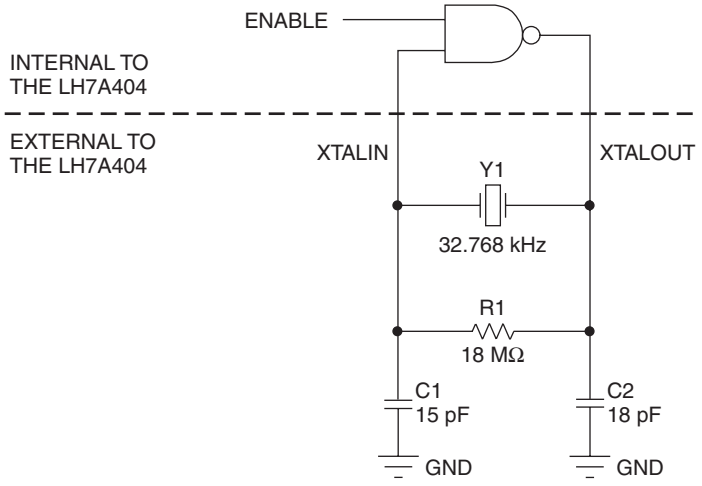
Reference Oscillator Circuit Design

Figure 52 and Figure 53 show a reference oscillator design for both the 32.768 kHz and 14.7456 MHz clocks.

Low Operating Temperatures and Noise Immunity

The junction temperature, Tj, is the operating temperature of the transistors in the integrated circuit. The switching speed of the CMOS circuitry within the SoC depends partly on Tj, and the lower the operating temperature, the faster the CMOS circuits will switch. Increased switching noise generated by faster switching circuits could affect the overall system stability. The amount of switching noise is directly affected by the application executed on the SoC.

NXP suggests that users implementing a system to meet the full –40°C to +85°C specification use an external oscillator rather than a crystal to drive the system clock input of the System-on-Chip. This change from crystal to oscillator will increase the robustness (ie, noise immunity of the clock input to the SoC).



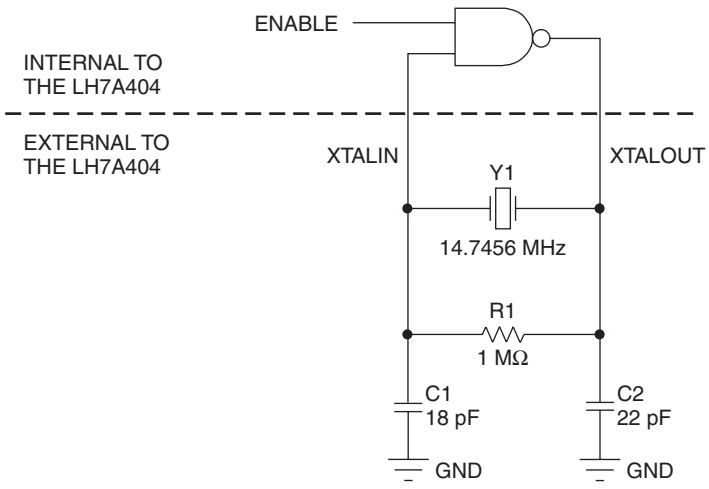
NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 12.5 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

REFERENCE CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
32.768 kHz Crystal	Parallel Mode
Tolerance	±30 ppm
Aging	±3 ppm
Load Capacitance	12.5 pF
ESR (MAX.)	50 kΩ
Drive Level	1.0 µW (MAX.)
Reference crystal	MTRON SX1555 or equivalent

LH7A404-168

Figure 52. 32.768 kHz External Oscillator Components and Schematic



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

REFERENCE CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
14.7456 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 µW (MAX.)
Reference crystal	MTRON SX2050 or equivalent

LH7A404-167

Figure 53. 14.7456 MHz External Oscillator Components and Schematic

Printed Circuit Board Layout Practices

LH7A404 POWER SUPPLY DECOUPLING

The LH7A404 has separate power and ground pins for different internal circuitry sections. The VDD and VSS pins supply power to I/O buffers, while VDDC and VSSC supply power to the core logic, and VDDA/VSSA supply analog power to the PLLs.

Each of the VDD and VDDC pins must be provided with a low impedance path to the corresponding board power supply. Likewise, the VSS and VSSC pins must be provided with a low impedance path to the board ground.

Each power supply must be decoupled to ground using at least one 0.1 µF high frequency capacitor located as close as possible to a VDDx-VSSx pin pair on each of the four sides of the chip. If room on the circuit board allows, add one 0.01 µF high frequency capacitor near each VDDx-VSSx pair on the chip.

To be effective, the capacitor leads and associated circuit board traces connecting to the chip VDDx-VSSx pins must be kept to less than half an inch (12.7 mm) per capacitor lead. There must be one bulk 10 µF capacitor for each power supply placed near one side of the chip.

REFERENCE PLL, VDDA, VSSA FILTER

The VDDA pins supply power to the chip PLL circuitry. VSSA is the ground return path for the PLL circuit. NXP recommends a low-pass filter attached as shown in Figure 54. The values of the inductor and capacitors are not critical. The low-pass filter prevents high frequency noise from adversely affecting the PLL circuits. The distance from the IC pin to the high frequency capacitor should be as short as possible.

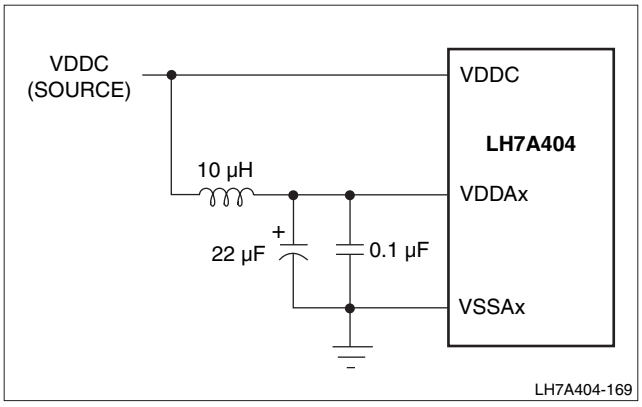


Figure 54. VDDA, VSSA Filter Circuit

UNUSED INPUT SIGNAL CONDITIONING

Floating input signals can cause excessive power consumption. Unused inputs without internal pull-up or pull-down resistors should be pulled up or down externally, to tie the signal to its inactive state. NXP recommends using no larger than 33 kΩ.

Some GPIO signals may default to inputs. If the pins that carry these signals are unused, software can program these signals as outputs, eliminating the need for pull-ups or pull-downs. Power consumption may be higher than expected until software completes programming the GPIO. Some LH7A404 inputs have internal pull-ups or pull-downs. If unused, these inputs do not require external conditioning.

OTHER CIRCUIT BOARD LAYOUT PRACTICES

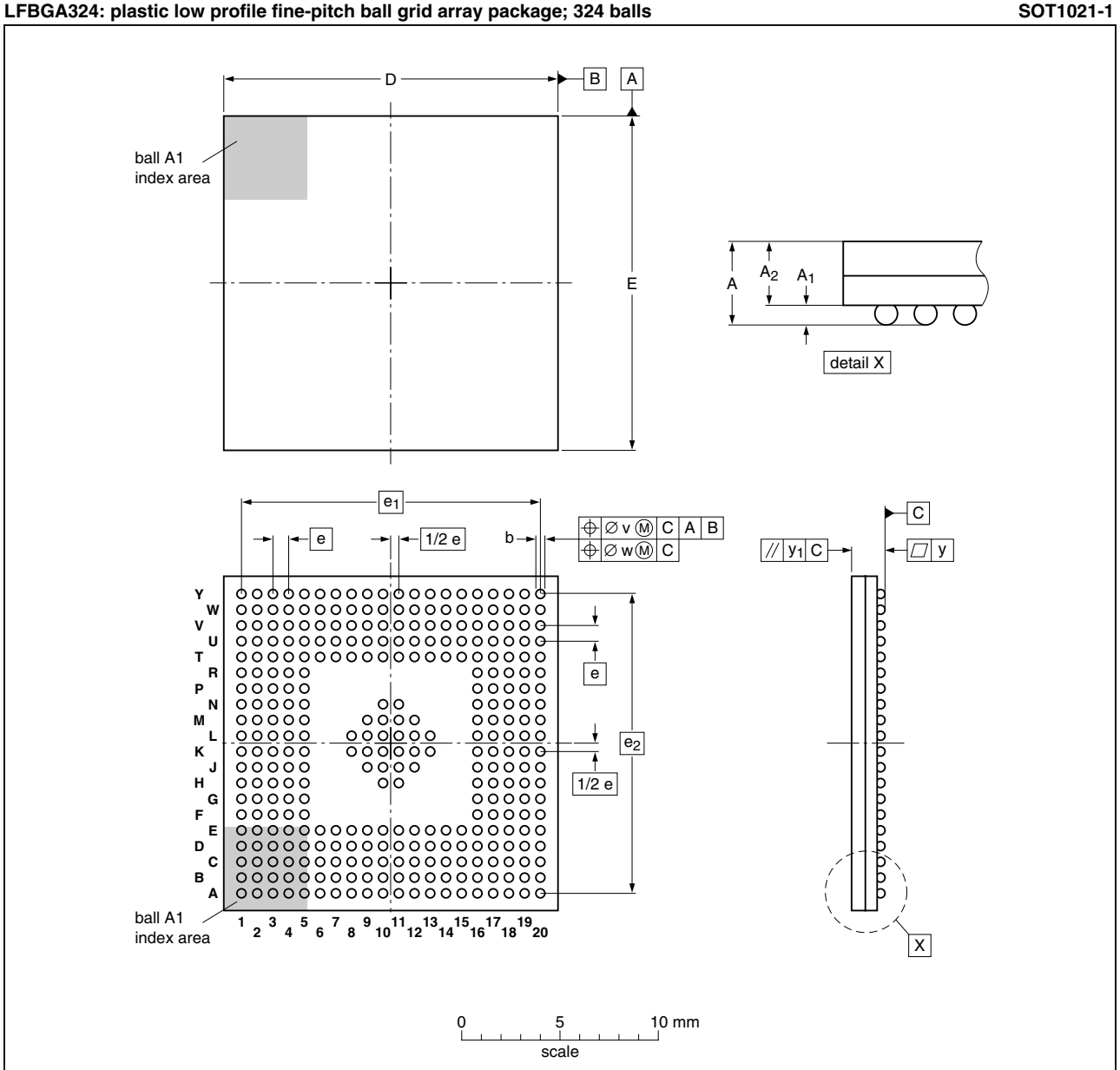
All outputs have fast rise and fall times. Printed circuit trace interconnection length must therefore be reduced to minimize overshoot, undershoot and reflections caused by transmission line effects of these fast output switching times. This recommendation particularly applies to the address and data buses.

When considering capacitance, calculations must consider all device loads and capacitances due to the circuit board traces. Capacitance due to the traces will depend upon a number of factors, including the trace width, dielectric material the circuit board is made from and proximity to ground and power planes.

Attention to power supply decoupling and printed circuit board layout becomes more critical in systems with higher capacitive loads. As these capacitive loads increase, transient currents in the power supply and ground return paths also increase.

PACKAGE SPECIFICATIONS

LFBGA324: plastic low profile fine-pitch ball grid array package; 324 balls **SOT1021-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.7	0.4 0.3	1.35 1.15	0.5 0.4	17.1 16.9	17.1 16.9	0.8	15.2	15.2	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1021-1						

Figure 55. Package outline SOT1021-1 (LFBGA324)

REVISION HISTORY

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LH7A404_N_1	20070716	Preliminary data sheet	-	LH7A404 V1-5 12-1-2006
Modifications: • First NXP version based on the LH7A404 data sheet of 20061201				

1. Legal information

1.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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