LH52B256LL

PRELIMINARY

CMOS 32K × 8 Static RAM

FEATURES

- Access Times: 70/100 ns
- Automatic Power Down During Long Read Cycles
- Low-Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully-Static Operation
- 2 V Data Retention
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 600-mil DIP
  28-Pin, 450-mil SOP
  28-Pin, 8 × 13 mm^2 TSOP (Type I)

FUNCTIONAL DESCRIPTION

The LH52B256LL is a high-density 262,144 bit static RAM organized as 32K × 8. An efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address. An Automatic Power Down feature decreases current consumption when Read cycles extend beyond their minimum cycle time.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

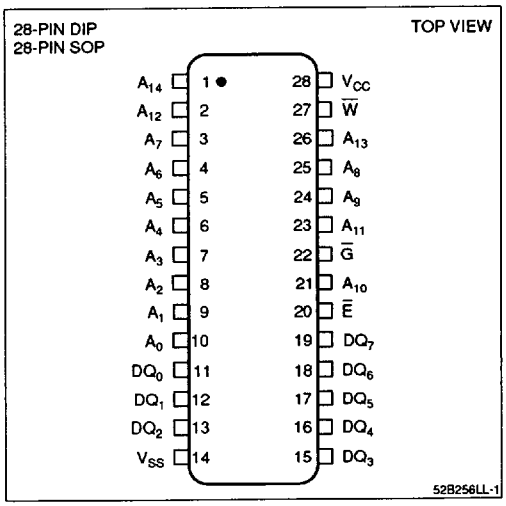
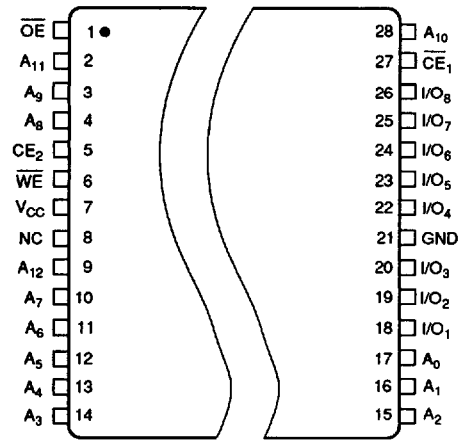


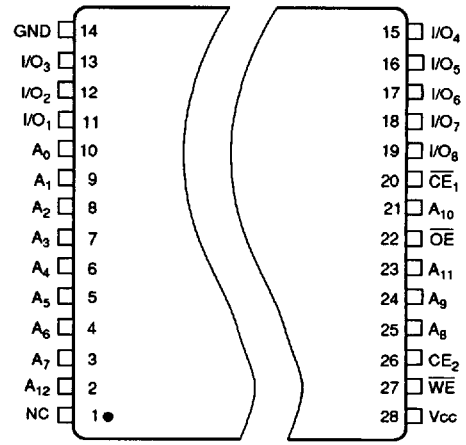
Figure 1. Pin Connections for DIP and SOP Packages

SHARP CORP 61E D 8180798 0009758 729 SRPJ

28-PIN TSOP (I) (NORMAL BEND)



28-PIN TSOP (I) (REVERSE BEND)



52B256LL-2

Figure 2. Pin Connections for TSOP Packages

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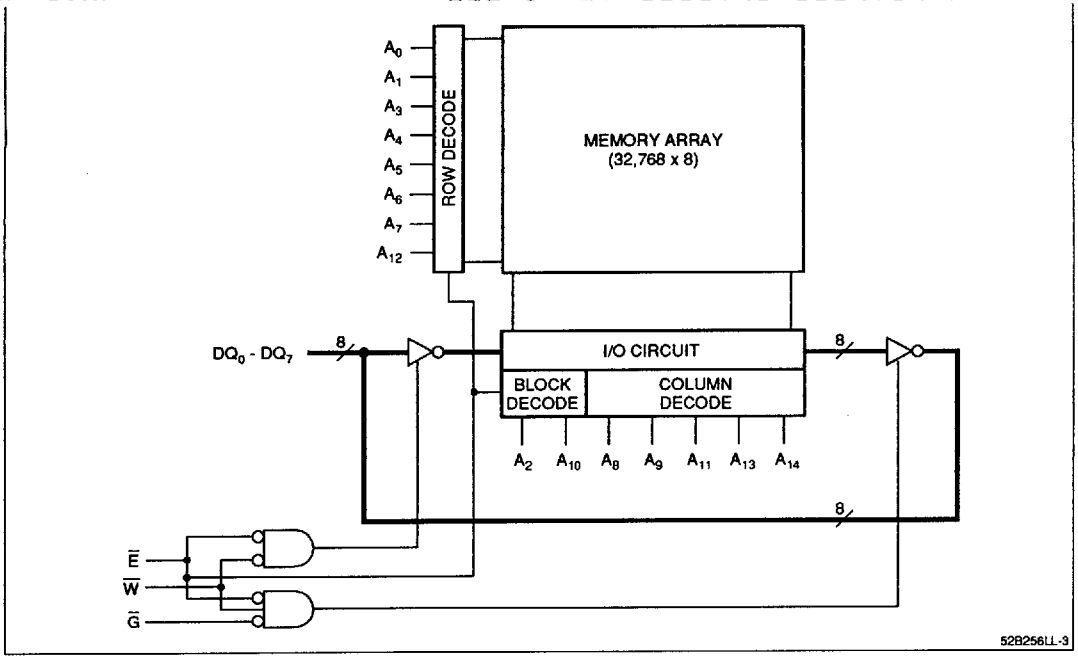


Figure 3. LH52B256LL Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Standby	High-Z	Standby
L	H	H	Read	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

SHARP CORP 61E D 8180798 0009760 387 SRPJ

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{RC} = 70 ns			70	mA
I_{CC1}	Operating Current [1]	t_{RC} = 100 ns			70	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V			40	µA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−1		1	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−1		1	µA
V_{OH}	Output High Voltage	I_{OH} = −1.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	VCC = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V		6	20	µA

NOTE:

1. Icc is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	0.6 to 2.4 V
Input Rise and Fall Times	10 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

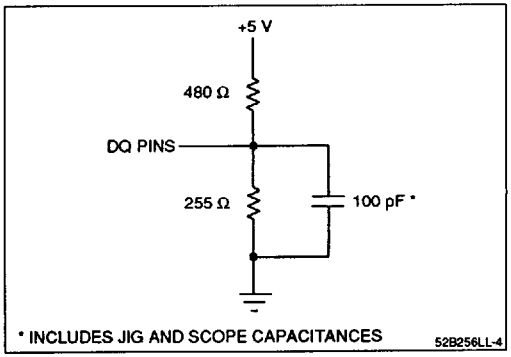


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	10 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are 'Don't Care.'

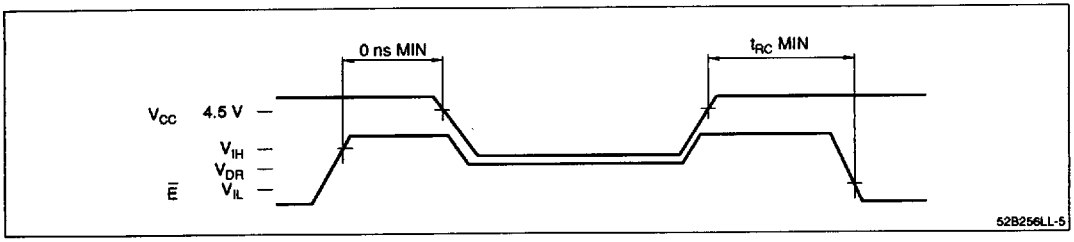


Figure 5. Data Retention Timing

SHARP CORP 61E D 8180798 0009762 15T SRPJ

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-70		-10		UNITS
		MIN	MAX	MIN	MAX	
	READ CYCLE					
t_{RC}	Read Cycle Time	70		100		ns
t_{AA}	Address Access Time		70		100	ns
t_{OH}	Output Hold from Address Change	10		10		ns
t_{EA}	$\overline{E}$ Low to Valid Data		70		100	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	10		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]	0	35	0	45	ns
t_{GA}	$\overline{G}$ Low to Valid Data		40		60	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	5		5		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	35	0	45	ns
	WRITE CYCLE					
t_{WC}	Write Cycle Time	70		100		ns
t_{EW}	$\overline{E}$ Low to End of Write	60		65		ns
t_{AW}	Address Valid to End of Write	60		90		ns
t_{AS}	Address Setup	0		0		ns
t_{WR}	Address Hold from End of Write	0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	55		65		ns
t_{DW}	Input Data Setup Time	30		35		ns
t_{DH}	Input Data Hold Time	0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]	0	40	0	45	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	5		5		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Sample tested only.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read Cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid Data will be present following t_{GA} only if t_{EA} timing is met.

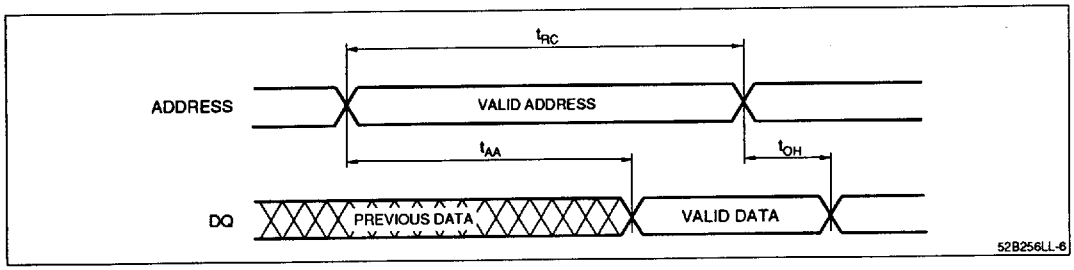


Figure 6. Read Cycle No. 1

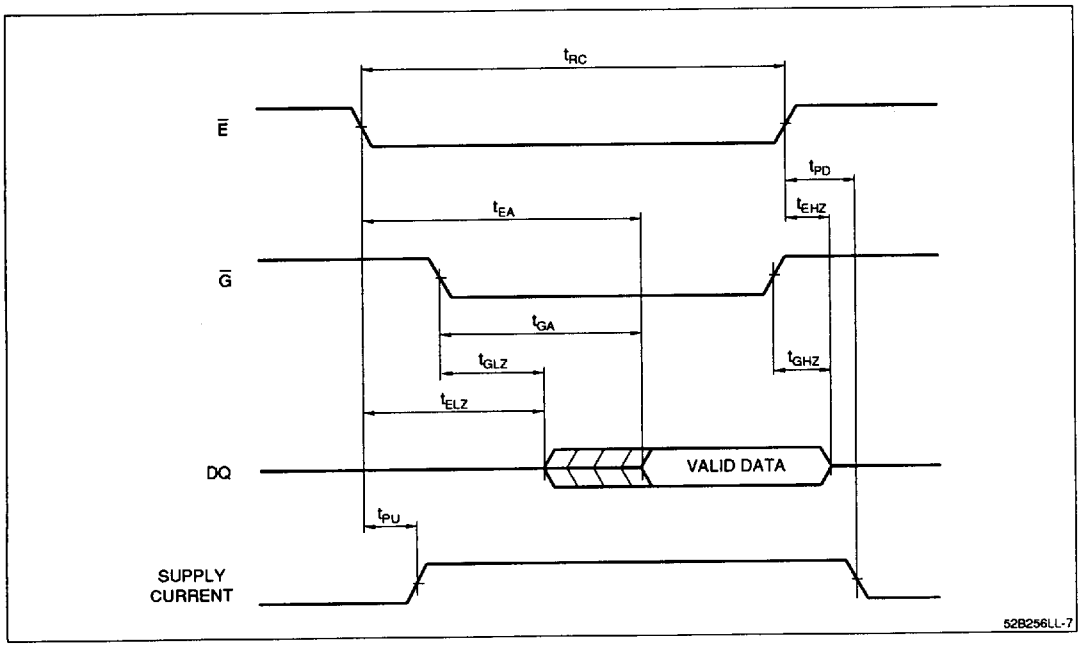


Figure 7. Read Cycle No. 2

SHARP CORP 61E D 8180798 0009763 096 SRPJ

SHARP CORP 61E D 8180798 0009764 T22 SRPJ

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write Cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52B256LL's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 (W Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write Cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

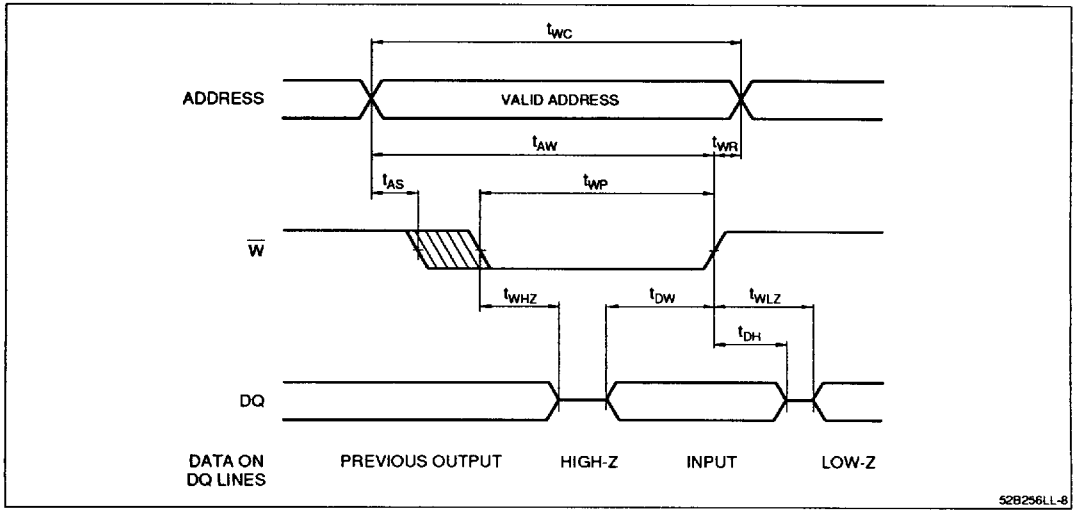


Figure 8. Write Cycle No. 1

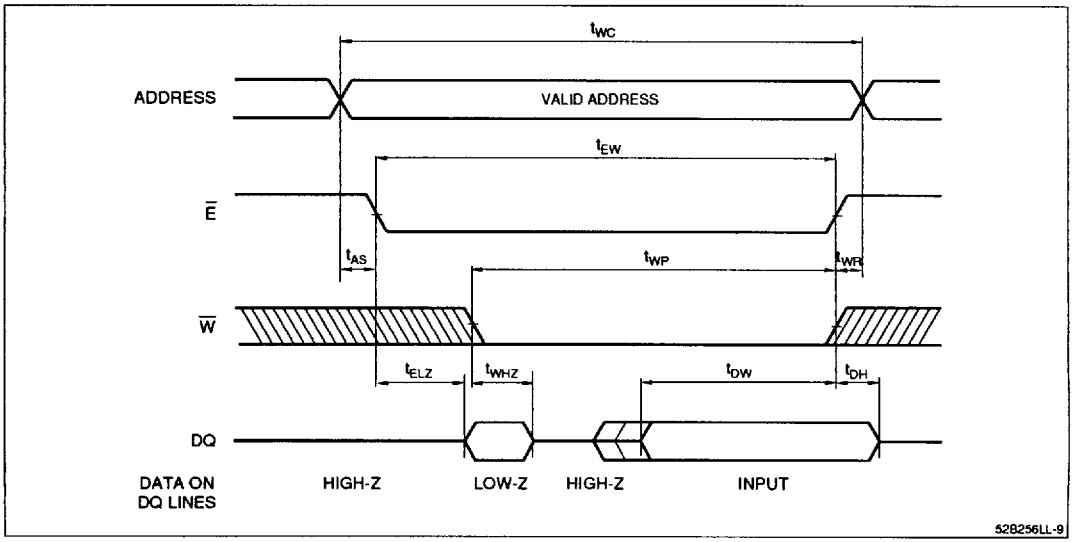
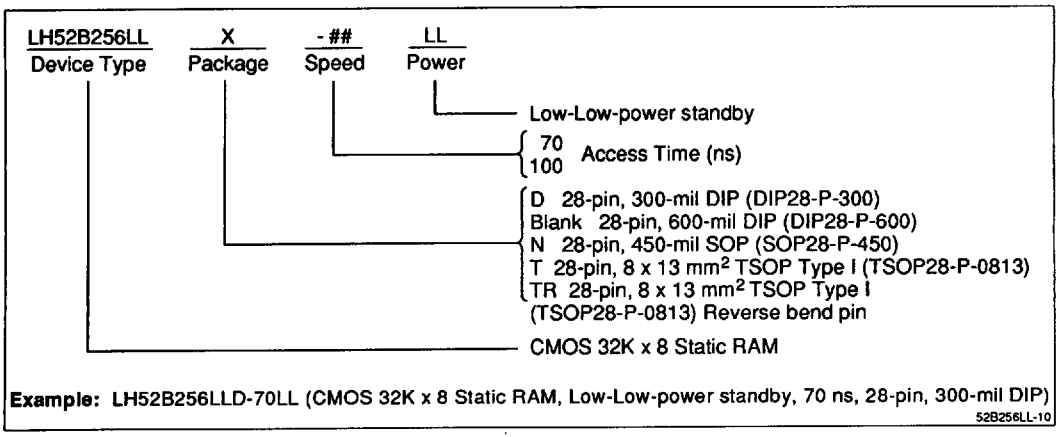


Figure 9. Write Cycle No. 2

SHARP CORP 61E D 8180798 0009765 969 SRPJ

ORDERING INFORMATION



Example: LH52B256LLD-70LL (CMOS 32K x 8 Static RAM, Low-Low-power standby, 70 ns, 28-pin, 300-mil DIP)

52B256LL-10