LF2301
Image Resampling Sequencer

FEATURES

- 40 MHz Clock Rate
- High-Speed Image Manipulation
- Maximum Image Size: 4096 x 4096 Pixels
- Supports Following Interpolation Algorithms:
  - Nearest-Neighbor
  - Bilinear Interpolation
  - Cubic Convolution
- Applications:
  - Video Special-Effects
  - Image Recognition
  - High-Speed Data Encoding/ Decoding
- Replaces TRW/Raytheon/Fairchild TMC2301
- 68-pin PLCC, J-Lead

DESCRIPTION

The **LF2301** is a self-sequencing address generator designed to filter a two-dimensional image or remap and resample it from one set of Cartesian coordinates (x,y) into a new set (u,v).

The LF2301 can resample digitized images or perform such manipulations as rotation, panning, zooming, and warping as well as compression in real-time.

By using two LF2301s in a Image Transformation System (ITS), nearest-neighbor, bilinear interpolation, and cubic convolution algorithms, with kernel sizes up to 4 x 4 pixels, are all possible (see Figure 1). This system can also implement simple static filters with kernel sizes up to 16 x 16 pixels.

DETAILS OF OPERATION

Most video applications use a pair of LF2301s in tandem to construct an ITS. One LF2301 is the row coordinate generator (x to u) and the other is the column generator (y to v). External RAM is needed for storage of the interpolation coefficient lookup table, as well as for buffers of the source and destination images. An external Multiplier-Accumulator is required when performing interpolation or implementing static filters.

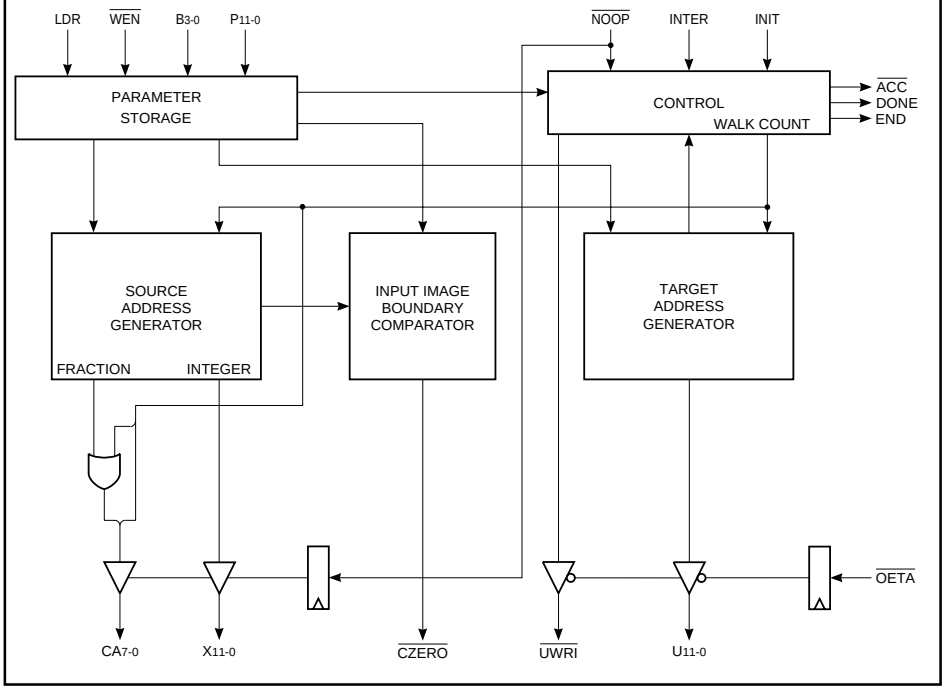
The ITS is capable of performing the general second-order coordinate transformation of the form:

$$x(u,v) = Au^2+Bu+Cuv+Dv^2+Ev+F$$

$$y(u,v) = Gu^2+Hu+Kuv+Lv^2+Mv+N$$

where parameters A through N of the transform are user-defined. The system steps sequentially through each pixel in the "target" image lying within a user-defined rectangle. For each "target" pixel at (u,v), the LF2301 points to a corresponding "source" pixel at (x,y).

LF2301 BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

Vcc and GND

+5V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

P11-0 — Parameter Register Data Input

P11-0 is the 12-bit Parameter Register Data input port. P11-0 is latched on the rising edge of CLK.

B3-0 — Parameter Register Address Input

B3-0 is the 4-bit Parameter Register Address input port. B3-0 is latched on the rising edge of CLK.

Outputs

X11-0 — Source Address Output

X11-0 is the 12-bit registered Source Address output port.

CA7-0 — Coefficient Address Output

CA7-0 is the 8-bit registered Coefficient Address output port.

U11-0 — Target Address Output

U11-0 is the 12-bit registered Target Address output port.

Controls

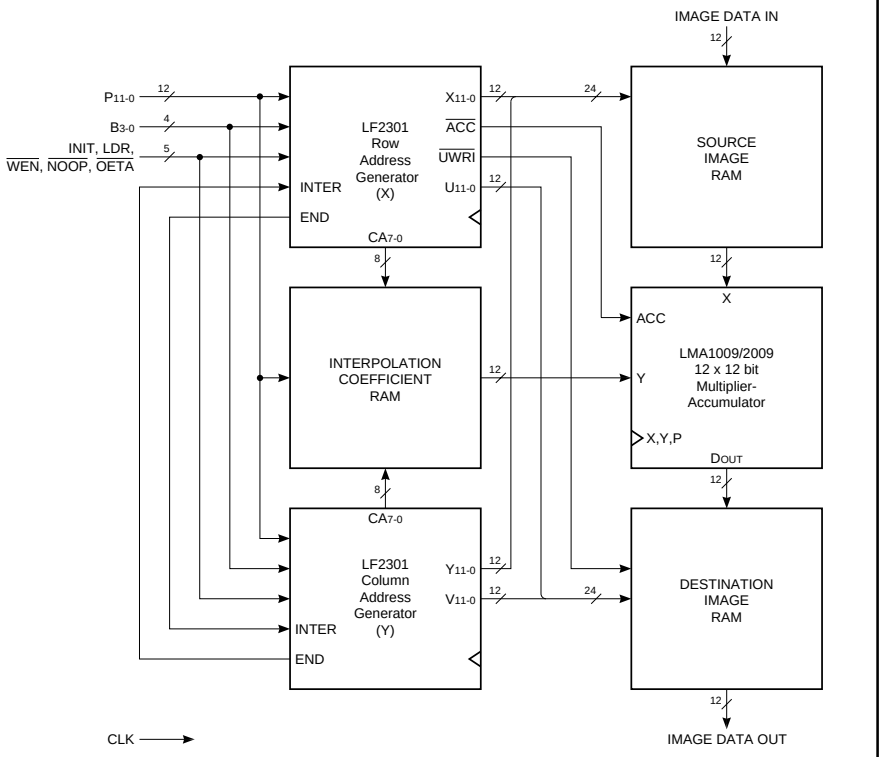
INIT — Initialize

When INIT is HIGH for a minimum of two clock cycles, the control logic is cleared and initialized for the start of a new image transformation. When INIT goes LOW, normal operation begins after two clock cycles. INIT is latched on the rising edge of CLK.

$\overline{WEN}$ — Write Enable

When $\overline{WEN}$ is LOW, data latched into the device on P11-0 is loaded into the preload register addressed by the data latched into the device on B3-0. When $\overline{WEN}$ is HIGH, data cannot be loaded into the preload registers and their contents will not be changed. $\overline{WEN}$ is latched on the rising edge of CLK.

FIGURE 1. IMAGE TRANSFORMATION SYSTEM (ITS)



LDR — Load Data Register

When LDR is HIGH, data in all preload registers is latched into the Transformation Parameter Registers. When LDR is LOW, data cannot be loaded into the Transformation Parameter Registers and their contents will not be changed. LDR is latched on the rising edge of CLK.

$\overline{ACC}$ — Accumulate

The registered $\overline{ACC}$ output initializes the accumulation register of the external multiplier-accumulator. At the start of each interpolation "walk," $\overline{ACC}$ goes LOW for one cycle effectively clearing the storage register by loading in only the new first product. $\overline{ACC}$ from either the row or column LF2301 may be used.

$\overline{UWRI}$ — Target Memory Write Enable

The Target Memory Write Enable goes LOW for one clock cycle after the end of each interpolation "walk." When $\overline{OETA}$ is HIGH, this registered output is forced to the high-impedance state. $\overline{UWRI}$ from either the row or column LF2301 may be used.

INTER — Interconnect

When two LF2301s are used to form an ITS, the END flag on each device is connected to INTER on the other device. The END flag from the row device indicates an "end of line" to the column device. The END flag from the column device indicates a "bottom of frame" to the row device, forcing a reset of the address counter.

$\overline{NOOP}$ — No Operation

When $\overline{NOOP}$ is LOW, the clock is overridden holding all address generators in their current state. X11-0 and CA7-0 are forced to the high-

impedance state. Users may then access external memory. Normal operation resumes on the next clock cycle after $\overline{NOOP}$ goes HIGH. $\overline{NOOP}$ is latched on the rising edge of CLK.

$\overline{OETA}$ — Target Memory Output Enable

When $\overline{OETA}$ is HIGH, $\overline{UWRI}$ and U_{11-0} are forced to the high-impedance state. When $\overline{OETA}$ is $\overline{LOW}$, UWRI and U_{11-0} are enabled on the next clock cycle. $\overline{OETA}$ is latched on the rising edge of CLK.

Flags

$\overline{CZERO}$ — Coefficient Zero

If in a row device x<0, XMIN≤x≤XMAX, or x≥4096, the registered $\overline{CZERO}$ flag goes HIGH . If 0≤x<XMIN or XMAX<x<4096, $\overline{CZERO}$ goes LOW. In an ITS, when the source address falls outside a rectangle with vertices (XMIN, YMIN), (XMAX, YMIN), (XMIN, YMAX), and (XMAX, YMAX), the logical AND of the $\overline{CZERO}$ flags from the row and column of the LF2301s will go LOW representing an invalid address.

END — End of Row/Frame

When two LF2301s are used to form an ITS, the END flag on each device is connected to INTER on the other device. The END flag from the row device indicates an "end of line" to the column device. The END flag from the column device indicates a "bottom of frame" to the row device, forcing a reset of the address counter.

When Mode is set to "00" or "10" END goes HIGH on the row device for (K+1) x (K+1) clock cycles starting[2 x (K+1) x (K+1)] + 1 clock cycles before the last X address of a row. END goes HIGH on the column device for $(K+1)^3$ x (UMAX-UMIN) clock cycles starting at $(K+1)^3$ x (UMAX-UMIN) + 1 clock cycles before the last X address of a frame.

When Mode is set to "01" or "11" END goes HIGH on the row device for K+1 clock cycles starting at (K+1) + 2 clock cycles before the last X address of a row. END goes HIGH on the column device for (K+1) x (K+1) clock cycles starting at [(K+1) x (K+1)] + 1 clock cycles before the last X address of a frame.

DONE — End of Transform

In a two LF2301 system, after the last walk of the last row of an image, the registered DONE flag goes HIGH indicating the end of the transform. DONE goes HIGH one clock cycle before the last X address of a frame. If AIN is HIGH, DONE will remain HIGH for one clock cycle. If AIN is LOW, DONE will remain HIGH until a new transform begins.

Transformation Control Parameters

XMIN, XMAX, YMIN, YMAX

XMIN, XMAX, YMIN, YMAX define the valid area in the source image from which pixels may be read. The $\overline{CZERO}$ flags will denote a valid memory read whenever the LF2301s generate an (x,y) address within this boundary.

UMIN, UMAX, VMIN, VMAX

UMIN, UMAX, VMIN, VMAX define the area in the destination image into which pixels will be written. (UMIN, VMIN) is the top left corner and (UMAX + 1, VMAX) is the bottom right corner. The following conditions must be met: UMAX>UMIN and VMAX>VMIN.

x_0, y_0

x_0, y_0 determine what the first pixel read out of the source image will be at the beginning of an image transformation. x_0, y_0 will be the upper left corner of the original image in non-inverting, non-reversing applications.

dx/du

dx/du is the displacement along the x axis corresponding to a one-pixel movement along the u axis.

dx/dv

dx/dv is the displacement along the x axis corresponding to each one-pixel movement along the v axis.

dy/du

dy/du is the displacement along the y axis corresponding to each one-pixel movement along the u axis.

dy/dv

dy/dv is the displacement along the y axis corresponding to each one-pixel movement along the v axis.

d^2x/du^2

d^2x/du^2 determines the rate of change of dx/du with each step along a line in the output image.

d^2x/dv^2

d^2x/dv^2 determines the rate of change of dx/dv with each step down a column in the output image.

d^2y/du^2

d^2y/du^2 determines the rate of change of dy/du with each step along a line in the output image.

d^2y/dv^2

d^2y/dv^2 determines the rate of change of dy/dv with each step down a column in the output image.

$d^2x/dudv$

$d^2x/dudv$ determines the rate of change of dx/du while moving vertically through the output image. $d^2x/dudv$ also determines the rate of change of dx/dv while moving horizontally through the output image.

$d^2y/dudv$

$d^2y/dudv$ determines the rate of change of dy/dv while moving horizontally through the output image. $d^2y/dudv$ also determines the rate of change of dy/du while moving vertically through the output image.

TABLE 1. MODE SELECTION		
M_1	M_0	MODE
0	0	single-pass operation (CW)
0	1	pass 1 of two-pass operation
1	0	single-pass operation (CCW)
1	1	pass 2 of two-pass operation

R/C — Row/Column Select

When set to 0, the LF2301 functions as a row device. When set to 1, the LF2301 functions as a column device.

M_{1-0} — Mode

This 2-bit control word defines four modes as follows (see table 1):

The 1st and 3rd modes are single-pass operations where the device walks through a (K + 1) x (K + 1) kernel for each output pixel. K is the kernel size determined by K_{3-0} in Parameter Register 7. In mode 00, the spiral walk is in the clockwise direction. In mode 10, the spiral walk is in the counter clockwise direction.

The 2nd and 4th modes are used together to perform a two-pass operation. The first pass (mode 01) performs a (K+1) kernel in the horizontal dimension. The second pass (mode 11) performs a (K+1) kernel in the vertical dimension.

The result of pass 1 is stored in the destination image memory and is used as the source image data for the second pass. A system to switch source and destination memory banks could be designed, or utilization of a second LF2301 pair in a pipelined architecture could be used. In this case, the system would require a third image buffer for the final destination image.

K_{3-0} — Kernel

Kernel determines the length of the spiral walk when performing image transformations and the size of the filter when implementing static filters (see table 2). When performing image transformations, the longest spiral walk possible is 4 x 4 pixels (Kernel = 3). For static filters, kernels of up to 16 x 16 pixels (Kernel = 15) are possible.

FOV — Field of View

FOV determines the distance between pixels in a spiral walk. An FOV of 1 means each step in a spiral walk is one pixel. An FOV of 2 means each step is two pixels, and so on. FOV can be set as high as 7 (see Table 3). It is important to note when FOV is 0, the x and y addresses will not change during a spiral walk. They will remain fixed at the first pixel address of the spiral walk.

ALR — Autoload

When set HIGH and upon INIT being strobed, the LDR control is automatically asserted which causes the data currently stored in the Preload Registers to be loaded into the Transformation Parameter Registers.

AIN — Autoinit

A new transform automatically begins if the AIN bit is HIGH when the end of an image is reached. The DONE flag will go HIGH for one clock cycle. If AIN is LOW, $\overline{\text{UWRI}}$ and the DONE flag remain HIGH until the user strobes the INIT control to begin a new image transformation.

PIPE — Pipe Control

In order to compensate for buffered source image RAM, PIPE adjusts the timing of $\overline{\text{UWRI}}$ and $\overline{\text{ACC}}$. If the PIPE bit is HIGH, $\overline{\text{UWRI}}$ and $\overline{\text{ACC}}$ will have a one clock cycle delay added relative to the generation of the target address.

TM — Test Mode

Calculations of the source image and coefficient addresses are made by an internal 28-bit accumulator. TM allows access to the sign bit and the seven bits below the four coefficient address bits in the accumulator. When TM is HIGH the sign bit and 11 bits below the source image address are fed to X_{11-0} (see Figure 2). When TM is LOW, the source image address is fed to X_{11-0}. Two clock cycles are required to access both the MS and LS words of the internal accumulator.

Functional Description

The LF2301 is an address generator designed to be used in an image transformation system (ITS). When implementing an LF2301-based ITS, second-order image transformations can be performed like resampling, rotation, warping, panning, and rescaling, all at real-time video rates. 2D filtering operations, like pixel convolutions, can also be performed.

In most applications two LF2301s are used, one to generate the row addresses and the other to generate the column

TABLE 2. KERNEL				
K_3	K_2	K_1	K_0	Kernel
0	0	0	0	1 x 1
0	0	0	1	2 x 2
0	0	1	0	3 x 3
0	0	1	1	4 x 4
0	1	0	0	5 x 5
0	1	0	1	6 x 6
0	1	1	0	7 x 7
0	1	1	1	8 x 8
1	0	0	0	9 x 9
1	0	0	1	10 x 10
1	0	1	0	11 x 11
1	0	1	1	12 x 12
1	1	0	0	13 x 13
1	1	0	1	14 x 14
1	1	1	0	15 x 15
1	1	1	1	16 x 16

TABLE 3. FIELD OF VIEW			
F_2	F_1	F_0	FOV
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

addresses. An example of an ITS implemented with two LF2301s is shown in Figure 1. In this system the following components are used: two LF2301s, a multiplier-accumulator (MAC), interpolation coefficient RAM, and source/target image RAM. Maximum image size is 4096 x 4096 pixels. Data word size is determined by the word size of the external RAM.

A typical ITS performs image transformations as follows:

a. The LF2301s generate sequential pixel addresses (left to right, top to bottom) which fill the rectangle in the target image RAM defined by (UMIN,VMIN) and (UMAX +1, VMAX). It is important to note that the U value of the last pixel address on each line of the target RAM is UMAX + 1.

b. The LF2301s calculate the address of the corresponding pixel in the source image RAM for each target pixel address generated.

c. If interpolation is needed, the external MAC sums the products of the source pixels and the interpolation coefficients. Control signals for the MAC and address signals for the interpolation coefficient RAM are provided by the LF2301s.

d. The new pixel value is written into the target image RAM.

The LF2301s generate source pixel addresses according to the following general second order equations:

$x = Au^2 + Bu + Cuv + Dv^2 + Ev + F$

$y = Gu^2 + Hu + Kuv + Lv^2 + Mv + N$

where (x,y) and (u,v) are the source and target coordinates respectively. A through N are user-defined parameters. The actual second order equations used are shown in Figure 3.

FIGURE 2. TEST MODE DATA ROUTING

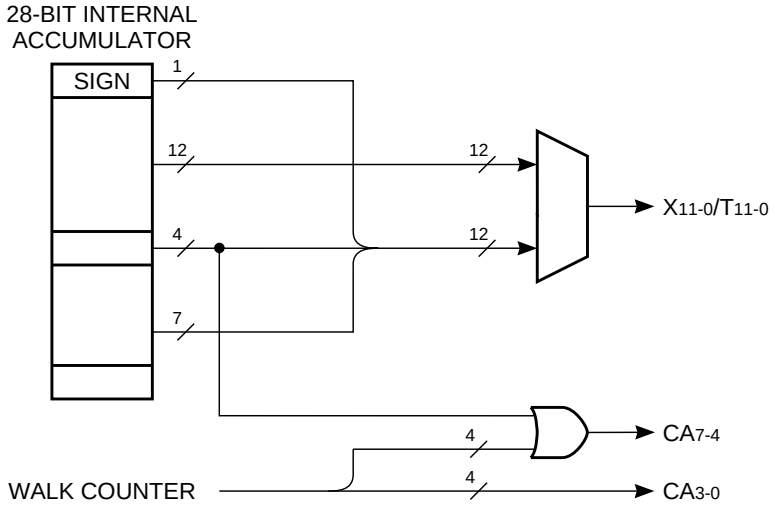


FIGURE 3. ADDRESS TRANSFORMATION EQUATIONS

$$x = x_0 + \left(\frac{dx}{du}\right)m + \left(\frac{dx}{dv}\right)n + \left(\frac{d^2x}{dudv}\right)mn + \left(\frac{d^2x}{du^2}\right)\left(\frac{m^2 - m}{2}\right) + \left(\frac{d^2x}{dv^2}\right)\left(\frac{n^2 - n}{2}\right)$$

$$+ FOV \cdot CAX(w) + FOV \cdot m \cdot CAX(ker)$$

$$y = y_0 + \left(\frac{dy}{du}\right)m + \left(\frac{dy}{dv}\right)n + \left(\frac{d^2y}{dudv}\right)mn + \left(\frac{d^2y}{du^2}\right)\left(\frac{m^2 - m}{2}\right) + \left(\frac{d^2y}{dv^2}\right)\left(\frac{n^2 - n}{2}\right)$$

$$+ FOV \cdot CAY(w) + FOV \cdot m \cdot CAY(ker)$$

$$u = UMIN + m$$

$$v = VMIN + n$$

NOTE: $\left(\frac{m^2 - m}{2}\right)$ APPROXIMATES THE EXPONENTIAL CHARACTERISTIC OF m^2.

Transformation Parameter Register Loading

The LF2301 allows Transformation Parameters to be updated on-the-fly. The loading of these registers is double-buffered (see Figure 4). Any or all of the first level registers can be loaded using P11-0, B3-0, and $\overline{WEN}$ without affecting the parameters currently in use.

LDR simultaneously updates all Transformation Parameter Registers. If Autoload (ALR) is active, these registers will be updated automatically at the beginning of each new image. Note that $\overline{NOOP}$ does not affect the loading of the Transformation Parameter Registers.

FIGURE 4. LDR CONTROL FOR PARAMETER UPDATE

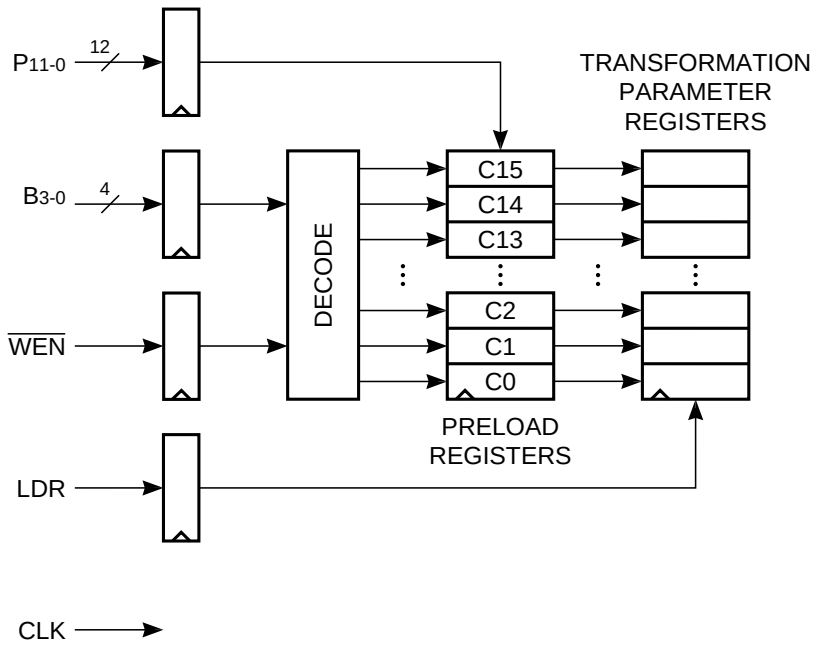


TABLE 4. PARAMETER REGISTER FORMATS (ROW OR COLUMN MODE)

ADDR	MSB				FORMAT							LSB	ROW	COLUMN
0000	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	XMIN	YMIN
0001	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	XMAX	YMAX
0010	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	x_0 (LS)	y_0 (LS)
0011	ALR	AIN	PIPE	R/C	M_1	M_0	-2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	Controls, x_0 (MS)	Controls, y_0 (LS)
0100	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	dx/du (LS)	dy/du (LS)
0101	TM	F_2	F_1	F_0	-2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Controls, dx/du (MS)	Controls, dy/du (MS)
0110	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	dx/dv (LS)	dy/dv (LS)
0111	K_3	K_2	K_1	K_0	-2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Kernel, dx/dv (MS)	Kernel, dy/dv (MS)
1000	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	$d^2x/dudv$ (LS)	$d^2y/dudv$ (LS)
1001	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	$d^2x/dudv$ (MS)	$d^2y/dudv$ (MS)
1010	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	d^2x/du^2 (LS)	d^2y/du^2 (LS)
1011	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	d^2x/du^2 (MS)	d^2y/du^2 (MS)
1100	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	d^2x/dv^2 (LS)	d^2y/dv^2 (LS)
1101	-2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	d^2x/dv^2 (MS)	d^2y/dv^2 (MS)
1110	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	UMIN	VMIN
1111	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	UMAX	VMAX

Static Filter

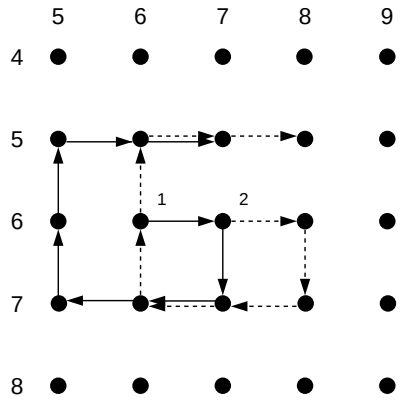
Static filtering at real-time video rates can be performed as shown in Figure 5. This mode is selected by loading M_{1-0} with "00" for a clockwise spiral walk. A counterclockwise spiral walk could be selected by loading M_{1-0} with "10." In this example, a static filter with a kernel size of 3 x 3 pixels is desired. Loading K_{3-0} with "0010" selects a kernel size of 3 x 3. The first pixel selected is determined by x_0 and y_0. In this example, the first pixel is (6,6). In this case, the LF2301s should address consecutive pixels during each spiral walk. For this to occur, FOV must be set to 1 (F_{2-0} loaded with "001").

After the last pixel of a spiral walk has been selected, the next pixel address is determined by adding dx/du to the current X address and by adding dy/du to the current Y address (unless the kernel just completed was the last for that line). At the end of the first spiral walk, pixel (7,5) is addressed. Since the first pixel of the next spiral walk should be (7,6), dx/du is selected to be 0 and dy/du is selected to be 1.

After the last pixel of the last spiral walk on the first line has been selected, the first pixel address of the second line is determined by adding dx/dv to x_0 and by adding dy/dv to y_0. Since the first pixel of the first spiral walk on the second line should be (6,7), dx/dv is selected to be 0 and dy/dv is selected to be 1. Second order differential terms are not used in this filter and are therefore set to 0.

UMIN and VMIN are both selected to be 6. UMAX and VMAX are both selected to be 7. Table 5 shows the values loaded into all Parameter Registers. Table 6 shows the ITS outputs for the 3 x 3 static filter.

FIGURE 5. 3 × 3 STATIC FILTER



1 = 1st pixel of 1st spiral walk,
2 = 1st pixel of 2nd spiral walk, etc.

TABLE 5. PARAMETER REGISTERS

ADDR	Row (HEX)	Column (HEX)
0000	000	000
0001	FFF	FFF
0010	0C0	0C0
0011	000	100
0100	000	000
0101	100	101
0110	000	000
0111	200	201
1000	000	000
1001	000	000
1010	000	000
1011	000	000
1100	000	000
1101	000	000
1110	006	006
1111	007	007

TABLE 6. ITS OUTPUTS FOR 3 × 3 STATIC FILTER

Cycle	x	y	CA_X (HEX)	CA_Y (HEX)	u	v	INIT	$\overline{ACC}$	$\overline{UWRI}$	END_X	END_Y	DONE
1	6	6	00	00	x	x	1	0	1	0	0	0
2	6	6	00	00	x	x	0	0	1	0	0	0
3	6	6	00	00	x	x	0	0	1	0	0	0
4	6	6	00	00	x	x	0	0	1	0	0	0
5	7	6	01	01	x	x	0	1	0	0	0	0
6	7	7	02	02	x	x	0	1	1	0	0	0
7	6	7	03	03	x	x	0	1	1	0	0	0
8	5	7	04	04	x	x	0	1	1	0	0	0
9	5	6	05	05	x	x	0	1	1	0	0	0
10	5	5	06	06	x	x	0	1	1	0	0	0
11	6	5	07	07	x	x	0	1	1	1	0	0
12	7	5	08	08	x	x	0	1	1	1	0	0
13	7	6	00	00	6	6	0	0	1	1	0	0
14	8	6	01	01	6	6	0	1	0	1	0	0
15	8	7	02	02	6	6	0	1	1	1	0	0
16	7	7	03	03	6	6	0	1	1	1	0	0
17	6	7	04	04	6	6	0	1	1	1	0	0
18	6	6	05	05	6	6	0	1	1	1	0	0
19	6	5	06	06	6	6	0	1	1	1	0	0
20	7	5	07	07	6	6	0	1	1	0	0	0
21	8	5	08	08	6	6	0	1	1	0	0	0
22	8	6	00	00	7	6	0	0	1	0	0	0
23	9	6	01	01	7	6	0	1	0	0	0	0
24	9	7	02	02	7	6	0	1	1	0	0	0
25	8	7	03	03	7	6	0	1	1	0	0	0
26	7	7	04	04	7	6	0	1	1	0	0	0
27	7	6	05	05	7	6	0	1	1	0	0	0
28	7	5	06	06	7	6	0	1	1	0	0	0
29	8	5	07	07	7	6	0	1	1	0	1	0
30	9	5	08	08	7	6	0	1	1	0	1	0
31	6	7	00	00	8	6	0	0	1	0	1	0
32	7	7	01	01	8	6	0	1	0	0	1	0
33	7	8	02	02	8	6	0	1	1	0	1	0
34	6	8	03	03	8	6	0	1	1	0	1	0
35	5	8	04	04	8	6	0	1	1	0	1	0
36	5	7	05	05	8	6	0	1	1	0	1	0
37	5	6	06	06	8	6	0	1	1	0	1	0
38	6	6	07	07	8	6	0	1	1	1	1	0
39	7	6	08	08	8	6	0	1	1	1	1	0
40	7	7	00	00	6	7	0	0	1	1	1	0
41	8	7	01	01	6	7	0	1	0	1	1	0
42	8	8	02	02	6	7	0	1	1	1	1	0
43	7	8	03	03	6	7	0	1	1	1	1	0
44	6	8	04	04	6	7	0	1	1	1	1	0
45	6	7	05	05	6	7	0	1	1	1	1	0
46	6	6	06	06	6	7	0	1	1	1	1	0
47	7	6	07	07	6	7	0	1	1	0	1	0
48	8	6	08	08	6	7	0	1	1	0	1	0
49	8	7	00	00	7	7	0	0	1	0	1	0
50	9	7	01	01	7	7	0	1	0	0	1	0
51	9	8	02	02	7	7	0	1	1	0	1	0
52	8	8	03	03	7	7	0	1	1	0	1	0
53	7	8	04	04	7	7	0	1	1	0	1	0
54	7	7	05	05	7	7	0	1	1	0	1	0
55	7	6	06	06	7	7	0	1	1	0	1	0
56	8	6	07	07	7	7	0	1	1	0	0	1
57	9	6	08	08	7	7	0	1	1	0	0	1
58	6	6	00	00	8	7	0	0	1	0	0	1

Image Rotation & Bilinear Interpolation

Figure 8 shows an example of rotating an image 30° and using bilinear interpolation. This mode is selected by loading M_{1-0} with "00" for a clockwise spiral walk. A counterclockwise spiral walk could be selected by loading M_{1-0} with "10." Bilinear interpolation requires a kernel size of 2 x 2 pixels. Loading K_{3-0} with "0001" selects a kernel size of 2 x 2. The first pixel selected is determined by x_0 and y_0. In this example, the first pixel is (0,0). In this case, the LF2301s should address consecutive pixels during each spiral walk. For this to occur, FOV must be set to 1 (F_{2-0} loaded with "001").

After the last pixel of a spiral walk has been selected, the next pixel address is determined by adding dx/du to the current X address and by adding dy/du to the current Y address (unless the kernel just completed was the last for that line). At the end of the first spiral walk, pixel (0,1) is addressed. Since the next calculated pixel should be (0.866,0.5), dx/du is selected to be 0.866 and dy/du is selected to be 0.5. However, after adding dx/du and dy/du to the X and Y addresses respectively, the generated address is (0.866,1.5). The Y address is off by a value of 1. This is due to the fact that the last pixel address of a spiral walk is used to calculate the first pixel address of the next spiral walk. In order for the LF2301s to generate the correct result, dy/du must be modified by subtracting a 1 from it. The correct value of dy/du is -0.5. Figure 6 shows how the unmodified differential terms were calculated.

After the last pixel of the last spiral walk on the first line has been selected, the first pixel address of the second line is determined by adding dx/dv to x_0 and by adding dy/dv to y_0. Since the first calculated pixel of the first spiral walk on the second line should be (-0.5,0.866), dx/dv is selected to be -0.5 and dy/dv is selected to be 0.866. Second order differential terms are not used in this transform and are therefore set to 0.

It is important to note that the integer portion of the address generated in the LF2301 is used as the X or Y pixel address. The fractional portion (sub-pixel portion) is used as the coefficient RAM address.

UMIN and VMIN are both selected to be 0. UMAX and VMAX are both selected to be 2. Table 7 shows the values loaded into all Parameter Registers. Table 8 shows the ITS outputs for this example.

Figure 6. Differential Terms

$$\frac{dx}{du} = \cos 30^\circ = 0.866$$

$$\frac{dy}{du} = \sin 30^\circ = 0.5$$

$$\frac{dx}{dv} = -\sin 30^\circ = -0.5$$

$$\frac{dy}{dv} = \cos 30^\circ = 0.866$$

Figure 7. 30° Image Rotation

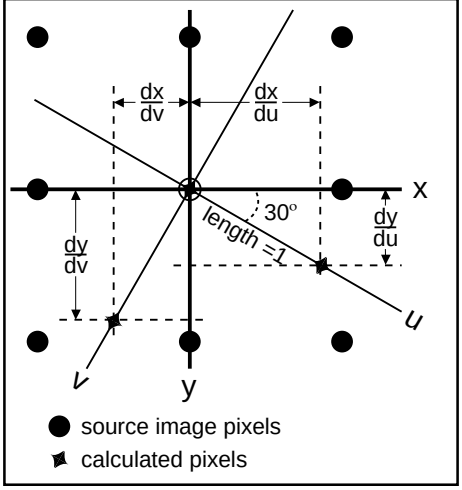


Figure 8. 30° Image Rotation

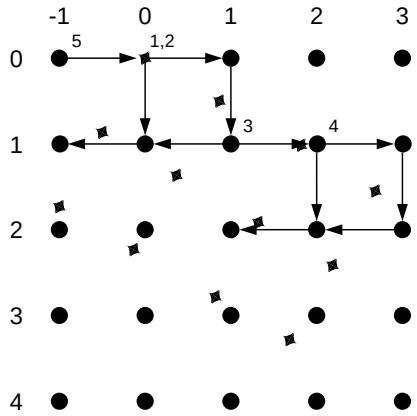


Table 7. Parameter Registers

ADDR	Row (HEX)	Column (HEX)
0000	000	000
0001	FFF	FFF
0010	000	000
0011	000	100
0100	DDB	800
0101	100	1FF
0110	800	DDB
0111	1FF	100
1000	000	000
1001	000	000
1010	000	000
1011	000	000
1100	000	000
1101	000	000
1110	000	000
1111	002	002

TABLE 8. ITS OUTPUTS FOR 30° IMAGE ROTATION WITH BILINEAR INTERPOLATION

Cycle	x	y	CA_X (HEX)	CA_Y (HEX)	u	v	INIT	$\overline{ACC}$	$\overline{UWRI}$	END_X	END_Y	DONE
1	0	0	00	00	x	x	1	0	1	0	0	0
2	0	0	00	00	x	x	0	0	1	0	0	0
3	0	0	00	00	x	x	0	0	1	0	0	0
4	0	0	00	00	x	x	0	0	1	0	0	0
5	1	0	01	01	x	x	0	1	0	0	0	0
6	1	1	02	02	x	x	0	1	1	0	0	0
7	0	1	03	03	x	x	0	1	1	0	0	0
8	0	0	D0	80	0	0	0	0	1	0	0	0
9	1	0	D1	81	0	0	0	1	0	0	0	0
10	1	1	D2	82	0	0	0	1	1	1	0	0
11	0	1	D3	83	0	0	0	1	1	1	0	0
12	1	1	B0	00	1	0	0	0	1	1	0	0
13	2	1	B1	01	1	0	0	1	0	1	0	0
14	2	2	B2	02	1	0	0	1	1	0	0	0
15	1	2	B3	03	1	0	0	1	1	0	0	0
16	2	1	90	80	2	0	0	0	1	0	0	0
17	3	1	91	81	2	0	0	1	0	0	0	0
18	3	2	92	82	2	0	0	1	1	0	0	0
19	2	2	93	83	2	0	0	1	1	0	0	0
20	-1	0	80	D0	3	0	0	0	1	0	0	0
21	0	0	81	D1	3	0	0	1	0	0	0	0
22	0	1	82	D2	3	0	0	1	1	0	0	0
23	-1	1	83	D3	3	0	0	1	1	0	0	0
24	0	1	50	50	0	1	0	0	1	0	0	0
25	1	1	51	51	0	1	0	1	0	0	0	0
26	1	2	52	52	0	1	0	1	1	1	0	0
27	0	2	53	53	0	1	0	1	1	1	0	0
28	1	1	30	D0	1	1	0	0	1	1	0	0
29	2	1	31	D1	1	1	0	1	0	1	0	0
30	2	2	32	D2	1	1	0	1	1	0	0	0
31	1	2	33	D3	1	1	0	1	1	0	0	0
32	2	2	10	50	2	1	0	0	1	0	0	0
33	3	2	11	51	2	1	0	1	0	0	0	0
34	3	3	12	52	2	1	0	1	1	0	1	0
35	2	3	13	53	2	1	0	1	1	0	1	0
36	-1	1	00	B0	3	1	0	0	1	0	1	0
37	0	1	01	B1	3	1	0	1	0	0	1	0
38	0	2	02	B2	3	1	0	1	1	0	1	0
39	-1	2	03	B3	3	1	0	1	1	0	1	0
40	-1	2	D0	30	0	2	0	0	1	0	1	0
41	0	2	D1	31	0	2	0	1	0	0	1	0
42	0	3	D2	32	0	2	0	1	1	1	1	0
43	-1	3	D3	33	0	2	0	1	1	1	1	0
44	0	2	B0	B0	1	2	0	0	1	1	1	0
45	1	2	B1	B1	1	2	0	1	0	1	1	0
46	1	3	B2	B2	1	2	0	1	1	0	1	0
47	0	3	B3	B3	1	2	0	1	1	0	1	0
48	1	3	90	30	2	2	0	0	1	0	1	0
49	2	3	91	31	2	2	0	1	0	0	1	0
50	2	4	92	32	2	2	0	1	1	0	0	1
51	1	4	93	33	2	2	0	1	1	0	0	1
52	0	0	00	00	3	2	0	0	1	0	0	1
53	1	0	01	01	3	2	0	1	0	0	0	1
54	1	1	02	02	3	2	0	1	1	0	0	1
55	0	1	03	03	3	2	0	1	1	0	0	1

Pass 1 of Two-Pass Operation

Pass 1 of the two-pass operation performs horizontal filtering on an image as shown in Figure 9. This mode is selected by loading M_{1-0} with "01." In this example, a horizontal filter with a kernel size of 3 pixels is desired. Loading K_{3-0} with "0010" selects a kernel size of 3. The first pixel selected is determined by x_0 and y_0. In this example, the first pixel is (0,0). In this case, the LF2301s should address consecutive pixels during each pixel walk. For this to occur, FOV must be set to 1 (F_{2-0} loaded with "001").

After the last pixel of a pixel walk has been selected, the next pixel address is determined by adding dx/du to the current X address and by adding dy/du to the current Y address (unless the kernel just completed was the last for that line). At the end of the first pixel walk, pixel (2,0) is addressed. Since the first pixel of the next pixel walk should be (1,0), dx/du is selected to be -1 and dy/du is selected to be 0. After the last pixel of the last pixel walk on the first line has been selected, the first pixel address of the second line is determined by adding dx/dv to x_0 and by adding dy/dv to y_0. Since the first pixel of the first pixel walk on the second line should be (0,1), dx/dv is selected to be 0 and dy/dv is selected to be 1. Second order differential terms are not used in this filter and are therefore set to 0.

Figure 9. Pass 1 Of Two-Pass

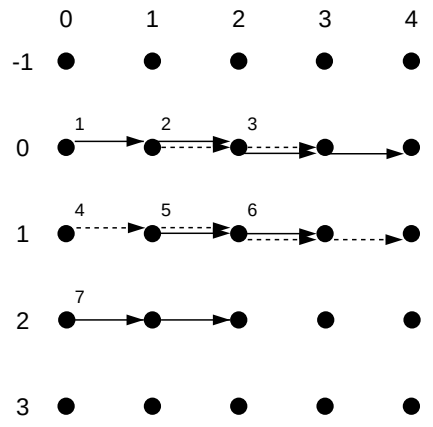


Table 9. Parameter Registers

ADDR	Row (HEX)	Column (HEX)
0000	000	000
0001	FFF	FFF
0010	000	000
0011	040	140
0100	000	000
0101	1FF	000
0110	000	000
0111	200	201
1000	000	000
1001	000	000
1010	000	000
1011	000	000
1100	000	000
1101	000	000
1110	005	005
1111	006	006

UMIN and VMIN are both selected to be 5. UMAX and VMAX are both selected to be 6. Table 9 shows the values loaded into all Parameter Registers. Table 10 shows the ITS outputs for the Pass 1 of a Two-Pass operation.

Table 10. ITS Outputs For Pass 1 Of Two-Pass

Cycle	x	y	CA_X (HEX)	CA_Y (HEX)	u	v	INIT	$\overline{ACC}$	$\overline{UWRI}$	END_X	END_Y	DONE
1	0	0	00	00	x	x	1	0	1	0	0	0
2	0	0	00	00	x	x	0	0	1	0	0	0
3	0	0	00	00	x	x	0	0	1	0	0	0
4	0	0	00	00	x	x	0	0	1	0	0	0
5	1	0	01	01	x	x	0	1	0	1	0	0
6	2	0	02	02	x	x	0	1	1	1	0	0
7	1	0	00	00	5	5	0	0	1	1	0	0
8	2	0	01	01	5	5	0	1	0	0	0	0
9	3	0	02	02	5	5	0	1	1	0	0	0
10	2	0	00	00	6	5	0	0	1	0	0	0
11	3	0	01	01	6	5	0	1	0	0	1	0
12	4	0	02	02	6	5	0	1	1	0	1	0
13	0	1	00	00	7	5	0	0	1	0	1	0
14	1	1	01	01	7	5	0	1	0	1	1	0
15	2	1	02	02	7	5	0	1	1	1	1	0
16	1	1	00	00	5	6	0	0	1	1	1	0
17	2	1	01	01	5	6	0	1	0	0	1	0
18	3	1	02	02	5	6	0	1	1	0	1	0
19	2	1	00	00	6	6	0	0	1	0	1	0
20	3	1	01	01	6	6	0	1	0	0	0	1
21	4	1	02	02	6	6	0	1	1	0	0	1
22	0	0	00	00	7	6	0	0	1	0	0	1
23	1	0	01	01	7	6	0	1	0	1	0	1
24	2	0	02	02	7	6	0	1	1	1	0	1

Pass 2 of Two-Pass Operation

Pass 2 of the two-pass operation performs vertical filtering on an image as shown in Figure 10. This mode is selected by loading M_{1-0} with "11." In this example, a vertical filter with a kernel size of 3 pixels is desired. Loading K_{3-0} with "0010" selects a kernel size of 3. The first pixel selected is determined by x_0 and y_0. In this example, the first pixel is (0,0). In this case, the LF2301s should address consecutive pixels during each pixel walk. For this to occur, FOV must be set to 1 (F_{2-0} loaded with "001").

After the last pixel of a pixel walk has been selected, the next pixel address is determined by adding dx/du to the current X address and by adding dy/du to the current Y address (unless the kernel just completed was the last for that line). At the end of the first pixel walk, pixel (0,2) is addressed. Since the first pixel of the next pixel walk should be (1,0), dx/du is selected to be 1 and dy/du is selected to be -2. After the last pixel of the last pixel walk on the first line has been selected, the first pixel address of the second line is determined by adding dx/dv to x_0 and by adding dy/dv to y_0. Since the first pixel of the first pixel walk on the second line should be (0,1), dx/dv is selected to be 0 and dy/dv is selected to be 1. Second order differential terms are not used in this filter and are therefore set to 0.

FIGURE 10. PASS 2 OF TWO-PASS

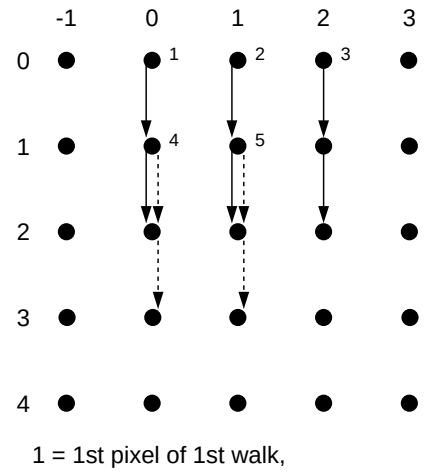


TABLE 11. PARAMETER REGISTERS

ADDR	Row (HEX)	Column (HEX)
0000	000	000
0001	FFF	FFF
0010	000	000
0011	0C0	1C0
0100	000	000
0101	101	1FE
0110	000	000
0111	200	201
1000	000	000
1001	000	000
1010	000	000
1011	000	000
1100	000	000
1101	000	000
1110	005	005
1111	006	006

UMIN and VMIN are both selected to be 5. UMAX and VMAX are both selected to be 6. Table 11 shows the values loaded into all Parameter Registers. Table 12 shows the ITS outputs for the Pass 2 of a Two-Pass operation.

TABLE 12. ITS OUTPUTS FOR PASS 2 OF TWO-PASS

Cycle	x	y	CA_X (HEX)	CA_Y (HEX)	u	v	INIT	$\overline{ACC}$	$\overline{UWRI}$	END_X	END_Y	DONE
1	0	0	00	00	x	x	1	0	1	0	0	0
2	0	0	00	00	x	x	0	0	1	0	0	0
3	0	0	00	00	x	x	0	0	1	0	0	0
4	0	0	00	00	x	x	0	0	1	0	0	0
5	0	1	01	01	x	x	0	1	0	1	0	0
6	0	2	02	02	x	x	0	1	1	1	0	0
7	1	0	00	00	5	5	0	0	1	1	0	0
8	1	1	01	01	5	5	0	1	0	0	0	0
9	1	2	02	02	5	5	0	1	1	0	0	0
10	2	0	00	00	6	5	0	0	1	0	0	0
11	2	1	01	01	6	5	0	1	0	0	1	0
12	2	2	02	02	6	5	0	1	1	0	1	0
13	0	1	00	00	7	5	0	0	1	0	1	0
14	0	2	01	01	7	5	0	1	0	1	1	0
15	0	3	02	02	7	5	0	1	1	1	1	0
16	1	1	00	00	5	6	0	0	1	1	1	0
17	1	2	01	01	5	6	0	1	0	0	1	0
18	1	3	02	02	5	6	0	1	1	0	1	0
19	2	1	00	00	6	6	0	0	1	0	1	0
20	2	2	01	01	6	6	0	1	0	0	0	1
21	2	3	02	02	6	6	0	1	1	0	0	1
22	0	0	00	00	7	6	0	0	1	0	0	1
23	0	1	01	01	7	6	0	1	0	1	0	1
24	0	2	02	02	7	6	0	1	1	1	0	1

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to VCC + 0.5 V
Signal applied to high impedance output ..... –0.5 V to VCC + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ **V**CC ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	**V**CC = Min., **I**OH = –2.0 mA	2.4			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 4.0 mA			0.4	V
VIH	Input High Voltage		2.0		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±10	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC (Note 12)			±10	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)			75	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			5	mA
CIN	Input Capacitance	**T**A = 25°C, f = 1 MHz			10	pF
COUT	Output Capacitance	**T**A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

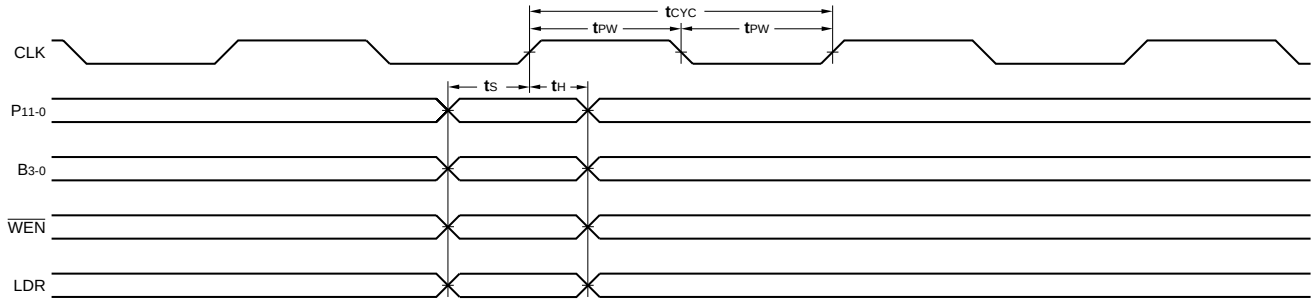
		LF2301–					
		66*		55		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	66		55		25	
t_{PW}	Clock Pulse Width	30		25		10	
t_S	Input Setup Time	20		18		10	
t_H	Input Hold Time	2		2		0	
t_{HI}	Input Hold Time, INTER	10		10		5	
t_D	Output Delay		35		27		18
t_{DE}	Output Delay, END		45		37		18
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		27		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		18		15

MILITARY OPERATING RANGE (-55°C to +125°C) *Notes 9, 10 (ns)*

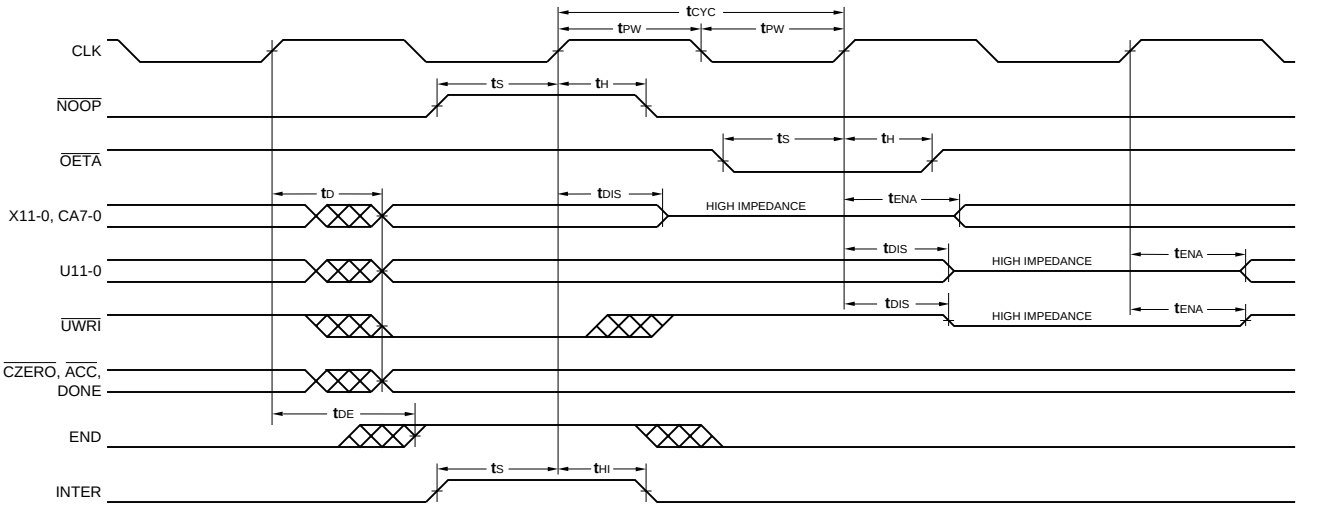
		LF2301–					
		66*		55*		30*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	66		55		30	
t_{PW}	Clock Pulse Width	30		25		10	
t_S	Input Setup Time	20		18		12	
t_H	Input Hold Time	2		2		0	
t_{HI}	Input Hold Time, INTER	10		10		6	
t_D	Output Delay		35		27		20
t_{DE}	Output Delay, END		45		37		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		27		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		18		18

*DISCONTINUED SPEED GRADE

Switching Waveforms: Data Inputs (Parameter Storage)



Switching Waveforms: Data Outputs and Control Lines



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with no output load at 15 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

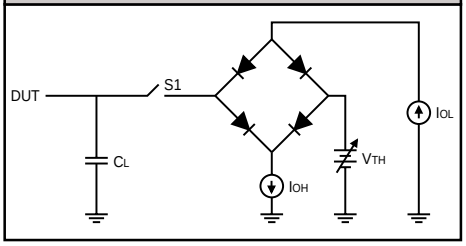
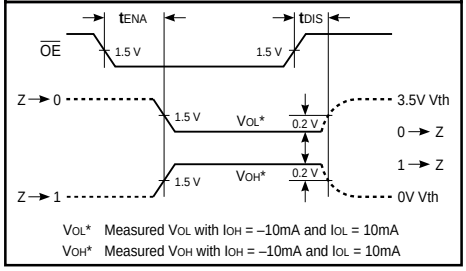
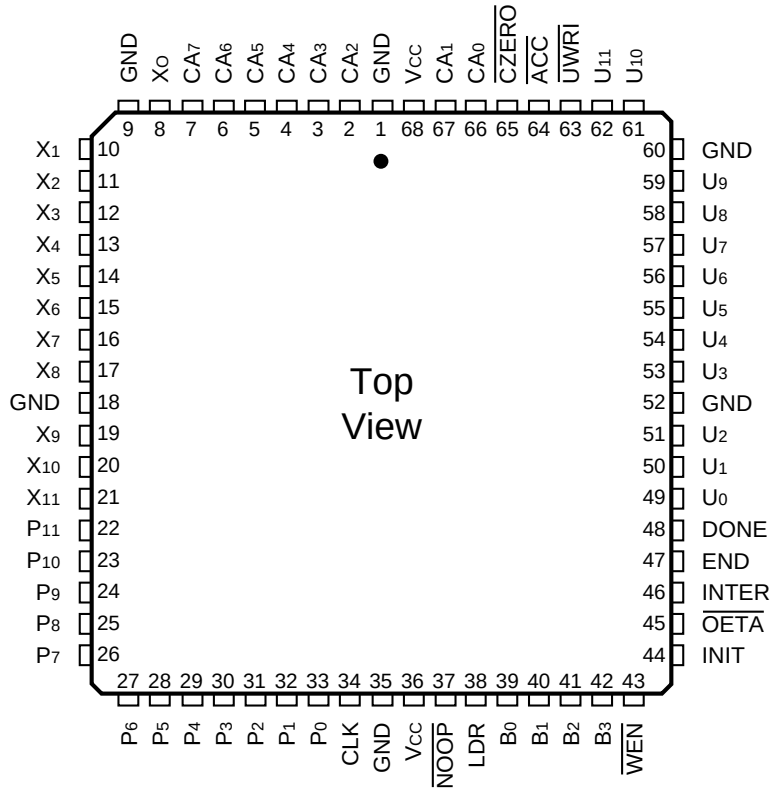


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

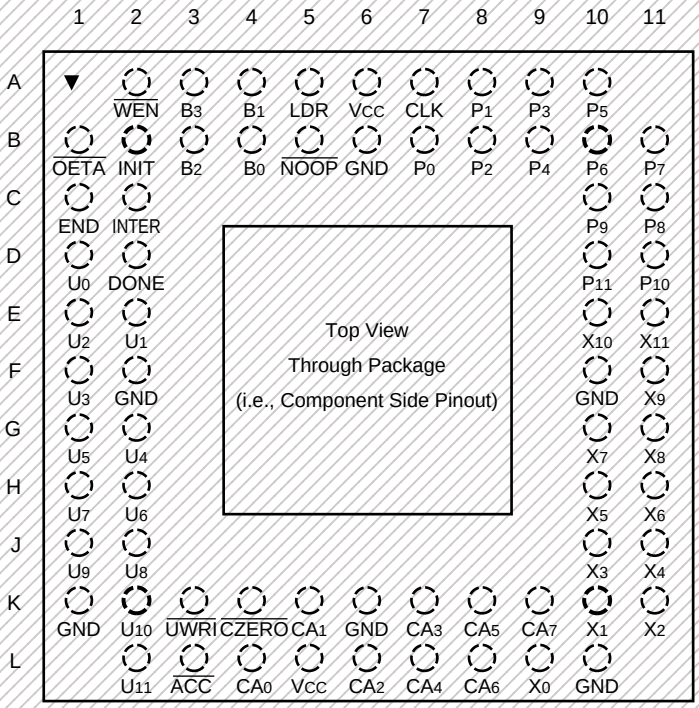
68-pin



Speed	Plastic J-Lead Chip Carrier (J2)
	0°C to +70°C — COMMERCIAL SCREENING
55 ns	LF2301JC55
25 ns	LF2301JC25

ORDERING INFORMATION

68-pin



Discontinued Package

Speed	Ceramic Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening
	–55°C to +125°C — Commercial Screening
	–55°C to +125°C — MIL-STD-883 Compliant