Ordering number : ENA2071

LE24162LBXA

ON Semiconductor®

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CMOS IC

Two Wire Serial Interface EEPROM (16k EEPROM)

Overview

The LE24162LBXA is a 2-wire serial interface EEPROM. It realizes high speed and a high level reliability by incorporating high performance CMOS EEPROM technology. This device is compatible with I^2C memory protocol; therefore it is best suited for application that requires small-scale re-writable nonvolatile parameter memory.

Functions

- Capacity: 16k bits (2k × 8 bits)
- Single supply voltage: 1.7V to 3.6V (to read)
- Operating temperature: -40 to +85ºC
- Interface: Two wire serial interface (I^2C Bus*)
- Operating clock frequency: 400kHz
- Low power consumption
  : Standby: 2μA (max)
  : Active (Read): 0.5mA (max)
- Automatic page write mode: 16 Bytes
- Read mode: Sequential read and random read
- Erase/Write cycles: 10^5 cycles (Page write)
- Data Retention: 20 years
- High reliability: Adopts proprietary symmetric memory array configuration (USP6947325)
  Noise filters connected to SCL and SDA pins
  Incorporates a feature to prohibit write operations under low voltage conditions.
- Package : WLFCP6(0.80 × 1.20)

* I^2C Bus is a trademark of Philips Corporation.

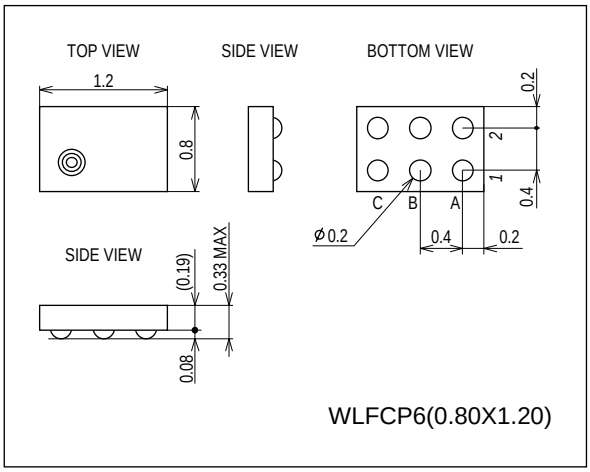
* This product is licensed from Silicon Storage Technology, Inc. (USA).

Semiconductor Components Industries, LLC, 2013
July, 2013

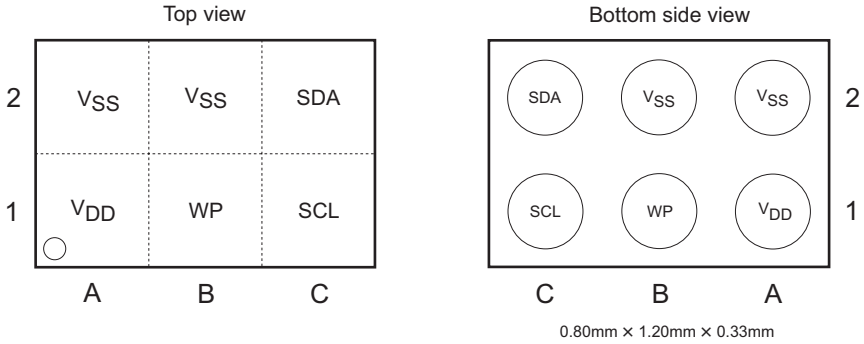
Package Dimensions

unit : mm (typ)

3435



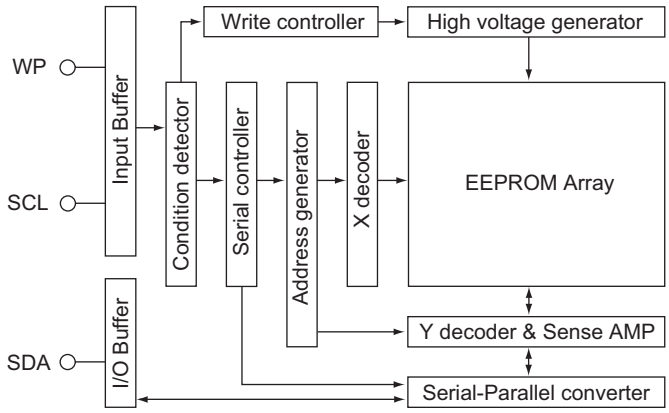
Pin Assignment



Pin Descriptions

PIN.A1	V_{DD}	Power supply
PIN.A2	V_{SS}	Ground
PIN.B1	WP	Write protect pin
PIN.B2	V_{SS}	Ground
PIN.C1	SCL	Serial clock input
PIN.C2	SDA	Serial data input/output

Block Diagram



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	unit
Supply voltage			-0.5 to +4.6	V
DC input voltage			-0.5 to V_{DD}+0.5	V
Over-shoot voltage		Below 20ns	-1.0 to V_{DD}+1.0	V
Storage temperature	Tstg		-65 to +150	°C

Note: If an electrical stress exceeding the maximum rating is applied, the device may be damaged.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Operating Conditions

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage		To read	1.7 to 3.6	V
		To write	1.8 to 3.6	V
Operating temperature			-40 to +85	°C

DC Electrical Characteristics

Parameter	Symbol	Conditions	V_{DD}=1.7V to 3.6V			unit
			min	typ	max	
Supply current at reading	$I_{CC}1$	f=400kHz			0.5	mA
Supply current at writing	$I_{CC}2$	f=400kHz, t_{WC}=5ms			5	mA
Standby current	I_{SB}	V_{IN} =V_{DD} or GND			2	µA
Input leakage current (SCL)	I_{LI}	V_{IN}=GND to V_{DD}	-2.0		+2.0	µA
Output leakage current (SDA)	I_{LO}	V_{OUT}=GND to V_{DD}	-2.0		+2.0	µA
Input low voltage	V_{IL}				V_{DD}*0.2	V
Input low voltage (CMOS)	V_{ILC}				0.2	V
Input high voltage	V_{IH}		V_{DD}*0.8			V
Input high voltage (CMOS)	V_{IHC}		V_{DD}-0.2			V
Output low voltage	V_{OL}	I_{OL}=0.7mA, V_{DD}=1.7V			0.2	V
		I_{OL}=2.0mA, V_{DD}=2.5V			0.4	V

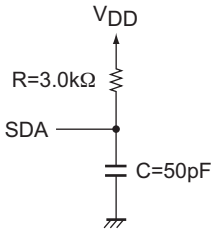
Capacitance/Ta=25°C, f=1MHz

Parameter	Symbol	Conditions	max	unit
In/Output pin capacitance	$C_{I/O}$	$V_{I/O}$=0V (SDA)	6	pF
Input pin capacitance	C_I	V_{IN}=0V (other than SDA)	6	pF

Note: This parameter is sampled and not 100% tested.

AC Electric Characteristics

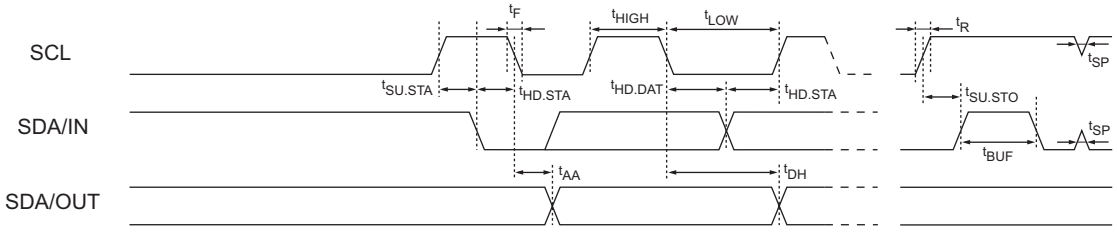
Input pulse level	$0.1\times V_{DD}$ to $0.9\times V_{DD}$
Input pulse rise / fall time	20ns
Output detection voltage	$0.5\times V_{DD}$
Output load	50pF+Pull up resistor 3.0kΩ



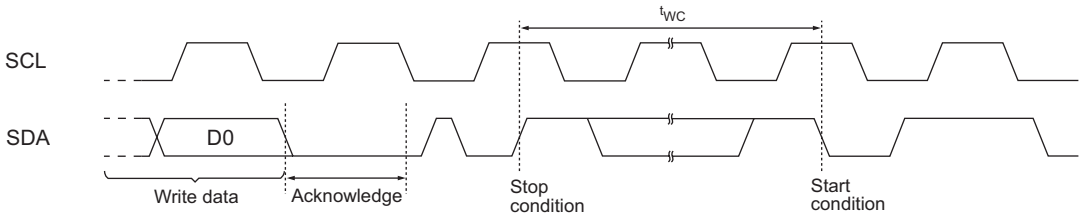
Output Load Circuit

Parameter	Symbol	V_{DD}=1.7V to 3.6V			unit
		min	typ	max	
Slave mode SCL clock frequency	f_{SCLS}	0		400	kHz
SCL clock low time	t_{LOW}	1200			ns
SCL clock high time	t_{HIGH}	600			ns
SDA output delay time	t_{AA}	100		900	ns
SDA data output hold time	t_{DH}	100			ns
Start condition setup time	$t_{SU.STA}$	600			ns
Start condition hold time	$t_{HD.STA}$	600			ns
Data in setup time	$t_{SU.DAT}$	100			ns
Data in hold time	$t_{HD.DAT}$	0			ns
Stop condition setup time	$t_{SU.STO}$	600			ns
SCL SDA rise time	t_R			300	ns
SCL SDA fall time	t_F			300	ns
Bus release time	t_{BUF}	1200			ns
Noise suppression time	t_{SP}			100	ns
Write cycle time	t_{WC}			5	ms

Bus Timing



Write Timing



Pin Functions

SCL (serial clock input) pin

The SCL pin is a serial clock input pin that processes signals at the rising and falling edges of SCL clock signals. The SCL pin must be pulled up by a resistor to the V_{DD} level and wired-ORed with an open drain (or open collector) output device for use.

SDA (serial data input/output) pin

The SDA pin is used to transfer serial data to the input/output, and it consists of a signal input pin and n-channel transistor open drain output pin.

Like the SCL pin, the SDA pin must be pulled up by a resistor to the V_{DD} level and wired-ORed with an open drain (or open collector) output device for use.

WP (write protect) pin

When the WP pin is high, write protection is enabled, and writing into the 16k bit memory areas is prohibited. When the pin is low, writing is possible to all memory areas. Read operations can be performed regardless of the WP pin status.

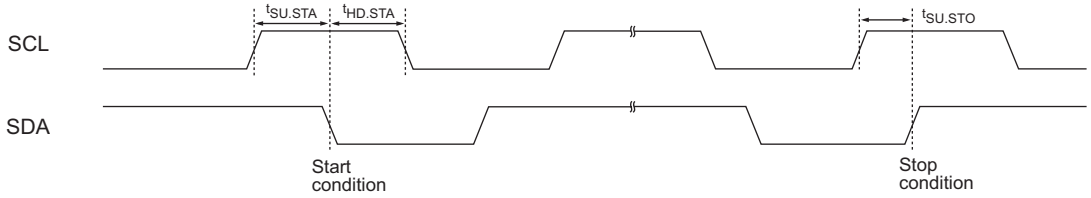
Functional Description

1 Start condition

When the SCL line is at the high level, the start condition is established by changing the SDA line from high to low. The operation of the EEPROM as a slave starts in the start condition.

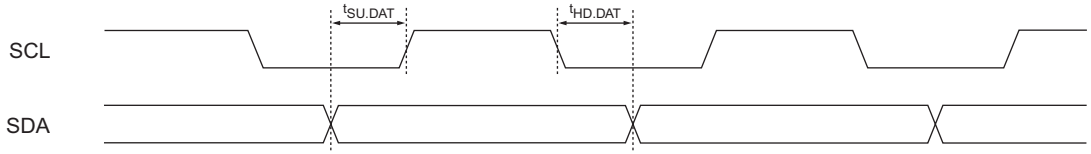
2 Stop condition

When the SCL line is at the high level, the stop condition is established by changing the SDA line from low to high. When the device is set up for the read sequence, the read operation is suspended when the stop condition is received, and the device is set to standby mode. When it is set up for the write sequence, the capture of the write data is ended when the stop condition is received, and the EEPROM internal write operation is started.



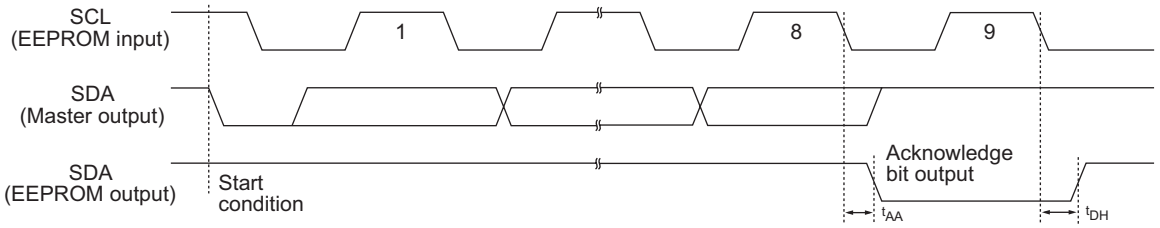
3 Data transfer

Data is transferred by changing the SDA line while the SCL line is low. When the SDA line is changed while the SCL line is high, the resulting condition will be recognized as the start or stop condition.



4 Acknowledge

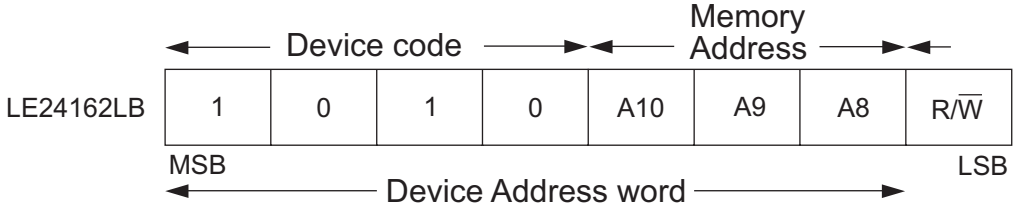
During data transfer, 8-bits are transferred in succession, and then in the ninth clock cycle period the device on the system bus receiving the data sets the SDA line to low, and sends the acknowledge signal indicating that the data has been received. The acknowledge signal is not sent during an EEPROM internal write operation.



5 Device addressing

For the purposes of communication, the master device in the system generates the start condition for the slave device. Communication with a particular slave device is enabled by sending along the SDA bus the device address, which is 7-bits long, and the read/write command code, which is 1 bit long, immediately following the start condition.

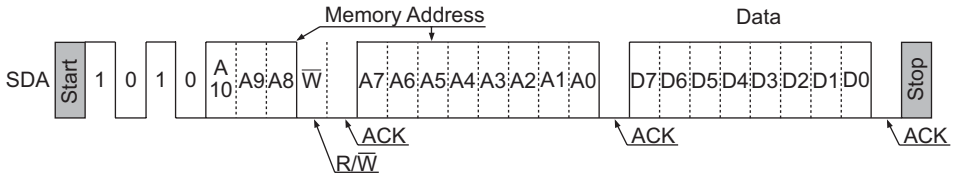
The upper four bits of the device address are called the device code which, for this product, is fixed as “1010.” Two or more pieces cannot be connected about this IC because there is no slave address.



6 EEPROM write operation

6-1. Byte writing

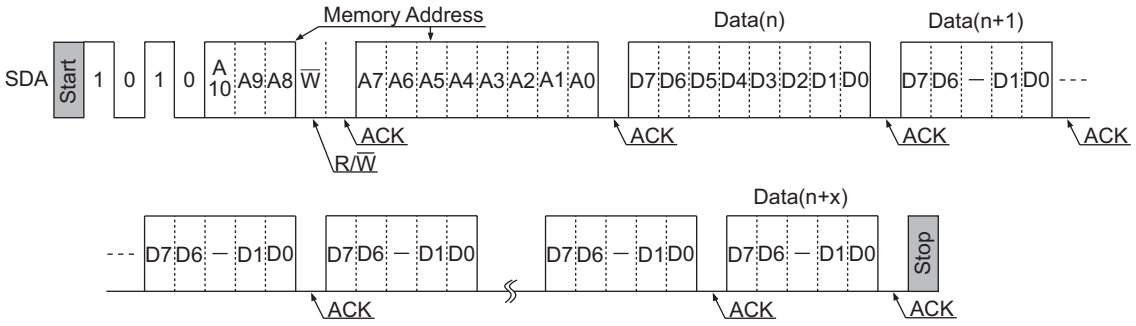
When the EEPROM receives the 7-bit device address and write command code "0" after the start condition, it generates an acknowledge signal. After this, if it receives 4-bit don't-care bits and a 12-bit word address, generates an acknowledge signal, receives the 8-bit writing data, and generates an acknowledge signal when it receives the stop condition, the rewrite operation of the EEPROM in the designated memory address will start. Rewriting is completed in the t_{WC} period after the stop condition. During an EEPROM rewrite operation, no input is accepted and no acknowledge signals are generated.



6-2. Page writing

This product enables pages with up to 16 bytes to be written. The basic data transfer procedure is the same as for byte writing: Following the start condition, the 7-bit device address and write command code "0," word address (n), and data (n) are input in this order while confirming acknowledge "0" every 9 bits. The page write mode is established if, after data (n) is input, the write data (n+1) is input without inputting the stop condition. After this, the write data equivalent to the largest page size can be received by a continuous process of repeating the receiving of the 8-bit write data and generating the acknowledge signals.

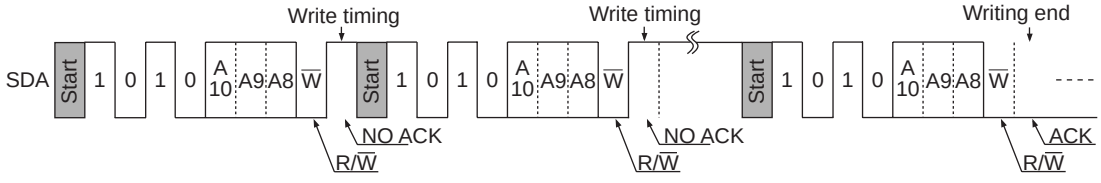
At the point when the write data (n+1) has been input, the lower 4 bits (A0-A3) of the word addresses are automatically incremented to form the (n+1) address. In this way, the write data can be successively input, and the word address on the page is incremented each time the write data is input. If the write data exceeds 16 bytes or the last address of the page is exceeded, the word address on the page is rolled over. Write data will be input into the same address two or more times, but in such cases the write data that was input last will take effect. Finally, the EEPROM internal write operation corresponding to the page size for which the write data is received starts from the designated memory address when the stop condition is received.



6-3. Acknowledge polling

Acknowledge polling is used to find out when the EEPROM internal write operation is completed. When the stop condition is received and the EEPROM starts rewriting, all operations are prohibited, and no response can be given to the signals sent by the master device. Therefore, in order to find out when the EEPROM internal write operation is completed, the start condition, device address and write command code are sent from the master device to the EEPROM (slave device), and the response of the slave device is detected.

In other words, if the slave device does not send the acknowledge signal, it means that the internal write operation is in progress; conversely, if it does send the acknowledge signal, it means that the internal write operation has been completed.



7 EEPROM read operations

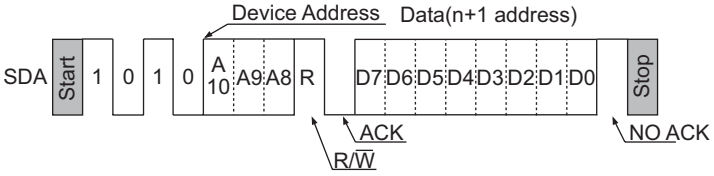
7-1. Current address reading

The address equivalent to the memory address accessed last +1 is held as the internal address of the EEPROM for both write* and read operations. Therefore, provided that the master device has recognized the position of the EEPROM address pointer, data can be read from the memory address with the current address pointer without specifying the word address.

As with writing, current address reading involves receiving the 7-bit device address and read command code “1” following the start condition, at which time the EEPROM generates an acknowledge signal. After this, the 8-bit data of the (n+1) address is output serially starting with the highest bits. After the 8 bits have been output, by not sending an acknowledge signal and inputting the stop condition, the EEPROM completes the read operation and is set to standby mode.

If the previous read address is the last address, the address for the current address reading is rolled over to become address 0.

*: If the write data is 1 or more bytes but less than 16 bytes, the current address after page writing is the address equivalent to the number of bytes to be written in the specified word address +1. If the write data is 16 or more bytes, it is the designated word address. If the last address (A3-A0=1111b) on the page has been designated by byte write as the word address, the first address (A3-A0=0000b) on the page serves as the internal address after writing.

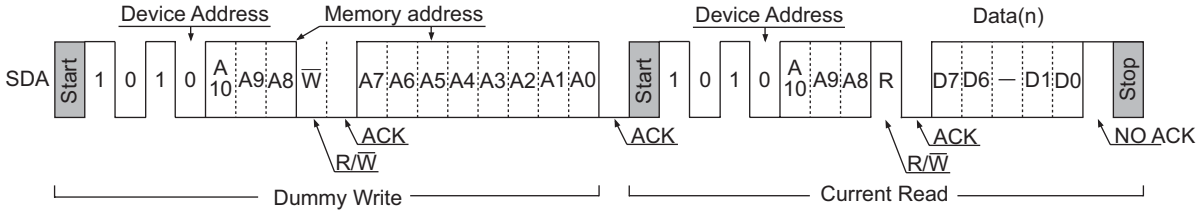


7-2. Random read

Random read is a mode in which a selected memory address is specified and its data is read. The address is specified by a dummy write input.

First, when the EEPROM receives the 7-bit device address and write command code "0" following the start condition, it generates an acknowledge signal. It then receives 4-bit don’t-care bits and a 12-bit word address and generates an acknowledge signal. These operations are used to load the word address to the address counter in the EEPROM.

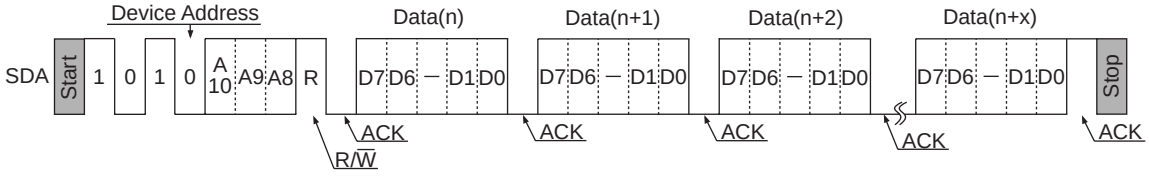
Next, the start condition is input again, and the current read is performed. This generates the word address data that was input using the dummy write input. After the data is generated, if the stop condition is input without the input of an acknowledge signal, reading is completed, and standby mode is established.



7-3. Sequential read

In this mode, the data is read continuously, and sequential read operations can be performed with both current address read and random read. If, after the 8-bit data has been output, acknowledge “0” is input and reading is continued without issuing the stop condition, the address is incremented, and the data of the next address is output.

If acknowledge “0” continues to be input after the data has been output in this way, the data is successively output while the address is incremented. When the last address is reached, it is rolled over to address 0, and the data continues to be read. As with current address read and random read, the operation is completed by inputting the stop condition without sending an acknowledge signal.

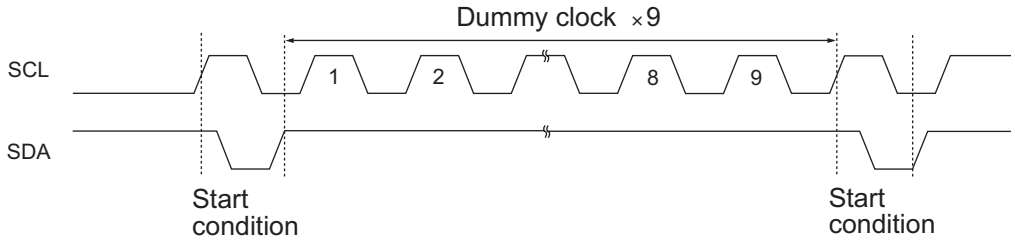


Application Notes

1) Software reset function

Software reset (start condition + 9 dummy clock cycles + start condition), shown in the figure below, is executed in order to avoid erroneous operation after power-on and to reset while the command input sequence. During the dummy clock input period, the SDA bus must be opened (set to high by a pull-up resistor). Since it is possible for the ACK output and read data to be output from the EEPROM during the dummy clock period, forcibly entering H will result in an overcurrent flow.

Note that this software reset function does not work during the internal write cycle.



2) Pull-up resistor of SDA pin

Due to the demands of the I^2C bus protocol function, the SDA pin must be connected to a pull-up resistor (with a resistance from several kΩ to several tens of kΩ) without fail. The appropriate value must be selected for this resistance (R_{PU}) on the basis of the V_{IL} and I_{IL} of the microcontroller and other devices controlling this product as well as the V_{OL}–I_{OL} characteristics of the product. Generally, when the resistance is too high, the operating frequency will be restricted; conversely, when it is too low, the operating current consumption will increase.

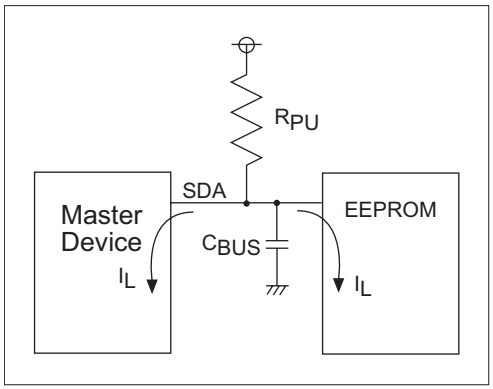
R_{PU} maximum resistance

The maximum resistance must be set in such a way that the bus potential, which is determined by the sum total (I_L) of the input leaks of the devices connected to the SDA bus and by R_{PU}, can completely satisfy the input high level (V_{IH} min) of the microcontroller and EEPROM. However, a resistance value that satisfies SDA rise time t_R and fall time t_F must be set.

R_{PU} maximum value = $(V_{DD} - V_{IH})/I_L$

Example: When V_{DD}=2.5V and I_L= 2μA

R_{PU} maximum value = $(2.5V - 2.5V \times 0.8)/2\mu A = 250k\Omega$



R_{PU} minimum value

A resistance corresponding to the low-level output voltage (V_{OL} max) of EEPROM must be set.

R_{PU} minimum value = $(V_{DD} - V_{OL})/I_{OL}$

Example: When V_{DD}=2.5V, V_{OL} = 0.4V and I_{OL} = 1mA

R_{PU} minimum value = $(2.5V - 0.4)/1mA = 2.1k\Omega$

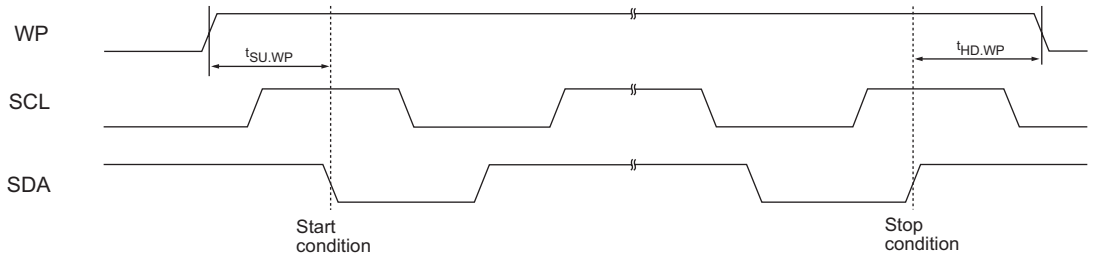
Recommended R_{PU} setting

R_{PU} is set to strike a good balance between the operating frequency requirements and power consumption. If it is assumed that the SDA load capacitance is 50pF and the SDA output data strobe time is 500ns, R_{PU} will be about R_{PU} = 500ns/50pF = 10kΩ.

3) Notes on write protect operation

This product prohibits all 16k bit writing when the WP pin is high. To ensure full write protection, the WP is set high for all periods from the start condition to the stop condition, and the conditions below must be satisfied.

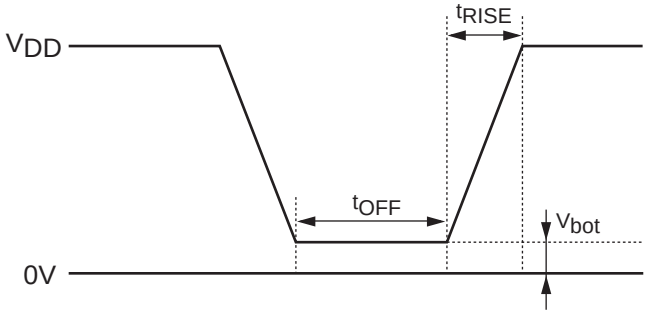
Item	Symbol	V_{DD}=1.7 to 3.6V			unit
		min	typ	max	
WP Setup time	$t_{SU.WP}$	600			ns
WP Hold time	$t_{HD.WP}$	600			ns



4) Precautions when turning on the power

This product contains a power-on reset circuit for preventing the inadvertent writing of data when the power is turned on. The following conditions must be met in order to ensure stable operation of this circuit. No data guarantees are given in the event of an instantaneous power failure during the internal write operation.

Item	Symbol	V_{DD}=1.7 to 3.6V			unit
		min	typ	max	
Power rise time	t_{RISE}			100	ms
Power off time	t_{OFF}	10			ms
Power bottom voltage	V_{bot}			0.2	V



Notes:

1) The SDA pin must be set to high and the SCL pin to low or high.
2) Steps must be taken to ensure that the SDA and SCL pins are not placed in a high-impedance state.

5) Noise filter for the SCL and SDA pins
This product contains a filter circuit for eliminating noise at the SCL and SDA pins. Pulses of 100ns or less are not recognized because of this function.

6) Function to inhibit writing when supply voltage is low
This product contains a supply voltage monitoring circuit that inhibits inadvertent writing below the guaranteed operating supply voltage range. The data is protected by ensuring that write operations are not started at voltages (typ.) of 1.3V and below.

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