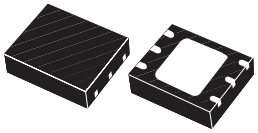
LDO40L

Datasheet

400 mA, 38 V low-dropout regulator, with 45 µA quiescent current



DFN6
(wettable flanks)

Maturity status link
LDO40L

Features

- AEC-Q100 qualified
- Low quiescent current: typ. 45 µA at no load
- Wide input voltage operating range up to 38 V
- Low startup voltage: 3.5 V
- Output current up to 400 mA
- Output voltage options: Adj from 2.5 V and fixed, 3.0, 3.3, 5.0 and 8.5 V
- Output voltage accuracy:
  - ± 1% typ. @ 25 °C
  - ± 3% (including line, load and temperature variation)
- Ultra low-dropout:
  - 36 mV @ 100 mA load current
  - 140 mV @ 400 mA load current
- High PSRR: 70 dB @ 1 kHz
- Very low noise: 20 $\mu V_{RMS}/V_{OUT}$
- Protection features: current limitation, thermal shutdown
- -40 °C to +125 °C operating temperature range
- Package: DFN6 (3x3) (wettable flanks)

Applications

- Automotive applications
- Body control modules
- Instruments and clusters
- Automotive LED lighting

Description

The LDO40L is a 400 mA LDO regulator, designed for being used in severe automotive environments.

Low quiescent current makes it suitable for applications permanently connected to battery. This feature is especially critical when electronic modules remain in active mode when ignition is off.

The LDO40L embeds protection functions, such as: current limit and thermal shutdown.

The extended input voltage range, low drop voltage and low quiescent current features make it suitable also for low power industrial and consumer applications.

1 Block diagram

Figure 1. **Block diagram, fixed version**

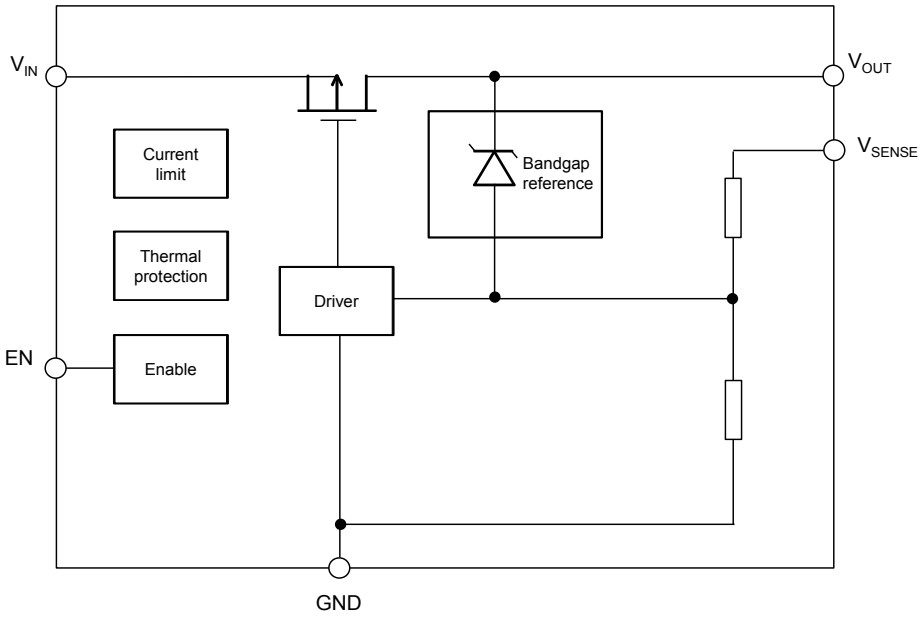
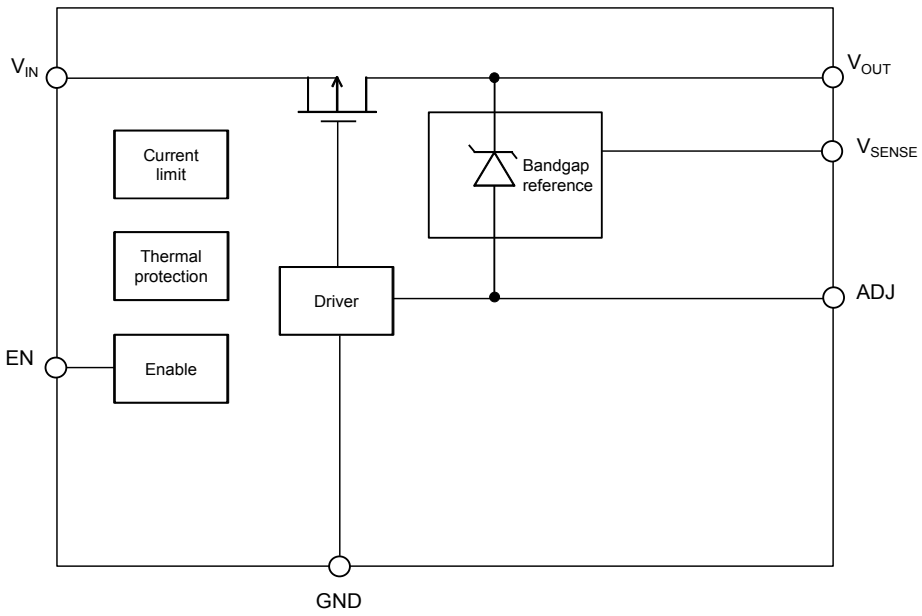


Figure 2. **Block diagram, adjustable version**



2 Pin configuration

Figure 3. **Pin configuration (marking view)**

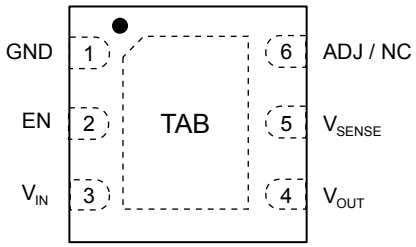


Table 1. **Pin description**

Symbol	Pin n°	Description
V_{IN}	3	LDO supply voltage
GND	1	Ground
V_{OUT}	4	LDO output voltage
EN	2	Enable input: set V_{EN} = high to turn on the device V_{EN} = low to turn off the device Don't leave this pin floating
V_{SENSE}	5	Output sensing pin. It must be connected to V_{OUT}
ADJ / NC	6	Adjust pin. Connect a resistor divider to set the output voltage This pin is not internally connected in the fixed version
TAB / Exposed pad	Exposed pad	It must be connected to GND

3 Typical application diagram

Figure 4. **Typical application diagram (fixed versions)**

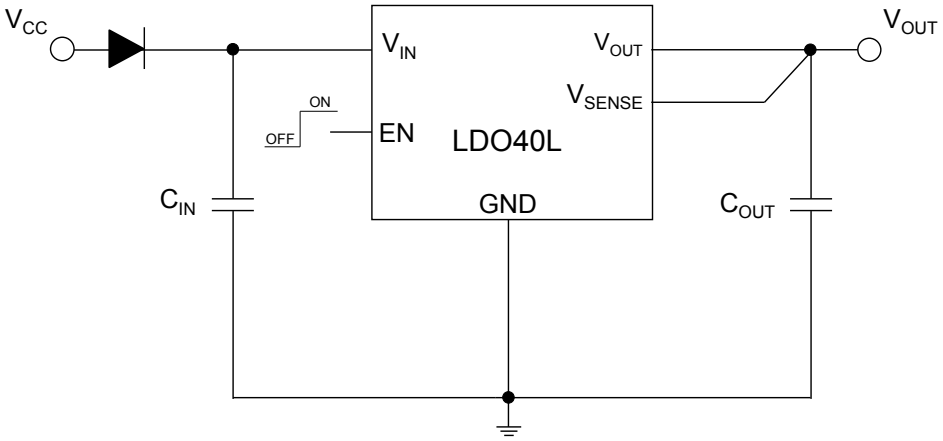
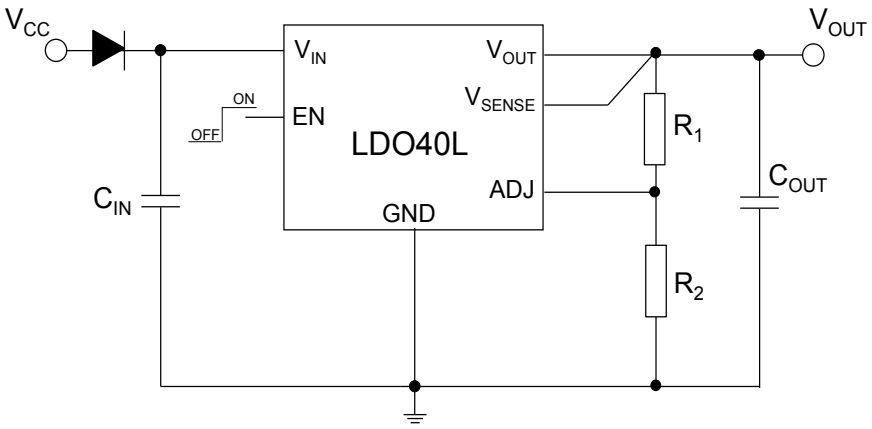


Figure 5. **Typical application diagram (adjustable versions)**



4 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input supply voltage	-0.3 to 40	V
V_{OUT}, V_{SENSE}	Output voltage	-0.3 to 12	V
V_{ADJ}	Adjust pin voltage	-0.3 to V_{OUT}	V
V_{EN}	Enable pin voltage	-0.3 to V_{IN}	V
I_{OUT}	Output current	Internally limited	A
P_D	Power dissipation	Internally limited	W
ESD	Charge device model	± 500	V
	Human body model	± 2000	
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature	-65 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	DFN6	Unit
R_{thJA}	Thermal resistance, junction-to-ambient	42	°C/W
R_{thJC}	Thermal resistance, junction-to-case	5	°C/W

Note: R_{thJA} for DFN6 based on a 4-layer JEDEC PCB (2S2P) test board with 2 thermal vias.

5 Electrical characteristics

Unless otherwise specified: T_J = -40 to 125 °C; V_{IN} = 13.2 V, V_{OUT} = 5 V, V_{EN} = 5 V, I_{OUT} = 1 mA; C_{IN} = C_{OUT} = 1 µF; Typical values referred to T_A = 25 °C.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range (see Section 6.1 Operating input voltage)	Device On	3.5		38	V
		Minimum input voltage for regulation (1)	V_{OUT}+ V_{DROP}		38	V
V_{OUT}	Operating output voltage range		2.5		11	V
V_{OUT}	Output voltage accuracy (fixed version)	V_{OUT} + 1 V (2) < V_{IN} < 18 V, 0.1 mA < I_{OUT} < 400 mA, -40 °C < T_J < 125 °C	-3		3	%
		T_J = 25 °C	-1		1	
V_{REF}	Reference voltage (adjustable version) (V_{OUT} - V_{ADJ})	V_{OUT} + 1 V (2) < V_{IN} < 18 V , 0.1 mA < I_{OUT} < 400 mA, -40 °C < T_J < 125 °C	1.164	1.2	1.236	V
		T_J = 25 °C	1.188		1.212	
$\Delta V_{OUT}/\Delta V_{IN}$	Static line regulation	V_{OUT} + 1 V (2) < V_{IN} < 18 V; I_{OUT} = 1 mA		0.002	0.02	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Static load regulation	0.1 mA < I_{OUT} < 400 mA		0.0001	0.002	%/mA
V_{DROP}	Dropout voltage (3)	I_{OUT} = 0.1 A; V_{OUT} = 5 V		36	70	mV
		I_{OUT} = 0.4 A; V_{OUT} = 5 V		140	270	
eN	Output noise voltage	f = 10 Hz to 100 kHz; I_{OUT} = 10 mA		20		$\mu V_{RMS}/V_{OUT}$
SVR	Supply voltage rejection	V_{OUT} = 5 V, f = 100 Hz; I_{OUT} = 10 mA		77		
		V_{OUT} = 5 V, f = 1 kHz; I_{OUT} = 10 mA		70		dB
		V_{OUT} = 5 V, f = 10 kHz; I_{OUT} = 10 mA		45		
		V_{OUT} = 11 V, f = 100 Hz; I_{OUT} = 10 mA		77		
		V_{OUT} = 11 V, f = 1 kHz; I_{OUT} = 10 mA		68		
		V_{OUT} = 11 V, f = 10 kHz; I_{OUT} = 10 mA		42		
I_Q	Quiescent current	I_{OUT} = 0 to 1 mA		45	90	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_Q	Quiescent current	I_{OUT} = 400 mA		80	140	µA
	Shutdown current	V_{EN} = 0 V, V_{IN} = 13.2 V		0.2	2.2	µA
I_{ADJ}	Adjustable input current				1	µA
I_{SC}	Short-circuit current	V_{IN} = 6 V, V_{OUT} = 0 V	1.2	1.6		A
V_{EN}	Enable input logic low, V_{EN-L}				0.65	V
	Enable input logic high, V_{EN-H}		2.7			
I_{EN}	Enable pin input current	V_{IN} = 6 V, V_{EN} = 5 V		0.5	1.5	µA
T_{SHDN}	Thermal shutdown			175		°C
	Hysteresis			25		

1. *V_{IN-MIN} = V_{OUT} + V_{DROP} or 5 V, whichever is greater.*
2. *V_{IN} = V_{OUT} + 1 V or 5 V, whichever is greater.*
3. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.*

6 Application information

6.1 Operating input voltage

The LDO40L is a low-dropout linear voltage regulator equipped with a low-$R_{DS-(on)}$ P-channel MOSFET used as a pass-element. The device internal circuits are able to start with an input voltage as low as 3.5 V, whatever is the nominal output voltage (see Figure 22. Output voltage vs. input voltage (no load). Defined the desired output voltage $V_{OUT-NOM}$, the minimum input voltage V_{IN-MIN} needed to fully bias the pass-element, is

$V_{IN-MIN} = V_{OUT-NOM} + V_{DROP}$. This allows to exit the dropout condition and achieve output voltage regulation.

The full regulation performance guaranteed by Section 5 Electrical characteristics in terms of output accuracy and tolerance versus line and load changes is achieved for the highest input voltage among $V_{IN-MIN} = V_{OUT-NOM}$ + 1 V and V_{IN-MIN} = 5 V .

At input voltages lower than $V_{IN-MIN} = (V_{OUT-NOM} + V_{DROP})$ the regulator enters dropout condition, regulation is not guaranteed and the output voltage tracks the input except for a voltage depending on the load current (I_{OUT}) and the pass-element resistance (see Figure 22. Output voltage vs. input voltage (no load). This tracking behavior can be useful during cold crank conditions.

6.2 Output voltage adjustment

The LDO40LY is available in fixed and adjustable output voltage versions. The latter option is usually chosen when the output voltage has to be set to non-standard values. In the adjustable version, the output voltage can be set from 2.5 V up to 11 V, by connecting a resistor divider between the ADJ pin and the output.

The architecture of the LDO40LY features a precise bandgap reference, which generates a fixed voltage V_{REF} = 1.2 V between V_{OUT} and ADJ terminals (refer to Figure 2. Block diagram, adjustable version and Figure 5. Typical application diagram (adjustable versions)). When the R1-R2 resistor divider is connected, a fixed current is generated through the divider. Since the contribution of current sourced by the ADJ pin is negligible (few tens of nA), the resulting output voltage is obtained by using the following equation:

$$V_{OUT} = V_{REF}(1 + R2/R1),\ with\ V_{REF} = 1.2V(typ.) \quad (1)$$

In order to guarantee a correct regulation, the resistor divider must be calculated for an output voltage of min. 2.5 V.

6.3 Output voltage sense pin

In the DFN6 package on pin 5, an additional V_{SENSE} connection is available. This pin must not be left floating, since it is necessary for a correct sensing of the output voltage. It can be either connected to the load in a remote-sensing configuration, or directly shorted to the V_{OUT} pin (pin 4, refer to Figure 4. Typical application diagram (fixed versions) and Figure 5. Typical application diagram (adjustable versions)).

6.4 Protection features

The device is self-protected from short-circuits and overtemperature events.

In case of strong overload or short-circuit on the output, the output current is limited to a value of typically 1.5 A and kept constant even when the load impedance is zero. If the overload persists, the temperature on the internal die rises, until the thermal protection is triggered, which happens when the junction temperature reaches 175 °C. The device is subsequently shut down. As soon as the junction temperature falls again below 150 °C the device re-starts.

Even if the above described protections are able to keep the device safe in the worst cases, a correct thermal design of the application is recommended, according to the operating ambient temperature and the maximum power dissipation allowed by the chosen package. In order to calculate the maximum power that the device can dissipate, keeping the junction temperature below T_{J-OP} = 125 °C, the following formula is used:

$$P_{DMAX} = \left(125 - T_{AMB}\right) / R_{THJ-A} \quad (2)$$

The power dissipation on the device is calculated as $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$.

6.5 Enable pin

The enable function allows the LDO output to be enabled/disabled. The regulator is turned on in case the pin EN is connected to a voltage higher than V_{EN-H}, the LDO can be turned off if the voltage on EN pin is lower than V_{EN-L}.

No internal pull-up / pull-down is present on the EN pin, therefore it must not be left floating in the application.

6.6 Input and output capacitors

The LDO40LY requires external capacitors to ensure the regulator control loop stability.

A capacitor with a minimum value of 1 µF is required on at the input port of the LDO40LY.

This capacitor must be located as close as possible to the input pin of the device and returned to a clean analog ground. Good quality ceramic capacitors are suggested.

The device control loop is designed to be stable with good quality ceramic capacitors (such as: X5R/X7R types) with a minimum capacitance of 1 µF and equivalent series resistance in the [5 mΩ – 12 Ω] range. There is no upper limit to the output capacitance. Figure 27. Stability plan shows the stability plan tested on real capacitors, up to 10 µF. A value of 4.7 µF is suitable for the majority of applications, improving dynamic response and minimizing the risk of ringing and oscillations. It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges, to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region. There is no maximum limit to the output capacitance, provided that the above conditions are respected.

7 Typical characteristics

The following plots are referred to the typical application circuit with C_{IN} = C_{OUT} = 1 µF and T_A = 25 °C unless otherwise noted.

Figure 6. Output voltage vs. temperature (V_{IN} = 6 V, V_{OUT} = adjusted to 5 V)

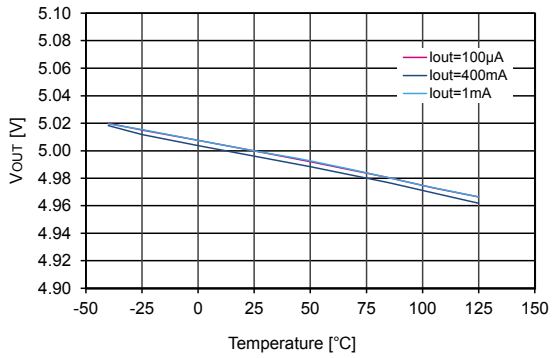


Figure 7. Output voltage vs. temperature (V_{IN} = 13.2 V, V_{OUT} adjusted to 5 V)

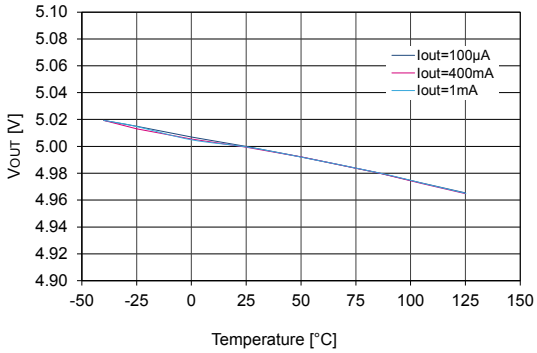


Figure 8. Output voltage vs. temperature (V_{IN} = 18 V, V_{OUT} = adjusted to 5 V)

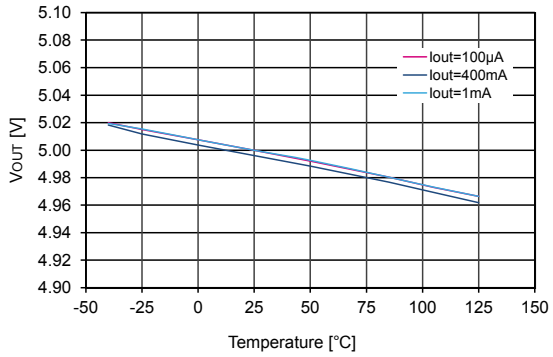


Figure 9. Output voltage vs. temperature (V_{IN} = 4.3 V, V_{OUT} = 3.3 V)

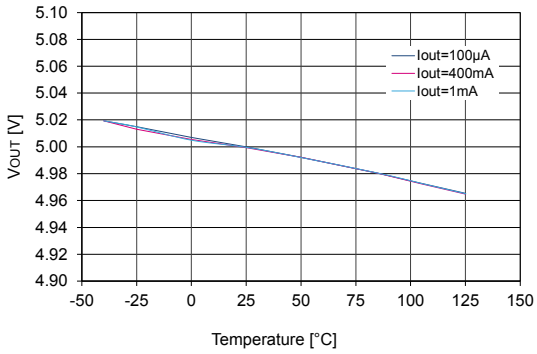


Figure 10. Output voltage vs. temperature (V_{IN} = 13.2 V, V_{OUT} = 3.3 V)

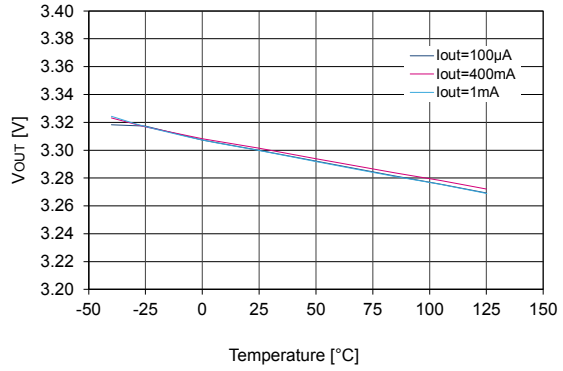


Figure 11. Output voltage vs. temperature (V_{IN} = 18 V, V_{OUT} = 3.3 V)

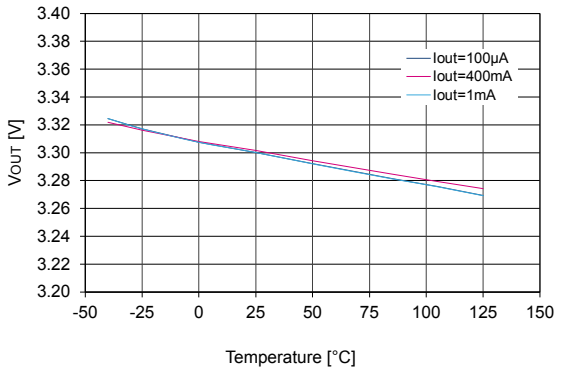


Figure 12. Reference voltage vs. temperature (V_{IN} = 6 V, V_{OUT} = adjusted to 5 V)

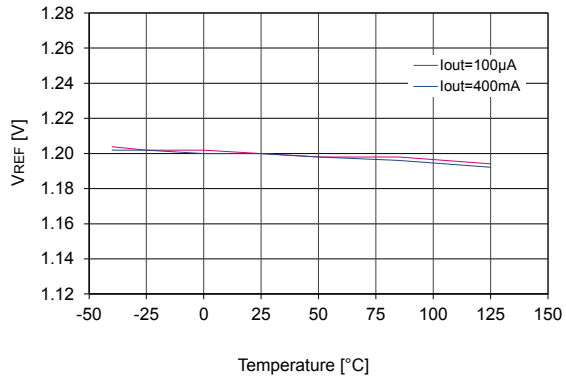


Figure 13. Reference voltage vs. temperature (V_{IN} = 18 V, V_{OUT} = adjusted to 5 V)

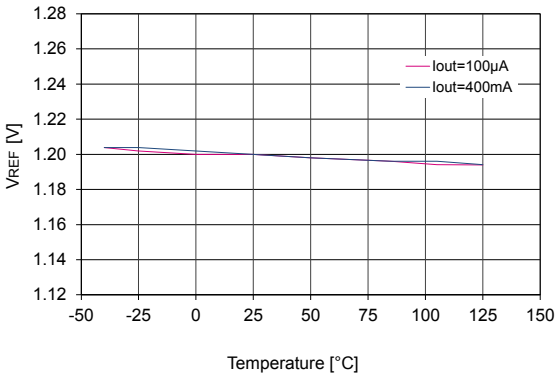


Figure 14. Line regulation vs. temperature

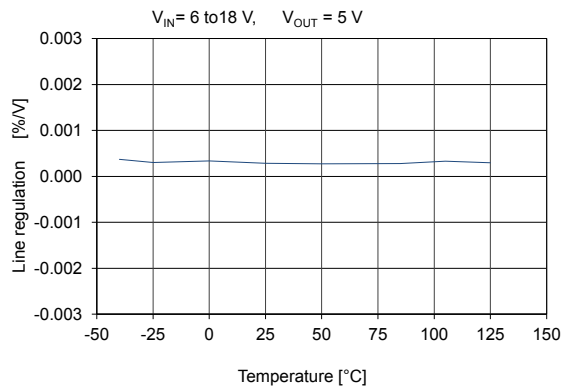


Figure 15. Load regulation vs. temperature

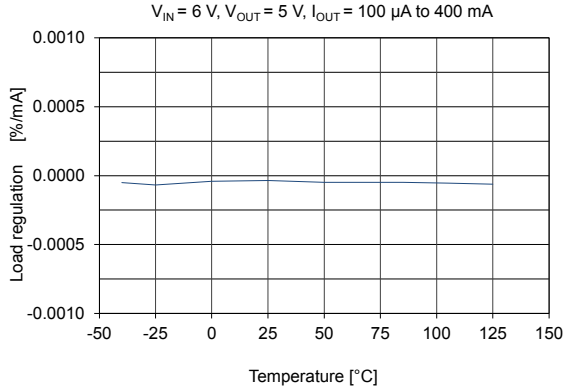


Figure 16. Dropout voltage vs. temperature

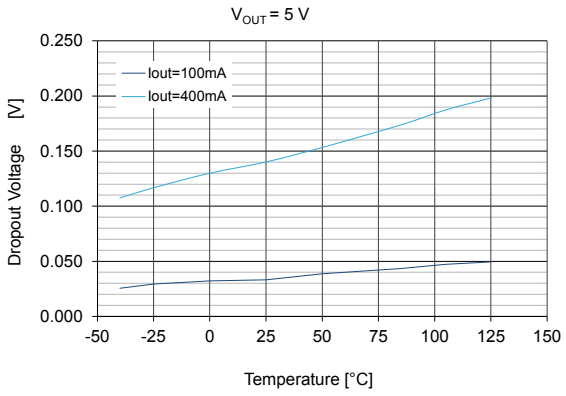


Figure 17. Short-circuit current vs. temperature

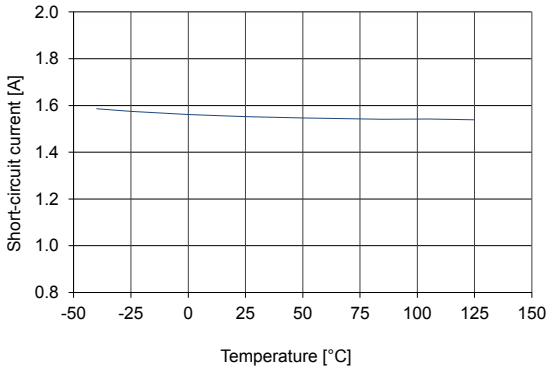


Figure 18. Quiescent current vs. temperature

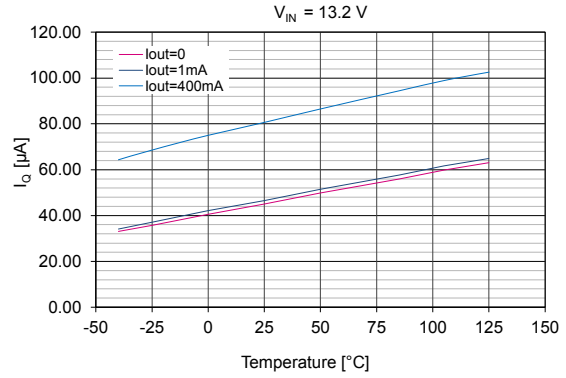


Figure 19. Off-state current vs. temperature

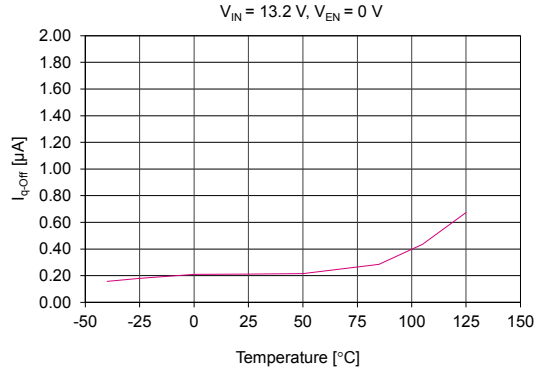


Figure 20. Enable thresholds vs. temperature

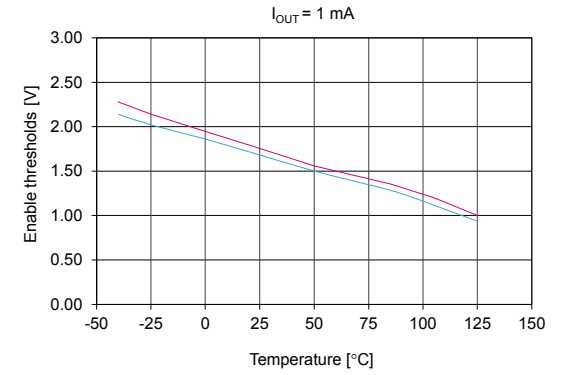


Figure 21. Enable input current vs. temperature

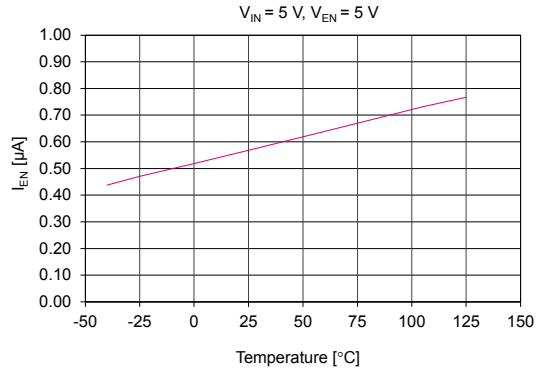


Figure 22. Output voltage vs. input voltage (no load)

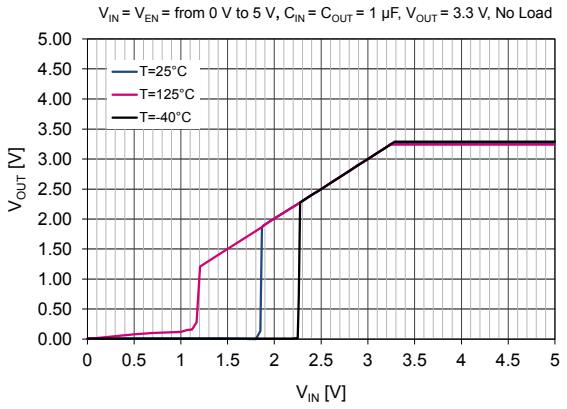


Figure 23. Output voltage vs. input voltage (I_{OUT} = 1 mA)

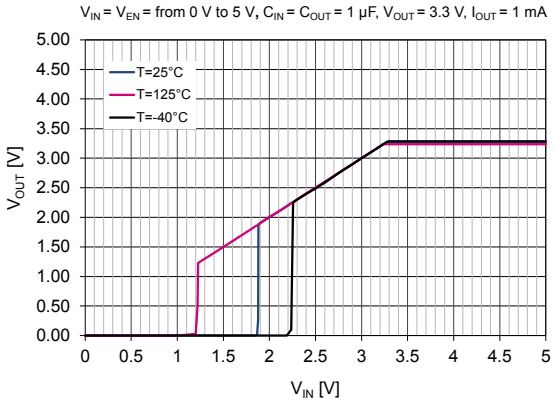


Figure 24. Output voltage vs. input voltage (I_{OUT} = 100 mA)

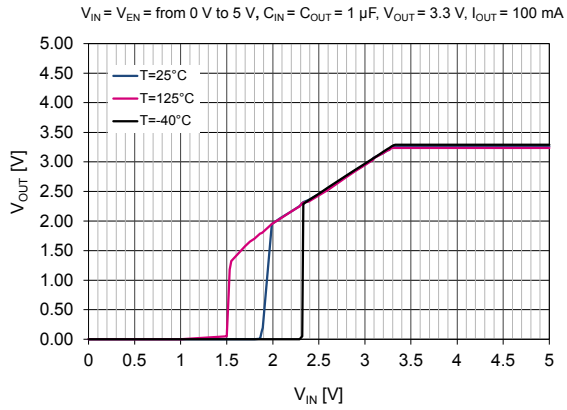


Figure 25. Output voltage vs. input voltage (I_{OUT} = 400 mA)

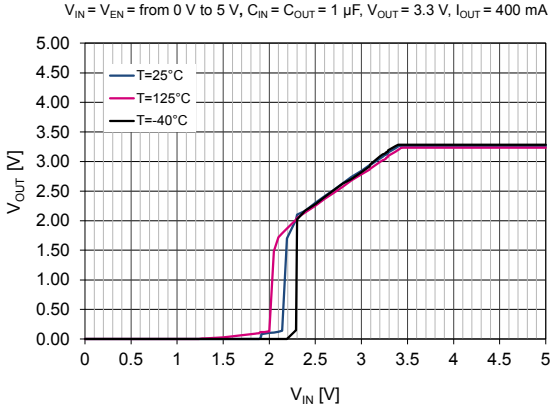


Figure 26. Quiescent current vs. input voltage

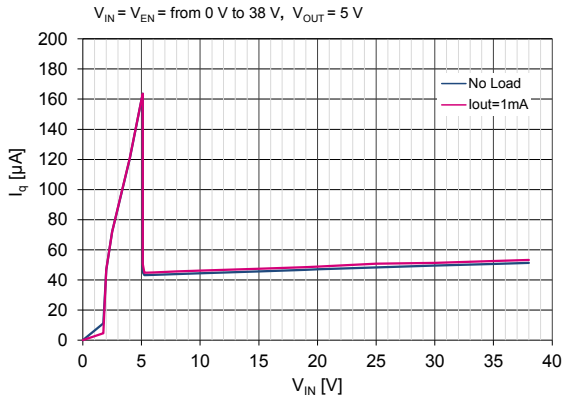


Figure 27. Stability plan

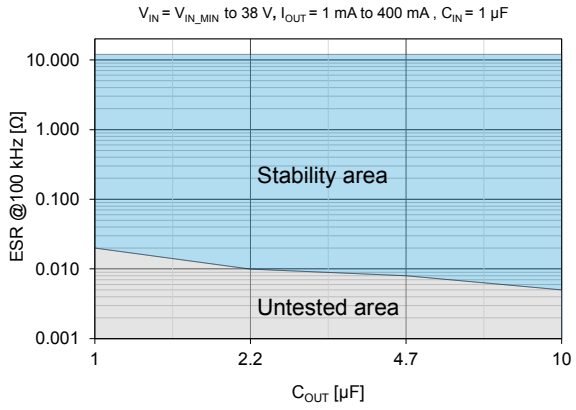


Figure 28. PSRR vs. frequency

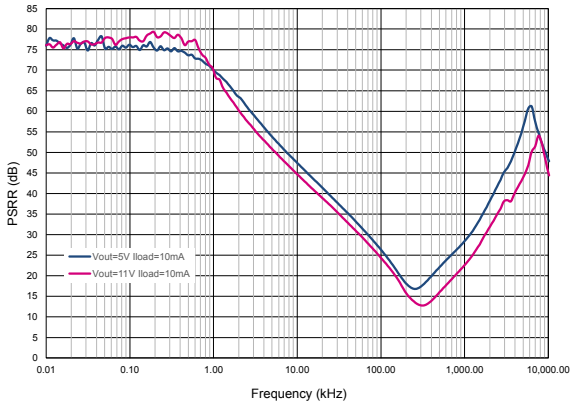


Figure 29. Output noise spectrum

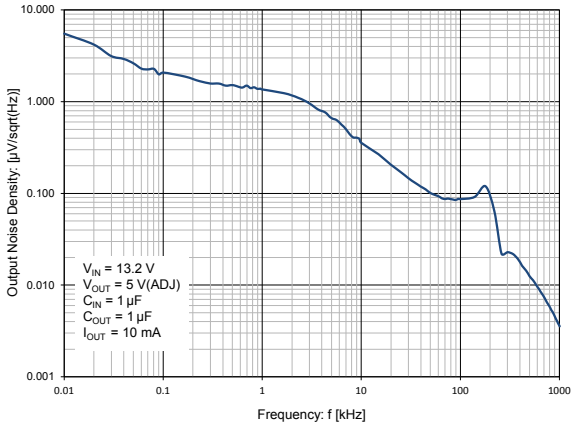


Figure 30. Line transient ($t_r = t_f = 1$ µs)

V_{IN} from 10 V to 15 V, V_{OUT} = 5 V, I_{OUT} = 1mA, $t_r = t_f$ = 1 µs, C_{OUT} = 2.2 µF

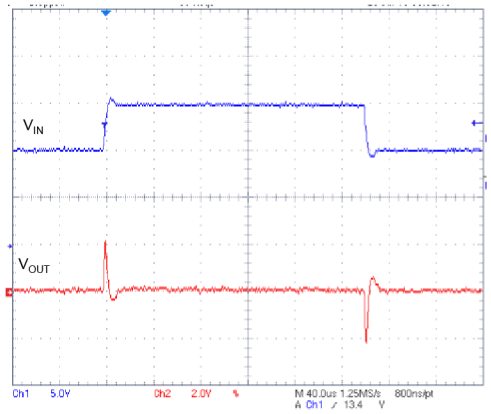


Figure 31. Line transient ($t_r = t_f = 10$ µs)

V_{IN} from 10 V to 15 V, V_{OUT} = 5 V, I_{OUT} = 1 mA, $t_r = t_f$ = 10 µs, C_{OUT} = 2.2 µF

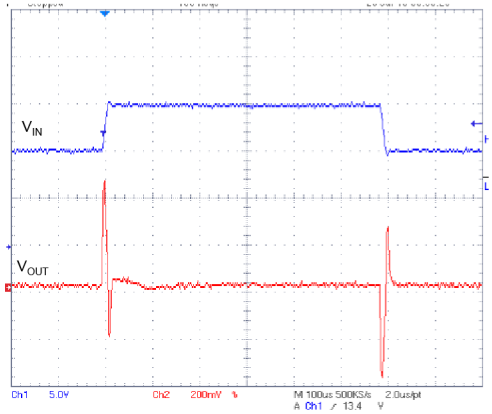


Figure 32. Load transient (0.1 mA to 100 mA, $t_r = t_f = 1$ µs)

V_{IN} = 13.2 V, V_{OUT} = 5 V, I_{OUT} = from 0.1 mA to 100 mA, $t_r = t_f$ = 1 µs, C_{OUT} = 10 µF

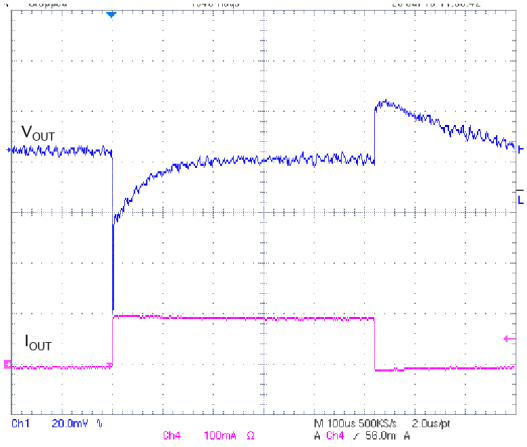


Figure 33. Load transient (0.1 mA to 100 mA, $t_r = t_f = 10$ µs)

V_{IN} = 13.2 V, V_{OUT} = 5 V, I_{OUT} = from 0.1 mA to 100 mA, $t_r = t_f$ = 10 µs, C_{OUT} = 10 µF

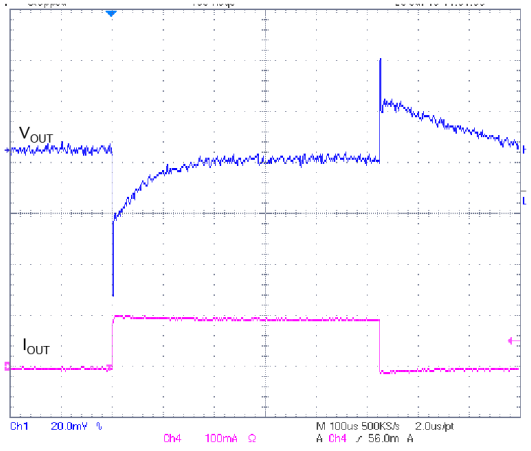


Figure 34. Load transient (1 mA to 400 mA, $t_r = t_f = 1$ µs)

V_{IN} = 13.2 V, V_{OUT} = 5 V, I_{OUT} = from 1 mA to 400 mA, $t_r = t_f$ = 1 µs, C_{OUT} = 10 µF

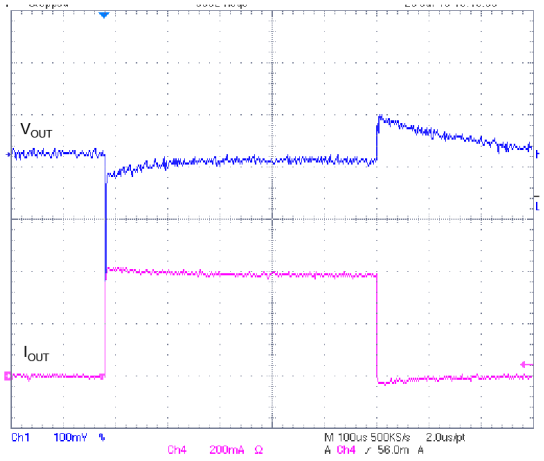


Figure 35. Load transient (1 mA to 400 mA, $t_r = t_f = 10$ µs)

V_{IN} = 13.2 V, V_{OUT} = 5 V, I_{OUT} = from 1 mA to 400 mA, $t_r = t_f$ = 10 µs, C_{OUT} = 2.2 µF

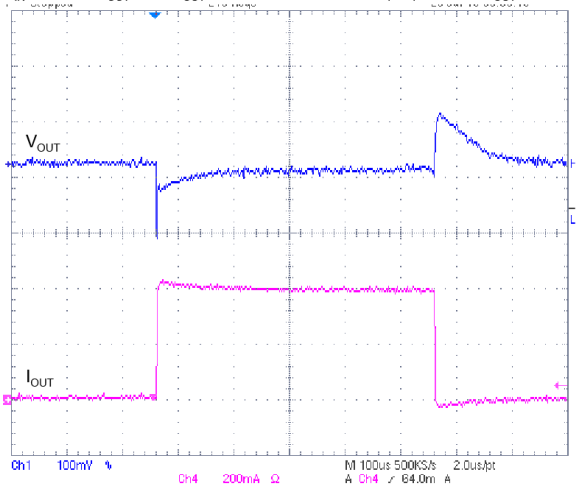


Figure 36. Enable transient (I_{OUT} = 0.1 mA)

V_{IN} = 14 V, V_{EN} = from 0 to 5 V, V_{OUT} = 5 V, I_{OUT} = 0.1 mA, t_r = 1 µs, C_{OUT} = 2.2 µF

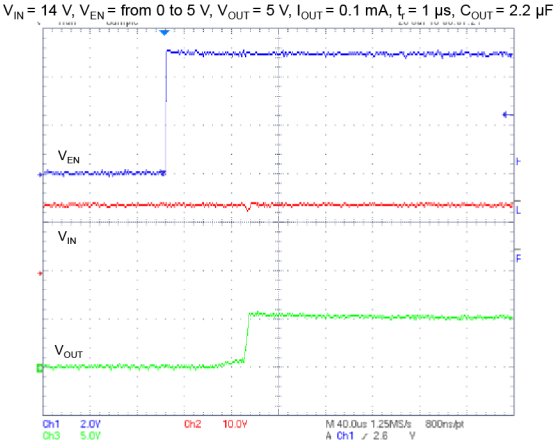


Figure 37. Enable transient (I_{OUT} = 400 mA)

V_{IN} = 14 V, V_{EN} = from 0 to 5 V, V_{OUT} = 5 V, I_{OUT} = 400 mA, t_r = 1 µs, C_{OUT} = 2.2 µF

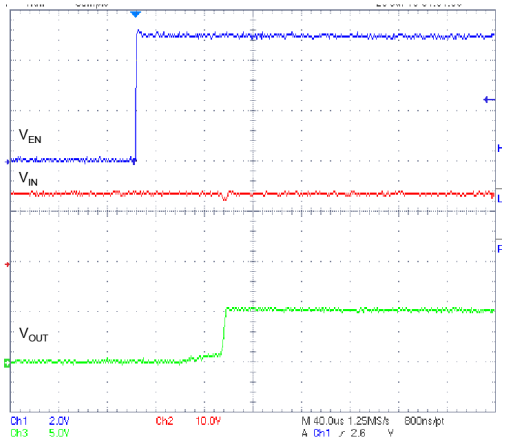


Figure 38. Start-up transient (I_{OUT} = 0.1 mA)

V_{IN} = V_{EN} = from 0 to 14 V, V_{OUT} = 5 V, I_{OUT} = 0.1 mA, t_r = 10 µs, C_{OUT} = 2.2 µF

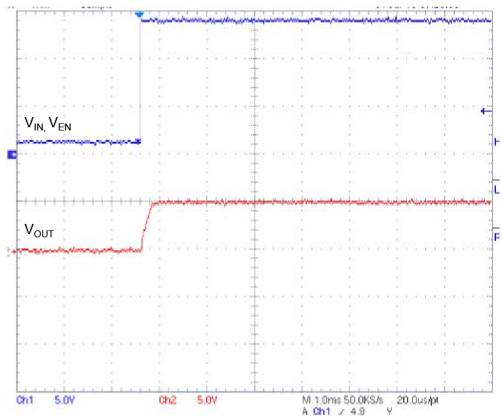
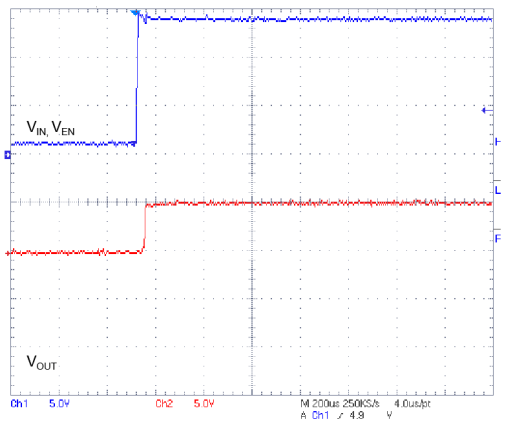


Figure 39. Start-up transient (I_{OUT} = 400 mA)

V_{IN} = V_{EN} = from 0 to 14 V, V_{OUT} = 5 V, I_{OUT} = 400 mA, t_r = 10 µs, C_{OUT} = 2.2 µF



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 DFN6 (3x3) package information

Figure 40. DFN6 (3x3) package outline

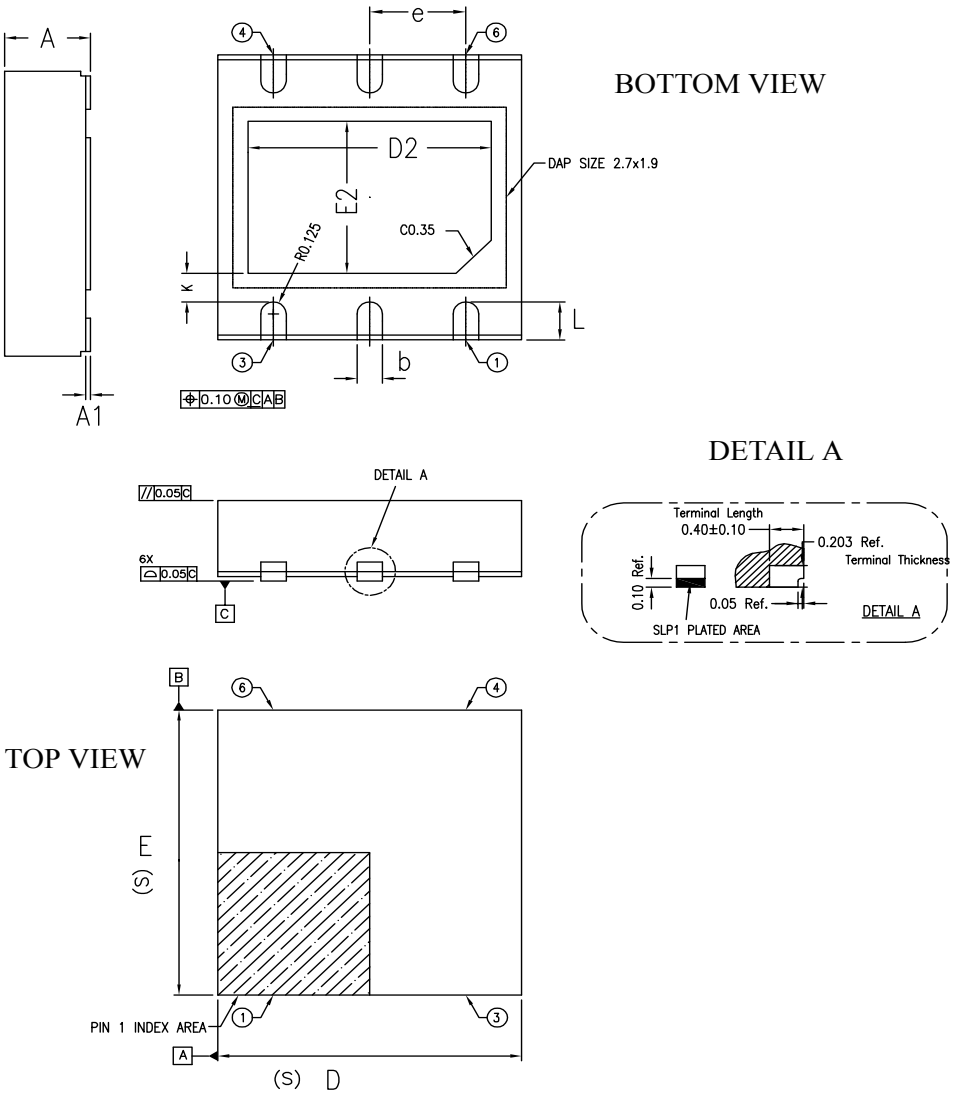
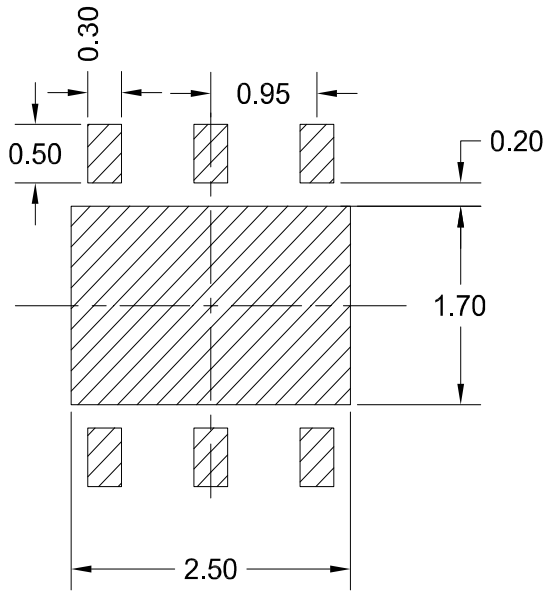


Table 5. DFN6 (3x3) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90

Dim.	mm		
	Min.	Typ.	Max.
A1	0.00		0.05
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
e		0.95 BSC	
E	2.95	3.00	3.05
E2	1.50	1.60	1.70
L	0.30	0.40	0.50
K		0.30 Ref.	
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.10	

Figure 41. DFN6 (3x3) recommended footprint (dimensions are in mm)



8.2 DFN6 (3x3) packing information

Figure 42. **DFN6 (3x3) tape outline**

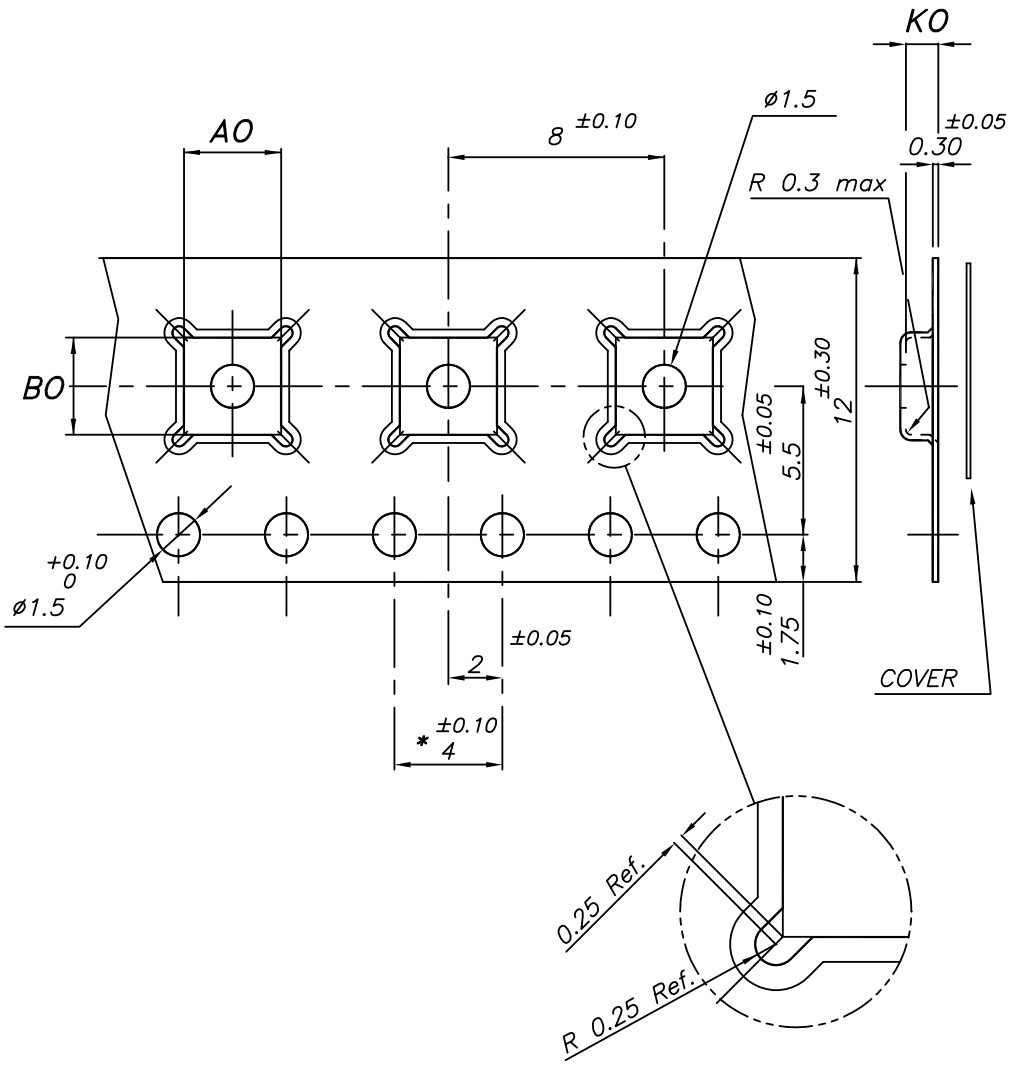


Figure 43. **DFN6 (3x3) reel outline**

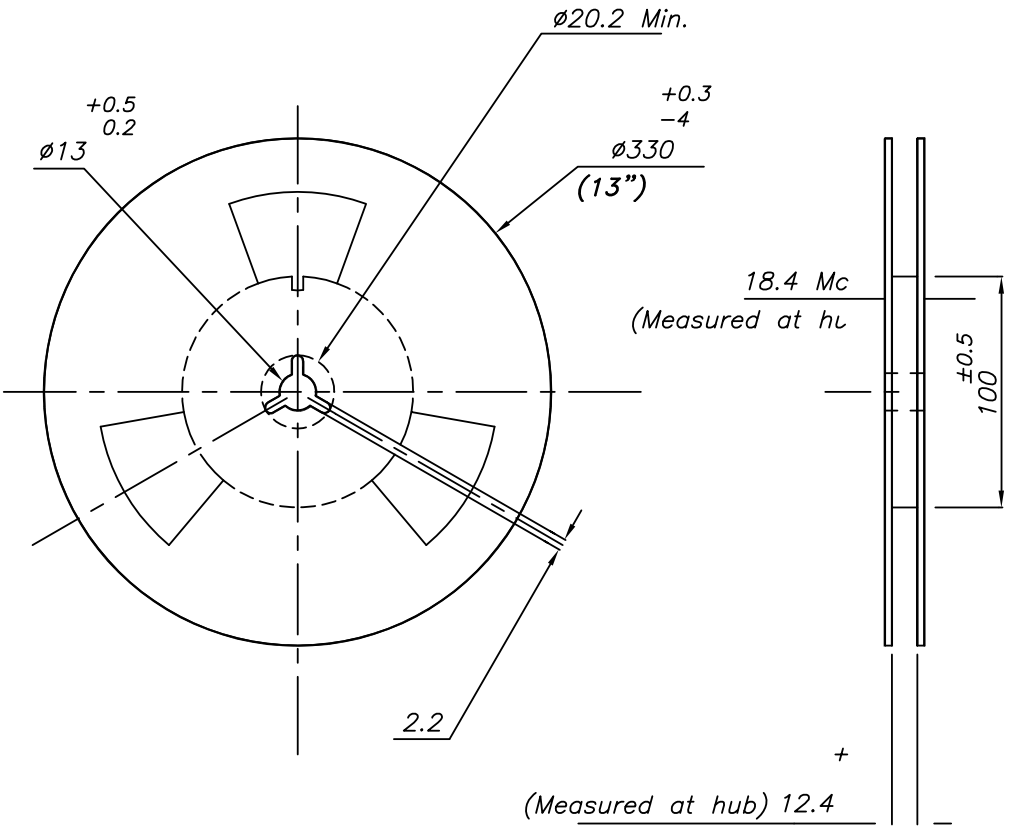


Table 6. **DFN6 (3x3) tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

9 Ordering information

Table 7. **Order code**

Order code	Package	Output voltage	Total accuracy	Marking	Packing
LDO40LPURY	DFN6	ADJ	3%	4LBA	Tape and reel
LDO40LPU33RY	DFN6	3.3 V	3%	4LBC	Tape and reel
LDO40LPU50RY	DFN6	5.0 V	3%	4LBD	Tape and reel

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
12-Sep-2018	1	Initial release.
15-Jan-2019	2	Updated: Figure 3. Pin configuration (marking view) and Table 1. Pin description. Added: footnote in Table 7. Order code.
10-Feb-2020	3	Updated Table 7. Order code.

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