LD120/121A
4½ Digit A/D Converter Set

Siliconix

FEATURES

- 0.005% ±1 Count Accuracy
- ±200.0 mV and ±2.000 V Ranges
- Auto Zero
- Auto-Polarity
- Over and Under Range Outputs

BENEFITS

- High System Performance
- Single Resistor Programming
- Nulls Out Offsets
- Single Reference
- Easily Interfaced

APPLICATIONS

- High Accuracy Digital Voltmeters and Panel Meters
- Digital Scales and Thermometer
- μP Data Acquisition Systems
- Scientific Instrumentation

DESCRIPTION

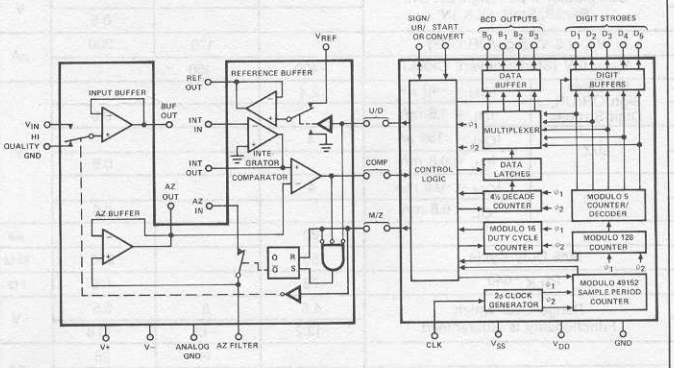
The LD120 and LD121A form a precision 4 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation. Except for a stable reference, no critical components are required to achieve rated performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

The LD120 analog processor is fabricated with a unique PMOS/Bipolar process. It contains all the necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered in LD120 to eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD120 directly interfaces the LD121A digital processor with no additional active components required.

The LD121A synchronous processor contains all the digital circuitry for the quantized feedback system. Device outputs supply two overrange signals, underrange, sign and 4½ digits of multiplexed BCD data. (All outputs are TTL compatible). Overrange is also indicated by blinking digit strobes above 20,000 counts. An input is provided to inhibit this feature at user option. Microprocessor controlled operation is simplified by a start conversion input that allows conversion-on-command.

Both devices are supplied in space saving 300 mil dual-in-line plastic packages. The LD120 has 16 pins and the LD121A has 18 pins.

FUNCTIONAL BLOCK DIAGRAM



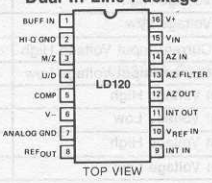
LD120
Analog Processor

LD121A
Synchronous Digital Processor

Switch States are for a Logic "0" at U/D and M/Z Inputs.

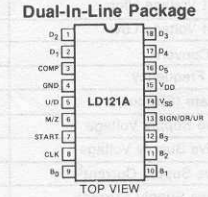
PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Order Numbers:
LD120CJ
See Package 8
LD121ACJ
See Package 19

3

ABSOLUTE MAXIMUM RATINGS

V_{IN} (Pin 15, 2 LD120) ..... $V- < V_{IN} < V+$
I_{INPUT} (LD120) ..... ±1 mA
V+ − V− (LD120) ..... 32 V
$V_{SS} - V_{DD}$ (LD121A) ..... 20 V
Any Pin (LD121A) ..... V_{DD} to V_{SS} ± 0.3
V_{REF} ..... V+

Operating Temperature ..... 0 to 70°C
Storage Temperature ..... −65 to 125°C
Power Dissipation (Package)* ..... 750 mW
*Device mounted with all leads welded or soldered to PC Board. Derated 6.3 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS[1]

T_A = 25°C

		PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V− = V_{DD} = −12 V, V_{SS} = 5 V		LIMITS MIN[2]	LIMITS TYP[3]	LIMITS MAX	UNIT
LD120 LINEAR	SYSTEM[4]	Linearity		f_{CLK} = 163.84 kHz, V_{REF} = 6.8 V	2 V Scale	−1	±1/4	1	Count
					200 mV Scale	−2	±1/2	2	
		Noise[5]			2 V Scale		1/3	1	
					200 mV Scale		1/2	2	
		Normal Mode Rejection Ratio	NMRR	f_L = 50 or 60 Hz			40		dB
		Power Supply Rejection Ratio	PSRR				80		
		Gain T.C.					5	15	ppm/°C
		Zero Drift		C_{STRG} = 1 µF, R_{in} ≤ 100 kΩ			1	5	Count
	INPUT BUFFER	Analog Input Voltage	V_{ANALOG}			−5		5	V
		Output Source Current	I_{SOURCE}	V_{in} = 2 V, Buff Out = 0 V			−100	−50	µA
		Output Sink Current	I_{SINK}	V_{in} = −2 V, Buff Out = 0 V		400	800		
		Input Current	I_{IN}	V_{in} = ±2.8 V			2		pA
		Common Mode Rejection Ratio	CMRR				−72		dB
		Input Current/Input Voltage High	I_{IH}	M/Z, U/D Inputs	V_{in} = 2.0 V			20	µA
		Input Current/Input Voltage Low	I_{IL}		V_{in} = 0.8 V	−100			
	AZ BUFFER	Output Source Current	I_{SOURCE}				−100		µA
		Output Sink Current	I_{SINK}				800		
		Offset Voltage	V_{OFFSET}	V_{OUT} = 0 V		−50		50	mV
		Switch Resistance (on)[9]		V_{STRG} = −4 V, I_{DS} = 30 µA			6	20	kΩ
	REF BUFF	Reference Buffer Source Current	I_{SOURCE}	V_{in} (U/D IN) = 0.8 V, V_O = 0 V			−800	−400	µA
		Reference Buffer Sink Current	I_{SINK}	V_{in} (U/D IN) = 2.0 V, V_O = 2 V			100		
	INTEGRATOR	Integrator Source Current[10]	I_{SOURCE}	V_{in} (Int. IN) = −100 mV, V_O = 0 V			−100	−50	
		Integrator Sink Current[10]	I_{SINK}	V_{in} (Int. IN) = 100 mV, V_O = 0 V		400	800		
		Output Swing				−10		10	V
	COMP	Comparator Output Voltage	V_{OUT}	R_L = 10 k to 5 V, AZ FILTER IN = 100 mV, INTEGRATOR OUT = 0 V		−5			
		Comparator Offset Voltage	V_{OFFSET}			−5		5	mV
	SUPPLY	Positive Supply Voltage	V+			9	12	15	V
		Negative Supply Voltage	V−			−15	−12	−9	
		Positive Supply Current	I+					3.5	mA
		Negative Supply Current	I−			−3.5			
LD121A DIGITAL	INPUTS	Input Voltage High	V_{INH}	Comparator Input, Sign/UR/OR/ Blink[6], Start, CLK IN		4			V
		Input Voltage Low	V_{INL}					0.5	
		Input Current/Input Voltage High	I_{INH}	V_{in} = 5 V (Sign/OR/UR[6])			170	300	µA
		Input Current/Input Voltage Low	I_{INL}	V_{in} = 0 V (Start Convert, Clock)		−400	−150		
	OUTPUTS	Output Voltage High	V_{OH}	Bit Lines, Sign/OR/UR, Digit Strobes	I_{OH} = −40 µA	2.4			V
		Output Voltage Low	V_{OL}		I_{OL} = 1.6 mA			0.6	
		Output Voltage High	V_{OH}	M/Z	I_{OH} = −150 µA	4			
		Output Voltage Low	V_{OL}		I_{OL} = 0.8 mA			0.6	
		Output Voltage High	V_{OH}	U/D	I_{OH} = −0.5 mA	4			
		Output Voltage Low	V_{OL}		I_{OL} = 0.8 mA			0.6	
	DYNAMIC	Start Convert[7]	t_p			20			µs
		Clock Frequency	f_{CLK}	50% Duty Cycle		50		250	kHz
		Rep Rate (Strobes)		f_{CLK} ÷640		78		470	Hz
	SUPPLY	Positive Supply Voltage	V_{SS}	Range Over which Functionality is Guaranteed		4.5	5	5.5	V
		Negative Supply Voltage	V_{DD}			−13.2	−12	−10.8	
		Positive Supply Current[8]	I_{SS}				14	25	mA
		Negative Supply Current	I_{DD}			−25	−14		

NOTES

(See next page)

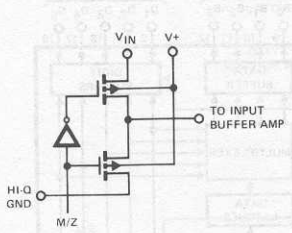
ELECTRICAL CHARACTERISTICS[1] (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: V+ = 12 V, V− = V_{DD} = −12 V, V_{SS} = 5 V	LIMITS MIN[2]	LIMITS TYP[3]	LIMITS MAX	UNIT
Zero Drift[4]		f_{CLK} = 163.84 kHz, V_{REF} = 6.8 V, C_{STRG} = 1 μF, R_{in} ≤ 100 kΩ			5	Count

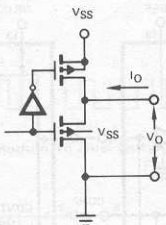
NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. System parameters not directly tested.
5. Bit width over which reading is stable 95% of the time.
6. Pin characteristic only during D_4 strobe time.
7. Minimum positive going pulse width to initiate a conversion.
8. All outputs disconnected.
9. V_{STRG} must be more positive than −4 V.
10. Reference source impedance must be less than 10 k.

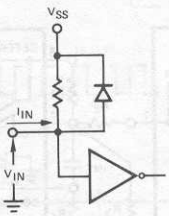
INPUT/OUTPUT SCHEMATICS



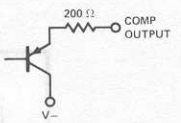
LD120 Input



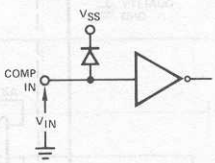
LD121A Output Buffers (Digits, Bits, Sign, M/Z U/D)



LD121A Clock Input Start Convert



LD120 Comparator Output



LD121A Comparator Input

FUCTIONAL SYSTEM OPERATION

Timing: The external oscillator is divided to generate a 2-ϕ clock on the synchronous digital chip. A time base generator divides the clock frequency into sampling intervals of 49,152 pulses of which 16,384 pulses are the Auto-Zero interval and 32,768 pulses are the measure interval.

Auto-Zero Interval: The connection diagram in Figure 1 illustrates the system during the Auto-Zero interval. The input buffer is switched to reference ground and supplies a current equal to its offset voltage divided by R_2 to the integrator summing mode. The U/D buffer is toggled by the digital processor between V_{REF} and ground with a 50% duty cycle. This results in a current flow equal to V_{REF}/R_1 to the summing node half of the time. The AZ capacitor, C_{STRG}, assumes a voltage, V_{STRG}, that is equal to the average value of integrator output. The AZ buffer supplies a current to the summing node equal to the V_{STRG} voltage divided by R_3.

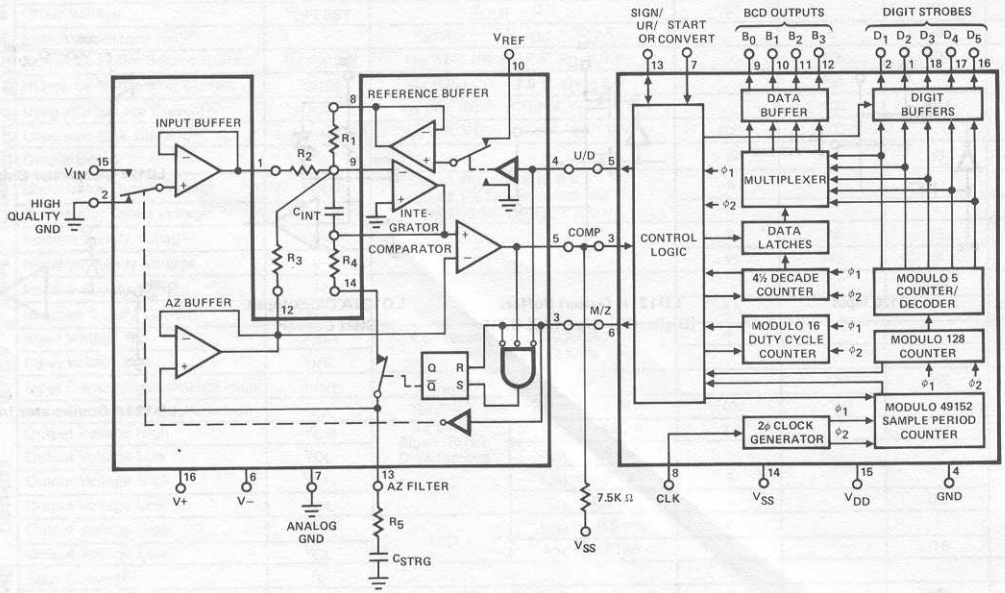
The system will reach an equilibrium when the sum of the DC currents into the summing node equal zero. At this time, the current through R_3 equals $-\frac{1}{2} V_{REF}/R_1$ plus the small currents necessary to cancel the offset of the input buffer and integrator input bias current. Capacitor C_{STRG} "stores" V_{STRG} when the AZ switch opens at the end of the Auto-Zero interval. The digital BCD counter is inactive during Auto-Zero. It is reset to zero during the last clock pulse of the Auto-Zero interval.

THE U/D CONTROL DURING THE MEASURE INTERVAL

The U/D buffer is switched to V_{REF} when the U/D control is low. In this state the currents through R_1 and R_3 sum to $\frac{1}{2} V_{REF}/R_1$. A high level on the U/D control connects the U/D buffer to ground. During this state the sum of the currents through R_1 and R_3 sum to $-\frac{1}{2} V_{REF}/R_1$. In one clock cycle, a charge equal to $V_{REF}/2R_1f_{IN}$ coulombs is either added or subtracted to the integrator capacitor. The BCD counter is decremented for each addition of this quantized charge and incremented for each subtraction of quantized charge.

THE MEASURE ALGORITHM

The input is connected to V_{IN} during the measure interval and supplies a current to the integrator equal to V_{IN}/R_2.



Connection Diagram
Figure 1

This causes the integrator output to move away from V_{STRG}. The digital processor attempts to keep the integrator output near V_{STRG} by adding or subtracting quantized charge to C_{INT}. The **net** amount of charge required to accomplish this is totaled by the BCD counter. The BCD count at the end of conversion equals the number of charge parcels necessary to cancel the input current supplied through R_2. The resulting count is proportional to the voltage at V_{IN}.

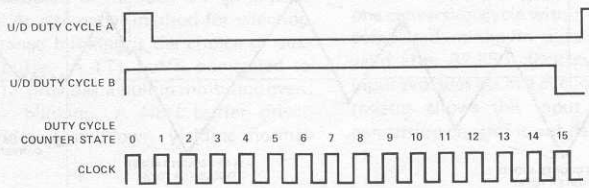
U/D DUTY CYCLE CONTROL DURING THE MEASURE INTERVAL

The digital processor contains a modulo 16 duty cycle counter that provides the U/D control output. This counter examines the state of the comparator once each 16 clock cycles during state 15. If the comparator is high, the U/D control will be high for one cycle and low for 15 cycles in the next 16 clock cycle period of the duty cycle counter. If the comparator output is low, the U/D control will be high for 15 cycles and low for one cycle in the next period of the duty cycle counter. Figure 2 illustrates these waveforms. The effect of these two duty cycles is to source or sink a net 14 charge parcels to C_{INT}, thus driving the integrator output toward V_{STRG} and accumulating counts in the BCD counter in groups of 14 counts. This dual duty cycle control technique results in a fixed number of U/D control transitions, regardless of the value of V_{IN}; therefore, these transitions cannot cause linearity error. The first few periods of the measure interval are illustrated in Figure 3 for a negative V_{IN}.

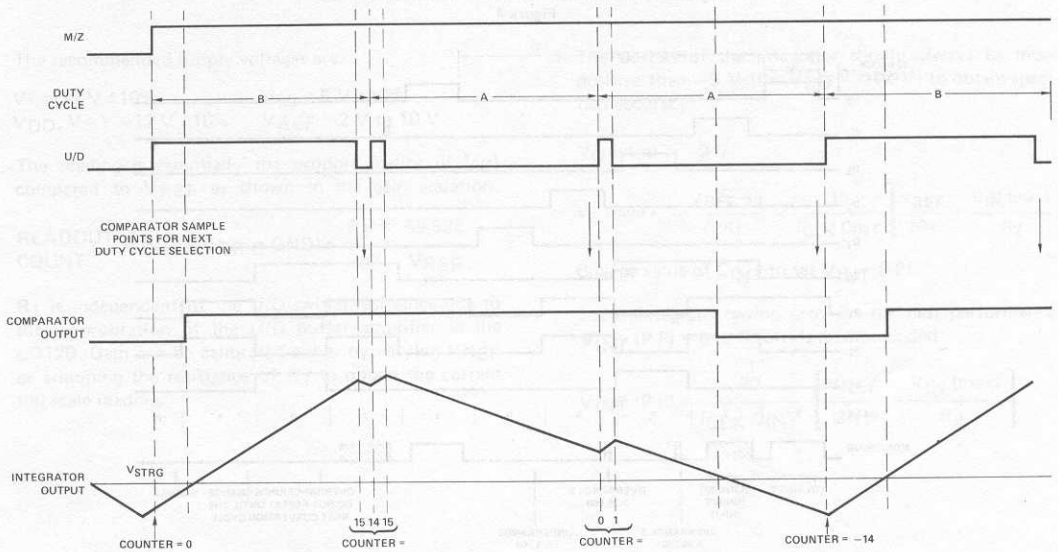
AUTO-ZERO OVERRIDE AT THE END OF MEASURE

The BCD counter contents equal a multiple of 14 counts at the end of the measure interval. A residual voltage on C_{INT} represents the remaining unresolved portion of the input voltage. This voltage is cancelled and the corresponding counts accumulated during a brief override period at the start of the AZ interval. Normal AZ interval action is inhibited until this residual count is resolved.

The override period starts at the end of the Measure Interval. The input buffer is switched to reference ground as no additional charge is desired from V_{IN}. The U/D control is set high. After the comparator goes high, the U/D control is switched low at the next state 8 of the duty cycle counter. The next transition of the comparator ends the



Modulo 16 Dual Duty Cycle Counter Waveforms
Figure 2



Measure Interval Timing ($V_{IN} \approx -1$ V)
Figure 3

FUNCTIONAL SYSTEM OPERATION (Cont.)

conversion and the BCD counter is synchronously inhibited. The output latches are updated on the next clock pulse with the sign and contents of the BCD counter. The override period ends (end of conversion) and normal AZ action is initiated by the closing of the AZ switch. The duty cycle counter now drives the U/D control high during states 0 through 7 and low during states 8 through 15 for the required AZ interval 50% duty cycle.

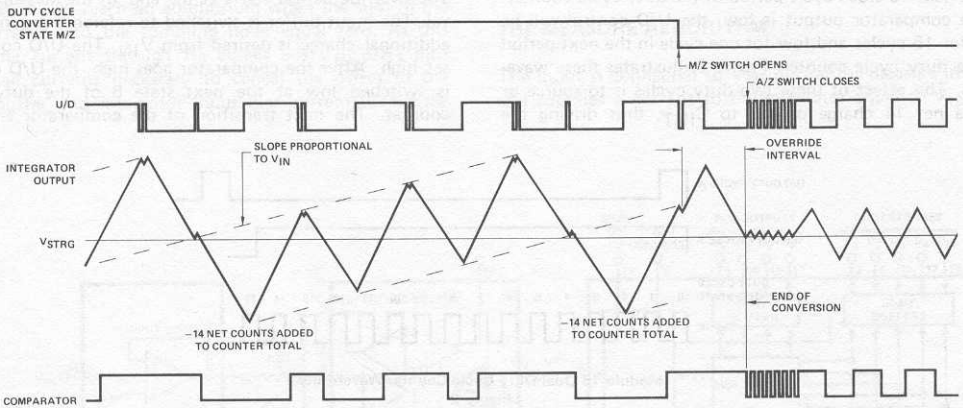
Figure 4 illustrates the events at the end of the measure interval. The slope of the dotted lines is proportional to the unknown current through R_2.

The self oscillation following the override period keeps V_{INT} near V_{STRG} until sync is achieved with the duty cycle counter. This feature eliminates large transients on C_{STRG} and results in highly stable Auto-Zero loop characteristics.

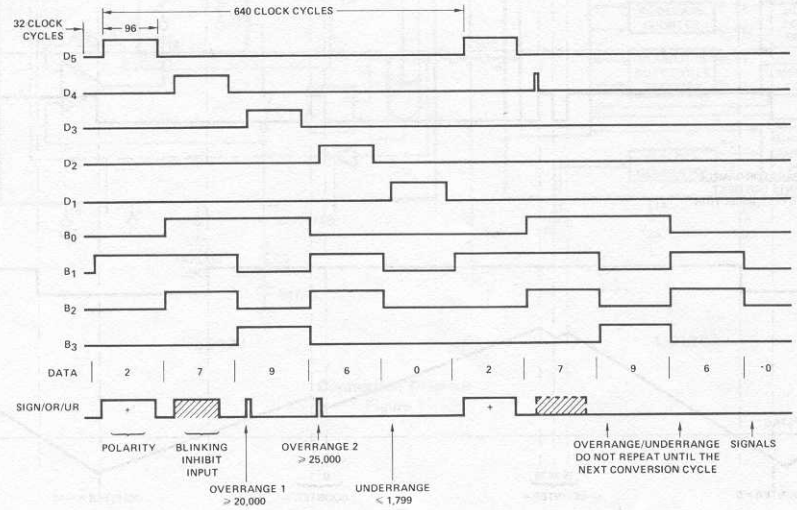
DIGITAL INTERFACE FUNCTIONAL DESCRIPTION

BCD Outputs– (Pins 9, 10, 11 and 12): The output latch contents are time multiplexed in a digit serial, bit parallel fashion through 4 push-pull TTL compatible output buffers. A high level (sourcing current from V_{SS}) indicates a one and a low level (sinking current to ground) indicates a zero. B_0 is the least significant Bit. Figure 5 illustrates the timing relationship. All BCD outputs are valid during digit strobe time.

Digit Strobes–(Pins 1, 2, 16, 17 and 18): Figure 5 indicates the operation of these outputs. The strobes are TTL compatible. Only one strobe is high at one time. The strobe period is equal to 640 clock cycles with a 15% duty cycle. An inter-digit blanking period of 32 clock cycles permits easy interface with gas discharge displays. The strobe sequence is D_5 (MSD), D_4, D_3, D_2, D_1 (LSD).



Alogrithim Waveforms at the End of the Measure Period
Figure 4



LD121 Digital Output Timing Diagram
Figure 5

FUNCTIONAL SYSTEM OPERATION (Cont.)

Clock Input (Pin 8): Pin 8 requires an external clock input. The system operates from the positive clock transition allowing a 30 to 70% duty cycle in the external oscillator waveform. To maintain the linearity specifications of the A/D converter set the short term stability of this oscillator should be better than 1 part in 2×10^4.

Sign/Overrange/Underrange (Pin 13): This pin operates as a TTL compatible output during D_1, D_2, D_3 and D_5 strobe times and as an input during D_4 strobe time. Figure 5 indicates the timing relationship. Information is presented to this output as follows:

At D_5 Time – Polarity is indicated by a high level for positive and a low level for negative. It is valid approximately 0.25 μsec after D_5 goes high until the end of each D_5 strobe.

At D_4 Time – The output buffer assumes a high impedance state. An input latch samples the voltage level imposed on this pin during D_4 time. A high level will inhibit the overrange blinking (digit strobes are suppressed during zero interval). An internal pull down resistor will hold the pin voltage low if the pin is unconnected or the load is high impedance. An alternative method for selecting overrange blinking is the choice of output buffer. A TTL buffer connected to pin 13 provides a pullup inhibiting overrange blinking. A NPN buffer driver provides a pulldown yielding normal overrange blinking.

At D_3 Time – If the count is equal to or greater than 20,000, a single positive going pulse will occur at the beginning of the first D_3 time after the end of conversion cycle. The pulse width equals one clock cycle. The overrange blinking is momentarily inhibited when overrange pulses are present to prevent the display blinking feature from interfering with the decoding of the overrange output.

At D_2 Strobe Time – A second overrange pulse occurs at the beginning of the first D_2 time, after the end of conversion, if the count is equal or exceeds 25,000 counts.

At D_1 Strobe Time – A single pulse occurs at the beginning of the first D_1 time after the end of conversion, if the count is less than 1800 counts.

All overrange and underrange signals are one clock pulse wide. They occur only once per measure/zero cycle.

Start Conversion (Pin 7): A low level on this TTL compatible input holds the system in the zero mode continuously. A positive going pulse at least one clock time wide initiates one conversion cycle within 16 clock cycles after system has completed minimum auto zero cycle. The digital data is valid after 32,850 clock cycles. A static high level on this input provides normal cyclical operation. An internal pull up resistor allows this input to remain unconnected when conversion control is not desired.

3

APPLICATIONS

1. The recommended supply voltages are:

   $V+ = 12\ V \pm 10\%$ $\quad V_{SS} = 5\ V \pm 10\%$
   $V_{DD}, V- = -12\ V \pm 10\%$ $\quad V_{REF} = 2\ V$ to $10\ V$

2. The reading is essentially the proportionality of V_{IN} compared to V_{REF} as shown in the gain equation:

$$\text{READOUT COUNT} = (V_{IN} - V_{HI\text{-}Q}\ GND) \bullet \frac{R_1}{R_2} \bullet \frac{65{,}536}{V_{REF}}$$

   R_1 is independent of the U/D switch resistance due to the incorporation of the U/D buffer amplifier in the LD120. Gain can be calibrated either by varying V_{REF} or trimming the resistance of R_1 to obtain the correct full scale reading.

3. The output of the integrator should always be more positive than −9 V (for $V_{DD} = -12$ V) to obtain specified accuracy:

$$V_O\ (min) > -9\ V$$

$$V_O\ (min) = -\frac{V_{REF}\ R_3}{2R_1} - \frac{15}{f_{CLK}\ C_{INT}}\left[\frac{V_{REF}}{2R_1} + \frac{V_{IN}\ (max)}{R_2}\right]$$

   Change value of C_{INT} to set V_{INT}(P-P).

   Large integrator swing provides the best performance. V_{INT} (P-P) = 6 to 8 volts is recommended.

$$V_{INT}\ (P\text{-}P) = \frac{30}{f_{CLK}\ C_{INT}}\left[\frac{V_{REF}}{2R_1} + \frac{V_{IN}\ (max)}{R_2}\right]$$

APPLICATIONS (Cont.)

4. Although any oscillator frequency from 50 kHz to 250 kHz can be used, frequencies that provide integer number of line frequency cycles per measure period provide maximum line noise rejection. These frequencies are:

$$f_{CLK} = \frac{32{,}768\ F_{LINE}}{n}, \quad n = 8, 9, 10, \ldots 40$$

f_{CLK} = 163,840 is popular since it provides both 50 and 60 Hz rejection.

5. The sampling rate = $f_{CLK}/49{,}152$ cycles/sample.

6. After a start conversion pulse, data is valid 32,850 clock pulses later and remains valid until at least 32,768 clock pulses after the next start pulse. During continuous cycle operation, data is assured valid when M/Z is high or 100 clock cycles after the one/zero transition of M/Z.

7. Any capacitive coupling between U/D and Comp. is detrimental to proper algorithm operation. PC board layouts should not allow these traces to be adjacent.

8. All power supplies should be capacitively bypassed to ground for maximum count stability.

9. C_{INT} and C_{STRG} should be selected for low leakage. Silvered mica is recommended for C_{INT} and mylar for C_{STRG}. Polypropylene capacitors also work well for both C_{STRG} and C_{INT}.

10. For a given leakage into C_{STRG} of I_{STRG}:

$$\Delta V_{STRG} = \frac{\Delta t\ I_{AZ}}{C_{STRG}}$$

where Δt = a measure interval $= \frac{2}{3} \times \frac{1}{F_{SAMPLE}}$

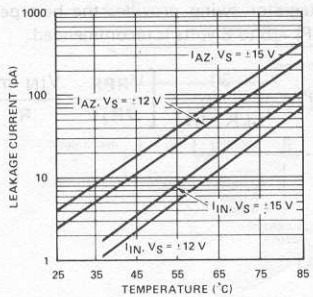
ΔV_{STRG} will inject a ΔI integrator of $\Delta V_{STRG}/R_3$

Now a ΔI integrator would have been equivalent to a $\Delta V_{IN}/R_2$

So the equivalent input drift is

$$\Delta V_{IN} = \frac{1}{2} \times \frac{R_2}{R_3} \times \frac{2}{3} \times \frac{I_{STRG}}{F_{SAMPLE} \bullet C_{STRG}}$$

Typical Leakage Over Temperature



the ½ factor is provided by integrator action.

Example: We wish to see 1 count (0.1 mV of ΔV_{IN} on the 2 V range) of drift for the circuit of Figure 7 with I_{STRG} = 100 pA @ 70° C. What C_{STRG} is needed?

Answer:

$$C_{STRG} = \frac{R_2}{R_3} \times \frac{1}{3} \times \frac{I_{STRG}}{F_{SAMPLE} \cdot \Delta V_{IN}} =$$

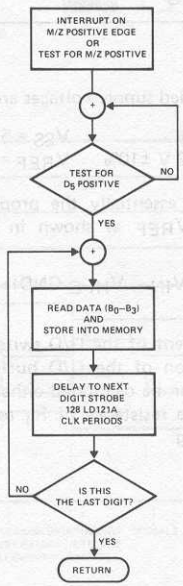
$$\frac{100K\ \Omega}{62K\ \Omega} \times \frac{1}{3} \times \frac{10^{-10}\ F}{3\ Hz \times 10^{-4}\ V}$$

= 0.18 μF Minimum

11. Interfacing the LD120/LD121A to Microprocessors: A description of interfacing the LD120/LD121A to the 8080 μP is given in AN77-3. Some of the timing details warrant description here.

The end-of-conversion is determined by gating $\overline{M/Z} \cdot \overline{U/D} \cdot \overline{COMP}$. At this time, all BCD latches are updated with the contents of the latest conversion.

We recommend using the negative edge of M/Z to interrupt the processor. Next, test for a high D_5 digit strobe (MSD). Once D_5 is high load the BCD data from B_0–B_3 lines and the polarity information from the SIGN/OR/UR line. Next delay 128 LD121A clock times (this assures that the D_4 data is valid) then load B_0–B_3 lines containing the D_4 data. Next delay another 128 LD121A clock times (this assures that the D_3 data is valid) then load B_0–B_3 lines containing the D_3 data. Repeat this process for D_2 and finally the D_1 (LSD) data load. In flowchart form (see Figure 6).

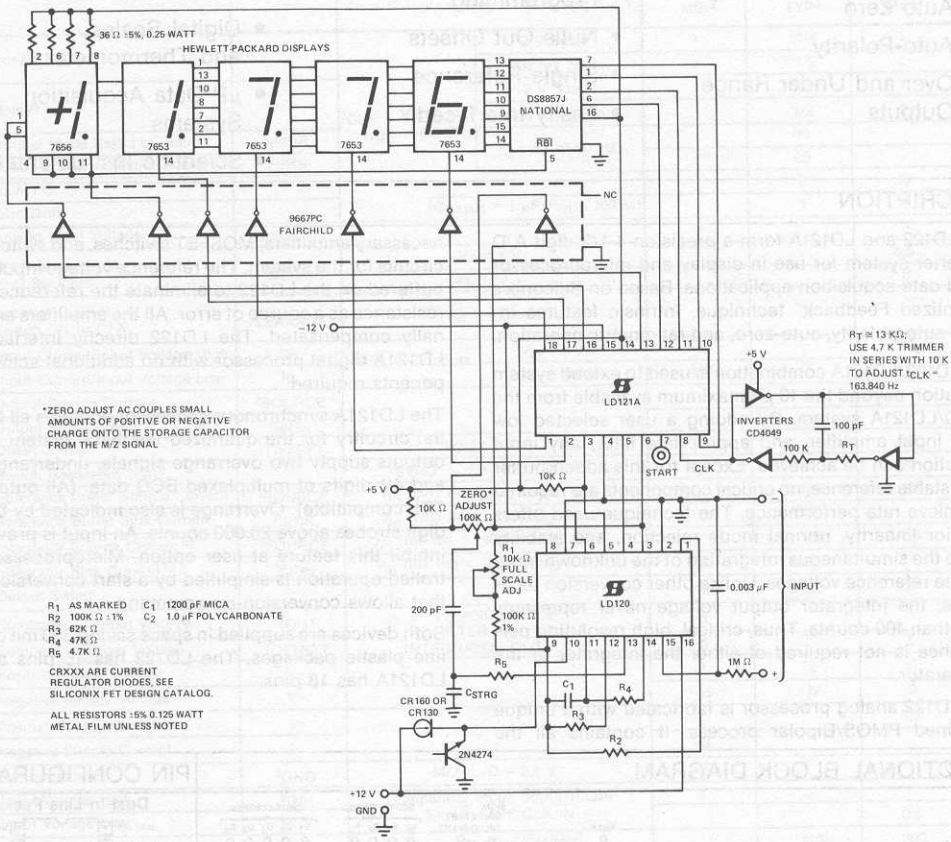


Flow Chart for 8080 Interface
Figure 6

APPLICATIONS (Cont.)

CIRCUIT BENEFITS

- Overrange Blinking
- 0 → ±1.9999 Input Voltages
- Zero Adjust to Null Offset Introduced by PC Board Leakages and Comparator



4½ Digit DVM
Figure 7