LC898217XH

Auto Focus (AF) Controller & Driver

ON Semiconductor®

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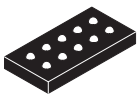

WLCSP10, 1.04x2.04x0.265

1. Overview

LC898217XH is the AF control LSI. It consists of 1 system of feedback circuit for AF control. Built-in equalizer circuit using digital operation. Built-in A/D converter, D/A converter, Constant Current Driver. LC898217XH contains an internal EEPROM. It easily accomplishes Hall calibration and power-on sequence. Also LC898217XH has fast settling function for quickly moving focus lens. This is suitable for small & thinner camera module.

2. Features

- Built-in equalizer circuit using digital operation
  - AF control equalize circuit
  - Any coefficient can be specified by 2-wire serial I/F (TWIF)
- 2-wire serial interface
  (The communication protocol is compatible with I^2C.)
- Built-in A/D converter
  - Input 1 channel
- Built-in D/A converter
  - Output 2 channel (Hall offset, Constant current bias)
- Built-in VGA
  - Hall Amp
  - 1 channel
- Built-in EEPROM
  - 128 byte (16 byte/page)
- Built-in OSC
- Built-in Constant Current Driver
  - 110 mA
  - 1 channel
- Package
  - WL-CSP 10-pin
  - Pb-Free, Halogen Free
- Supply voltage
  - V_{DD} (2.6 V to 3.3 V)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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3. Pin Description

TYPE					
I	INPUT	P	Power supply, GND	NC	NOT CONNECT
O	OUTPUT				
B	BIDIRECTION				

■ 2-wire serial interface

SCL	I	2-wire serial interface clock pin
SDA	B	2-wire serial interface data pin

■ Hall interface

BIASO	O	D/A output (to Hall element)
OPINP	I	VGA input (from Hall element)
OPINM	I	VGA input (from Hall element)

■ Driver interface

OUT1	O	Driver output (to Actuator)
OUT2	O	Driver output (to Actuator)

■ Power supply pin

V_{DD}	P	Power supply
V_{SS}	P	GND

■ Test pin

PORT	B	Analog test signal input/output Convergence detection monitor output VSYNC input

* Process when pins are not used

PIN TYPE “O” – Ensure that it is set to OPEN.
PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the V_{DD} or V_{SS} even when it is unused.
(Please contact ON Semiconductor for more information about selection of V_{DD} or V_{SS}.)
PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

* In case of connecting PORT pin with HOST CPU

When LC898217XH is power off and HOST CPU is power on, a HOST CPU pin connected with PORT pin have to be fixed "L" level.

4. Pin Layout

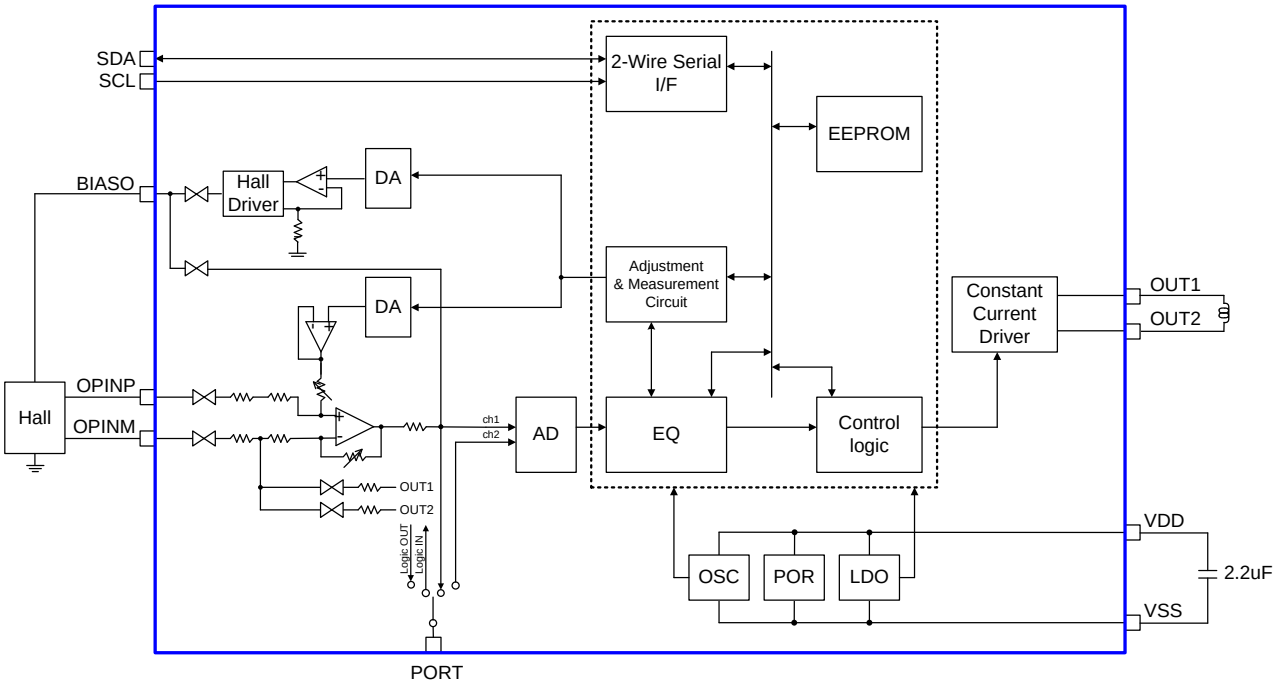
Circuit Name	Number of PINs	Circuit Name	Number of PINs
Analog	4	Driver	2
Logic	2	Power	2

“PORT” pin has analog function and digital function.

BOTTOM VIEW

	A	B
1	OUT2	OUT1
2	VSS	VDD
3	PORT	SCL
4	BIASO	SDA
5	OPINM	OPINP

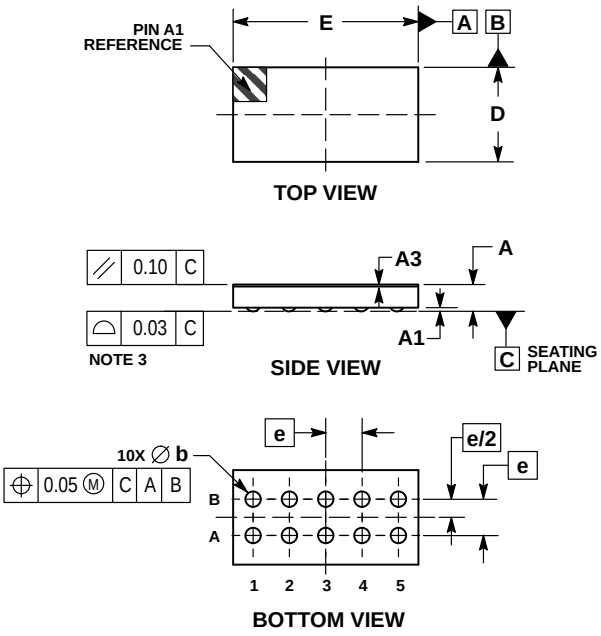
5. Block Diagram



6. Package Dimensions

unit : mm

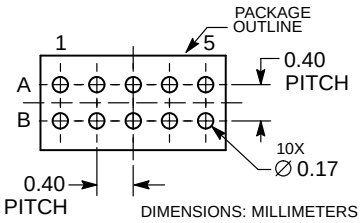
WLCSP10, 1.04x2.04x0.265
CASE 567TH
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.240	0.265	0.290
A1		0.040 REF	
A3		0.025 REF	
b	0.12	0.17	0.22
D	0.99	1.04	1.09
E	1.99	2.04	2.09
e		0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

7. Electrical Characteristics

1) Absolute Maximum Rating at V_{SS} = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	$V_{DD}33$ max	Ta ≤ 25°C	−0.3 to 4.6	V
Input/output voltage	V_I33, V_O33	Ta ≤ 25°C	−0.3 to $V_{DD}33$+0.3	V
Storage ambient temperature	Tstg		−55 to 125	°C
Operating ambient temperature	Topr		−30 to 70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2) Allowable Operating Ratings at Ta = −30 to 70°C, V_{SS} = 0 V

3 V power supply (V_{DD})

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DD}33$	2.6	2.8	3.3	V
Input voltage range	V_{IN}	0		$V_{DD}33$	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3) DC Characteristics : Input/Output level at V_{SS} = 0 V, V_{DD} = 2.6 to 3.6 V, Ta = −30 to 70°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable pins
High-level input voltage	V_{IH}	CMOS compliant Schmidt	1.4			V	SCL, SDA, PORT
Low-level input voltage	V_{IL}				0.4	V	
High-level output voltage	V_{OH}	IOL = −2 mA	V_{DD}−0.4			V	PORT
Low-level output voltage	V_{OL}	IOL = 2 mA			0.4	V	SDA, PORT
Pulldown resistor	Rdn		50		220	kΩ	PORT

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4) Driver output (OUT1, OUT2) at V_{SS} = 0 V, V_{DD} = 2.8 V, Ta = 25°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable pins
Maximum current	Ifull		105		115	mA	OUT1, OUT2
Output leak current	Ioleak			1		μA	

5) Non-volatile Memory Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable circuit
Endurance	EN				1000	Cycles	EEPROM
Data retention	RT		10			Years	
Write time	tWT				20	ms	

8. AC Characteristics

8.1 V_{DD} supply timing

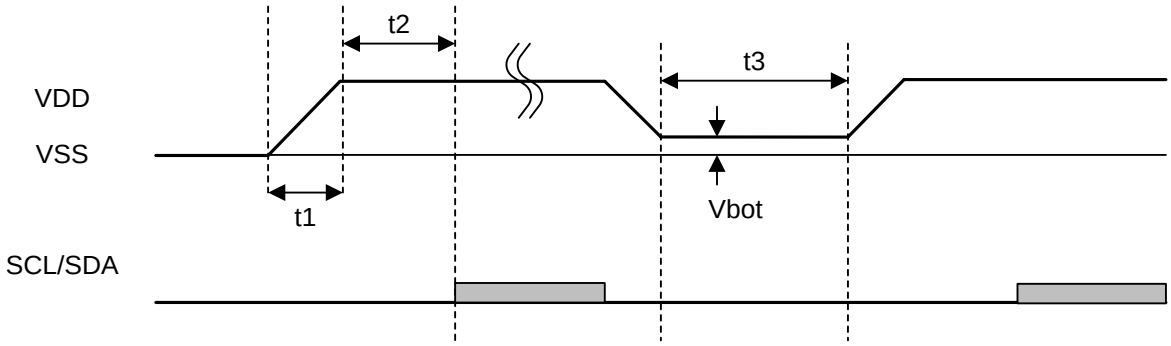


Figure 8.1 V_{DD} supply timing

It is available to use 2-wire serial interface 5 ms later for Power On Reset of V_{DD}.

Item	Symbol	Min	Typ	Max	Unit
V_{DD} turn on time	t1			3	ms
2-wire serial interface start time from V_{DD} on	t2	5			ms
V_{DD} off time	t3	100			ms
Bottom Voltage	Vbot			0.1	V

8.2 AC specification

Figure 8.2 shows interface timing definition and Table 8.1 shows electric characteristics.

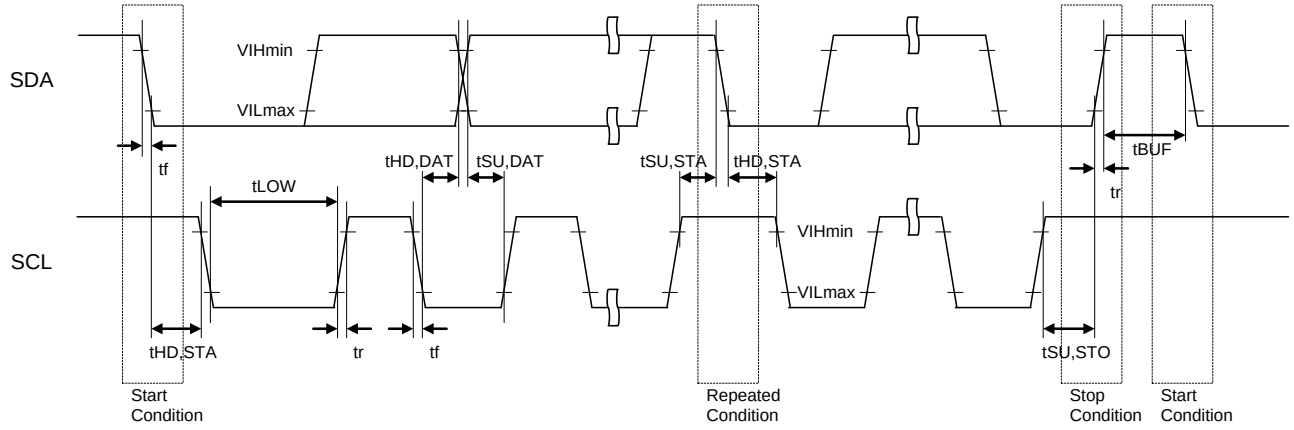


Figure 8.2 2-wire serial interface timing definition

Table 8.1 Electric characteritics for 2-wire serial interface (AC characteristics)

Item	Symbol	Pin name	Fast-mode			Fast-mode Plus			Unit
			Min	Typ	Max	Min	Typ	Max	
SCL clock frequency	FSCL	SCL			400			1000	kHz
START condition hold time	tHD, STA	SCL SDA	0.6			0.26			µs
SCL clock Low period	tLOW	SCL	1.3			0.5			µs
SCL clock High period	tHIGH	SCL	0.6			0.26			µs
Setup time for repetition START condition	tSU, STA	SCL SDA	0.6			0.26			µs
Data hold time	tHD, DAT	SCL SDA	0 *		0.9	0 *			µs
Data setup time	tSU, DAT	SCL SDA	100			50			ns
SDA, SCL rising time	tr	SCL SDA			300			120	ns
SDA, SCL falling time	tf	SCL SDA			300			120	ns
STOP condition setup time	tSU, STO	SCL SDA	0.6			0.26			µs
Bus free time between STOP and START	tBUF	SCL SDA	1.3			0.5			µs

* : LC898217XH is designed for a condition with typ. 20 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898217XH-MH	WLCSP10, 1.04x2.04x0.265 (Pb-Free / Halogen Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

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