Ordering number : EN※4161

CMOS LSI

No. ※4161

LC8920

FAX Modem

Preliminary

Overview

The LC8920 is designed for synchronous, half-duplex, 9,600 bps CMOS single chip modem applications using public telephone networks. This LSI has built-in modulation-demodulation components meeting modem requirements, along with transmitter-receiver filters and V.24 interfacing. In addition, construction of Group 3 and Group 2 facsimile systems has been simplified.

The LC8920 conforms to V.29, V.27ter, T.30, T.4 and T.3 recommendations for telecommunications as set forth by CCITT (CCITT: International Telephone and Telegraph Consultative Committee). Transfer speeds supported by this LSI include 300, 2400, 4800, 7200 and 9600 bps rates. Advanced signal processing functions permit data transmission and reception even under poor line conditions.

Features

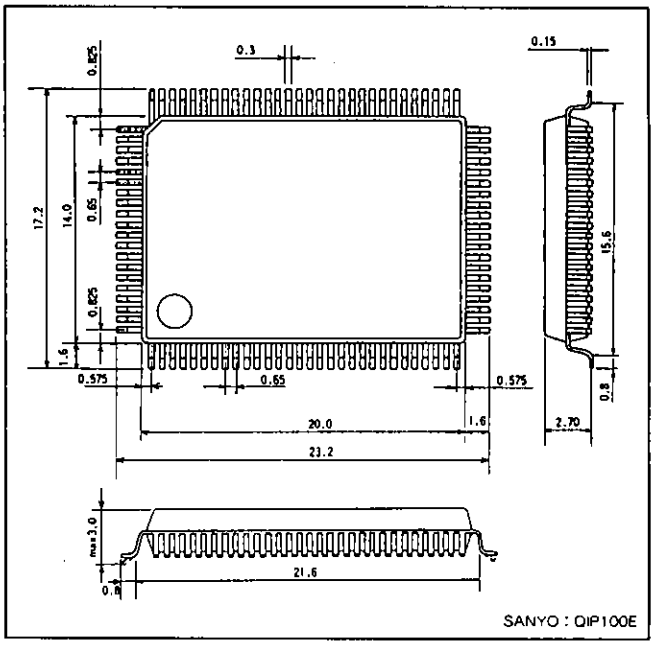
- CCITT recommendations
  V.29 (9600 bps, 7200 bps and 4800 bps)
  V.27ter (4800 bps and 2400 bps)
  V.21ch2 (300 bps)
  T.30, T.4 and T.3
- Supports high-speed (V.29 and V.27ter) and low-speed (V.21ch2) simultaneous reception
- Half-duplex operation
- Capable of supporting Group 3 and Group 2 facsimiles
- Programmable signal tone generation and detection
- Programmable DTMF (Dual Tone Multi Frequency) generation and detection
- Built-in adaptive automatic equalizer
- Built-in amplitude equalizers (rink amplitude equalizer and cable amplitude equalizer)
- Built-in transmitter-receiver filter (digital filter)
- Supports transmit level adjustment (–0.5 dBm step intervals)
- Dynamic receiving range (–7 dBm to –43 dBm)
- Supports adjustment of transmit-receive sensitivity

Continued on the following page.

Package Dimensions

unit : mm

3151-QIP100E



Continued from the preceding page.

- DTE (Data Terminal Equipment) interface
  Serial interface (conforming to CCITT recommended V.24) and parallel interface
- HDLC (High-level Data Link Control) framing function (during applications of CCITT recommended V.21 ch2)
- Programmable call progress tone detection
- Built-in eye-pattern generator
- Built-in diagnostic function
- Low consumption electric power (typ 250mW) and adopted CMOS (Complementary Metal Oxide Semiconductor)
- +5 V single power supply

Specifications

Absolute Maximum Ratings at GND = 0V

				unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
I/O voltage	V_I, V_O	Ta = 25°C	–0.3 to V_{DD} +0.3	V
Allowable power dissipation	Pd max	Ta≤70°C	400	mW
Operating temperature range	Topr		–30 to +70	°C
Storage temperature range	Tstg		–55 to +125	°C
Solder heat resistance		Hand soldering (3 seconds)	350	°C
		Reflow (10 seconds)	235	°C

Allowable Operating Range at Ta = –30 to +70°C, GND = 0V

		min	typ	max	unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Input voltage range	V_{IN}	0		V_{DD}	V

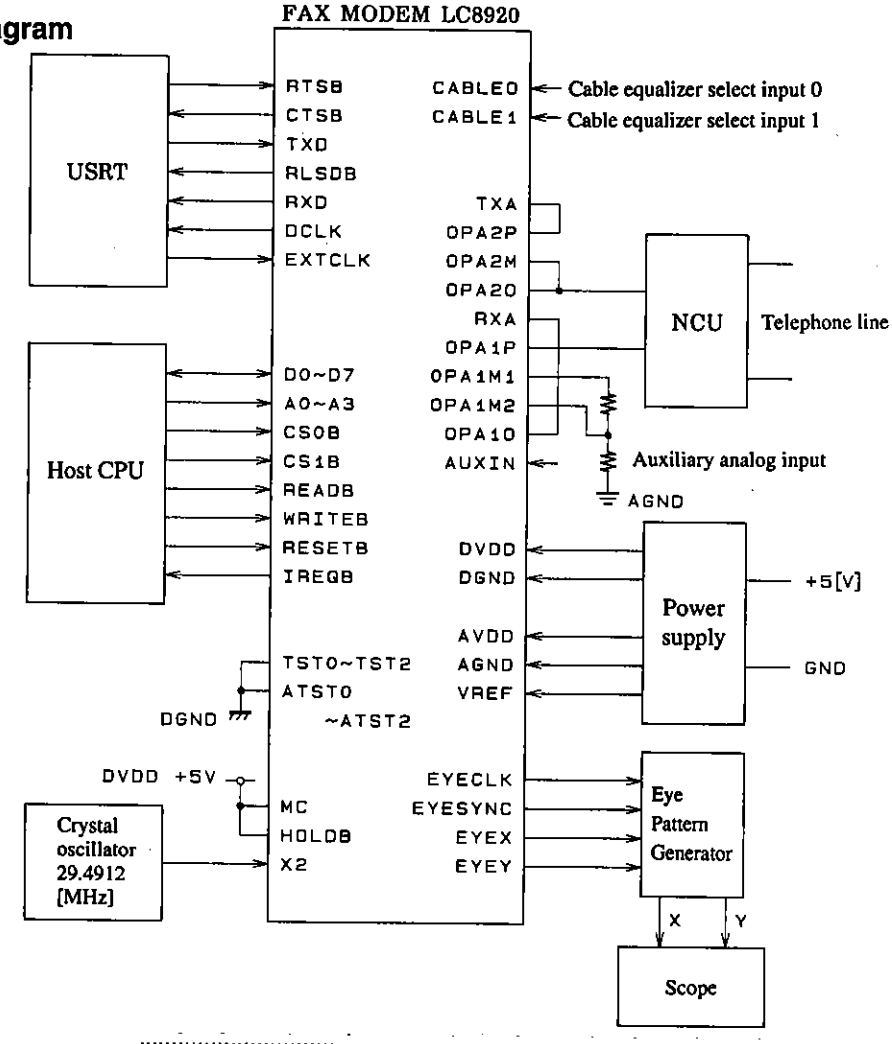
Electrical Characteristics

DC Characteristics Input Characteristic at GND = 0 V, V_{DD} = 4.5 to 5.5 V and Ta = -30 to +70°C

Item	Symbol	Condition	Adaptive Pin	min	typ	max	unit
Input "H" level voltage	V_{IH}	TTL correspondence	RESETB, MC, A3 to A0, D7 to D0, CS0B, CS1B, READB, WRITEB, RTSB, TXD, CABLE1, CABLE0, TST2 to TST0, PD15 to PD0, HOLDB, EXTCLK	2.2			V
Input "L" level voltage	V_{IL}	TTL correspondence				0.8	V
Input leakage voltage	I_L	V_{IN} = GND, V_{DD}		–1		+1	µA
Output "H" level voltage	V_{OH}	I_{OH} = –3mA: TTL	WEB, D7 to D0, IRQB, RLSDB, CTSB, RXD, DCLK, EYEX, EYEY, EYECLK, EYESYNC, PD15 to PD0, PA13 to PA0, MENB, CLKOUT, HOLDACB	2.4			V
Output "L" level voltage	V_{OL}	I_{OL} = 3mA: TTL				0.4	V
Output leakage voltage	Ioz	During high-impedance output	D7 to D0, PD15 to PD0	–10	+10		µA
Input frequency	f_{IN}		X2		29.4912		MHz
V_{REF} input voltage	V_{REF}		V_{REF}		V_{DD}/2		V
V_{REF} impedance	R_{REF}			1			MΩ
Input voltage range	V_{IA}		RAX	V_{DD} X 0.2		V_{DD} X 0.8	V
Output voltage range	V_{OA}		TXA	V_{DD} X 0.2		V_{DD} X 0.8	V
Output impedance	R_O					7.0	kΩ
Consumable current	I_{DD}	V_{DD} = 5.5V				80	mA
		V_{DD} = 5.0V			50		

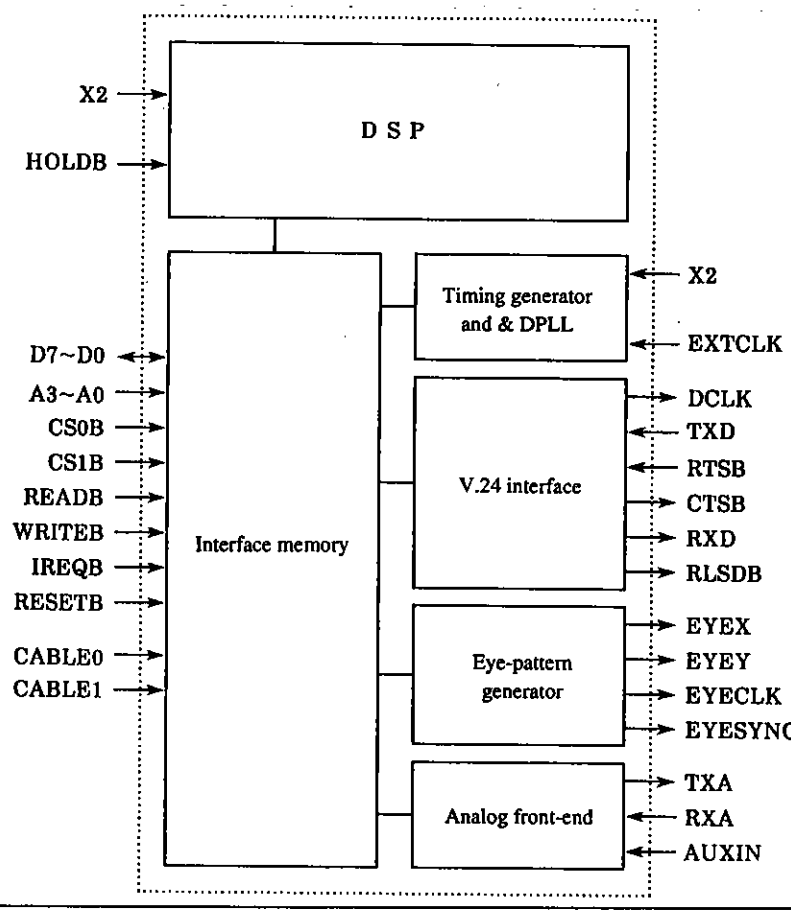
Note: GND = (AGND, DGND), V_{DD} = (AV_{DD}, DV_{DD})

System Block Diagram



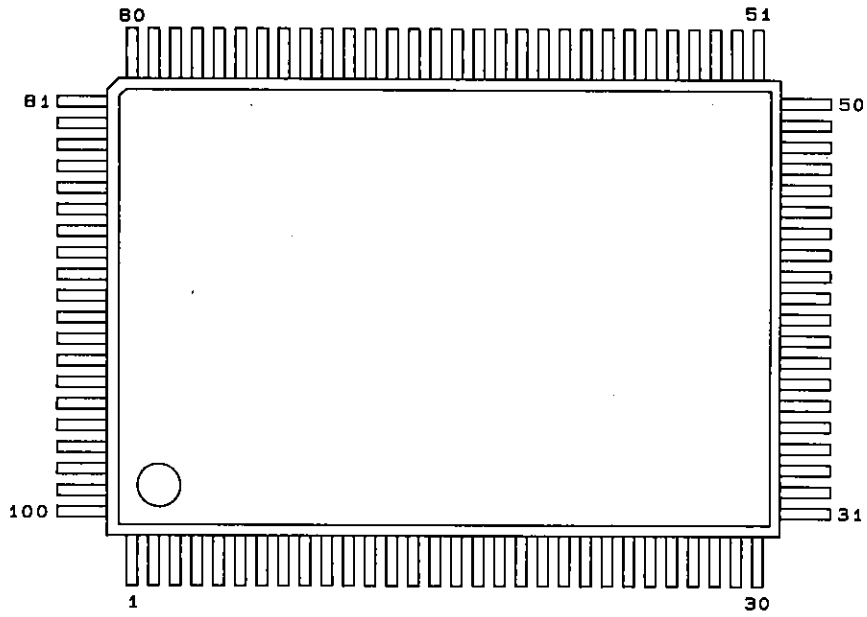
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Block Diagram



Pin Assignment

I : Input pin
O : Output pin
B : Bidirectional pin
P : Power source pin
NC : No Connection



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Number	Name	type
1	RESETB	I
2	DGND	P
3	X2	I
4	WEB	O
5	MC	I
6	A3	I
7	A2	I
8	A1	I
9	A0	I
10	D7	B
11	D6	B
12	D5	B
13	D4	B
14	DGND	P
15	DV_{DD}	P
16	D3	B
17	D2	B
18	D1	B
19	D0	B
20	CS0B	I
21	CS1B	I
22	READB	I
23	WRITEB	I
24	IRQB	O
25	RTSB	I
26	RLSDB	O
27	CTSB	O
28	RXD	O
29	TXD	I
30	DGND	P
31	DCLK	O
32	EXTCLK	I
33	EYEX	O
34	EYEY	O

Number	Name	type
35	EYECLK	O
36	EYESYNC	O
37	CABLE0	I
38	CABLE1	I
39	TST0	I
40	DGND	P
41	DV_{DD}	P
42	TST1	I
43	TST2	I
44	ATST0	O
45	AGND	P
46	AV_{DD}	P
47	ATST2	O
48	ATST1	O
49	V_{REF}	I
50	AUXIN	I
51	RXA	I
52	OPA10	O
53	OPA1M1	I
54	OPA1M2	I
55	OPA1P	I
56	OPA2P	I
57	OPA2M	I
58	OPA20	O
59	TXA	O
60	AGND	P
61	AV_{DD}	P
62	DGND	P
63	DV_{DD}	P
64	PD15	B
65	PD14	B
66	PD13	B
67	PD12	B
68	PD11	B

Number	Name	type
69	PD10	B
70	PD9	B
71	DGND	P
72	PD8	B
73	PD7	B
74	PD6	B
75	PD5	B
76	PD4	B
77	PD3	B
78	PD2	B
79	PD1	B
80	PD0	B
81	PA13	O
82	PA12	O
83	PA11	O
84	PA10	O
85	PA9	O
86	PA8	O
87	PA7	O
88	PA6	O
89	DV_{DD}	P
90	DGND	P
91	PA5	O
92	PA4	O
93	PA3	O
94	PA2	O
95	PA1	O
96	PA0	O
97	HOLDACB	O
98	HOLDB	I
99	MENB	O
100	CLKOUT	O

Pin Description

1. Power Supply, Clock and Test Pins

Name	Pin No.	I/O	Functions
DV_{DD}	15 41 63 89	P	These pins are for connecting to the digital power supply (+5 V).
DGND	2 14 30 40 62 71 90	P	These pins are for connecting to the digital ground (0 V).
AV_{DD}	46 61	P	These pins are for connecting to the analog power supply (+5 V).
AGND	45 60	P	These pins are for connecting to the analog ground (0 V).
V_{REF}	49	P	This pin is for connecting to the power supply reference (AV_{DD}/2V).
X2	3	I	This pin is for connecting to the master clock (29.4912 MHz).
CLKOUT	100	O	This pin outputs 1/4 of the frequency (7.3728 MHz) of the master clock (X2).
TST0 TST1 TST2	39 42 43	I	These pins are for use during testing and are connected to the ground (0 V).
ATST0 ATST1 ATST2	44 48 47	O	These pins are for use with analog testing.

2 Data Terminal Equipment (DTE) Interface

Name	Pin No.	I/O	Functions
D0 D1 D2 D3 D4 D5 D6 D7	19 18 17 16 13 12 11 10	I/O	These pins are for host CPU and data bus interfacing.
A0 A1 A2 A3	9 8 7 6	I	These pins are for host CPU and address bus interfacing.
CS0B CS1B	20 21	I	These pins are for chip select signal interfacing.
READB	22	I	This pin is for interfacing the interface memory read signal.
WRITEB	23	I	This pin is for interfacing the interface memory write signal.
IREQB	24	O	This pin is for interfacing the interruption request signal to the host CPU.
RESETB	1	I	This pin is for interfacing the system reset signal.

3. Diagnosis

Name	Pin No.	I/O	Functions
EYECLK	35	O	This pin is for diagnosis of the timing clock for generating eye pattern data. It can be used with an external shift register shift clock.
EYESYNC	36	O	This pin is for diagnosis of eye pattern synchronization signal.
EYEX EYEY	33 34	O	These pins are for eye pattern data (8 bit MSB first) serial output.

4. V.24 Interface

Name	Pin No.	I/O	Functions
RTSB	25	I	This pin is for interfacing the request to send (RTS) signal. When RTSB sets to an "L" level, transmission begins. When RTSB sets to an "H" level, transmission stops.
CTSB	27	O	This pin is for interfacing the clear to send (CTS) signal. When CTSB sets to an "L" level, transmission can proceed. When CTSB sets to an "H" level, transmission will not be accepted.
RLSDB	26	O	This pin is for interfacing received line signal detect (RLSD). When RLSDB sets to an "L" level and transmission is set to proceed, this pin functions as a timing signal for transmitting transmission data to a terminal.
TXD	29	I	This pin is for input of transmit data (TXD).
RXD	28	O	This pin is for output of receive data (RXD).
DCLK	31	O	This pin is for clock output using transmit-receive data.
EXTCLK	32	I	This is the external input clock pin for use with Group 2.

5. Cable Equalizer

Name	Pin No.	I/O	Functions
CABLE0	37	I	This pin is for cable equalizer sector 0.
CABLE1	38	I	This pin is for cable equalizer sector 1.

6. Analog Signal

Name	Pin No.	I/O	Functions
TXA	59	O	This pin is for transmitter analog output.
RXA	51	I	This pin is for receiver analog input.
AUXIN	50	I	This pin is for auxiliary analog input.
OPA2P	56	I	This pin is for transmission buffer input and output. (For further details, refer to the circuit diagram.)
OPA2M	57	I	
OPA20	58	O	
OPA1P	55	I	This pin is for receiving buffer input and output. (For further details, refer to the circuit diagram.)
OPA1M1	53	I	
OPA1M2	54	I	
OPA10	52	O	

7. System Signal

Name	Pin No.	I/O	Functions
MC	5	I	This pin is for the program mode control signal and is connected to a +5 V power supply.
HOLDB	98	I	This pin is for the system hold signal and is connected to a +5 V power supply.

Note: Other pins are all left open.

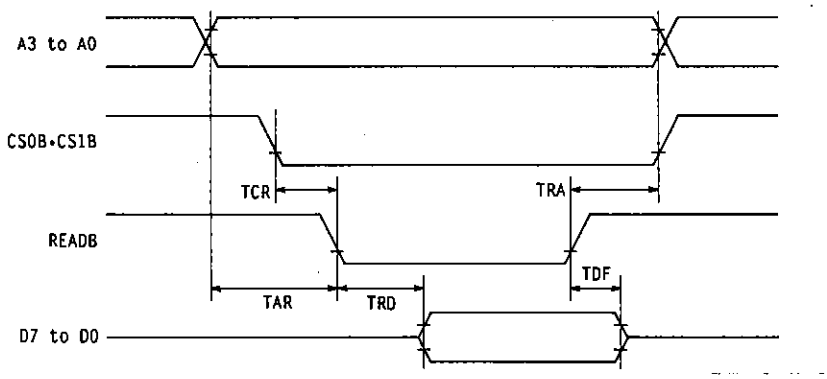
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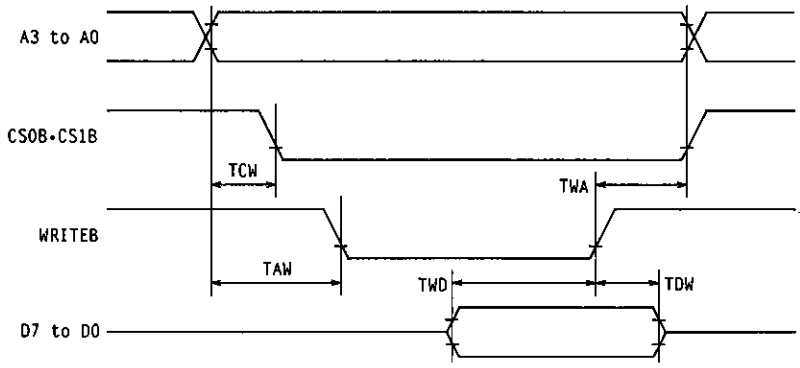
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2. AC Characteristics

• DTE Interface Timing

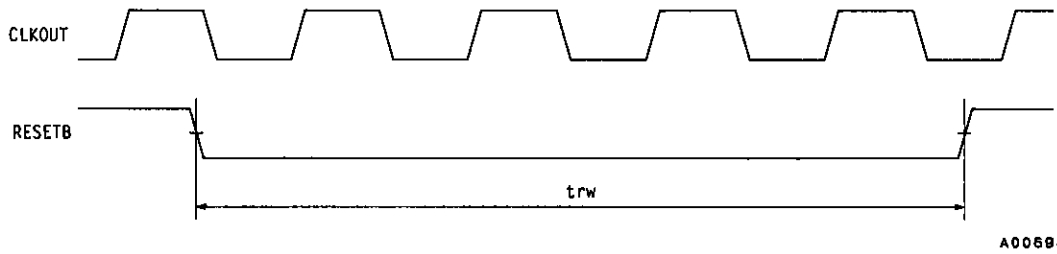


(a) Read Cycle Timing



(b) Write Cycle Timing

• Reset Timing



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Item	Symbol	min	max	unit
Address stabilization time (in response to READB signal)	TAR	40		nsec
Chip-select stabilization time (in response to READB signal)	TCR	40		nsec
Data delay time	TRD	30		nsec
Data float delay time	TDF	10		nsec
Address hold time (in response to READB signal)	TRA	10		nsec
Address stabilization time (in response to WRITEB signal)	TAW	40		nsec
Chip-select stabilization time (in response to WRITEB signal)	TCW	40		nsec
Data setting time	TDW	30		nsec
Data hold time	TWD	10		nsec
Address hold time (in response to WRITEB signal)	TWA	10		nsec
Reset pulse width	Trw	500		nsec

Circuit Connection Diagram

