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# LC87F1JJ8A

CMOS IC

FROM 192K byte, RAM 24576 byte on-chip

## 8-bit 1-chip Microcontroller with USB-host controller

### Overview

The LC87F1JJ8A is an 8-bit microcomputer that, integrates on a single chip a number of hardware features such as 192K-byte flash ROM, 24576-byte RAM, an on-chip debugger, a 16-bit timer/counter, a 16-bit timer, four 8-bit timers, a base timer serving as a realtime clock, 3 channels of synchronous SIO interface with automatic data transfer capabilities, an asynchronous/synchronous SIO interface, a UART interface, a full-speed USB interface (host control function), a 12-channel AD converter, 2 channels of 12-bit PWM, a system clock frequency divider, an infrared remote control receiver circuit, and an interrupt feature.

### Features

#### ■Flash ROM

- 196608 × 8 bits
- Capable of on-board programming with a wide range of supply voltages: 3.0 to 5.5V
- Block-erasable in 128 byte units
- Writes data in 2-byte units

#### ■RAM

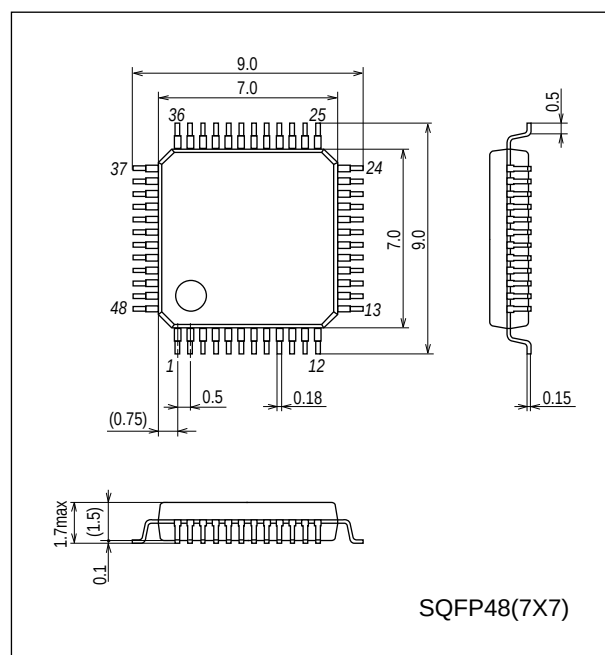
- 24576 × 9 bits

#### ■Package Form

- SQFP48(7×7): Lead-/Halogen-free type

### Package Dimensions

unit : mm (typ) 3163B



\* This product is licensed from Silicon Storage Technology, Inc. (USA).

**■ Bus Cycle Time**

- 83.3ns (When CF=12MHz)

Note: The bus cycle time here refers to the ROM read speed.

**■ Minimum Instruction Cycle Time (tCYC)**

- 250ns (When CF=12MHz)

**■ Ports**

- I/O ports

Ports whose I/O direction can be designated in 1-bit units    28 (P10 to P17, P20 to P27, P30 to P34, P70 to P73, PWM0, PWM1, XT2)

Ports whose I/O direction can be designated in 4-bit units    8 (P00 to P07)

- USB ports    2 (UHD+, UHD-)
- Dedicated oscillator ports    2 (CF1, CF2)
- Input-only port (also used for oscillation)    1 (XT1)
- Reset pin    1 (RES)
- Power supply pins    6 (VSS1 to VSS3, VDD1 to VDD3)

**■ Timers**

- Timer 0: 16-bit timer/counter with 2 capture registers.

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers)  
+ 8-bit counter (with two 8-bit capture registers)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)

Mode 3: 16-bit counter (with two 16-bit capture registers)

- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/  
counter with an 8-bit prescaler (with toggle outputs)

Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels

Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)  
(toggle outputs also possible from lower-order 8 bits)

Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs)  
(lower-order 8 bits may be used as PWM outputs)

- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer

1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.

2) Interrupts programmable in 5 different time schemes

**■ SIO**

- SIO0: Synchronous serial interface

1) LSB first/MSB first mode selectable

2) Transfer clock cycle: 4/3 to 512/3 tCYC

3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1-bit units)  
(Suspension and resumption of data transmission possible in 1 byte units)

- SIO1: 8-bit asynchronous/synchronous serial interface

Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)

Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)

Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)

Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

- SIO4: Synchronous serial interface

1) LSB first/MSB first mode selectable

2) Transfer clock cycle: 4/3 to 1020/3 tCYC

3) Automatic continuous data transmission (1 to 8192 bytes, specifiable in 1 byte units)  
(Suspension and resumption of data transmission possible in 1 byte units or in word units)

4) Auto-start-on-falling-edge function

5) Clock polarity selectable

6) CRC16 calculator circuit built in

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- SIO9: Synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Transfer clock cycle: 4/3 to 1020/3 tCYC
  - 3) Automatic continuous data transmission (1 to 8192 bytes, specifiable in 1 byte units)  
(Suspension and resumption of data transmission possible in 1 byte units or word units)
  - 4) Auto-start-on-falling-edge function
  - 5) Clock polarity selectable
  - 6) CRC16 calculator circuit built in

### ■ Full Duplex UART

- 1) Data length: 7/8/9 bits selectable
- 2) Stop bits: 1 bit (2 bits in continuous transmission mode)
- 3) Baud rate: 16/3 to 8192/3 tCYC

### ■ AD Converter: 8 bits × 12 channels

### ■ PWM: Multifrequency 12-bit PWM × 2 channels

### ■ Infrared Remote Control Receiver Circuit

- 1) Noise rejection function (noise filter time constant: Approx. 120μs when the 32.768kHz crystal oscillator is selected as the base clock)
- 2) Supports data encoding systems such as PPM (Pulse Position Modulation) and Manchester encoding.
- 3) X'tal HOLD mode release function

### ■ USB Interface (host control function)

- 1) Compliant with full-speed (12M bps) specifications
- 2) Supports 4 transfer types (control transfer, bulk transfer, interrupt transfer, and isochronous transfer).

### ■ Audio Interface

- 1) Sampling frequency (fs): 8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz
- 2) Master clock frequency: 256fs/384fs
- 3) Bit clock selectable: 48fs/64fs
- 4) Data bit length: 16/18/20/24 bits
- 5) LSB first/MSB first mode selectable
- 6) Left-justification/right-justification/I2S format selectable

### ■ Watchdog Timer

- Watchdog timer using external RC circuitry
- Interrupt and reset signals selectable

### ■ Clock Output Function

- 1) Can output a clock with a clock rate of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source oscillator clock selected as the system clock.
- 2) Can output the source oscillation clock for the subclock.

## ■ Interrupts

- 41 sources, 10 vector addresses

- 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
- 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Level  | Interrupt Source                                           |
|-----|----------------|--------|------------------------------------------------------------|
| 1   | 00003H         | X or L | INT0                                                       |
| 2   | 0000BH         | X or L | INT1                                                       |
| 3   | 00013H         | H or L | INT2/T0L/INT4/UHC bus active/remote control signal receive |
| 4   | 0001BH         | H or L | INT3/INT5/base timer                                       |
| 5   | 00023H         | H or L | T0H/INT6/UHC device attach/UHC device detach/UHC resume    |
| 6   | 0002BH         | H or L | T1L/T1H/INT7/SIO9/AIF start                                |
| 7   | 00033H         | H or L | SIO0/UART1 receive                                         |
| 8   | 0003BH         | H or L | SIO1/SIO4/UART1 transmit/AIF end                           |
| 9   | 00043H         | H or L | ADC/T6/T7/UHC-ACK/UHC-NAK/UHC error/UHC-STALL              |
| 10  | 0004BH         | H or L | Port 0/PWM0/PWM1/T4/T5/UHC-SOF/DMCOPY/AIF error            |

- Priority levels  $X > H > L$
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

## ■ Subroutine Stack Levels: 12288 levels maximum (The stack is allocated in RAM.)

## ■ High-speed Multiplication/Division Instructions

- 16 bits  $\times$  8 bits (5 tCYC execution time)
- 24 bits  $\times$  16 bits (12 tCYC execution time)
- 16 bits  $\div$  8 bits (8 tCYC execution time)
- 24 bits  $\div$  16 bits (12 tCYC execution time)

## ■ Oscillation and PLL Circuits

- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock
- Crystal oscillation circuit: For system clock, and realtime clock
- PLL circuit (internal): For USB interface (see Fig.5) and audio interface (see Fig. 6)

## ■ Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) There are three ways of releasing the HALT mode.
    - (1) Setting the reset pin to the lower level.
    - (2) System resetting by watchdog timer
    - (3) Generating an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The PLL base clock generator, CF, RC and crystal oscillators automatically stop operation.
  - 2) There are five ways of releasing the HOLD mode.
    - (1) Setting the reset pin to the lower level
    - (2) System resetting by watchdog timer
    - (3) Having an interrupt source established at one of the INT0, INT1, INT2, INT4, and INT5 pins
      - \* The INT0 and INT1 pins must be configured only for level detection.
    - (4) Having an interrupt source established at port 0
    - (5) Having an bus active interrupt source established in the USB host control circuit
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  - 1) The PLL base clock generator, CF and RC oscillator automatically stop operation.
  - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  - 3) There are seven ways of releasing the X'tal HOLD mode.
    - (1) Setting the reset pin to the low level
    - (2) System resetting by watchdog timer
    - (3) Having an interrupt source established at one of the INT0, INT1, INT2, INT4, and INT5 pins
      - \* The INT0 and INT1 pins must be configured only for level detection.
    - (4) Having an interrupt source established at port 0
    - (5) Having an interrupt source established in the base timer circuit
    - (6) Having an bus active interrupt source established in the USB host control circuit
    - (7) Having an interrupt source established in the infrared remote controller receiver circuit

## ■ Development Tools

- On-chip debugger: TCB87- type B + LC87F1JJ8A

## ■ Flash ROM Programming Boards

| Package     | Programming board |
|-------------|-------------------|
| SQFP48(7×7) | W87F55256SQ       |

## ■ Flash ROM Programmer

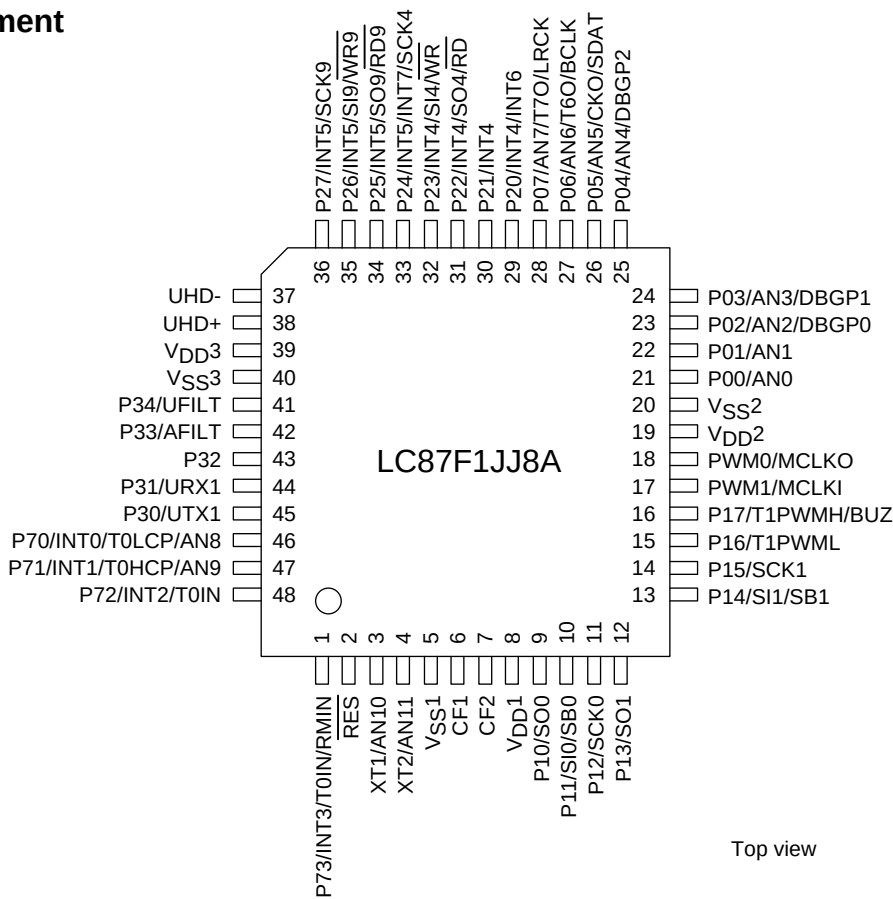
| Maker                                                          |                          | Model                                                                               | Supported Version                                                            | Device     |
|----------------------------------------------------------------|--------------------------|-------------------------------------------------------------------------------------|------------------------------------------------------------------------------|------------|
| Flash Support Group, Inc.<br>(FSG)                             | Single                   | AF9708/<br>AF9709/AF9709B/AF9709C<br>(including Ando Electric Co., Ltd. models)     | Rev. 03.12 or later                                                          | LC87F1JJ2A |
| Flash Support Group, Inc.<br>(FSG)<br>+<br>Our company(Note 1) | Onboard<br>single/ganged | AF9101/AF9103(main unit)<br>(FSG)<br>SIB87(interface driver)<br>(Our company model) | (Note 2)                                                                     | LC87F1JJ2A |
| Our company                                                    | Single/ganged            | SKK/SKK Type B<br>(SANYO FWS)                                                       | Application version:<br>1.04 or later<br>Chip data version:<br>2.17 or later | LC87F1JJ8  |
|                                                                | Onboard<br>single/ganged | SKK-DBG Type B<br>(SANYO FWS)                                                       |                                                                              |            |

Note 1: PC-less standalone onboard programming is possible using the FSG onboard programmer (AF9101/AF9103) and the serial interface driver (SIB87) provided by Our company in pair.

Note 2: Dedicated programming device and program are required depending on the programming conditions. Contact Our company or FSG if you have any questions or difficulties regarding this matter.

LC87F1JJ8A

Pin Assignment

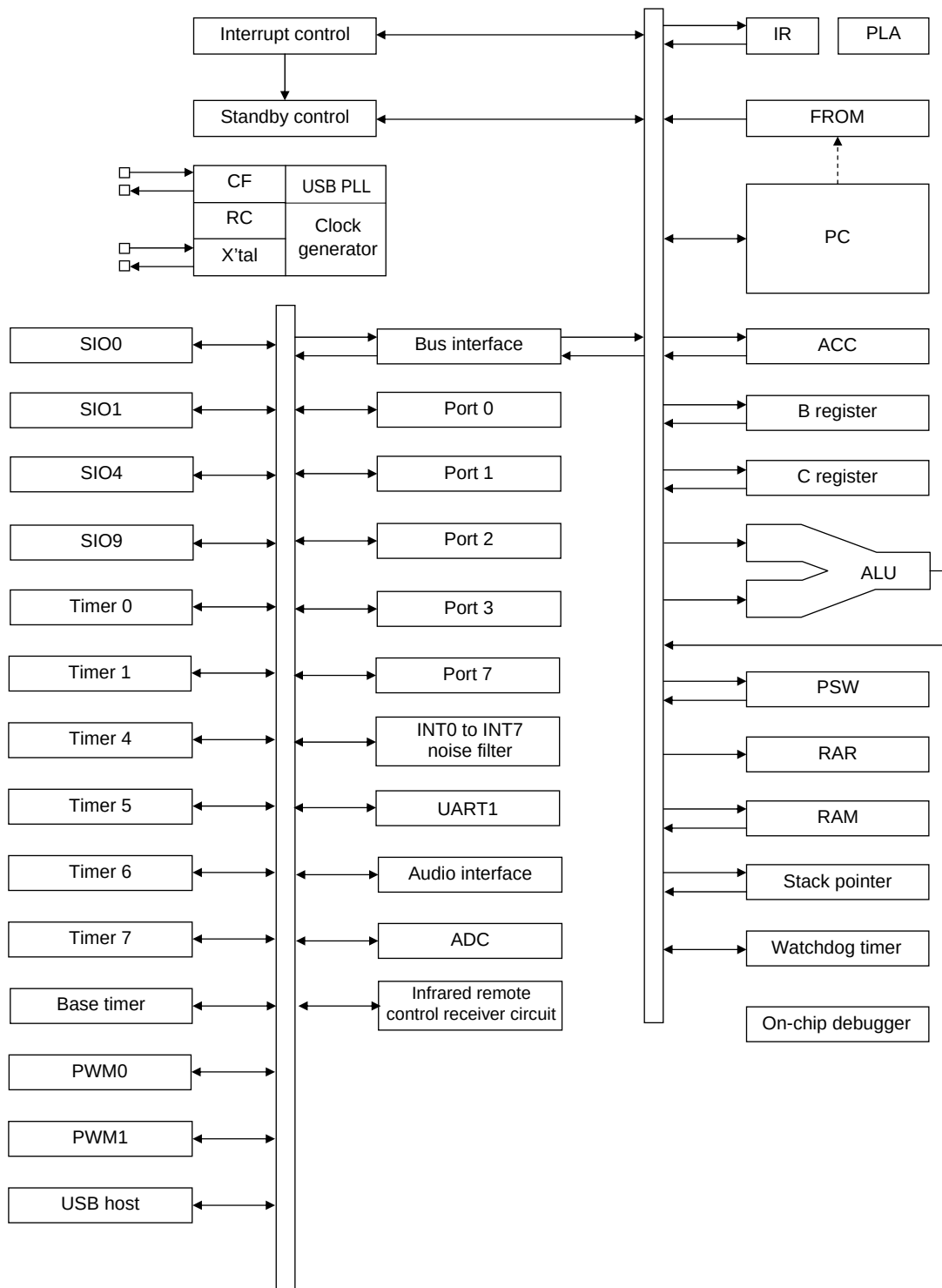


SQFP48(7×7) “Lead-/Halogen-free type”

| SQFP48 | NAME               |
|--------|--------------------|
| 1      | P73/INT3/T0IN/RMIN |
| 2      | RES                |
| 3      | XT1/AN10           |
| 4      | XT2/AN11           |
| 5      | VSS1               |
| 6      | CF1                |
| 7      | CF2                |
| 8      | VDD1               |
| 9      | P10/SO0            |
| 10     | P11/SI0/SB0        |
| 11     | P12/SCK0           |
| 12     | P13/SO1            |
| 13     | P14/SI1/SB1        |
| 14     | P15/SCK1           |
| 15     | P16/T1PWML         |
| 16     | P17/T1PWMH/BUZ     |
| 17     | PWM1/MCLKI         |
| 18     | PWM0/MCLKO         |
| 19     | VDD2               |
| 20     | VSS2               |
| 21     | P00/AN0            |
| 22     | P01/AN1            |
| 23     | P02/AN2/DBGP0      |
| 24     | P03/AN3/DBGP1      |

| SQFP48 | NAME               |
|--------|--------------------|
| 25     | P04/AN4/DBGP2      |
| 26     | P05/AN5/CKO/SDAT   |
| 27     | P06/AN6/T6O/BCLK   |
| 28     | P07/AN7/T7O/LRCK   |
| 29     | P20/INT4/INT6      |
| 30     | P21/INT4           |
| 31     | P22/INT4/SO4/RD    |
| 32     | P23/INT4/SI4/WR    |
| 33     | P24/INT5/INT7/SCK4 |
| 34     | P25/INT5/SO9/RD9   |
| 35     | P26/INT5/SI9/WR9   |
| 36     | P27/INT5/SCK9      |
| 37     | UHD-               |
| 38     | UHD+               |
| 39     | VDD3               |
| 40     | VSS3               |
| 41     | P34/UFILT          |
| 42     | P33/AFILT          |
| 43     | P32                |
| 44     | P31/URX1           |
| 45     | P30/UTX1           |
| 46     | P70/INT0/T0LCP/AN8 |
| 47     | P71/INT1/T0HCP/AN9 |
| 48     | P72/INT2/T0IN      |

# System Block Diagram



## Pin Description

| Pin Name                                                  | I/O    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Option |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
|-----------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------|------------------|------------------|---------|---------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|-----|
| V <sub>SS</sub> 1,V <sub>SS</sub> 2,<br>V <sub>SS</sub> 3 | -      | - power supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | No     |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| V <sub>DD</sub> 1, V <sub>DD</sub> 2                      | -      | + power supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | No     |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| V <sub>DD</sub> 3                                         | -      | USB reference voltage                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Yes    |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| Port 0                                                    | I/O    | <ul style="list-style-type: none"><li>• 8-bit I/O ports</li><li>• I/O specifiable in 4-bit units</li><li>• Pull-up resistors can be turned on and off in 4-bit units.</li><li>• HOLD release input</li><li>• Port 0 interrupt input</li><li>• Pin functions</li></ul> AD converter input ports: AN0 to AN7(P00 to P07)<br>On-chip debugger pins: DBG P0 to DBG P2(P02 to P04)<br>P05: System clock output/audio interface SDAT input/output<br>P06: Timer 6 toggle output/audio interface BCLK input/output<br>P07: Timer 7 toggle output/audio interface LRCK input/output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Yes    |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| P00 to P07                                                |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |        |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| Port 1                                                    | I/O    | <ul style="list-style-type: none"><li>• 8-bit I/O ports</li><li>• I/O specifiable in 1-bit units</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Pin functions</li></ul> P10: SIO0 data output                      P14: SIO1 data input/bus input/output<br>P11: SIO0 data input/bus input/output   P15: SIO1 clock input/output<br>P12: SIO0 clock input/output            P16: Timer 1 PWML output<br>P13: SIO1 data output                      P17: Timer 1 PWMH output/beeper output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Yes    |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| P10 to P17                                                |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |        |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| Port 2                                                    | I/O    | <ul style="list-style-type: none"><li>• 8-bit I/O ports</li><li>• I/O specifiable in 1-bit units</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Pin functions</li></ul> P20 to P23: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/<br>timer 0H capture input<br>P24 to P27: INT5 input/HOLD release input/timer 1 event input/timer 0L capture input/<br>timer 0H capture input<br>P20: INT6 input/timer 0L capture 1 input<br>P22: SIO4 data input/output/parallel interface $\overline{RD}$ output<br>P23: SIO4 data input/output/parallel interface $\overline{WR}$ output<br>P24: SIO4 clock input/output/INT7 input/timer 0H capture 1 input<br>P25: SIO9 data input/output/parallel interface $\overline{RD9}$ output<br>P26: SIO9 data input/output/parallel interface $\overline{WR9}$ output<br>P27: SIO9 clock input/output<br>Interrupt acknowledge types <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising &amp; Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table> |        | Rising  | Falling          | Rising & Falling | H level | L level | INT4 | enable | enable | enable | disable | disable | INT5 | enable | enable | enable | disable | disable | INT6 | enable | enable | enable | disable | disable | INT7 | enable | enable | enable | disable | disable | Yes |
|                                                           |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Rising | Falling | Rising & Falling | H level          | L level |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| INT4                                                      | enable | enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | enable | disable | disable          |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| INT5                                                      | enable | enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | enable | disable | disable          |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| INT6                                                      | enable | enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | enable | disable | disable          |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| INT7                                                      | enable | enable                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | enable | disable | disable          |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| P20 to P27                                                |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |        |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| Port 3                                                    | I/O    | <ul style="list-style-type: none"><li>• 5-bit I/O ports</li><li>• I/O specifiable in 1-bit units</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Pin functions</li></ul> P30: UART1 transmit<br>P31: UART1 receive<br><br>P33: Audio interface PLL filter circuit connection pin (See Fig. 6.)<br>P34: USB interface PLL filter circuit connection pin (See Fig. 5.)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Yes    |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |
| P30 to P34                                                |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |        |         |                  |                  |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |      |        |        |        |         |         |     |

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| Pin Name   | I/O | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Option |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
|------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------|------------------|------------------|---------|---------|------|--------|--------|---------|--------|--------|------|--------|--------|---------|--------|--------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|----|
| Port 7     | I/O | <ul style="list-style-type: none"><li>• 4-bit I/O ports</li><li>• I/O specifiable in 1-bit units</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Pin functions</li></ul> <p>P70: INT0 input/HOLD release input/timer 0L capture input/watchdog timer output</p> <p>P71: INT1 input/HOLD release input/timer 0H capture input</p> <p>P72: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input/<br/>high speed clock counter input</p> <p>P73: INT3 input (input with noise filter)/timer 0 event input/timer 0H capture input/<br/>infrared remote control receiver input</p> <p>AD converter input ports: AN8(P70), AN9(P71)</p> <p>Interrupt acknowledge types</p> <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising &amp; Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table> |        | Rising  | Falling          | Rising & Falling | H level | L level | INT0 | enable | enable | disable | enable | enable | INT1 | enable | enable | disable | enable | enable | INT2 | enable | enable | enable | disable | disable | INT3 | enable | enable | enable | disable | disable | No |
|            |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Rising | Falling | Rising & Falling | H level          | L level |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| INT0       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | enable | enable  | disable          | enable           | enable  |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| INT1       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | enable | enable  | disable          | enable           | enable  |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| INT2       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | enable | enable  | enable           | disable          | disable |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| INT3       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | enable | enable  | enable           | disable          | disable |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| P70 to P73 |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| PWM0       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| PWM1       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
|            |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| PWM0       | I/O | PWM0, PWM1 output ports<br>General-purpose input port <ul style="list-style-type: none"><li>• Pin functions</li></ul> PWM0: Audio interface master clock output<br>PWM1: Audio interface master clock input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | No     |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| PWM1       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| UHD-       | I/O | USB data I/O pin UHD-/general-purpose I/O port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | No     |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| UHD+       | I/O | USB data I/O pin UHD+/general-purpose I/O port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | No     |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| RES        | I   | Reset pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | No     |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| XT1        | I   | <ul style="list-style-type: none"><li>• 32.768kHz crystal oscillator input</li><li>• Pin functions</li></ul> General-purpose input port<br>AD converter input port: AN10<br>Must be connected to V <sub>DD1</sub> when not to be used.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | No     |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| XT2        | I/O | <ul style="list-style-type: none"><li>• 32.768kHz crystal oscillator output</li><li>• Pin functions</li></ul> General-purpose input port<br>AD converter input port: AN11<br>Must be configured for oscillation and kept open if not to be used.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | No     |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| CF1        | I   | Ceramic/crystal resonator input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | No     |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| CF2        | O   | Ceramic/crystal resonator output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | No     |         |                  |                  |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |

## Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

| Port Name                              | Option Selected in Units of | Option Type | Output Type                                                                             | Pull-up Resistor      |
|----------------------------------------|-----------------------------|-------------|-----------------------------------------------------------------------------------------|-----------------------|
| P00 to P07                             | 1 bit                       | 1           | CMOS                                                                                    | Programmable (Note 1) |
|                                        |                             | 2           | Nch-open drain                                                                          | No                    |
| P10 to P17<br>P20 to P27<br>P30 to P34 | 1 bit                       | 1           | CMOS                                                                                    | Programmable          |
|                                        |                             | 2           | Nch-open drain                                                                          | Programmable          |
| P70                                    | -                           | No          | Nch-open drain                                                                          | Programmable          |
| P71 to P73                             | -                           | No          | CMOS                                                                                    | Programmable          |
| PWM0, PWM1                             | -                           | No          | CMOS                                                                                    | No                    |
| UHD+, UHD-                             | -                           | No          | CMOS                                                                                    | No                    |
| XT1                                    | -                           | No          | Input only                                                                              | No                    |
| XT2                                    | -                           | No          | 32.768kHz crystal resonator output (Nch-open drain when in general-purpose output mode) | No                    |

Note 1: Programmable pull-up resistors for port 0 are controlled in 4 bit units (P00 to 03, P04 to 07).

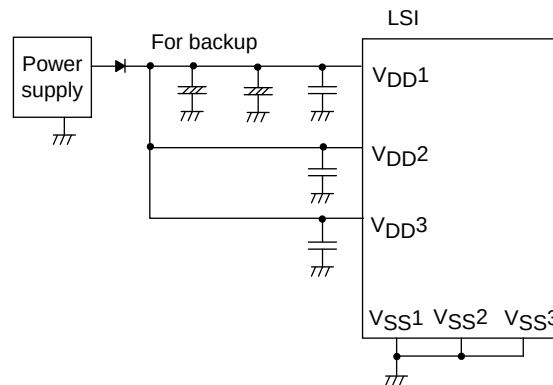
## User Options

| Option Name           | Type                         | Flash ROM Version | Option Selected in Units of | Setting        |
|-----------------------|------------------------------|-------------------|-----------------------------|----------------|
| Port output type      | P00 to P07                   | ○                 | 1 bit                       | CMOS           |
|                       |                              |                   |                             | Nch-open drain |
|                       | P10 to P17                   | ○                 | 1 bit                       | CMOS           |
|                       |                              |                   |                             | Nch-open drain |
|                       | P20 to P27                   | ○                 | 1 bit                       | CMOS           |
|                       |                              |                   |                             | Nch-open drain |
|                       | P30 to P34                   | ○                 | 1 bit                       | CMOS           |
|                       |                              |                   |                             | Nch-open drain |
| Program start address | -                            | ○                 | -                           | 00000h         |
|                       |                              |                   |                             | 1FE00h         |
| USB Regulator         | USB Regulator                | ○                 | -                           | Use            |
|                       |                              |                   |                             | Nonuse         |
|                       | USB Regulator (at HOLD mode) | ○                 | -                           | Use            |
|                       |                              |                   |                             | Nonuse         |
|                       | USB Regulator (at HALT mode) | ○                 | -                           | Use            |
|                       |                              |                   |                             | Nonuse         |

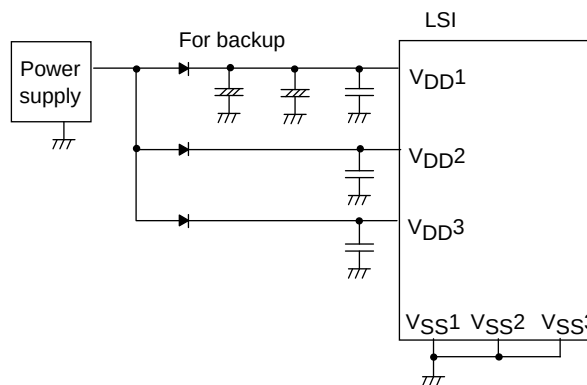
## Power Pin Treatment

Connect the IC as shown below to minimize the noise input to the  $V_{DD1}$  pin and extend the backup period. Be sure to electrically short the  $V_{SS1}$ ,  $V_{SS2}$ , and  $V_{SS3}$  pins.

Example 1: When the microcontroller is in the backup state in the HOLD mode, the power to sustain the high level of output ports is supplied by their backup capacitors.



Example 2: The high level output at ports is not sustained and unstable in the HOLD backup mode.



## USB Reference Power Option

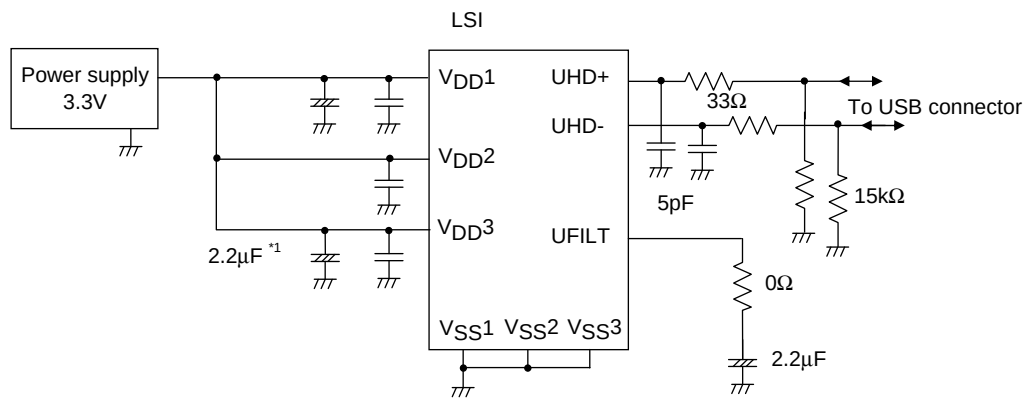
When a voltage 4.5 to 5.5V is supplied to  $V_{DD1}$  and the internal USB reference voltage circuit is activated, the reference voltage for USB port output is generated. The active/inactive state of the reference voltage circuit can be switched by optional settings. The procedure for marking the optional settings is described below.

| Option settings                 |                            | (1)    | (2)      | (3)      | (4)      |
|---------------------------------|----------------------------|--------|----------|----------|----------|
|                                 | USB regulator              | Use    | Use      | Use      | Nonuse   |
|                                 | USB regulator in HOLD mode | Use    | Nonuse   | Nonuse   | Nonuse   |
| Reference voltage circuit state | USB regulator in HALT mode | Use    | Nonuse   | Use      | Nonuse   |
|                                 | Normal mode                | Active | Active   | Active   | Inactive |
|                                 | HOLD mode                  | Active | Inactive | Inactive | Inactive |
|                                 | HALT mode                  | Active | Inactive | Active   | Inactive |

- When the USB reference voltage circuit is made inactive, the level of the reference voltage for USB port output is equal to  $V_{DD1}$ .
- Selection (2) or (3) can be used to set the reference voltage circuit inactive in HOLD or HALT mode.
- When the reference voltage circuit is activated, the current drain increases by approximately 100 $\mu$ A compared with when the reference voltage circuit is inactive.

Circuit example 1: When  $V_{DD1}=V_{DD2}=3.3V$

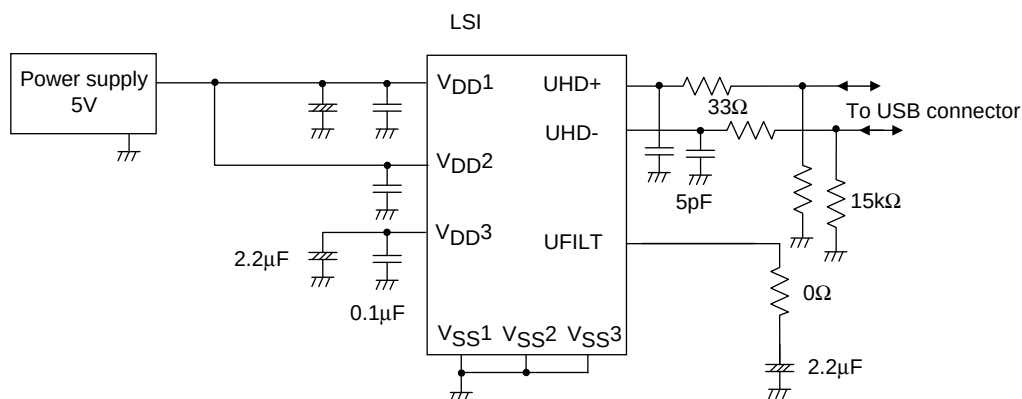
- Inactivating the reference voltage circuit (selection (4)).
- Connecting  $V_{DD3}$  to  $V_{DD1}$  and  $V_{DD2}$ .



\*1: Needs adjustment on target board.

Circuit example 2: When  $V_{DD1}=V_{DD2}=5.0V$

- Activating the reference voltage circuit (selection (1)).
- Isolating  $V_{DD3}$  from  $V_{DD1}$  and  $V_{DD2}$ , and connecting capacitor between  $V_{DD3}$  and  $V_{SS}$ .



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**Absolute Maximum Ratings** at Ta = 25°C, VSS1 = VSS2 = VSS3 = 0V

| Parameter                     | Symbol                            | Pin/Remarks                              | Conditions                             | Specification                                                                                                     |      |      |         |      |
|-------------------------------|-----------------------------------|------------------------------------------|----------------------------------------|-------------------------------------------------------------------------------------------------------------------|------|------|---------|------|
|                               |                                   |                                          |                                        | VDD[V]                                                                                                            | min  | typ  | max     | unit |
| Maximum supply voltage        | VDD max                           | VDD1, VDD2, VDD3                         | VDD1= VDD2= VDD3                       |                                                                                                                   | -0.3 |      | +6.5    | V    |
| Input voltage                 | VI(1)                             | XT1, CF1                                 |                                        |                                                                                                                   | -0.3 |      | VDD+0.3 |      |
| Input/output voltage          | VI/O(1)                           | Ports 0, 1, 2, 3, 7<br>PWM0, PWM1<br>XT2 |                                        |                                                                                                                   | -0.3 |      | VDD+0.3 |      |
| High level output current     | Peak output current               | IOPH(1)                                  | Ports 0, 1, 2                          | <ul style="list-style-type: none"> <li>When CMOS output type is selected</li> <li>Per 1 applicable pin</li> </ul> |      | -10  |         | mA   |
|                               |                                   | IOPH(2)                                  | PWM0, PWM1                             | Per 1 applicable pin                                                                                              |      | -20  |         |      |
|                               |                                   | IOPH(3)                                  | Port 3<br>P71 to P73                   | <ul style="list-style-type: none"> <li>When CMOS output type is selected</li> <li>Per 1 applicable pin</li> </ul> |      | -5   |         |      |
|                               | Average output current (Note 1-1) | IOMH(1)                                  | Ports 0, 1, 2                          | <ul style="list-style-type: none"> <li>When CMOS output type is selected</li> <li>Per 1 applicable pin</li> </ul> |      | -7.5 |         |      |
|                               |                                   | IOMH(2)                                  | PWM0, PWM1                             | Per 1 applicable pin                                                                                              |      | -15  |         |      |
|                               |                                   | IOMH(3)                                  | Port 3<br>P71 to P73                   | <ul style="list-style-type: none"> <li>When CMOS output type is selected</li> <li>Per 1 applicable pin</li> </ul> |      | -3   |         |      |
|                               | Total output current              | ΣIOAH(1)                                 | Ports 0, 2                             | Total current of all applicable pins                                                                              |      | -25  |         |      |
|                               |                                   | ΣIOAH(2)                                 | Port 1<br>PWM0, PWM1                   | Total current of all applicable pins                                                                              |      | -25  |         |      |
|                               |                                   | ΣIOAH(3)                                 | Ports 0, 1, 2<br>PWM0, PWM1            | Total current of all applicable pins                                                                              |      | -45  |         |      |
|                               |                                   | ΣIOAH(4)                                 | Port 3<br>P71 to P73                   | Total current of all applicable pins                                                                              |      | -10  |         |      |
|                               |                                   | ΣIOAH(5)                                 | UHD+, UHD-                             | Total current of all applicable pins                                                                              |      | -25  |         |      |
| Low level output current      | Peak output current               | IOPL(1)                                  | P02 to P07<br>Ports 1, 2<br>PWM0, PWM1 | Per 1 applicable pin                                                                                              |      |      | 20      | mA   |
|                               |                                   | IOPL(2)                                  | P00, P01                               | Per 1 applicable pin                                                                                              |      |      | 30      |      |
|                               |                                   | IOPL(3)                                  | Ports 3, 7<br>XT2                      | Per 1 applicable pin                                                                                              |      |      | 10      |      |
|                               | Average output current (Note 1-1) | IOML(1)                                  | P02 to P07<br>Ports 1, 2<br>PWM0, PWM1 | Per 1 applicable pin                                                                                              |      |      | 15      |      |
|                               |                                   | IOML(2)                                  | P00, P01                               | Per 1 applicable pin                                                                                              |      |      | 20      |      |
|                               |                                   | IOML(3)                                  | Ports 3, 7<br>XT2                      | Per 1 applicable pin                                                                                              |      |      | 7.5     |      |
|                               | Total output current              | ΣIOAL(1)                                 | Ports 0, 2                             | Total current of all applicable pins                                                                              |      |      | 45      |      |
|                               |                                   | ΣIOAL(2)                                 | Port 1<br>PWM0, PWM1                   | Total current of all applicable pins                                                                              |      |      | 45      |      |
|                               |                                   | ΣIOAL(3)                                 | Ports 0, 1, 2<br>PWM0, PWM1            | Total current of all applicable pins                                                                              |      |      | 80      |      |
|                               |                                   | ΣIOAL(4)                                 | Ports 3, 7<br>XT2                      | Total current of all applicable pins                                                                              |      |      | 15      |      |
|                               |                                   | ΣIOAL(5)                                 | UHD+, UHD-                             | Total current of all applicable pins                                                                              |      |      | 25      |      |
| Allowable power dissipation   | Pd max                            | SQFP48(7×7)                              | Ta=-40 to +85°C                        |                                                                                                                   |      |      | 140     | mW   |
| Operating ambient temperature | Topr                              |                                          |                                        |                                                                                                                   | -40  |      | +85     | °C   |
| Storage ambient temperature   | Tstg                              |                                          |                                        |                                                                                                                   | -55  |      | +125    |      |

Note 1-1: The average output current is an average of current values measured over 100ms intervals.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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## Allowable Operating Conditions at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = V<sub>SS3</sub> = 0V

| Parameter                                 | Symbol              | Pin/Remarks                                                                       | Conditions                                                                                                                                                   | Specification       |                            |        |                             |      |
|-------------------------------------------|---------------------|-----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|----------------------------|--------|-----------------------------|------|
|                                           |                     |                                                                                   |                                                                                                                                                              | V <sub>DD</sub> [V] | min                        | typ    | max                         | unit |
| Operating supply voltage<br>(Note 2-1)    | V <sub>DD</sub> (1) | V <sub>DD1</sub> =V <sub>DD2</sub> =V <sub>DD3</sub>                              | 0.245μs ≤ tCYC ≤ 200μs                                                                                                                                       |                     | 3.0                        |        | 5.5                         | V    |
|                                           |                     |                                                                                   | 0.490μs ≤ tCYC ≤ 200μs Except in onboard programming mode                                                                                                    |                     | 2.7                        |        | 5.5                         |      |
| Memory sustaining supply voltage          | V <sub>HD</sub>     | V <sub>DD1</sub> =V <sub>DD2</sub> =V <sub>DD3</sub>                              | RAM and register contents sustained in HOLD mode.                                                                                                            |                     | 2.0                        |        | 5.5                         |      |
| High level input voltage                  | V <sub>IH</sub> (1) | Ports 0, 1, 2, 3<br>P71 to P73<br>P70 port input/<br>interrupt side<br>PWM0, PWM1 |                                                                                                                                                              | 2.7 to 5.5          | 0.3V <sub>DD</sub><br>+0.7 |        | V <sub>DD</sub>             |      |
|                                           | V <sub>IH</sub> (2) | Port 70 watchdog timer side                                                       |                                                                                                                                                              | 2.7 to 5.5          | 0.9V <sub>DD</sub>         |        | V <sub>DD</sub>             |      |
|                                           | V <sub>IH</sub> (3) | XT1, XT2, CF1, RES                                                                |                                                                                                                                                              | 2.7 to 5.5          | 0.75V <sub>DD</sub>        |        | V <sub>DD</sub>             |      |
| Low level input voltage                   | V <sub>IL</sub> (1) | Ports 1, 2, 3<br>P71 to P73                                                       |                                                                                                                                                              | 4.0 to 5.5          | V <sub>SS</sub>            |        | 0.1V <sub>DD</sub><br>+0.4  |      |
|                                           | V <sub>IL</sub> (2) | P70 port input/<br>interrupt side                                                 |                                                                                                                                                              | 2.7 to 4.0          | V <sub>SS</sub>            |        | 0.2V <sub>DD</sub>          |      |
|                                           | V <sub>IL</sub> (3) | Port 0<br>PWM0, PWM1                                                              |                                                                                                                                                              | 4.0 to 5.5          | V <sub>SS</sub>            |        | 0.15V <sub>DD</sub><br>+0.4 |      |
|                                           | V <sub>IL</sub> (4) |                                                                                   |                                                                                                                                                              | 2.7 to 4.0          | V <sub>SS</sub>            |        | 0.2V <sub>DD</sub>          |      |
|                                           | V <sub>IL</sub> (5) | Port 70 watchdog timer side                                                       |                                                                                                                                                              | 2.7 to 5.5          | V <sub>SS</sub>            |        | 0.8V <sub>DD</sub><br>-1.0  |      |
|                                           | V <sub>IL</sub> (6) | XT1, XT2, CF1, RES                                                                |                                                                                                                                                              | 2.7 to 5.5          | V <sub>SS</sub>            |        | 0.25V <sub>DD</sub>         |      |
| Instruction cycle time<br>(Note 2-2)      | tCYC                |                                                                                   |                                                                                                                                                              | 3.0 to 5.5          | 0.245                      |        | 200                         | μs   |
|                                           |                     |                                                                                   | Except in onboard programming mode                                                                                                                           | 2.7 to 5.5          | 0.490                      |        | 200                         |      |
| External system clock frequency           | FEXCF(1)            | CF1                                                                               | <ul style="list-style-type: none"> <li>CF2 pin open</li> <li>System clock frequency division ratio=1/1</li> <li>External system clock duty =50±5%</li> </ul> | 3.0 to 5.5          | 0.1                        |        | 12                          | MHz  |
|                                           |                     |                                                                                   | <ul style="list-style-type: none"> <li>CF2 pin open</li> <li>System clock frequency division ratio=1/1</li> <li>External system clock duty =50±5%</li> </ul> | 2.7 to 5.5          | 0.1                        |        | 6                           |      |
| Oscillation frequency range<br>(Note 2-3) | FmCF(1)             | CF1, CF2                                                                          | When 12MHz ceramic oscillation<br>See Fig. 1.                                                                                                                | 3.0 to 5.5          |                            | 12     |                             | MHz  |
|                                           | FmCF(2)             | CF1, CF2                                                                          | When 6MHz ceramic oscillation<br>See Fig. 1.                                                                                                                 | 2.7 to 5.5          |                            | 6      |                             |      |
|                                           | FmRC                |                                                                                   | Internal RC oscillation                                                                                                                                      | 2.7 to 5.5          | 0.3                        | 1.0    | 2.0                         |      |
|                                           | FsX'tal             | XT1, XT2                                                                          | 32.768kHz crystal oscillation<br>See Fig. 2.                                                                                                                 | 2.7 to 5.5          |                            | 32.768 |                             | kHz  |

Note 2-1: V<sub>DD</sub> must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See oscillation characteristics examples.

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## Electrical Characteristics at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = V<sub>SS3</sub> = 0V

| Parameter                 | Symbol              | Pin/Remarks                                                                       | Conditions                                                                                                                 | Specification       |                      |                    |     |               |
|---------------------------|---------------------|-----------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|---------------------|----------------------|--------------------|-----|---------------|
|                           |                     |                                                                                   |                                                                                                                            | V <sub>DD</sub> [V] | min                  | typ                | max | unit          |
| High level input current  | I <sub>IH</sub> (1) | Ports 0, 1, 2, 3<br>Port 7<br>$\overline{\text{RES}}$<br>PWM0, PWM1<br>UHD+, UHD- | Output disabled<br>Pull-up resistor off<br>V <sub>IN</sub> =V <sub>DD</sub><br>(Including output Tr's off leakage current) | 2.7 to 5.5          |                      |                    | 1   | $\mu\text{A}$ |
|                           | I <sub>IH</sub> (2) | XT1, XT2                                                                          | Input port configuration<br>V <sub>IN</sub> =V <sub>DD</sub>                                                               | 2.7 to 5.5          |                      |                    | 1   |               |
|                           | I <sub>IH</sub> (3) | CF1                                                                               | V <sub>IN</sub> =V <sub>DD</sub>                                                                                           | 2.7 to 5.5          |                      |                    | 15  |               |
| Low level input current   | I <sub>IL</sub> (1) | Ports 0, 1, 2, 3<br>Port 7<br>$\overline{\text{RES}}$<br>PWM0, PWM1<br>UHD+, UHD- | Output disabled<br>Pull-up resistor off<br>V <sub>IN</sub> =V <sub>SS</sub><br>(Including output Tr's off leakage current) | 2.7 to 5.5          | -1                   |                    |     | $\mu\text{A}$ |
|                           | I <sub>IL</sub> (2) | XT1, XT2                                                                          | Input port configuration<br>V <sub>IN</sub> =V <sub>SS</sub>                                                               | 2.7 to 5.5          | -1                   |                    |     |               |
|                           | I <sub>IL</sub> (3) | CF1                                                                               | V <sub>IN</sub> =V <sub>SS</sub>                                                                                           | 2.7 to 5.5          | -15                  |                    |     |               |
| High level output voltage | V <sub>OH</sub> (1) | Ports 0, 1, 2, 3                                                                  | I <sub>OH</sub> =-1mA                                                                                                      | 4.5 to 5.5          | V <sub>DD</sub> -1   |                    |     | V             |
|                           | V <sub>OH</sub> (2) | P71 to P73                                                                        | I <sub>OH</sub> =-0.4mA                                                                                                    | 3.0 to 5.5          | V <sub>DD</sub> -0.4 |                    |     |               |
|                           | V <sub>OH</sub> (3) |                                                                                   | I <sub>OH</sub> =-0.2mA                                                                                                    | 2.7 to 5.5          | V <sub>DD</sub> -0.4 |                    |     |               |
|                           | V <sub>OH</sub> (4) | PWM0, PWM1                                                                        | I <sub>OH</sub> =-10mA                                                                                                     | 4.5 to 5.5          | V <sub>DD</sub> -1.5 |                    |     |               |
|                           | V <sub>OH</sub> (5) | P05 to P07<br>(Note 3-1)                                                          | I <sub>OH</sub> =-1.6mA                                                                                                    | 3.0 to 5.5          | V <sub>DD</sub> -0.4 |                    |     |               |
|                           | V <sub>OH</sub> (6) |                                                                                   | I <sub>OH</sub> =-1mA                                                                                                      | 2.7 to 5.5          | V <sub>DD</sub> -0.4 |                    |     |               |
| Low level output voltage  | V <sub>OL</sub> (1) | P00, P01                                                                          | I <sub>OL</sub> =30mA                                                                                                      | 4.5 to 5.5          |                      |                    | 1.5 | V             |
|                           | V <sub>OL</sub> (2) |                                                                                   | I <sub>OL</sub> =5mA                                                                                                       | 3.0 to 5.5          |                      |                    | 0.4 |               |
|                           | V <sub>OL</sub> (3) |                                                                                   | I <sub>OL</sub> =2.5mA                                                                                                     | 2.7 to 5.5          |                      |                    | 0.4 |               |
|                           | V <sub>OL</sub> (4) | Ports 0, 1, 2                                                                     | I <sub>OL</sub> =10mA                                                                                                      | 4.5 to 5.5          |                      |                    | 1.5 |               |
|                           | V <sub>OL</sub> (5) | PWM0, PWM1<br>XT2                                                                 | I <sub>OL</sub> =1.6mA                                                                                                     | 3.0 to 5.5          |                      |                    | 0.4 |               |
|                           | V <sub>OL</sub> (6) |                                                                                   | I <sub>OL</sub> =1mA                                                                                                       | 2.7 to 5.5          |                      |                    | 0.4 |               |
|                           | V <sub>OL</sub> (7) | Ports 3, 7                                                                        | I <sub>OL</sub> =1.6mA                                                                                                     | 3.0 to 5.5          |                      |                    | 0.4 |               |
|                           | V <sub>OL</sub> (8) |                                                                                   | I <sub>OL</sub> =1mA                                                                                                       | 2.7 to 5.5          |                      |                    | 0.4 |               |
| Pull-up resistance        | R <sub>pu</sub> (1) | Ports 0, 1, 2, 3                                                                  | V <sub>OH</sub> =0.9V <sub>DD</sub>                                                                                        | 4.5 to 5.5          | 15                   | 35                 | 80  | k $\Omega$    |
|                           | R <sub>pu</sub> (2) | Port 7                                                                            |                                                                                                                            | 2.7 to 4.5          | 18                   | 50                 | 150 |               |
| Hysteresis voltage        | V <sub>HYS</sub>    | $\overline{\text{RES}}$<br>Port 1, 2, 3, 7                                        |                                                                                                                            | 2.7 to 5.5          |                      | 0.1V <sub>DD</sub> |     | V             |
| Pin capacitance           | CP                  | All pins                                                                          | For pins other than that under test:<br>V <sub>IN</sub> =V <sub>SS</sub><br>f=1MHz<br>Ta=25°C                              | 2.7 to 5.5          |                      | 10                 |     | pF            |

Note 3-1: When the CKO system clock output function (P05) or audio interface output function (P05 to P07) is used.

**Serial I/O Characteristics** at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = V<sub>SS3</sub> = 0V

**1. SIO0 Serial I/O Characteristics (Note 4-1-1)**

| Parameter    |              | Symbol                 | Pin/<br>Remarks | Conditions                                                                                                                                                                                                                                          | V <sub>DD</sub> [V] | Specification    |     |                       |      |
|--------------|--------------|------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------------|-----|-----------------------|------|
|              |              |                        |                 |                                                                                                                                                                                                                                                     |                     | min              | typ | max                   | unit |
| Serial clock | Input clock  | Frequency              | SCK0(P12)       | See Fig. 9.                                                                                                                                                                                                                                         | 2.7 to 5.5          | 2                |     |                       | tCYC |
|              |              | Low level pulse width  |                 |                                                                                                                                                                                                                                                     |                     | 1                |     |                       |      |
|              |              | High level pulse width |                 |                                                                                                                                                                                                                                                     |                     | 1                |     |                       |      |
|              |              | tSCKHA(1a)             |                 | <ul style="list-style-type: none"> <li>Continuous data transfer mode</li> <li>USB, AIF, SIO4, SIO9, and DMCOPY not used at the same time.</li> <li>See Fig. 9.</li> <li>(Note 4-1-2)</li> </ul>                                                     |                     | 4                |     |                       |      |
|              |              | tSCKHA(1b)             |                 | <ul style="list-style-type: none"> <li>Continuous data transfer mode</li> <li>USB used at the same time.</li> <li>AIF, SIO4, SIO9, and DMCOPY not used at the same time.</li> <li>See Fig. 9.</li> <li>(Note 4-1-2)</li> </ul>                      |                     | 7                |     |                       |      |
|              |              | tSCKHA(1c)             |                 | <ul style="list-style-type: none"> <li>Continuous data transfer mode</li> <li>USB, AIF, SIO4, SIO9, and DMCOPY used at the same time.</li> <li>See Fig. 9.</li> <li>(Note 4-1-2)</li> </ul>                                                         |                     | 9                |     |                       |      |
|              | Output clock | Frequency              | SCK0(P12)       | <ul style="list-style-type: none"> <li>When CMOS output type is selected</li> <li>See Fig. 9.</li> </ul>                                                                                                                                            | 2.7 to 5.5          | 4/3              |     |                       | tSCK |
|              |              | Low level pulse width  |                 |                                                                                                                                                                                                                                                     |                     | 1/2              |     |                       |      |
|              |              | High level pulse width |                 |                                                                                                                                                                                                                                                     |                     | 1/2              |     |                       |      |
|              |              | tSCKHA(2a)             |                 | <ul style="list-style-type: none"> <li>Continuous data transfer mode</li> <li>USB, AIF, SIO4, SIO9, and DMCOPY not used at the same time.</li> <li>When CMOS output type is selected</li> <li>See Fig. 9.</li> </ul>                                |                     | tSCKH(2) + 2tCYC |     | tSCKH(2) + (10/3)tCYC | tCYC |
|              |              | tSCKHA(2b)             |                 | <ul style="list-style-type: none"> <li>Continuous data transfer mode</li> <li>USB used at the same time.</li> <li>AIF, SIO4, SIO9, and DMCOPY not used at the same time.</li> <li>When CMOS output type is selected.</li> <li>See Fig.9.</li> </ul> |                     | tSCKH(2) + 2tCYC |     | tSCKH(2) + (19/3)tCYC |      |
|              |              | tSCKHA(2c)             |                 | <ul style="list-style-type: none"> <li>Continuous data transfer mode</li> <li>USB, AIF, SIO4, SIO9, and DMCOPY used at the same time</li> <li>When CMOS output type is selected</li> <li>See Fig.9.</li> </ul>                                      |                     | tSCKH(2) + 2tCYC |     | tSCKH(2) + (25/3)tCYC |      |

Note 4-1-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-1-2: In an application where the serial clock input is to be used in the continuous data transfer mode, the time from SIO<sub>0</sub>RUN being set when serial clock is high to the falling edge of the first serial clock must be longer than tSCKHA.

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| Parameter     |                   | Symbol  | Pin/<br>Remarks       | Conditions                                                                                                                      | V <sub>DD</sub> [V] | Specification |     |                    |      |
|---------------|-------------------|---------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------|-----|--------------------|------|
|               |                   |         |                       |                                                                                                                                 |                     | min           | typ | max                | unit |
| Serial input  | Data setup time   | tsDI(1) | SB0(P11),<br>SI0(P11) | <ul style="list-style-type: none"> <li>Must be specified with respect to rising edge of SIOCLK.</li> <li>See Fig. 9.</li> </ul> | 2.7 to 5.5          | 0.03          |     |                    | μs   |
|               | Data hold time    | thDI(1) |                       |                                                                                                                                 |                     | 0.03          |     |                    |      |
| Serial output | Output delay time | tdDO(1) | SO0(P10),<br>SB0(P11) | <ul style="list-style-type: none"> <li>Continuous data transfer mode</li> <li>(Note 4-1-3)</li> </ul>                           | 2.7 to 5.5          |               |     | (1/3)tCYC<br>+0.05 |      |
|               |                   | tdDO(2) |                       | <ul style="list-style-type: none"> <li>Synchronous 8-bit mode</li> <li>(Note 4-1-3)</li> </ul>                                  |                     |               |     | 1tCYC<br>+0.05     |      |
|               | Output clock      | tdDO(3) |                       | (Note 4-1-3)                                                                                                                    |                     |               |     | (1/3)tCYC<br>+0.05 |      |

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK.

Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 9.

### 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

| Parameter     |                   | Symbol                 | Pin/<br>Remarks       | Conditions                                                                                                                                                                                                                                 | V <sub>DD</sub> [V] | Specification |     |                    |      |
|---------------|-------------------|------------------------|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------|-----|--------------------|------|
|               |                   |                        |                       |                                                                                                                                                                                                                                            |                     | min           | typ | max                | unit |
| Serial clock  | Input clock       | Frequency              | SCK1(P15)             | See Fig. 9.                                                                                                                                                                                                                                | 2.7 to 5.5          | 2             |     |                    | tCYC |
|               |                   | Low level pulse width  |                       |                                                                                                                                                                                                                                            |                     | 1             |     |                    |      |
|               |                   | High level pulse width |                       |                                                                                                                                                                                                                                            |                     | 1             |     |                    |      |
|               | Output clock      | Frequency              | SCK1(P15)             | <ul style="list-style-type: none"> <li>When CMOS output type is selected</li> <li>See Fig. 9.</li> </ul>                                                                                                                                   | 2.7 to 5.5          | 2             |     |                    | tSCK |
|               |                   | Low level pulse width  |                       |                                                                                                                                                                                                                                            |                     | 1/2           |     |                    |      |
|               |                   | High level pulse width |                       |                                                                                                                                                                                                                                            |                     | 1/2           |     |                    |      |
| Serial input  | Data setup time   | tsDI(2)                | SB1(P14),<br>SI1(P14) | <ul style="list-style-type: none"> <li>Must be specified with respect to rising edge of SIOCLK.</li> <li>See Fig. 9.</li> </ul>                                                                                                            | 2.7 to 5.5          | 0.03          |     |                    | μs   |
|               | Data hold time    | thDI(2)                |                       |                                                                                                                                                                                                                                            |                     | 0.03          |     |                    |      |
| Serial output | Output delay time | tdDO(4)                | SO1(P13),<br>SB1(P14) | <ul style="list-style-type: none"> <li>Must be specified with respect to falling edge of SIOCLK.</li> <li>Must be specified as the time to the beginning of output state change in open drain output mode.</li> <li>See Fig. 9.</li> </ul> | 2.7 to 5.5          |               |     | (1/3)tCYC<br>+0.05 | μs   |

Note 4-2-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.



3. SIO4 Serial I/O Characteristics (Note 4-3-1)

| Parameter    |              |                                        | Symbol                                                                                                                                                                                                                                    | Pin/<br>Remarks | Conditions                                                                                                                                                                                                                                | V <sub>DD</sub> [V] | Specification              |                             |                             |      |      |
|--------------|--------------|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|----------------------------|-----------------------------|-----------------------------|------|------|
|              |              |                                        |                                                                                                                                                                                                                                           |                 |                                                                                                                                                                                                                                           |                     | min                        | typ                         | max                         | unit |      |
| Serial clock | Input clock  | Frequency                              | tSCK(5)                                                                                                                                                                                                                                   | SCK4(P24)       | See Fig. 9.                                                                                                                                                                                                                               | 2.7 to 5.5          | 2                          |                             |                             | tCYC |      |
|              |              | Low level pulse width                  | tSCKL(5)                                                                                                                                                                                                                                  |                 |                                                                                                                                                                                                                                           |                     |                            |                             | 1                           |      |      |
|              |              | High level pulse width                 | tSCKH(5)                                                                                                                                                                                                                                  |                 |                                                                                                                                                                                                                                           |                     |                            |                             | 1                           |      |      |
|              |              |                                        | tSCKHA(5a)                                                                                                                                                                                                                                |                 | <ul style="list-style-type: none"><li>• USB, SIO0 continuous transfer mode, AIF, SIO9, and DMCOPY not used at the same time.</li><li>• See Fig. 9.</li><li>• (Note 4-3-2)</li></ul>                                                       |                     | 4                          |                             |                             |      |      |
|              |              |                                        | tSCKHA(5b)                                                                                                                                                                                                                                |                 | <ul style="list-style-type: none"><li>• USB used at the same time</li><li>• SIO0 continuous transfer mode, AIF, SIO9, and DMCOPY not used at the same time.</li><li>• See Fig. 9.</li><li>• (Note 4-3-2)</li></ul>                        |                     | 7                          |                             |                             |      |      |
|              |              | tSCKHA(5c)                             | <ul style="list-style-type: none"><li>• USB, SIO0 continuous transfer mode, SIO9, and DMCOPY used at the same time.</li><li>• AIF not used at the same time.</li><li>• See Fig. 9.</li><li>• (Note 4-3-2)</li></ul>                       |                 | 12                                                                                                                                                                                                                                        |                     |                            |                             |                             |      |      |
|              | Output clock | Frequency                              | tSCK(6)                                                                                                                                                                                                                                   | SCK4(P24)       | <ul style="list-style-type: none"><li>• When CMOS output type is selected.</li><li>• See Fig. 9.</li></ul>                                                                                                                                | 2.7 to 5.5          | 4/3                        |                             |                             | tSCK |      |
|              |              | Low level pulse width                  | tSCKL(6)                                                                                                                                                                                                                                  |                 |                                                                                                                                                                                                                                           |                     | 1/2                        |                             |                             |      | tCYC |
|              |              | High level pulse width<br>(Note 4-3-3) | tSCKH(6)                                                                                                                                                                                                                                  |                 |                                                                                                                                                                                                                                           |                     | 1/2                        |                             |                             |      |      |
|              |              |                                        | tSCKHA(6a)                                                                                                                                                                                                                                |                 | <ul style="list-style-type: none"><li>• USB, SIO0 continuous transfer mode, AIF, SIO9, and DMCOPY not used at the same time.</li><li>• When CMOS output type is selected.</li><li>• See Fig. 9.</li></ul>                                 |                     | tSCKH(6)<br>+<br>(5/3)tCYC |                             | tSCKH(6)<br>+<br>(10/3)tCYC | tCYC |      |
|              |              |                                        | tSCKHA(6b)                                                                                                                                                                                                                                |                 | <ul style="list-style-type: none"><li>• USB used at the same time.</li><li>• SIO0 continuous transfer mode, AIF, SIO9, and DMCOPY not used at the same time.</li><li>• When CMOS output type is selected.</li><li>• See Fig. 9.</li></ul> |                     | tSCKH(6)<br>+<br>(5/3)tCYC |                             | tSCKH(6)<br>+<br>(19/3)tCYC |      |      |
|              |              | tSCKHA(6c)                             | <ul style="list-style-type: none"><li>• USB, SIO0 continuous transfer mode, SIO9, and DMCOPY used at the same time.</li><li>• AIF not used at the same time.</li><li>• When CMOS output type is selected.</li><li>• See Fig. 9.</li></ul> |                 | tSCKH(6)<br>+<br>(5/3)tCYC                                                                                                                                                                                                                |                     |                            | tSCKH(6)<br>+<br>(34/3)tCYC |                             |      |      |

Note 4-3-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-3-2: In an application where the serial clock input is to be used in the continuous data transfer mode, the period from the time SI4RUN is set with the serial clock set high to the falling edge of the first serial clock must be longer than tSCKHA.

Note 4-3-3: When using the serial clock output, make sure that the load at the SCK4 (P24) pin meets the following conditions:

Clock rise time tSCKR < 0.037μs (see Figure 12.) at Ta=+25°C, V<sub>DD</sub>=3.3V

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| Parameter     |                   | Symbol  | Pin/<br>Remarks       | Conditions                                                                                                                                                                                                                                 | V <sub>DD</sub> [V] | Specification |     |                                |      |
|---------------|-------------------|---------|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------|-----|--------------------------------|------|
|               |                   |         |                       |                                                                                                                                                                                                                                            |                     | min           | typ | max                            | unit |
| Serial input  | Data setup time   | tsDI(3) | SO4(P22),<br>SI4(P23) | <ul style="list-style-type: none"> <li>Must be specified with respect to rising edge of SIOCLK.</li> <li>See Fig. 9</li> </ul>                                                                                                             | 2.7 to 5.5          | 0.03          |     |                                | μs   |
|               | Data hold time    | thDI(3) |                       |                                                                                                                                                                                                                                            |                     | 0.03          |     |                                |      |
| Serial output | Output delay time | tdDO(5) | SO4(P22),<br>SI4(P23) | <ul style="list-style-type: none"> <li>Must be specified with respect to falling edge of SIOCLK.</li> <li>Must be specified as the time to the beginning of output state change in open drain output mode.</li> <li>See Fig. 9.</li> </ul> | 2.7 to 5.5          |               |     | (1/3)t <sub>CYC</sub><br>+0.05 |      |

### 4. SIO9 Serial I/O Characteristics (Note 4-4-1)

| Parameter                   |                        | Symbol     | Pin/<br>Remarks | Conditions                                                                                                                                                                                                       | V <sub>DD</sub> [V] | Specification |     |     |                  |
|-----------------------------|------------------------|------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------|-----|-----|------------------|
|                             |                        |            |                 |                                                                                                                                                                                                                  |                     | min           | typ | max | unit             |
| Serial clock<br>input clock | Frequency              | tSCK(7)    | SCK9(P27)       | See Fig. 9.                                                                                                                                                                                                      | 2.7 to 5.5          | 2             |     |     | t <sub>CYC</sub> |
|                             | Low level pulse width  | tSCKL(7)   |                 |                                                                                                                                                                                                                  |                     | 1             |     |     |                  |
|                             | High level pulse width | tSCKH(7)   |                 |                                                                                                                                                                                                                  |                     | 1             |     |     |                  |
|                             |                        | tSCKHA(7a) |                 | <ul style="list-style-type: none"> <li>USB, SIO0 continuous transfer mode, AIF, SIO4, and DMCOPY not used at the same time.</li> <li>See Fig. 9.</li> <li>(Note 4-4-2)</li> </ul>                                |                     | 4             |     |     |                  |
|                             |                        | tSCKHA(7b) |                 | <ul style="list-style-type: none"> <li>USB used at the same time.</li> <li>SIO0 continuous transfer mode, AIF, SIO4, and DMCOPY not used at the same time.</li> <li>See Fig. 9.</li> <li>(Note 4-4-2)</li> </ul> |                     | 7             |     |     |                  |
|                             |                        | tSCKHA(7c) |                 | <ul style="list-style-type: none"> <li>USB, SIO0 continuous transfer mode, SIO4, and DMCOPY used at the same time.</li> <li>AIF not used at the same time.</li> <li>See Fig. 9.</li> <li>(Note 4-4-2)</li> </ul> |                     | 15            |     |     |                  |

Note 4-4-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-4-2: In an application where the serial clock input is to be used in the continuous data transfer mode, the period from the time SI9RUN is set with the serial clock set high to the falling edge of the first serial clock must be longer than tSCKHA.

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| Parameter     |                   |                                        | Symbol                | Pin/<br>Remarks                                                                                                                                                                                                                             | Conditions                                                                                                 | V <sub>DD</sub> [V] | Specification               |                    |     |      |
|---------------|-------------------|----------------------------------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|---------------------|-----------------------------|--------------------|-----|------|
|               |                   |                                        |                       |                                                                                                                                                                                                                                             |                                                                                                            |                     | min                         | typ                | max | unit |
| Serial clock  | Output clock      | Frequency                              | tSCK(8)               | SCK9(P27)                                                                                                                                                                                                                                   | <ul style="list-style-type: none"><li>• When CMOS output type is selected.</li><li>• See Fig. 9.</li></ul> | 2.7 to 5.5          | 4/3                         |                    |     | tCYC |
|               |                   | Low level pulse width                  | tSCKL(8)              |                                                                                                                                                                                                                                             |                                                                                                            |                     | 1/2                         |                    |     | tSCK |
|               |                   | High level pulse width<br>(Note 4-4-3) | tSCKH(8)              |                                                                                                                                                                                                                                             |                                                                                                            |                     | 1/2                         |                    |     |      |
|               |                   |                                        | tSCKHA(8a)            | <ul style="list-style-type: none"><li>• USB, SIO0 continuous transfer mode, AIF, SIO4, and DMCPY not used at the same time.</li><li>• When CMOS output type is selected.</li><li>• See Fig. 9.</li></ul>                                    | tSCKH(8)<br>+<br>(5/3)tCYC                                                                                 |                     | tSCKH(8)<br>+<br>(10/3)tCYC | tCYC               |     |      |
|               |                   |                                        | tSCKHA(8b)            | <ul style="list-style-type: none"><li>• USB used at the same time.</li><li>• SIO0 continuous transfer mode, AIF, SIO4, and DMCPY not used at the same time.</li><li>• When CMOS output type is selected</li><li>• See Fig. 9.</li></ul>     | tSCKH(8)<br>+<br>(5/3)tCYC                                                                                 |                     | tSCKH(8)<br>+<br>(19/3)tCYC |                    |     |      |
|               |                   |                                        | tSCKHA(8c)            | <ul style="list-style-type: none"><li>• USB, SIO0 continuous transfer mode , SIO4, and DMCPY used at the same time.</li><li>• AIF not used at the same time.</li><li>• When CMOS output type is selected.</li><li>• See Fig. 9.</li></ul>   | tSCKH(8)<br>+<br>(5/3)tCYC                                                                                 |                     | tSCKH(8)<br>+<br>(43/3)tCYC |                    |     |      |
| Serial input  | Data setup time   | tsDI(4)                                | SO9(P25),<br>SI9(P26) | <ul style="list-style-type: none"><li>• Must be specified with respect to rising edge of SIOCLK.</li><li>• See Fig. 9.</li></ul>                                                                                                            | 2.7 to 5.5                                                                                                 | 0.03                |                             |                    | μs  |      |
|               | Data hold time    | thDI(4)                                |                       |                                                                                                                                                                                                                                             |                                                                                                            | 0.03                |                             |                    |     |      |
| Serial output | Output delay time | tdDO(6)                                | SO9(P25),<br>SI9(P26) | <ul style="list-style-type: none"><li>• Must be specified with respect to falling edge of SIOCLK.</li><li>• Must be specified as the time to the beginning of output state change in open drain output mode</li><li>• See Fig. 9.</li></ul> | 2.7 to 5.5                                                                                                 |                     |                             | (1/3)tCYC<br>+0.05 |     |      |

Note 4-4-3: When using the serial clock output, make sure that the load at the SCK9 (P27) pin meets the following conditions:

Clock rise time tSCKR < 0.037μs (see Figure 12.) at Ta=+25°C, V<sub>DD</sub>=3.3V

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### Pulse Input Conditions at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

| Parameter                  | Symbol             | Pin/Remarks                                                                               | Conditions                                                                                                                              | Specification       |     |     |     |                    |
|----------------------------|--------------------|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|-----|-----|--------------------|
|                            |                    |                                                                                           |                                                                                                                                         | V <sub>DD</sub> [V] | min | typ | max | unit               |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27), INT6(P20), INT7(P24) | <ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 or 1 are enabled.</li> </ul> | 2.7 to 5.5          | 1   |     |     | tCYC               |
|                            | tPIH(2)<br>tPIL(2) | INT3(P73) when noise filter time constant is 1/1                                          | <ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul>      | 2.7 to 5.5          | 2   |     |     |                    |
|                            | tPIH(3)<br>tPIL(3) | INT3(P73) when noise filter time constant is 1/32                                         | <ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul>      | 2.7 to 5.5          | 64  |     |     |                    |
|                            | tPIH(4)<br>tPIL(4) | INT3(P73) when noise filter time constant is 1/128                                        | <ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul>      | 2.7 to 5.5          | 256 |     |     |                    |
|                            | tPIL(5)            | RMIN(P73)                                                                                 | Recognized by the infrared remote control receiver circuit as a signal                                                                  | 2.7 to 5.5          | 4   |     |     | RMCK<br>(Note 5-1) |
|                            | tPIL(6)            | RES                                                                                       | Resetting is enabled.                                                                                                                   | 2.7 to 5.5          | 200 |     |     | μs                 |

Note 5-1: Represents the period of the reference clock (1 tCYC to 128 tCYC or the source frequency of the subclock) for the infrared remote control receiver circuit.

### AD Converter Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

| Parameter                  | Symbol            | Pin/Remarks                                                    | Conditions                                           | Specification       |                      |     |                     |      |
|----------------------------|-------------------|----------------------------------------------------------------|------------------------------------------------------|---------------------|----------------------|-----|---------------------|------|
|                            |                   |                                                                |                                                      | V <sub>DD</sub> [V] | min                  | typ | max                 | unit |
| Resolution                 | N                 | AN0(P00) to AN7(P07), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2) |                                                      | 3.0 to 5.5          |                      | 8   |                     | bit  |
| Absolute accuracy          | ET                |                                                                | (Note 6-1)                                           | 3.0 to 5.5          |                      |     | ±1.5                | LSB  |
| Conversion time            | TCAD              |                                                                | AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2) | 4.5 to 5.5          | 15.68 (tCYC=0.490μs) |     | 97.92 (tCYC=3.06μs) | μs   |
|                            |                   |                                                                |                                                      | 3.0 to 5.5          | 23.52 (tCYC=0.735μs) |     | 97.92 (tCYC=3.06μs) |      |
|                            |                   |                                                                | AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2) | 4.5 to 5.5          | 18.82 (tCYC=0.294μs) |     | 97.92 (tCYC=1.53μs) |      |
|                            |                   |                                                                |                                                      | 3.0 to 5.5          | 47.04 (tCYC=0.735μs) |     | 97.92 (tCYC=1.53μs) |      |
| Analog input voltage range | VAIN              |                                                                |                                                      | 3.0 to 5.5          | V <sub>SS</sub>      |     | V <sub>DD</sub>     | V    |
| Analog port input current  | I <sub>AINH</sub> |                                                                | V <sub>AIN</sub> =V <sub>DD</sub>                    | 3.0 to 5.5          |                      |     | 1                   | μA   |
|                            | I <sub>AINL</sub> |                                                                | V <sub>AIN</sub> =V <sub>SS</sub>                    | 3.0 to 5.5          | -1                   |     |                     |      |

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy.

Note 6-2: The conversion time refers to the period from the time when an instruction for starting a conversion process is issued to the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

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## Consumption Current Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

| Parameter                                     | Symbol      | Pin/<br>Remarks        | Conditions                                                                                                                                                                                                                                                                                                                                                    | VDD[V]     | Specification |      |      |      |
|-----------------------------------------------|-------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|---------------|------|------|------|
|                                               |             |                        |                                                                                                                                                                                                                                                                                                                                                               |            | min           | typ  | max  | unit |
| Normal mode consumption current<br>(Note 7-1) | IDDOP(1)    | VDD1<br>=VDD2<br>=VDD3 | <ul style="list-style-type: none"> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 12MHz side</li> <li>Internal PLL oscillation stopped</li> <li>Internal RC oscillation stopped</li> <li>USB circuit stopped</li> <li>1/1 frequency division ratio</li> </ul>                       | 4.5 to 5.5 |               | 11   | 27   | mA   |
|                                               | IDDOP(2)    |                        | <ul style="list-style-type: none"> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 12MHz side</li> <li>Internal PLL oscillation stopped</li> <li>Internal RC oscillation stopped</li> <li>USB circuit stopped</li> <li>1/1 frequency division ratio</li> </ul>                       | 3.0 to 3.6 |               | 6.2  | 16   |      |
|                                               | IDDOP(3)    |                        | <ul style="list-style-type: none"> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 12MHz side</li> <li>Internal PLL oscillation mode active</li> <li>Internal RC oscillation stopped</li> <li>USB circuit active</li> <li>1/1 frequency division ratio</li> </ul>                    | 4.5 to 5.5 |               | 16   | 37   |      |
|                                               | IDDOP(4)    |                        | <ul style="list-style-type: none"> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 12MHz side</li> <li>Internal PLL oscillation mode active</li> <li>Internal RC oscillation stopped</li> <li>USB circuit active</li> <li>1/1 frequency division ratio</li> </ul>                    | 3.0 to 3.6 |               | 8.0  | 21   |      |
|                                               | IDDOP(5)    |                        | <ul style="list-style-type: none"> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 6MHz side</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio</li> </ul>                                                                                               | 4.5 to 5.5 |               | 7.2  | 17   |      |
|                                               | IDDOP(6)    |                        | <ul style="list-style-type: none"> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 6MHz side</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio</li> </ul>                                                                                               | 3.0 to 3.6 |               | 4.4  | 11   |      |
|                                               | IDDOP(7)    |                        | <ul style="list-style-type: none"> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 6MHz side</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio</li> </ul>                                                                                               | 2.7 to 3.0 |               | 3.6  | 8.2  |      |
|                                               | IDDOP(8)    |                        | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to internal RC oscillation</li> <li>1/2 frequency division ratio</li> </ul>                                                                                                                               | 4.5 to 5.5 |               | 0.77 | 3.7  |      |
|                                               | IDDOP(9)    |                        | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to internal RC oscillation</li> <li>1/2 frequency division ratio</li> </ul>                                                                                                                               | 3.0 to 3.6 |               | 0.43 | 2.0  |      |
|                                               | IDDOP(10)   |                        | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to internal RC oscillation</li> <li>1/2 frequency division ratio</li> </ul>                                                                                                                               | 2.7 to 3.0 |               | 0.36 | 1.6  |      |
|                                               | IDDOP(11)   |                        | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to crystal oscillation side (32.768kHz)</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio</li> </ul>                                                                         | 4.5 to 5.5 |               | 47   | 184  | μA   |
|                                               | IDDOP(12)   |                        | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to crystal oscillation side (32.768kHz)</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio</li> </ul>                                                                         | 3.0 to 3.6 |               | 19   | 65   |      |
|                                               | IDDOP(13)   |                        | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to crystal oscillation side (32.768kHz)</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio</li> </ul>                                                                         | 2.7 to 3.0 |               | 15   | 51   |      |
| HALT mode consumption current<br>(Note7-1)    | IDDHALT(1)  |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 12MHz side</li> <li>Internal PLL oscillation stopped</li> <li>Internal RC oscillation stopped</li> <li>USB circuit stopped</li> <li>1/1 frequency division ratio</li> </ul>    | 4.5 to 5.5 |               | 4.9  | 12   | mA   |
|                                               | IDDHALT(2)  |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 12MHz side</li> <li>Internal PLL oscillation stopped</li> <li>Internal RC oscillation stopped</li> <li>USB circuit stopped</li> <li>1/1 frequency division ratio</li> </ul>    | 3.0 to 3.6 |               | 2.7  | 6.4  |      |
|                                               | IDDHALT(3)  |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 12MHz side</li> <li>Internal PLL oscillation mode active</li> <li>Internal RC oscillation stopped</li> <li>USB circuit active</li> <li>1/1 frequency division ratio</li> </ul> | 4.5 to 5.5 |               | 9.5  | 23   |      |
|                                               | IDDHALT(4)  |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 12MHz side</li> <li>Internal PLL oscillation mode active</li> <li>Internal RC oscillation stopped</li> <li>USB circuit active</li> <li>1/1 frequency division ratio</li> </ul> | 3.0 to 3.6 |               | 4.7  | 12   |      |
|                                               | IDDHALT(5)  |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 6MHz side</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio</li> </ul>                                                                            | 4.5 to 5.5 |               | 3.0  | 7.3  |      |
|                                               | IDDHALT(6)  |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 6MHz side</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio</li> </ul>                                                                            | 3.0 to 3.6 |               | 1.6  | 3.8  |      |
|                                               | IDDHALT(7)  |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 6MHz side</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division ratio</li> </ul>                                                                            | 2.7 to 3.0 |               | 1.3  | 2.9  |      |
|                                               | IDDHALT(8)  |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=0Hz (oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to internal RC oscillation</li> <li>1/2 frequency division ratio</li> </ul>                                                                                                            | 4.5 to 5.5 |               | 0.41 | 2.0  |      |
|                                               | IDDHALT(9)  |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=0Hz (oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to internal RC oscillation</li> <li>1/2 frequency division ratio</li> </ul>                                                                                                            | 3.0 to 3.6 |               | 0.20 | 0.95 |      |
|                                               | IDDHALT(10) |                        | <ul style="list-style-type: none"> <li>HALT mode</li> <li>FmCF=0Hz (oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to internal RC oscillation</li> <li>1/2 frequency division ratio</li> </ul>                                                                                                            | 2.7 to 3.0 |               | 0.17 | 0.70 |      |

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

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Continued from preceding page.

| Parameter                                   | Symbol      | Pin/<br>Remarks                                            | Conditions                                                                                                                                                                                                                                                                                                           | Specification       |     |      |     |      |
|---------------------------------------------|-------------|------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|------|-----|------|
|                                             |             |                                                            |                                                                                                                                                                                                                                                                                                                      | V <sub>DD</sub> [V] | min | typ  | max | unit |
| HALT mode consumption current<br>(Note 7-1) | IDDHALT(11) | V <sub>DD1</sub><br>=V <sub>DD2</sub><br>=V <sub>DD3</sub> | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz (oscillation stopped)</li> <li>• FsX'tal=32.768kHz crystal oscillation mode</li> <li>• System clock set to crystal oscillation side (32.768kHz)</li> <li>• Internal RC oscillation stopped</li> <li>• 1/2 frequency division ratio</li> </ul> | 4.5 to 5.5          |     | 31   | 132 | μA   |
|                                             | IDDHALT(12) |                                                            |                                                                                                                                                                                                                                                                                                                      | 3.0 to 3.6          |     | 9.1  | 53  |      |
|                                             | IDDHALT(13) |                                                            |                                                                                                                                                                                                                                                                                                                      | 2.7 to 3.0          |     | 6.3  | 42  |      |
| HOLD mode consumption current               | IDDHOLD(1)  | V <sub>DD1</sub>                                           | <ul style="list-style-type: none"> <li>• HOLD mode</li> <li>• CF1=V<sub>DD</sub> or open (External clock mode)</li> </ul>                                                                                                                                                                                            | 4.5 to 5.5          |     | 0.24 | 72  |      |
|                                             | IDDHOLD(2)  |                                                            |                                                                                                                                                                                                                                                                                                                      | 3.0 to 3.6          |     | 0.12 | 38  |      |
|                                             | IDDHOLD(3)  |                                                            |                                                                                                                                                                                                                                                                                                                      | 2.7 to 3.0          |     | 0.11 | 33  |      |
| Timer HOLD mode consumption current         | IDDHOLD(4)  |                                                            | <ul style="list-style-type: none"> <li>• Timer HOLD mode</li> <li>• CF1=V<sub>DD</sub> or open (External clock mode)</li> <li>• FsX'tal=32.768kHz crystal oscillation mode</li> </ul>                                                                                                                                | 4.5 to 5.5          |     | 26   | 115 |      |
|                                             | IDDHOLD(5)  |                                                            |                                                                                                                                                                                                                                                                                                                      | 3.0 to 3.6          |     | 6.1  | 50  |      |
|                                             | IDDHOLD(6)  |                                                            |                                                                                                                                                                                                                                                                                                                      | 2.7 to 3.0          |     | 3.8  | 40  |      |

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

### USB Characteristics and Timing at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = V<sub>SS3</sub> = 0V

| Parameter                            | Symbol                | Conditions                                  | Specification |     |     |      |
|--------------------------------------|-----------------------|---------------------------------------------|---------------|-----|-----|------|
|                                      |                       |                                             | min           | typ | max | unit |
| High level output                    | V <sub>OH</sub> (USB) | • 15kΩ±5% to GND                            | 2.8           |     | 3.6 | V    |
| Low level output                     | V <sub>OL</sub> (USB) | • 1.5kΩ±5% to 3.6V                          | 0.0           |     | 0.3 | V    |
| Output signal crossover voltage      | V <sub>CRS</sub>      |                                             | 1.3           |     | 2.0 | V    |
| Differential input sensitivity       | V <sub>DI</sub>       | •  (UHD+)-(UHD-)                            | 0.2           |     |     | V    |
| Differential input common mode range | V <sub>CM</sub>       |                                             | 0.8           |     | 2.5 | V    |
| High level input                     | V <sub>IH</sub> (USB) |                                             | 2.0           |     |     | V    |
| Low level input                      | V <sub>IL</sub> (USB) |                                             |               |     | 0.8 | V    |
| USB data rise time                   | t <sub>R</sub>        | • R <sub>S</sub> =33Ω, C <sub>L</sub> =50pF | 4             |     | 20  | ns   |
| USB data fall time                   | t <sub>F</sub>        | • R <sub>S</sub> =33Ω, C <sub>L</sub> =50pF | 4             |     | 20  | ns   |

### F-ROM Programming Characteristics at Ta = +10°C to +55°C, V<sub>SS1</sub> = V<sub>SS2</sub> = V<sub>SS3</sub> = 0V

| Parameter                   | Symbol   | Pin/<br>Remarks  | Conditions                                                 | Specification       |     |     |     |      |
|-----------------------------|----------|------------------|------------------------------------------------------------|---------------------|-----|-----|-----|------|
|                             |          |                  |                                                            | V <sub>DD</sub> [V] | min | typ | max | unit |
| Onboard programming current | IDDFW(1) | V <sub>DD1</sub> | • Excluding power dissipation in the microcontroller block | 3.0 to 5.5          |     | 5   | 10  | mA   |
| Programming time            | tFW(1)   |                  | • Erase operation                                          | 3.0 to 5.5          |     | 20  | 30  | ms   |
|                             | tFW(2)   |                  | • Write operation                                          |                     |     | 40  | 60  | μs   |

### Main System Clock Oscillation

The constant values of the oscillator and oscillation circuit for the main and system clocks must be determined after exercising extensive oscillation evaluation tests. For an application in which the USB host function is to be used, use an oscillator having the accuracy and precision that satisfy the USB specifications.

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 4):

- Till the oscillation gets stabilized after V<sub>DD</sub> goes above the operating voltage lower limit.
- Till the oscillation gets stabilized after the instruction for starting the main clock oscillation circuit is executed.
- Till the oscillation gets stabilized after the HOLD mode is released.
- Till the oscillation gets stabilized after the X'tal HOLD mode is released with CFSTOP (OCR register, bit 0) set to 0.

Subsystem Clock Oscillation

Table 1 shows the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample subsystem Clock Oscillator Circuit with a Crystal Oscillator

| Nominal Frequency | Vendor Name   | Oscillator Name | Circuit Constant |         |        |         | Operating Voltage Range [V] | Oscillation Stabilization Time |         | Remarks                             |
|-------------------|---------------|-----------------|------------------|---------|--------|---------|-----------------------------|--------------------------------|---------|-------------------------------------|
|                   |               |                 | C3 [pF]          | C4 [pF] | Rf [Ω] | Rd2 [Ω] |                             | typ [s]                        | max [s] |                                     |
| 32.768kHz         | EPSON TOYOCOM | MC-306          | 18               | 18      | OPEN   | 560k    | 2.7 to 5.0                  | 1.1                            | 3.0     | Applicable CL value=12.5pF SMD type |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 4):

- Till the oscillation gets stabilized after the instruction for starting the subclock oscillation circuit is executed.
- Till the oscillation gets stabilized after the HOLD mode is released with EXTOSC (OCR register, bit 6) set to 1.

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

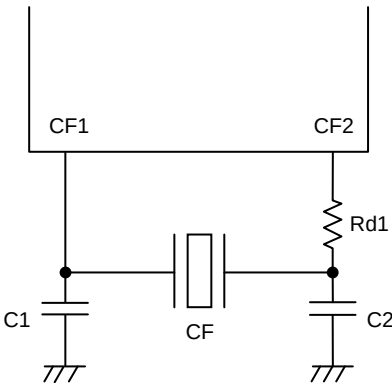


Figure 1 CF Oscillator Circuit

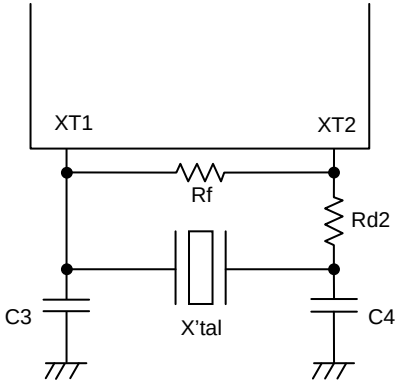


Figure 2 Crystal Oscillator Circuit

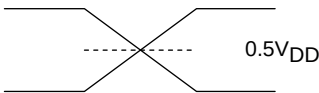
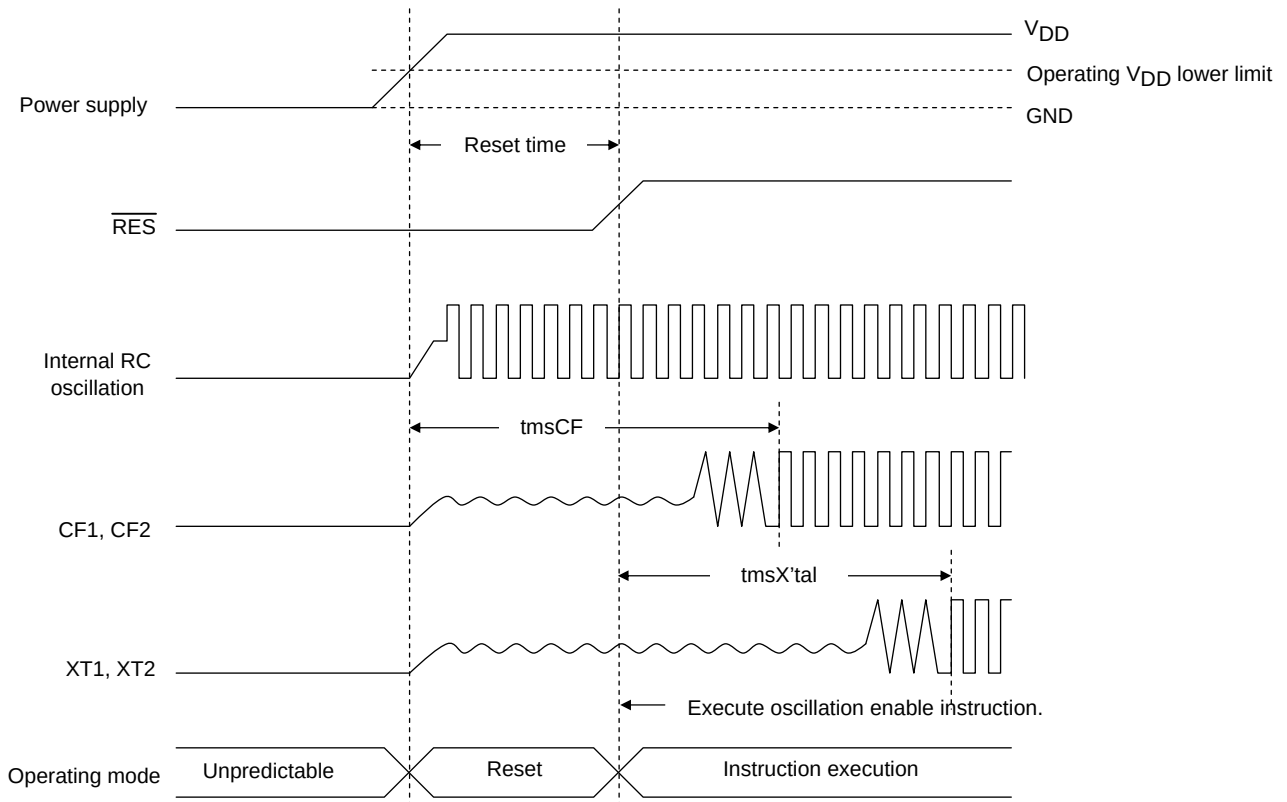
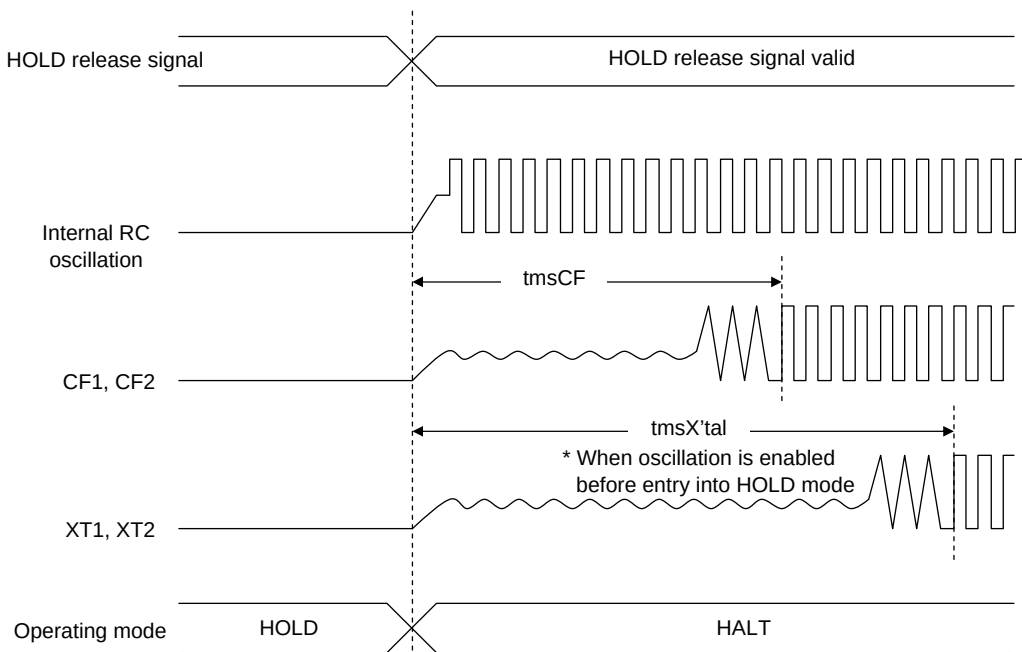


Figure 3 AC Timing Measurement Point



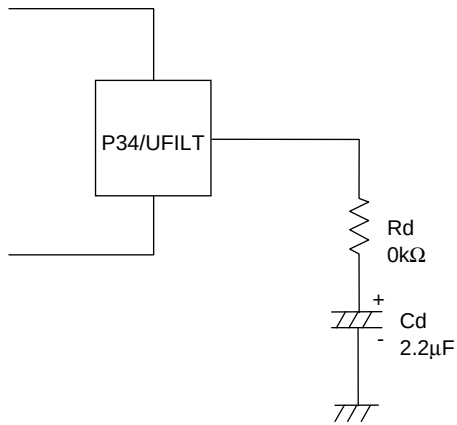
Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

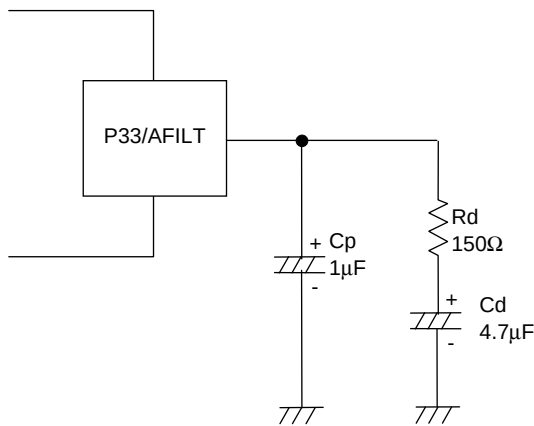
Figure 4 Oscillation Stabilization Time





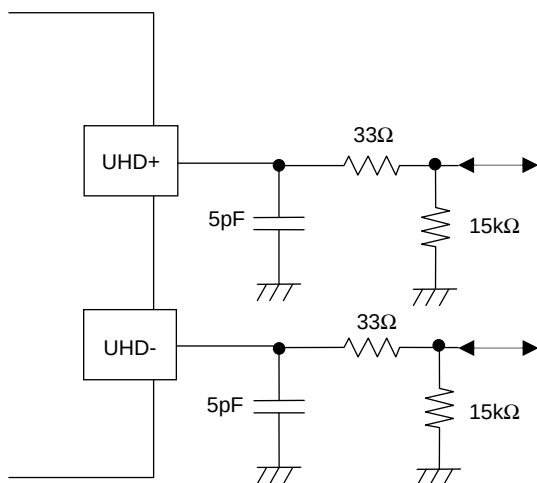
When using the internal PLL circuit to generate the 48MHz clock for USB, it is necessary to connect a filter circuit to the P34/UFILT pin such as that shown in the left figure.

Figure 5 External Filter Circuit for the Internal USB-dedicated PLL Circuit



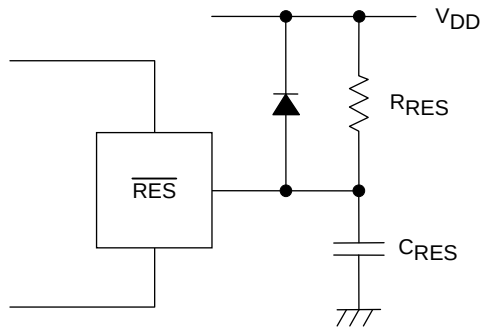
To generate the master clock for the audio interface using the internal PLL circuit, it is necessary to connect a filter circuit to the P33/AFILT pin that is shown in the left figure.

Figure 6 External Filter Circuit for Audio Interface (Used with Internal PLL Circuit)



It is necessary to adjust the Circuit Constant of the USB Port Peripheral Circuit for each mounting board.

Figure 7 USB Port Peripheral Circuit



Note:  
Determine the value of  $C_{RES}$  and  $R_{RES}$  so that the reset signal is present for a period of  $200\mu s$  after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 8 Reset Circuit

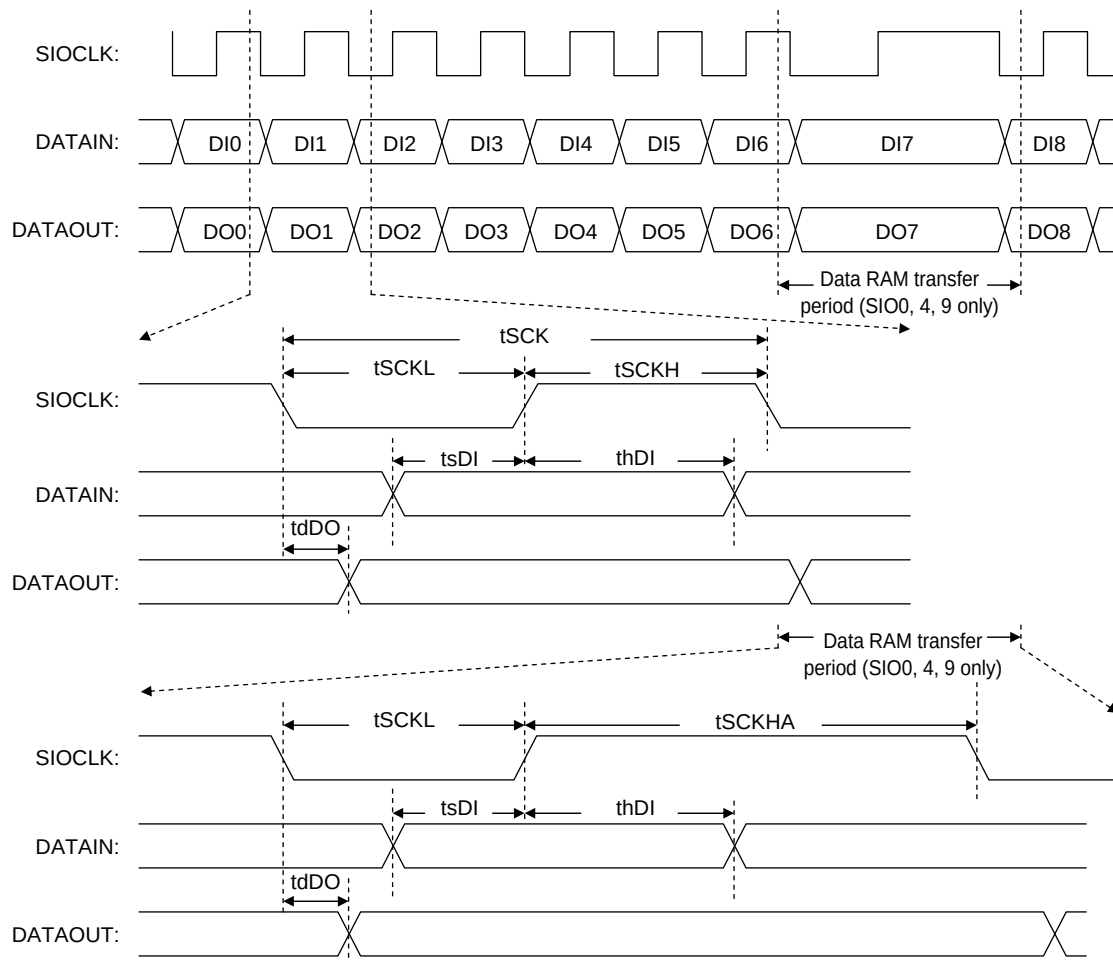


Figure 9 Serial I/O Waveform

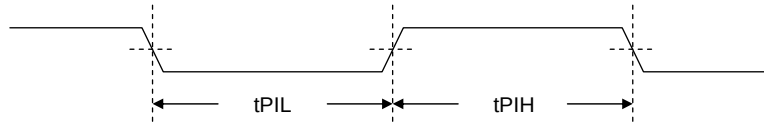


Figure 10 Pulse Input Timing Signal Waveform

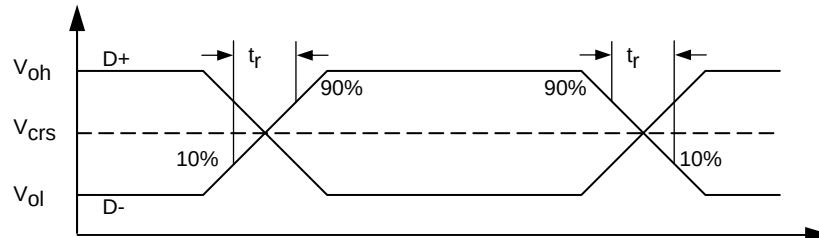
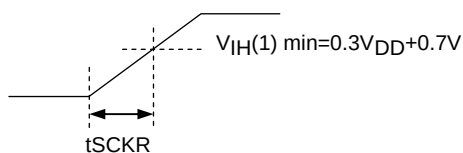


Figure 11 USB Data Signal Timing and Voltage Level



tSCKR:

Defined as the time period from the time the state of the output starts changing till the time it reaches the value of  $V_{IH(1)}$ .

Figure 12 Serial Clock Output Timing Signal Waveform

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