



LC78816MB, 78816MC

16-Bit D/A Converter for Use in Digital Audio Products

Preliminary

Overview

The LC78816MB and 78816MC are 16-bit CMOS D/A converters for use in digital audio products. They employ a dynamic level shift conversion technique that combines a resistor string (for the upper 9 bits), PWM (for the middle 3 bits), and level shifting (for the lower 4 bits).

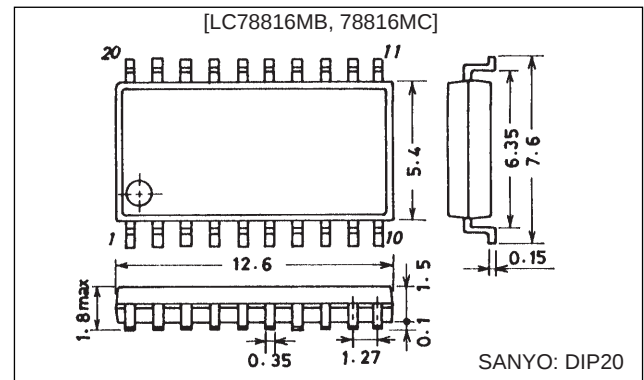
Features

- Two's complement data format
- Two D/A converter channels built in (in-phase outputs)
- Maximum conversion frequency of 400 kHz (support for 8 times oversampling)
- Built-in output op amps
- No deglitching circuit required
- Si gate CMOS process (low power consumption)
- 5 V single-voltage power supply
- Low voltage (3.5 V) operation possible

Package Dimensions

unit: mm

3036B-MFP20



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	$V_{DD\ max}$		-0.3 to +7.0	V
Input voltage	V_{IN}		-0.3 to $V_{DD} + 0.3$	V
Output voltage	V_{OUT}		-0.3 to $V_{DD} + 0.3$	V
Operating temperature	T_{opr}		-30 to +75	°C
Storage temperature	T_{stg}		-40 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply voltage	V_{DD}		3.5	5.0	5.5	V
Reference voltage high	V_{refH}		$V_{DD} - 0.3$		V_{DD}	V
Reference voltage low	V_{refL}		0		0.3	V
Operating temperature	T_{opr}		-30		+75	°C

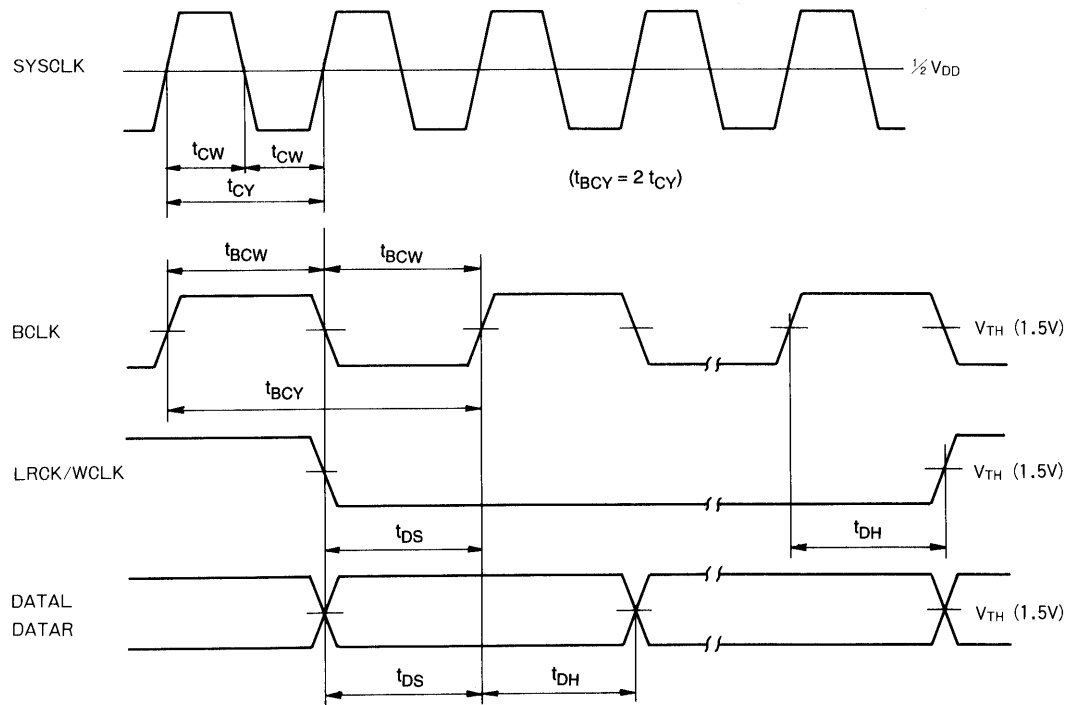
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DC Characteristics at Ta = -30 to +75°C, VDD = 3.5 to 5.5 V, VSS = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high level voltage (1)	V _{IH}	Input pins other than SYSCLK	2.2			V
Input low level voltage (1)	V _{IL}	Input pins other than SYSCLK			0.8	V
Input high level voltage (2)	V _{IH}	The SYSCLK pin	0.7 V _{DD}			V
Input low level voltage (2)	V _{IL}	The SYSCLK pin			0.3 V _{DD}	V

AC Characteristics at Ta = -30 to +75°C, VDD = 3.5 to 5.5 V, VSS = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock pulse width	t _{CW}	SYSCLK	25			ns
	t _{BCW}	BCLK	35			ns
Setup time	t _{DS}	LRCK/WCLK DAT _L DAT _R	20			ns
Hold time	t _{DH}		20			ns



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Electrical Characteristics (1) at $T_a = 25^\circ\text{C}$, $DV_{DD} = AV_{DD} = V_{refH} = 5.0\text{ V}$, $DGND = AGND = V_{refL} = 0.0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Resolution	RES			16		Bits
Conversion frequency	fs				400	kHz
Total harmonic distortion	THD1	LC78816MB at 1 kHz, 0 dB			0.05*	%
Total harmonic distortion	THD1	LC78816MC at 1 kHz, 0 dB			0.08	%
Dynamic range	D_R	At 1 kHz, -60 dB	94	96		dB
Cross talk	$C \cdot T$	At 1 kHz, 0 dB			-85	dB
Signal to noise ratio	S/N	JIS-A	96			dB
Full scale output voltage	VFS		3.0	3.3	3.5	Vp-p
Power dissipation	Pd			35	60	mW
Output load resistance	R_L	Pins 1 and 20	5			k Ω

Notes*: Screened units

Test circuit: based on the sample application circuit, with a sampling frequency (fs) of 88.2 kHz.

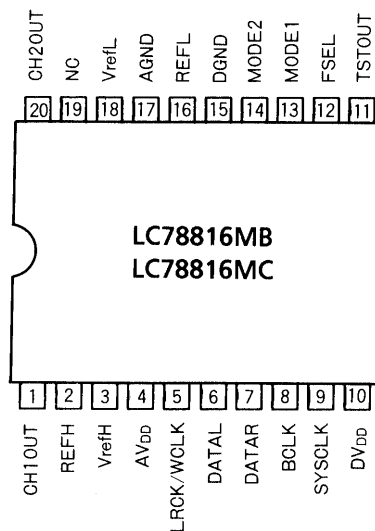
Electrical Characteristics (2) at $T_a = 25^\circ\text{C}$, $DV_{DD} = AV_{DD} = V_{refH} = 5.0\text{ V}$, $DGND = AGND = V_{refL} = 0.0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Resolution	RES			16		Bits
Conversion frequency	fs				400	kHz
Total harmonic distortion	THD1	LC78816MB at 1 kHz, 0 dB			0.06*	%
Total harmonic distortion	THD1	LC78816MC at 1 kHz, 0 dB			0.09	%
Dynamic range	D_R	At 1 kHz, -60 dB	92	94		dB
Cross talk	$C \cdot T$	At 1 kHz, 0 dB			-85	dB
Signal to noise ratio	S/N	JIS-A	96			dB
Full scale output voltage	VFS		2.0	2.3	2.5	Vp-p
Power dissipation	Pd			10	20	mW
Output load resistance	R_L	Pins 1 and 20	15			k Ω

Notes*: Screened units

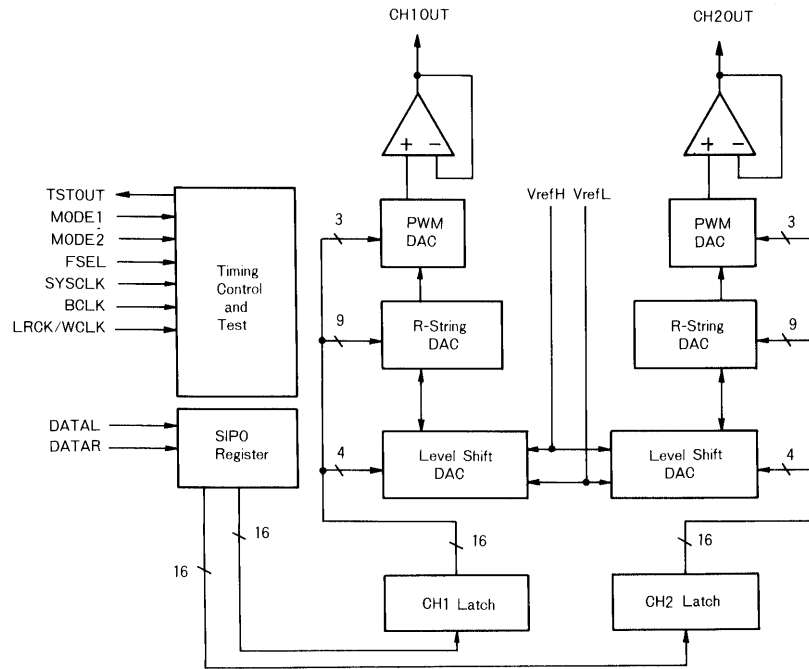
Test circuit: based on the sample application circuit, with a sampling frequency (fs) of 88.2 kHz.

Pin Assignment



Top view

Block Diagram



Pin Functions

Pin No.	Pin Name	Function and Operational Description
1	CH1OUT	Channel 1 output pin (left channel)
2	REFH	Reference voltage high level pin Normally connected to AGND through a capacitor.
3	VrefH	Reference voltage high level input pin
4	AV _{DD}	Analog system power supply voltage pin
5	LRCK/WCLK	LR clock and word clock input pin Used to generate the internal signal that latches the digital audio data (DATAL and DATAR).
6	DATAL	Digital audio data input pin Data is input from the MSB bit serially. When FSEL is low, channel 1 data is input. When FSEL is high, channel 1 and channel 2 data are input using time division.
7	DATAR	Digital audio data input pin Data is input from the MSB bit serially. When FSEL is low, channel 2 data is input. When FSEL is high, functions as the interface switching pin.
8	BCLK	Bit clock input pin This is the clock for reading in digital audio data bit serially. Also functions as the IC's system clock when SYSCLK is fixed low or high.
9	SYSCLK	System clock input pin This is the system clock that drives the IC. However, in certain modes it is used as the interface switching pin. (See the timing charts.)
10	DV _{DD}	Digital system power supply voltage pin
11	TSTOUT	Output pin for IC testing
12	FSEL	When low, digital audio data is input simultaneously from the DATAL and DATAR pins. When high, digital audio data is input from the DATAL pin in time division mode.
13	MODE1	Interface switching pins. (See the timing charts.)
14	MODE2	
15	DGND	Digital system ground pin
16	REFL	Reference voltage low level pin. Normally connected to AGND through a capacitor.
17	AGND	Analog system ground pin
18	VrefL	Reference voltage low level input pin
19	NC	No connection
20	CH2OUT	Channel 2 output pin (right channel)

Operation

(1) Input of digital audio data

Digital audio data is a 16-bit serial signal in an MSB first two's complement format.

The 16-bit serial data is read into the IC from MSB on the rising edge of the BCLK signal.

The LC78816MB and 78816MC can handle various interface types.

See the timing charts for details.

DSP ICs for CD players: See timing chart (1)-① when interfacing with the LC7868KE or the 7869E.

(2) Converter operation (See Figure 1.)

The LC78816MB and 78816MC have independent D/A converter circuits for channel 1 and channel 2. These D/A converters use a dynamic level shift conversion technique that combines resistor string (R-string DAC), PWM (pulse width modulation), and level shifting D/A converters. After latching, the 16-bit input digital audio data (D_{15} to D_0) is sent to these separate D/A converters as follows:

Upper 9 bits (D_{15} to D_7): To the R-string DAC.

Middle 3 bits (D_6 to D_4): To the PWM DAC.

Lower 4 bits (D_3 to D_0): To the level shifting DAC.

① R-string DAC

The resistor string D/A converter consists of 512 (2^9) unit resistances (R) connected in series. The voltage applied at the terminals of this resistor string is divided into 512 equal divisions to form the 9-bit D/A converter outputs.

The upper 9 bits of the input data value are used to select (using a switching circuit) two adjacent potentials, V1 and V2, from the divided voltages. These are output to the PWM DAC. The relationship between these two voltages is given by the following formula:

$$V2 - V1 = (VH - VL)/512$$

② PWM DAC

The PWM DAC is a 3-bit D/A converter that divides the interval between the two voltages, V1 and V2 output by the R-string DAC, into 8 using PWM (pulse width modulation).

Either V1 or V2, depending on the value of the middle three bits of the data, is output to the CH1OUT (or CH2OUT) pin.

SYSCCLK is used for the PWM clock when timing chart (2)-② and (2)-③ are used, and BCLK is used for all other timing charts.

③ Level Shift DAC

Two variable resistors, VRH and VRL, are connected in series at the ends of the R-string DAC resistor string to implement a 4-bit D/A converter circuit. The variable resistors VRH and VRL operate as follows in response to the lower 4 bits of the data value.

- Independent of the data value, the sum of the resistances ($VRH + VRL$) remains constant.
- According to the data value, VRH and VRL vary in the range from 0 to $15R/128$ (where R is the value of the resistors in the R-string DAC) in steps of $R/128$.

As a result, the R-string DAC outputs V2 and V1 vary according to the lower 4 bits of the data in steps of $\Delta V/128$ over a range 0 to $15 \times \Delta V/128$ (where $\Delta V = (VH - VL)/512$).

D/A Conversion Technique Used in the LC78816MB and 78816MC

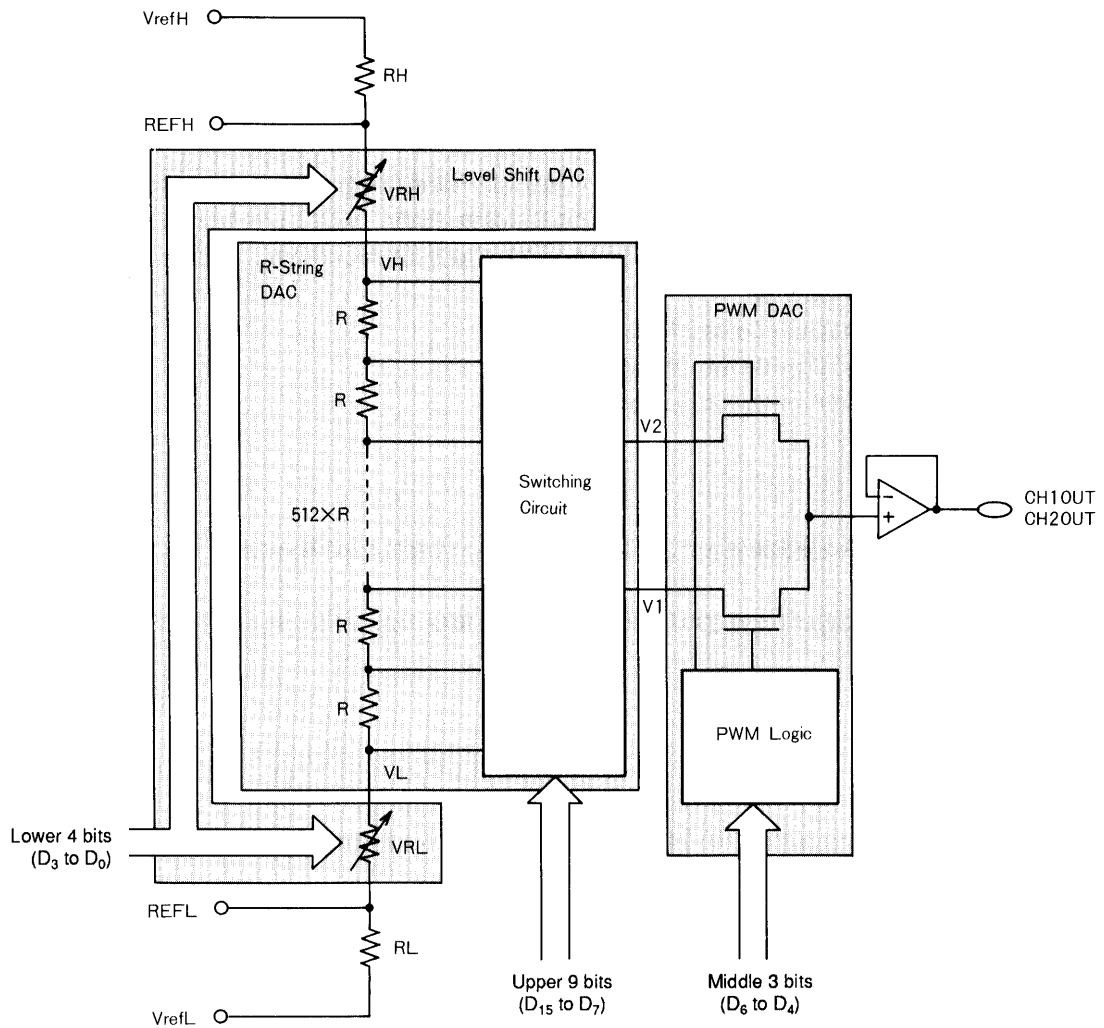


Figure 1 D/A Conversion Technique Used in the LC78816MB and 78816MC

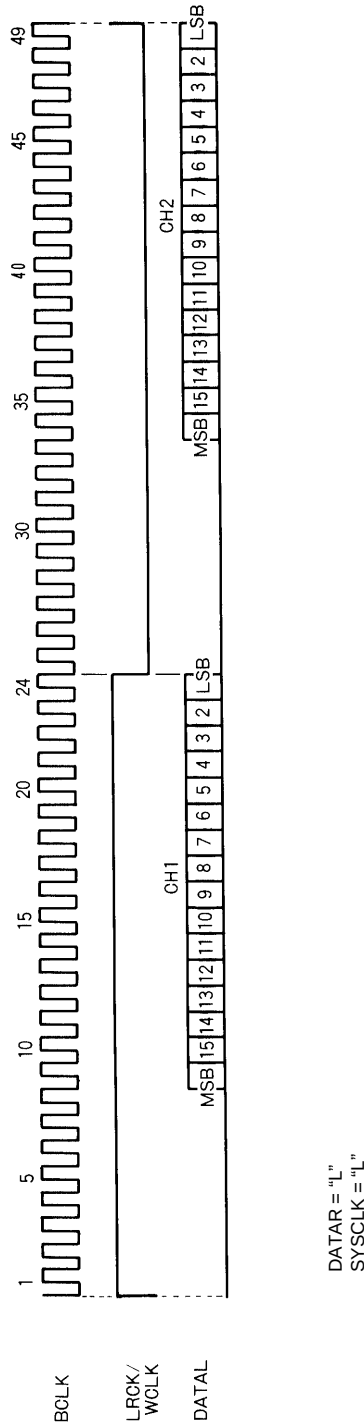
V_{ref} pins (See Figure 1.)

The V_{ref} pins that provide the reference voltages for the resistor string are normally set at $V_{refH} = 5\text{ V}$ and $V_{refL} = 0\text{ V}$.

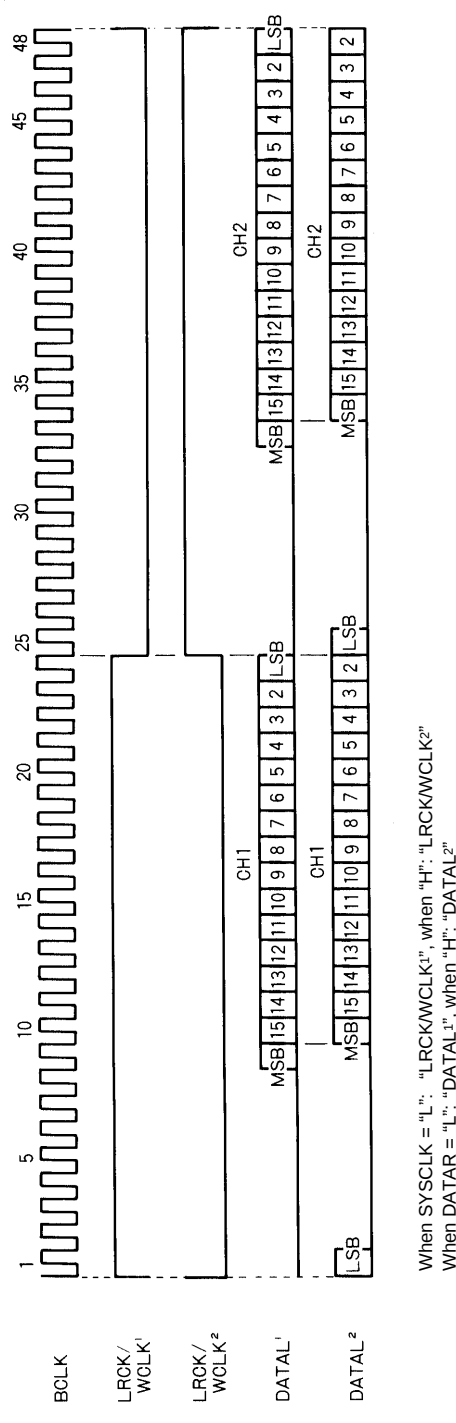
Also, a capacitor of about $47\text{ }\mu\text{F}$ should be connected between REFH and AGND, and another between REFL and AGND. As a result of the built-in resistors RH and RL, the maximum output amplitude of the LC78816MB and 78816MC is in a range of 0.5 V (min) to 3.8 V (max) (3.3 Vp-p) for 0 dB playback.

Timing Charts

(1) For time division input of the CH1 and CH2 data (FSEL = high)
(1)-① MODE1 = “L”, MODE2 = “L”, FSEL = “H”

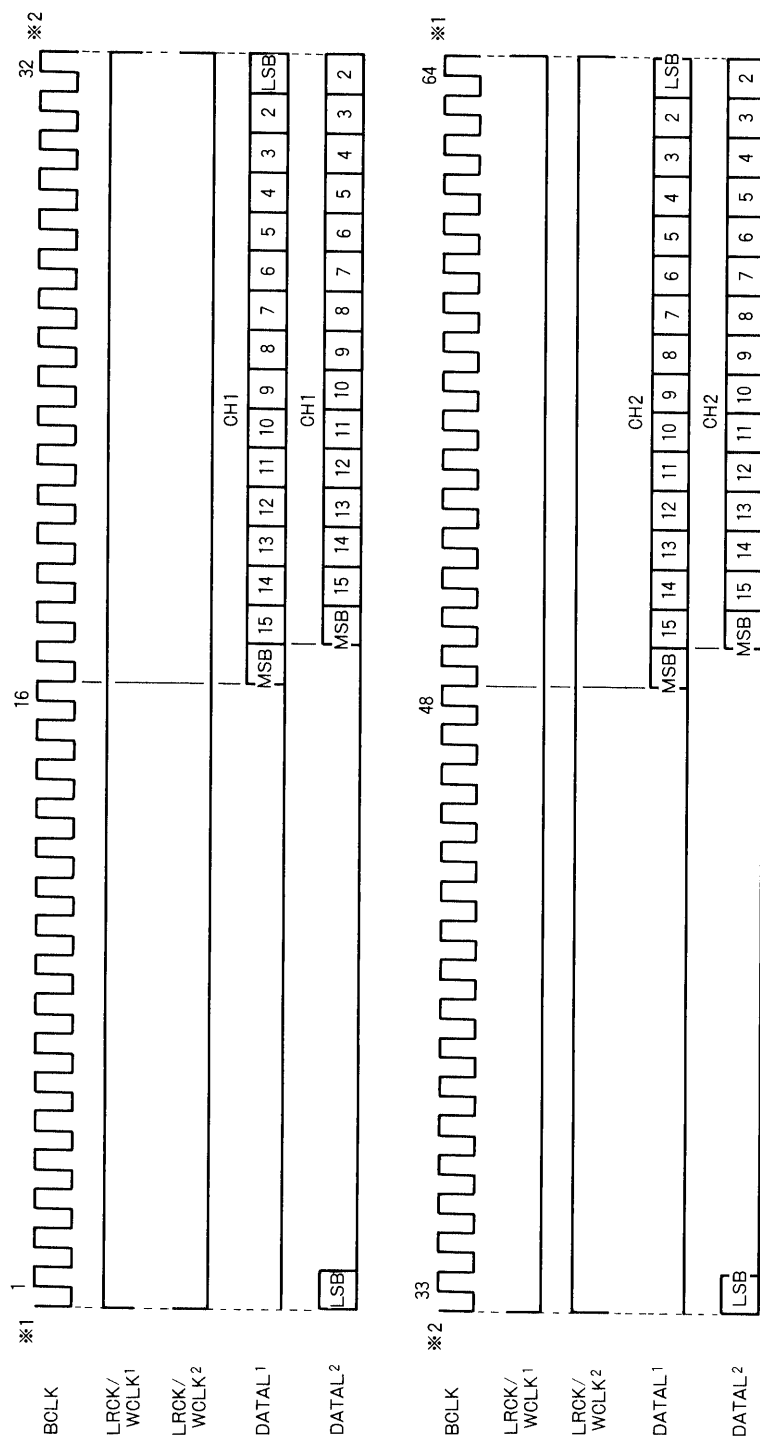


(1)-② MODE1 = “L”, MODE2 = “H”, FSEL = “H”



Timing Charts

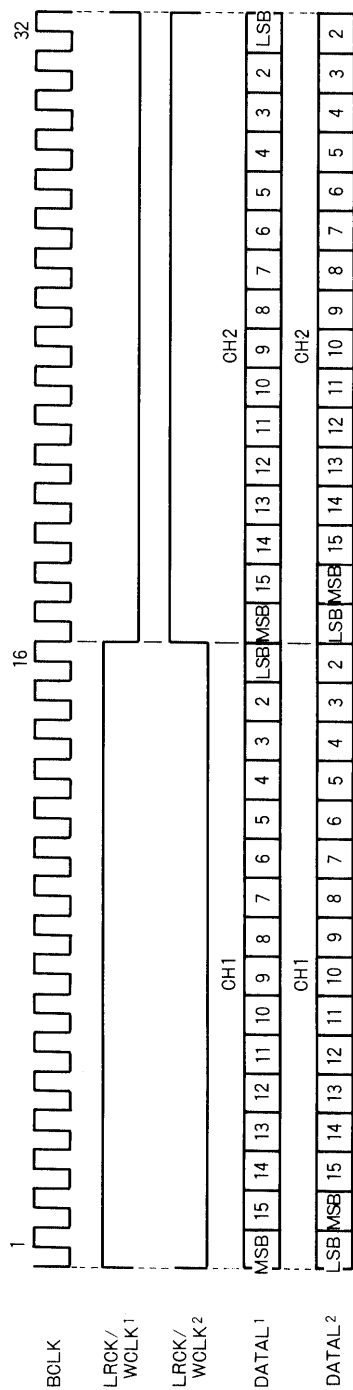
(1)-③ MODE1 = "H", MODE2 = "L", FSEL = "H"



When SYSCLK = "L": "LCLK/WCLK1", when "H": "LCLK/WCLK2"
 When DATAR = "L": "DATAL1", when "H": "DATAL2"

Timing Charts

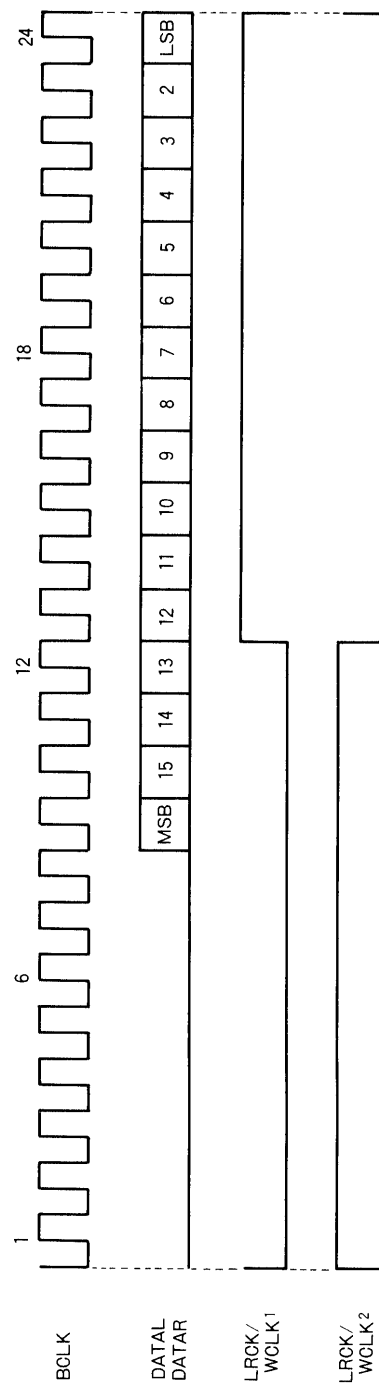
(1)-④ MODE1 = "H", MODE2 = "H", FSEL = "H"



When SYSCLK = "L": "LRCK/WCLK1", when "H": "LRCK/WCLK2"
 When DATAR = "L": "DATAL1", when "H": "DATAL2"

(2) For simultaneous input of CH1 and CH2 data (FSEL = low)

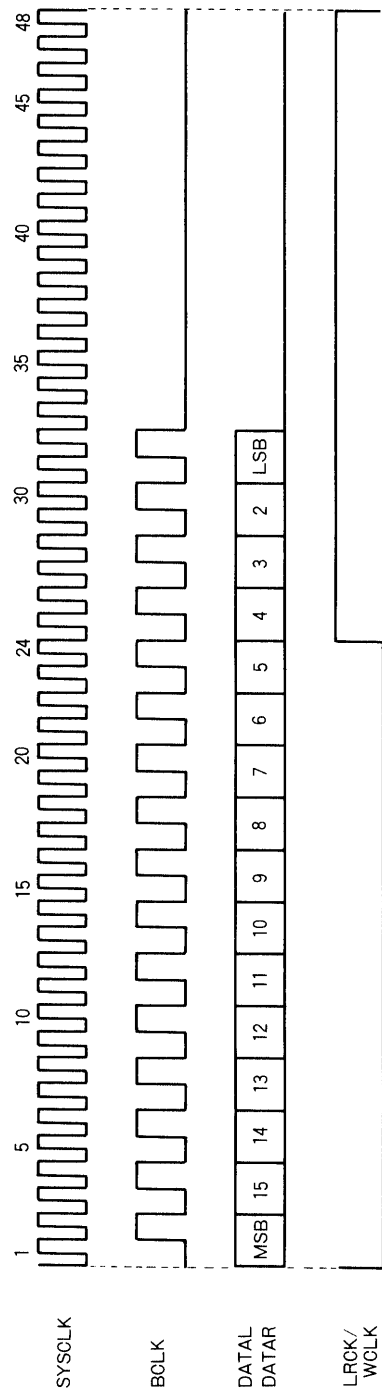
(2)-① MODE1 = "L", MODE2 = "L", FSEL = "L"



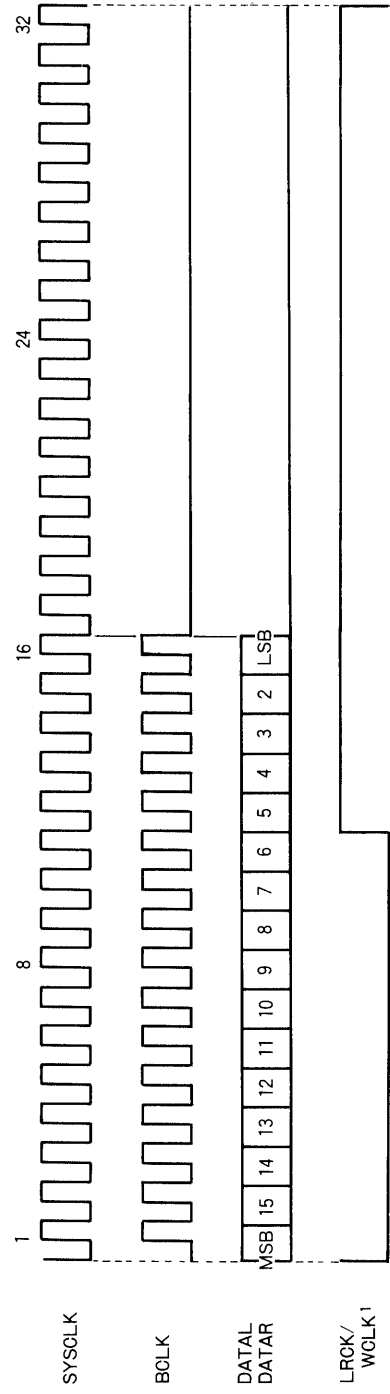
When SYSCLK = "L": "LRCK/WCLK1", when "H": "LRCK/WCLK2"

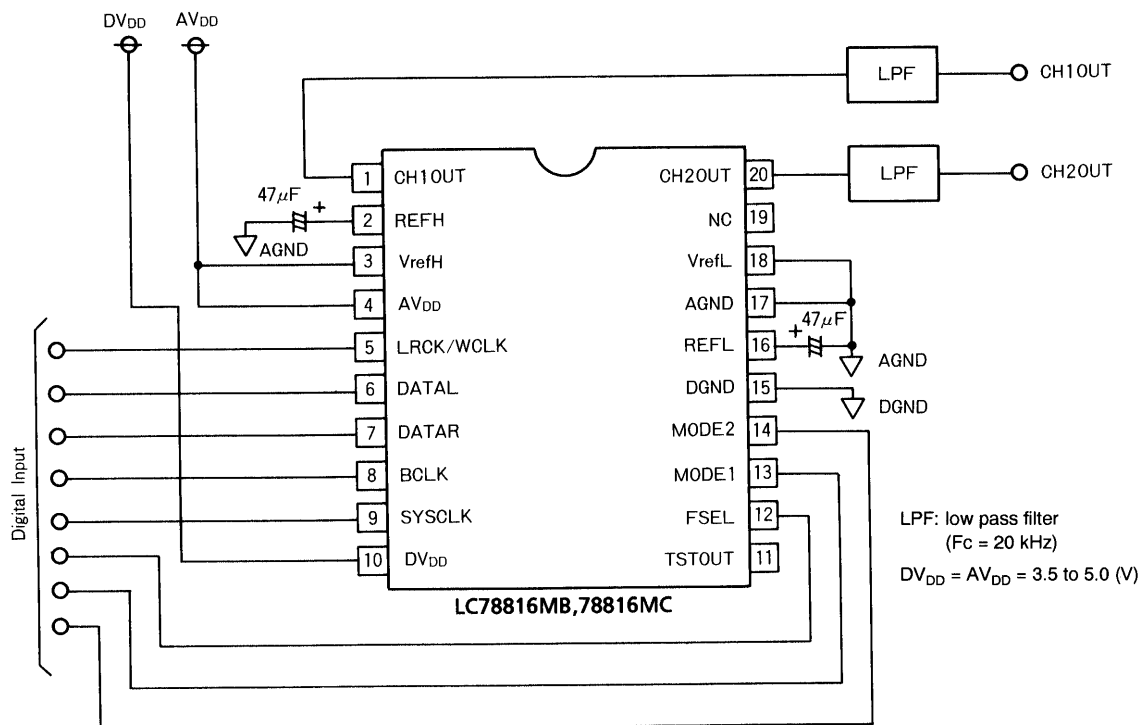
Timing Charts

(2)-② MODE1 = "L", MODE2 = "H", FSEL = "L"



(2)-③ MODE1 = "H", MODE2 = "H", FSEL = "L"





- Notes: 1. V_{DD} and DGND must be connected to the digital system power supply, and AV_{DD} and AGND to the analog system power supply.
2. Use a low impedance high stability power supply (a unit equivalent to a commercial three terminal regulator) for V_{DD} and VrefH.
3. Since latching is possible if there is a discrepancy between the power supply rise times for pin 4 (AV_{DD}) and pin 10 (V_{DD}), design the system so that there is no time lag between the pin 4 and pin 10 power application times.

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