Ordering number : ENA1687

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

CMOS IC

LC75879PT — 1/4, 1/3-Duty General-Purpose LCD Display Driver

Overview

The LC75879PT is the 1/4 duty and 1/3 duty general-purpose microprocessor-controlled LCD driver that can be used in applications such as frequency display in products with electronic tuning.In addition to being able to drive up to 272 segments directly, the LC75879PT can also control up to 8 general-purpose output ports. Because it has the PWM output of a maximum of 3 ch, the brightness control of the LED backlight of RGB can be done. Incorporation of an oscillation circuit helps to reduce the number of external resistors and capacitors required.

Features

- Support for 1/4-duty 1/3-bias or 1/3-duty 1/3-bias drive techniques under serial data control.
  When 1/4-duty: Capable of driving up to 272 segments
  When 1/3-duty: Capable of driving up to 207 segments
- Serial data input supports CCB format communication with the system controller (Support 3.3V and 5V operation).
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output portfunction.
  (Support for up to 8 general-purpose output ports)
- Support for the PWM output function of a maximum of 3ch (It can output from the general-purpose output port).
- Support for clock output function of 1ch (It can output from the general-purpose output port).
- Serial data control of the frame frequency of the common and segment output waveforms.
- Serial data control of switching between the internal oscillator operating mode and external clock operating mode.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- Built-in display contrast adjustment circuit.
- The $\overline{\text{INH}}$ pin allows the display to be forced to the off state.
- Incorporation of an oscillator circuit (Incorporation of resistor and capacitor for an oscillation).

- CCB is a registered trademark of SANYO Electric Co., Ltd.
- CCB is SANYO Semiconductor's original bus format. All bus addresses are managed by SANYO Semiconductor for this format.

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	-0.3 to +6.8	V
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	-0.3 to +6.8	V
	$V_{IN}2$	OSCI, $V_{DD}1$, $V_{DD}2$	-0.3 to V_{DD}+0.3	
Output voltage	V_{OUT}	S1 to S69, COM1 to COM4, P1 to P8	-0.3 to V_{DD}+0.3	V
Output current	$I_{OUT}1$	S1 to S68	300	μA
	$I_{OUT}2$	COM1 to COM4, S69	3	mA
	$I_{OUT}3$	P1 to P8	5	
Allowable power dissipation	Pd max	Ta=85°C	200	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta = -40 to +85°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		6.3	V
Input voltage *1	$V_{DD}1$	$V_{DD}1$		2/3$V_{DD}0$	$V_{DD}0$	V
	$V_{DD}2$	$V_{DD}2$		1/3$V_{DD}0$	$V_{DD}0$	
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.4V_{DD}		6.3	V
	$V_{IH}2$	OSCI: External clock operating mode	0.4V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$	0		0.2V_{DD}	V
	$V_{IL}2$	OSCI: External clock operating mode	0		0.2V_{DD}	
External clock operating frequency	f_{CK}	OSCI: External clock operating mode [Figure4]	10	300	600	kHz
External clock duty cycle	D_{CK}	OSCI: External clock operating mode [Figure4]	30	50	70	%
Data setup time	tds	CL, DI [Figure2], [Figure3]	160			ns
Data hold time	tdh	CL, DI [Figure2], [Figure3]	160			ns
CE wait time	tcp	CE, CL [Figure2], [Figure3]	160			ns
CE setup time	tcs	CE, CL [Figure2], [Figure3]	160			ns
CE hold time	tch	CE, CL [Figure2], [Figure3]	160			ns
High level clock pulse width	tφH	CL [Figure2], [Figure3]	160			ns
Low level clock pulse width	tφL	CL [Figure2], [Figure3]	160			ns
Rise time	tr	CE, CL, DI [Figure2], [Figure3]		160		ns
Fall time	tf	CE, CL, DI [Figure2], [Figure3]		160		ns
$\overline{INH}$ switching time	tc	$\overline{INH}$, CE [Figure5], [Figure6] [Figure7], [Figure8]	10			μs

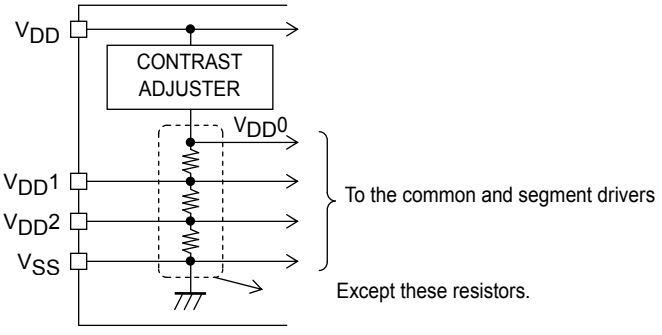
Note : *1. $V_{DD}0$=0.70V_{DD} to V_{DD}

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$			$0.03V_{DD}$		V
Input high level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I=6.3V			5.0	µA
	$I_{IH}2$	OSCI	$V_I=V_{DD}$: External clock operating mode			5.0	
Input low level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I=0V	-5.0			µA
	$I_{IL}2$	OSCI	V_I=0V: External clock operating mode	-5.0			
Output high level voltage *1	$V_{OH}1$	S1 to S69	I_O=-20µA	$V_{DD}0$-0.9			V
	$V_{OH}2$	COM1 to COM4	I_O=-100µA	$V_{DD}0$-0.9			
	$V_{OH}3$	P1 to P8	I_O=-1mA	V_{DD}-0.9			
Output low level voltage	$V_{OL}1$	S1 to S69	I_O=20µA			0.9	V
	$V_{OL}2$	COM1 to COM4	I_O=100µA			0.9	
	$V_{OL}3$	P1 to P8	I_O=1mA			0.9	
Output middle level voltage *1 *2	$V_{MID}1$	S1 to S69	1/3 bias I_O=±20µA	$2/3V_{DD}0$ -0.9		$2/3V_{DD}0$ +0.9	V
	$V_{MID}2$	S1 to S69	1/3 bias I_O=±20µA	$1/3V_{DD}0$ -0.9		$1/3V_{DD}0$ +0.9	
	$V_{MID}3$	COM1 to COM4	1/3 bias I_O=±100µA	$2/3V_{DD}0$ -0.9		$2/3V_{DD}0$ +0.9	
	$V_{MID}4$	COM1 to COM4	1/3 bias I_O=±100µA	$1/3V_{DD}0$ -0.9		$1/3V_{DD}0$ +0.9	
Oscillator frequency	fosc	Internal oscillator circuit	Internal oscillator operating mode	240	300	360	kHz
Current drain	$I_{DD}1$	V_{DD}	Power-saving mode			100	µA
	$I_{DD}2$	V_{DD}	V_{DD}=6.3V Output open Internal oscillator operating mode		1000	2000	
	$I_{DD}3$	V_{DD}	V_{DD}=6.3V Output open External clock operating mode f_{CK}=300kHz $V_{IH}2=0.5V_{DD}$ $V_{IL}2=0.1V_{DD}$		1000	2000	

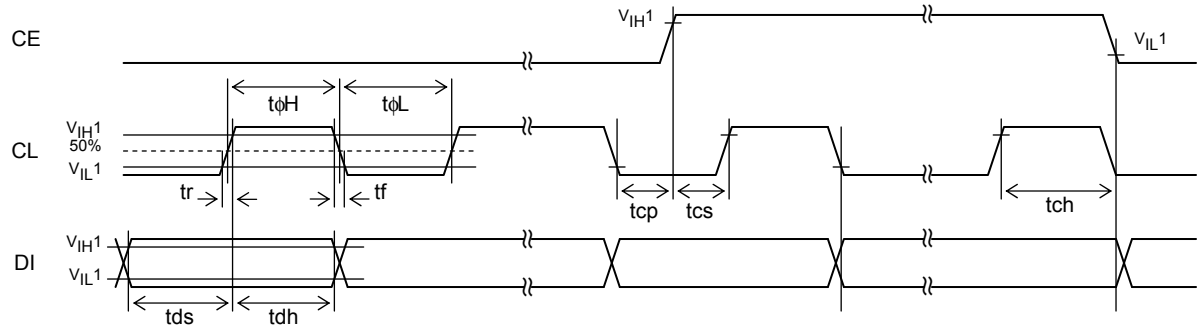
Note: *1. $V_{DD}0=0.70V_{DD}$ to V_{DD}

Note: *2. Excluding the bias voltage generation divider resistors built in the $V_{DD}1$ and $V_{DD}2$. (See Figure 1.)



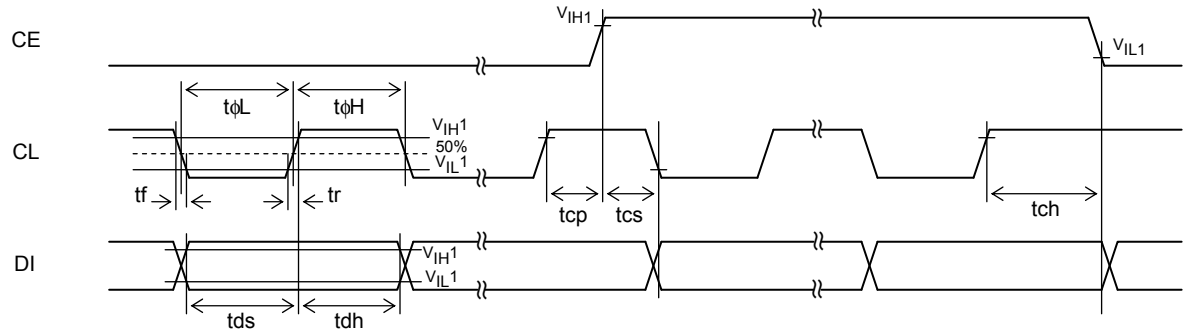
[Figure 1]

1. When CL is stopped at the low level



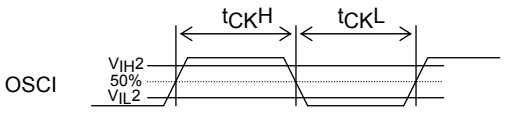
[Figure 2]

2. When CL is stopped at the high level



[Figure 3]

3. OSCI pin clock timing in external clock operating mode



$$f_{CK} = \frac{1}{t_{CK}H + t_{CK}L} \text{ [kHz]}$$

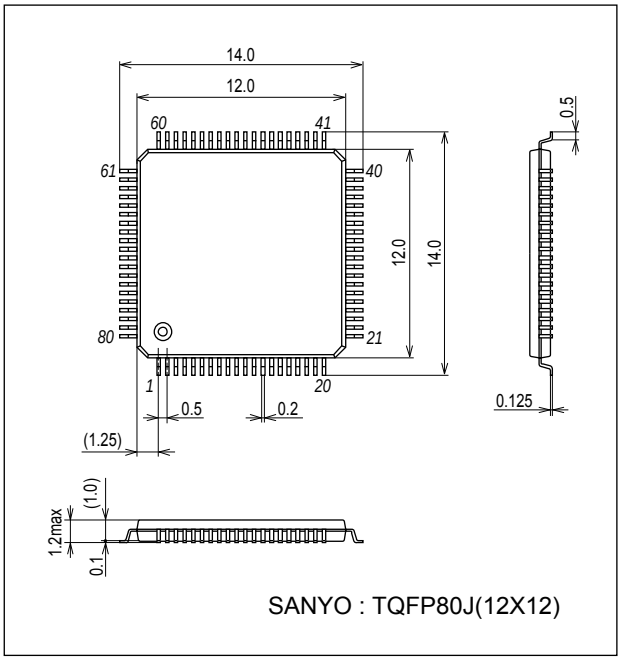
$$D_{CK} = \frac{t_{CK}H}{t_{CK}H + t_{CK}L} \times 100[\%]$$

[Figure 4]

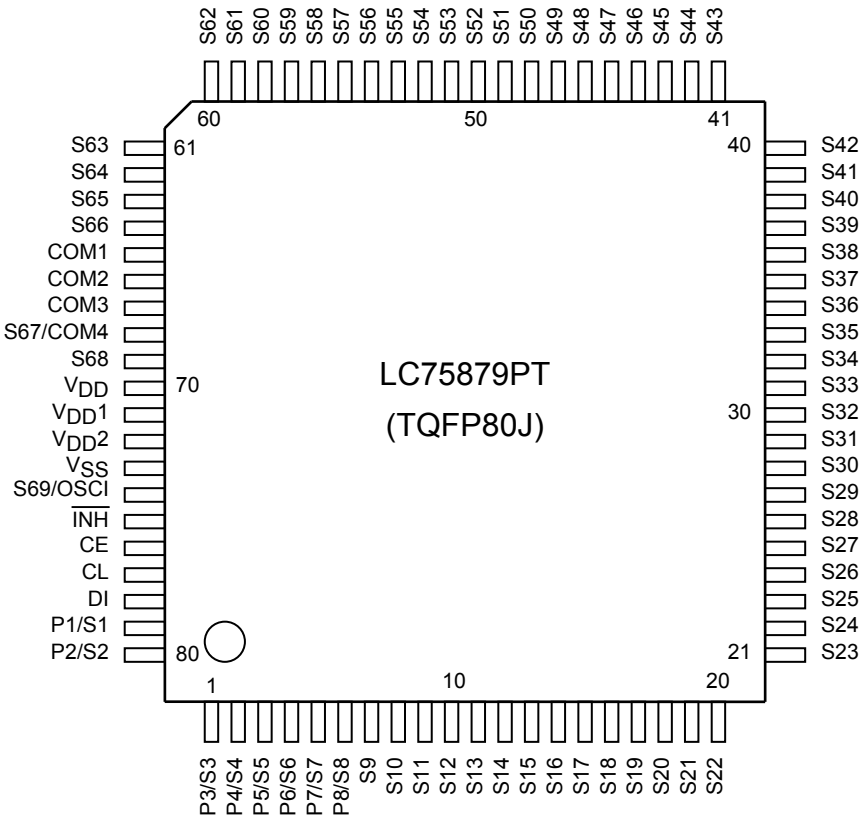
Package Dimensions

unit : mm (typ)

3290

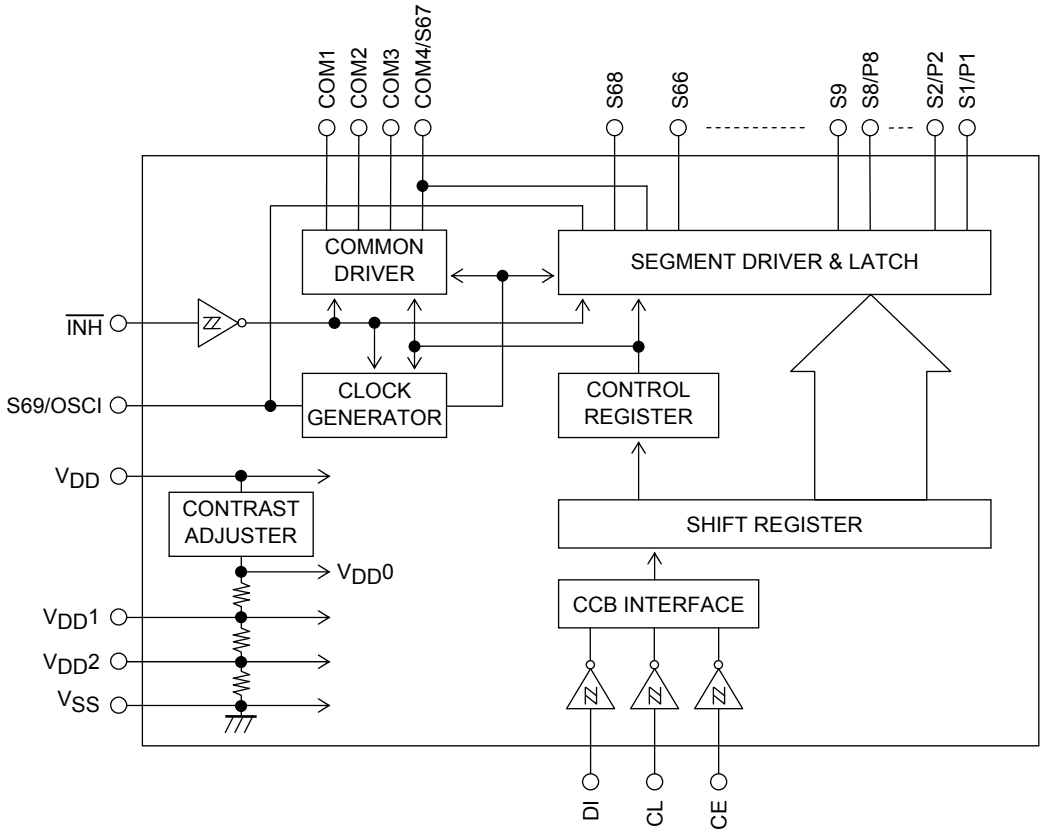


Pin Assignment



Top view

Block Diagram



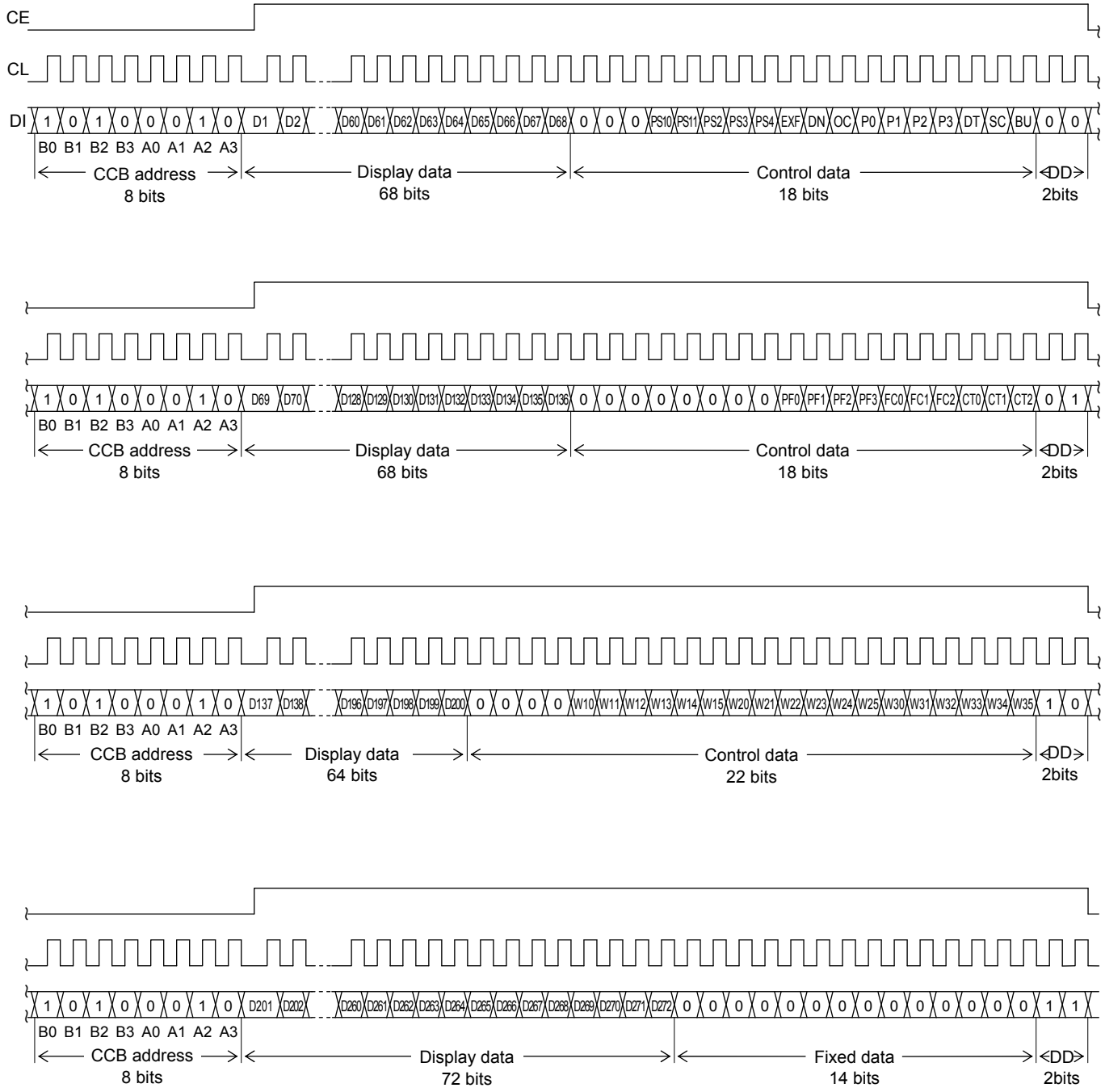
Pin Functions

Pin	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S8/P8 S9 to S66 S68	79, 80, 1 to 6 7 to 64 69	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S8/P8 pins can be used as general-purpose output ports under serial data control.	-	O	OPEN
COM1 to COM3 COM4/S67	65 to 67 68	Common driver outputs The frame frequency is fo[Hz]. The COM4/S67 pin can be used as a segment output in 1/3 duty.	-	O	OPEN
S69/OSCI	74	Segment output. This pin can also be used as the external clock input pin when the external clock operating mode is selected by control data.	-	I/O	OPEN
CE CL DI	76 77 78	Serial data transfer inputs. Must be connected to the controller. CE: Chip enable CL: Synchronization clock DI: Transfer data	H ↑ -	I I I	GND
$\overline{INH}$	75	Display off control input •$\overline{INH}$=low(V_{SS})….Display forced off S1/P1 to S8/P8=low (V_{SS}) (These pins are forcibly set to the general-purpose output port function and held at the V_{SS} level.) S9 to S66,S68=low(V_{SS}) COM1 to COM3=low(V_{SS}) COM4/S67=low(V_{SS}) S69/OSCI=low(V_{SS}) (This pin is forcibly set to the segment output port function and held at the V_{SS} level.) Stops the internal oscillator. Inhibits external clock input. Display contrast adjustment circuit stopped. •$\overline{INH}$=high(V_{DD})…Display on Enables the internal oscillator circuit. (Internal oscillator operating mode) Enables external clock input. (External clock operating mode) Display contrast adjustment circuit operation is enabled. However, serial data transfer is possible when the display is forced off.	L	I	GND
$V_{DD}1$	71	Used to apply the LCD drive 2/3 bias voltage externally.	-	I	OPEN
$V_{DD}2$	72	Used to apply the LCD drive 1/3 bias voltage externally.	-	I	OPEN
V_{DD}	70	Power supply pin. A power voltage of 4.5 to 6.3V must be applied to this pin.	-	-	-
V_{SS}	73	Ground pin. Must be connected to ground.	-	-	-

Serial Data Input

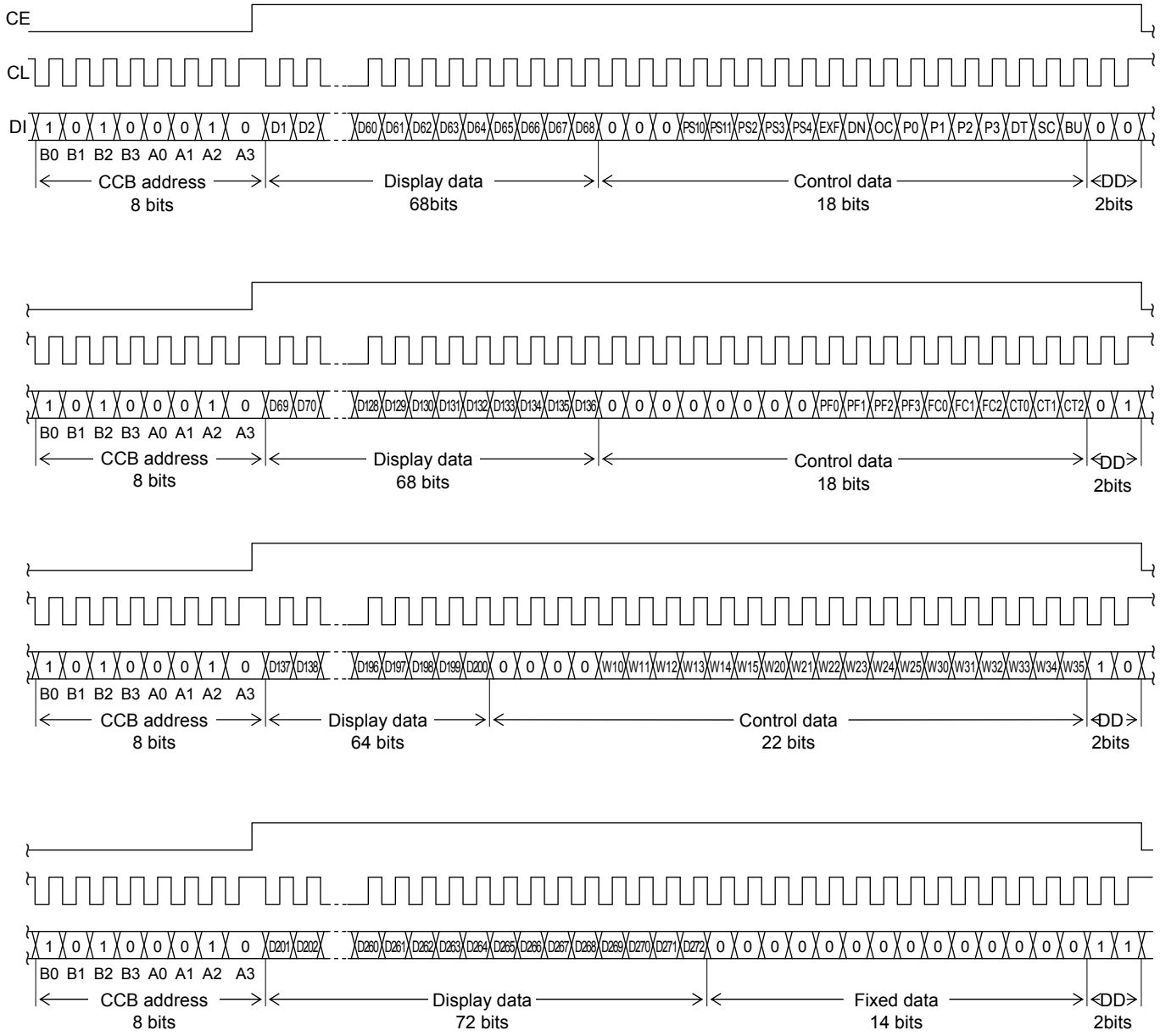
1. 1/4 duty

(1) When CL is stopped at the low level



Note: DD is the direction data.

(2) When CL is stopped at the high level

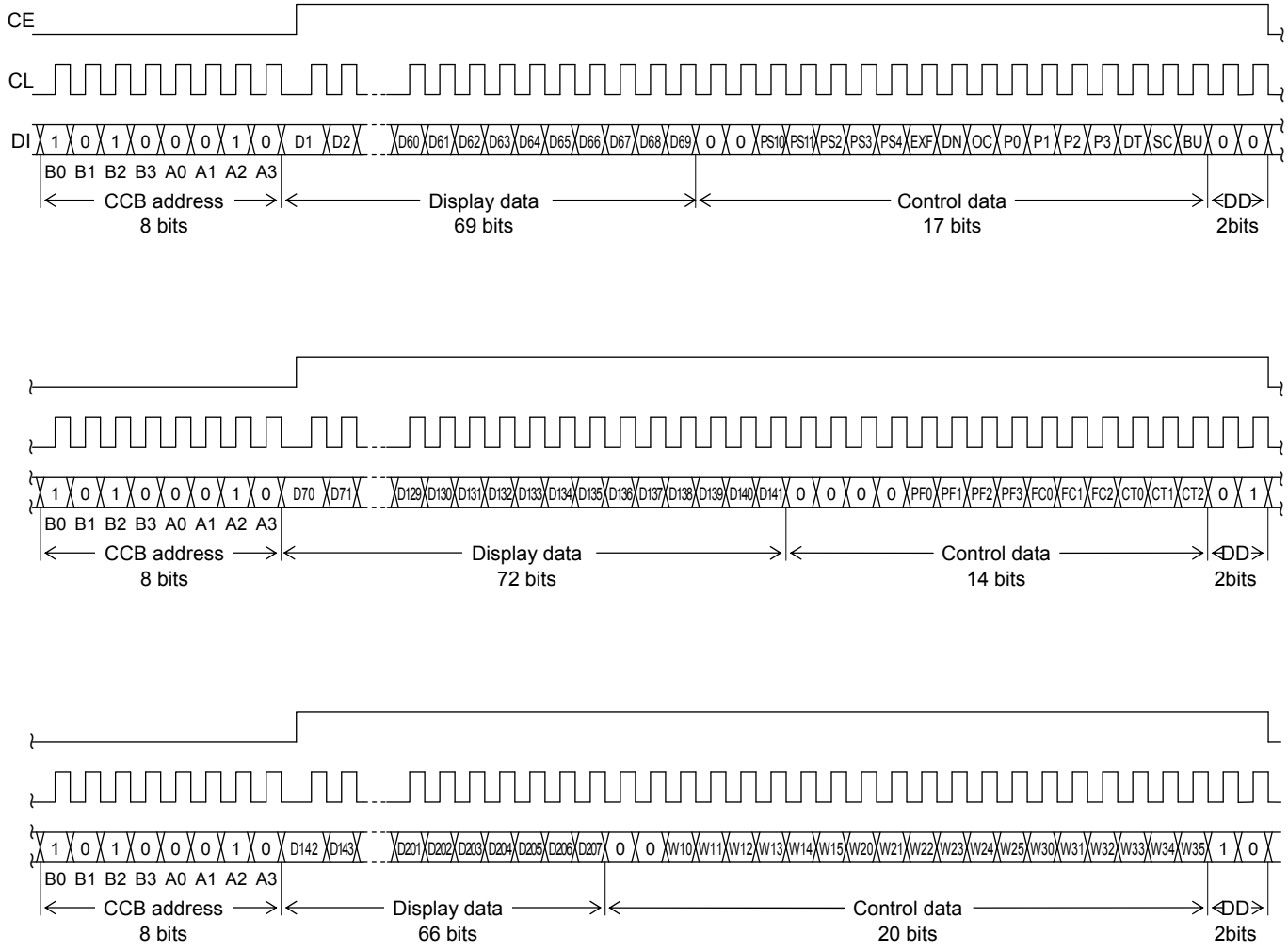


Note: DD is the direction data

- CCB address …….. “45H”
- D1 to D272 …… Display data
- PS10, PS11, PS2 to PS4 …. .. General-purpose output port (P1 to P4) function setting control data
- EXF …… External clock operating frequency setting control data
- DN ……. S68 pin and S69/OSCI pin state setting control data
- OC ……. Internal oscillator operating mode/external clock operating mode switching control data
- P0 to P3 …….. Segment output port/general-purpose output port switching control data
- DT …….. 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- SC ……..… Segment on/off control data
- BU ……..… Normal mode/power-saving mode control data
- PF0 to PF3 …… PWM output waveform frame frequency setting control data
- FC0 to FC2 …… Common/segment output waveform frame frequency setting control data
- CT0 to CT2 …… Display contrast setting control data
- W10 to W15, W20 to W25, ... PWM data of the PWM output
  W30 to W35

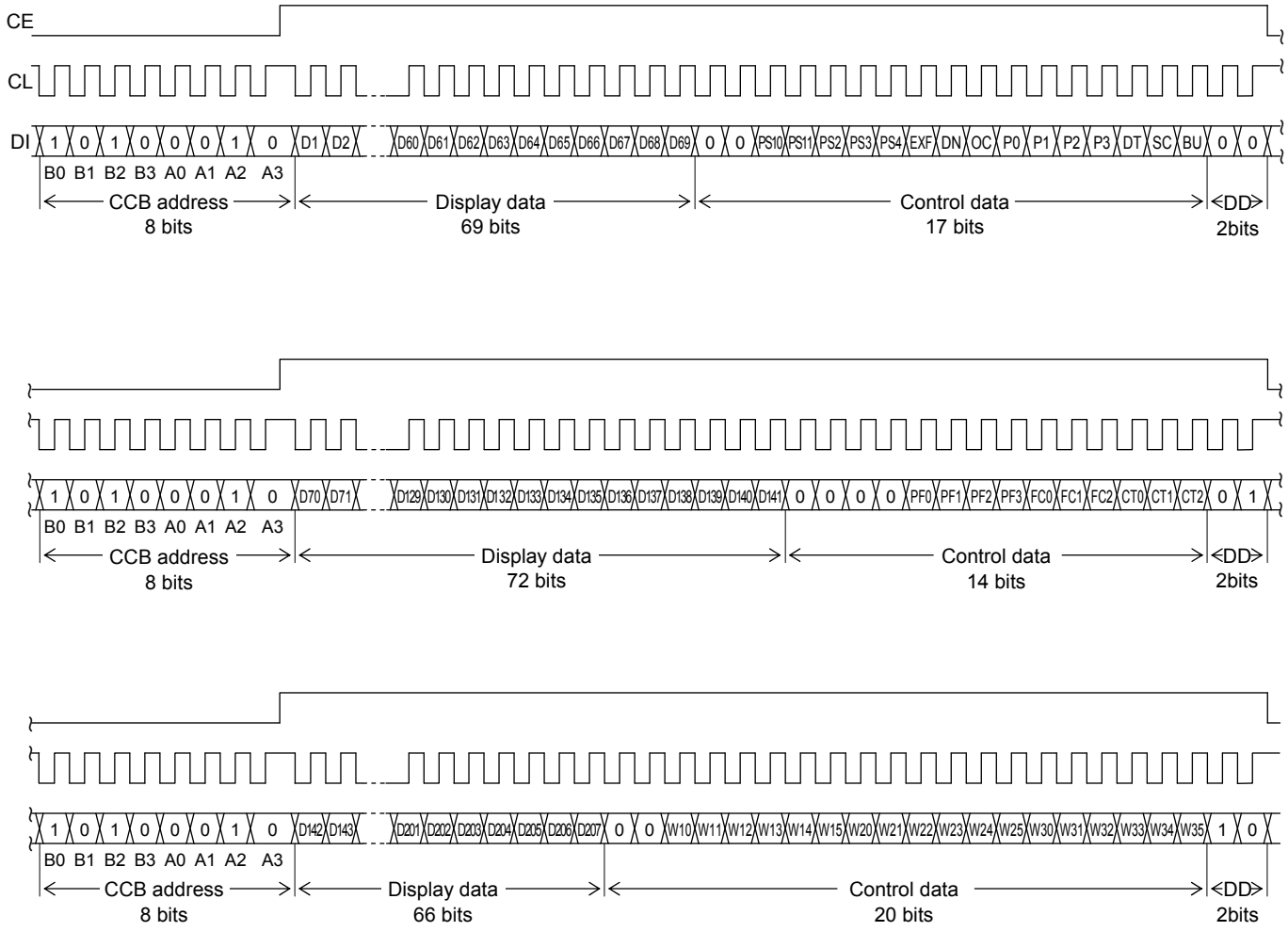
2. 1/3 duty

(1) When CL is stopped at the low level



Note: DD is the direction data.

(2) When CL is stopped at the low level

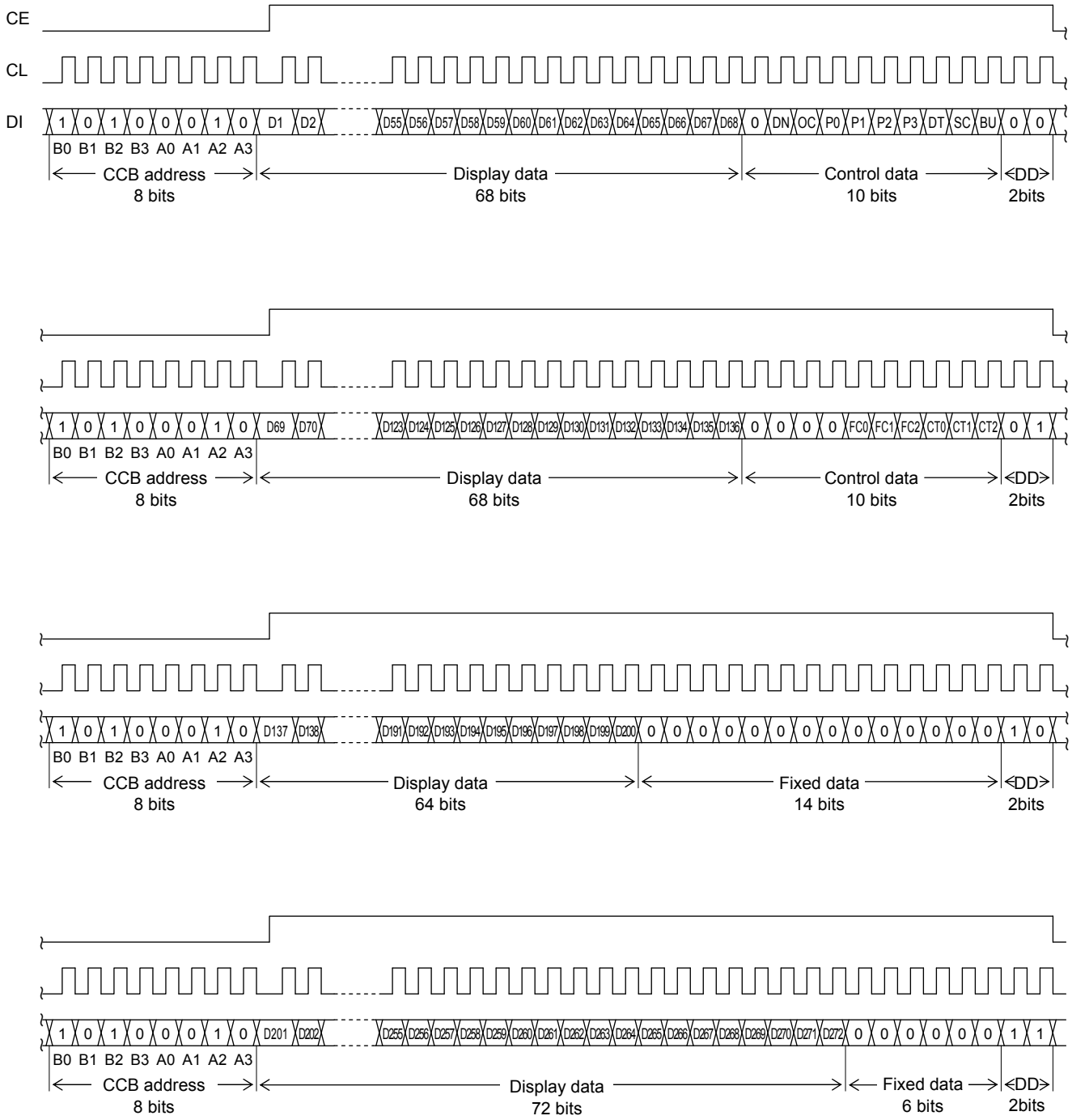


Note: DD is the direction data.

- CCB address …….. “45H”
- D1 to D207 ……..... Display data
- PS10, PS11, PS2 to PS4 …..... General-purpose output port (P1 to P4) function setting control data
- EXF ……... External clock operating frequency setting control data
- DN ……. S68 pin and S69/OSCI pin state setting control data
- OC ……. Internal oscillator operating mode/external clock operating mode switching control data
- P0 to P3 ……. Segment output port/general-purpose output port switching control data
- DT ……. 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- SC …….. Segment on/off control data
- BU ……. Normal mode/power-saving mode control data
- PF0 to PF3 ……. PWM output waveform frame frequency setting control data
- FC0 to FC2 …… Common/segment output waveform frame frequency setting control data
- CT0 to CT2 …… Display contrast setting control data
- W10 to W15, W20 to W25, ... PWM data of the PWM output
  W30 to W35

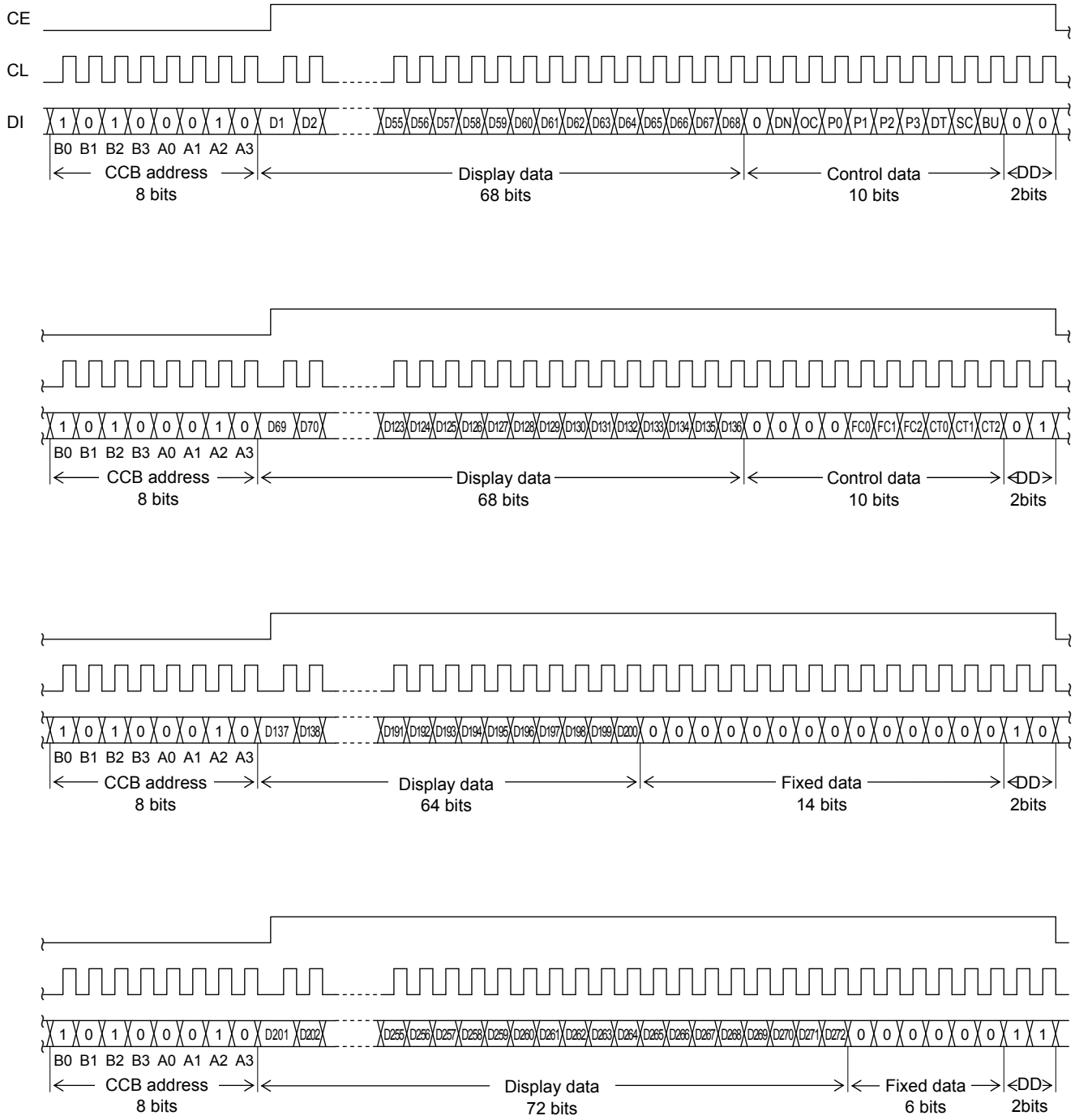
3. 1/4 duty (Simple mode transfer)

(1) When CL is stopped at the low level



Note: DD is the direction data.

(2) When CL is stopped at the high level

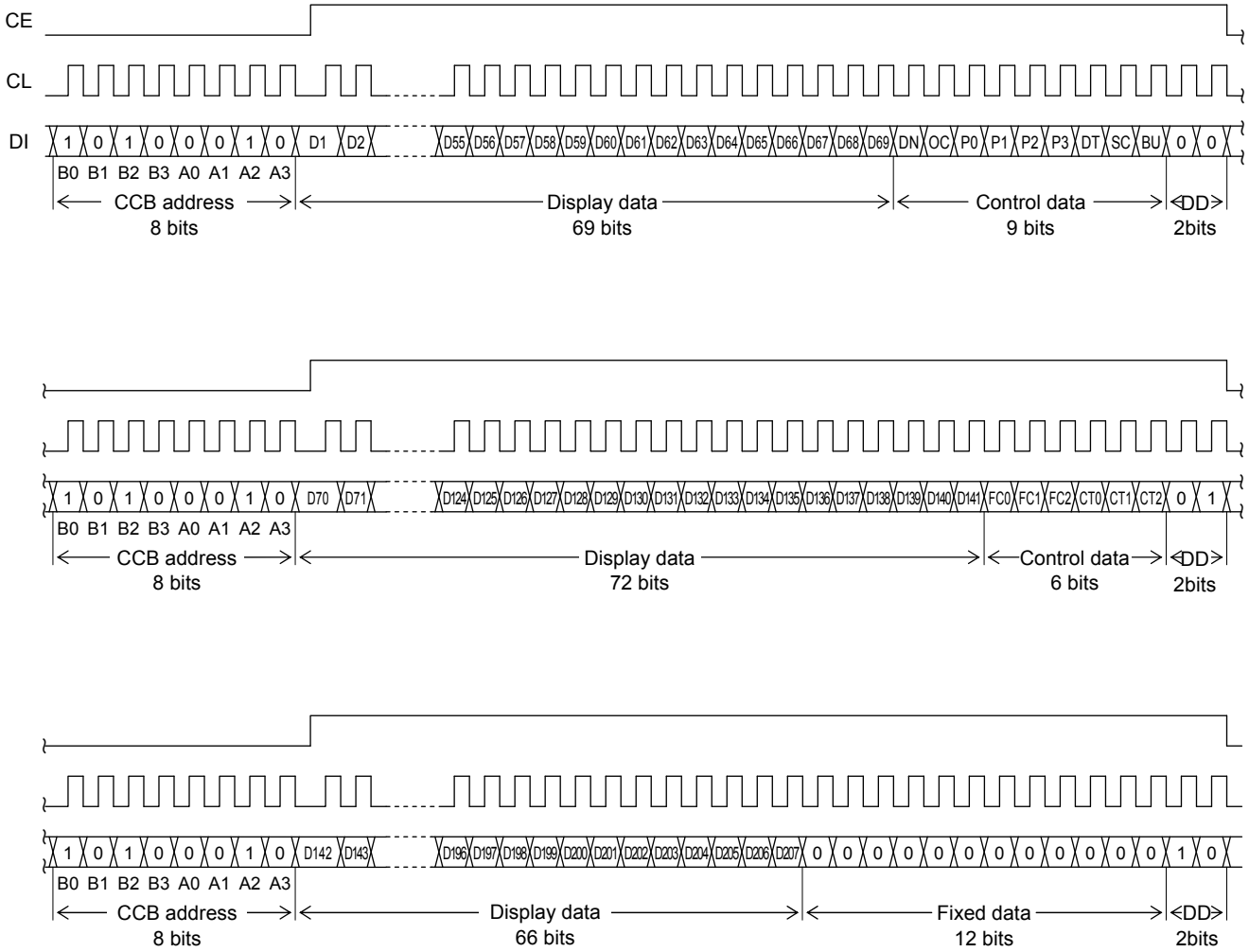


Note: DD is the direction data.

- CCB address ..... "45H"
- D1 to D272 ..... Display data
- DN …….. S68 pin and S69/OSCI pin state setting control data
- OC …….. Internal oscillator operating mode/external clock operating mode switching control data
- P0 to P3 …….. Segment output port/general-purpose output port switching control data
- DT …….. 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- SC …….... Segment on/off control data
- BU …….. Normal mode/power-saving mode control data
- FC0 to FC2 …..... Common/segment output waveform frame frequency setting control data
- CT0 to CT2 ……. Display contrast setting control data

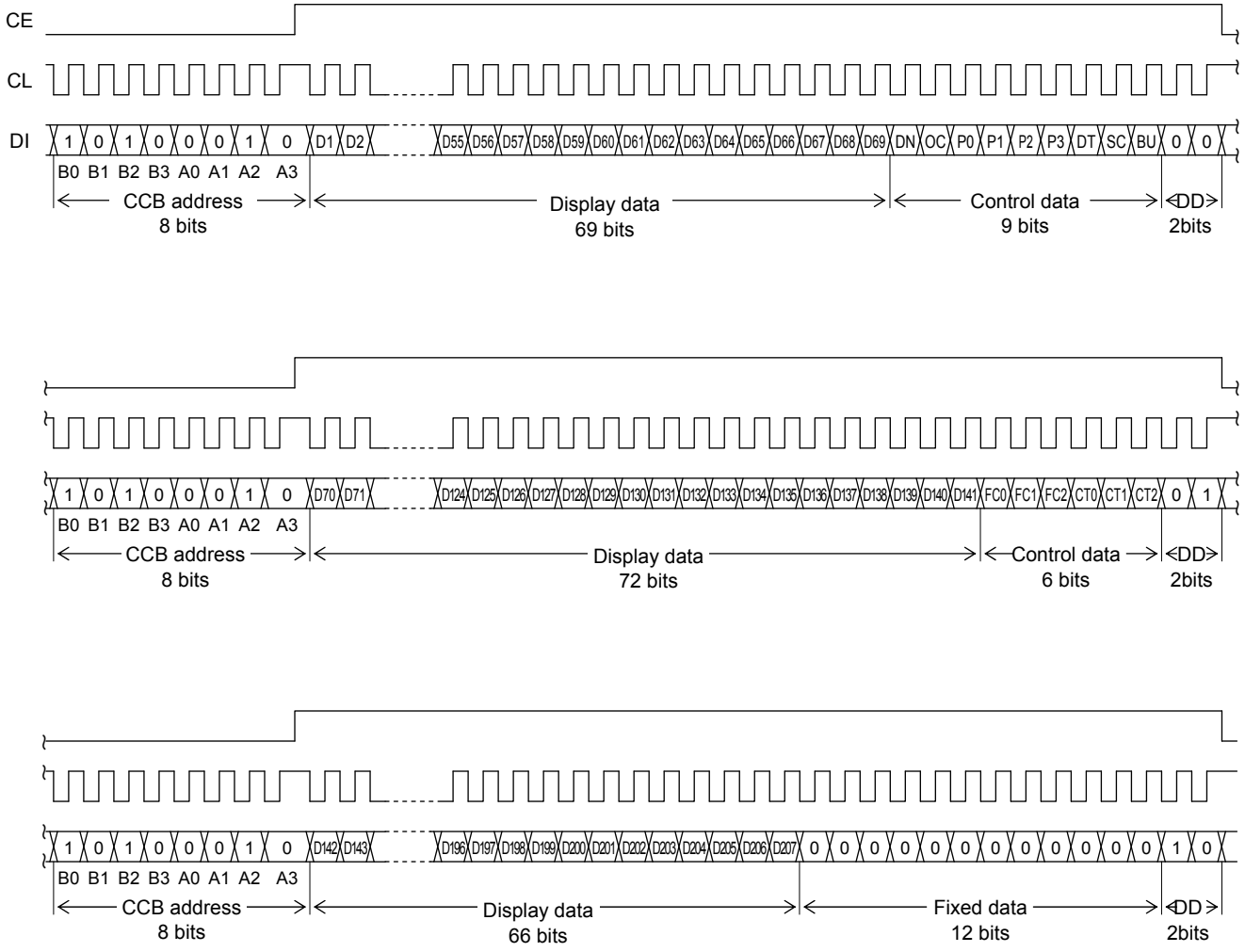
4. 1/3 duty (Simple mode transfer)

(1) When CL is stopped at the low level



Note: DD is the direction data.

(2) When CL is stopped at the high level



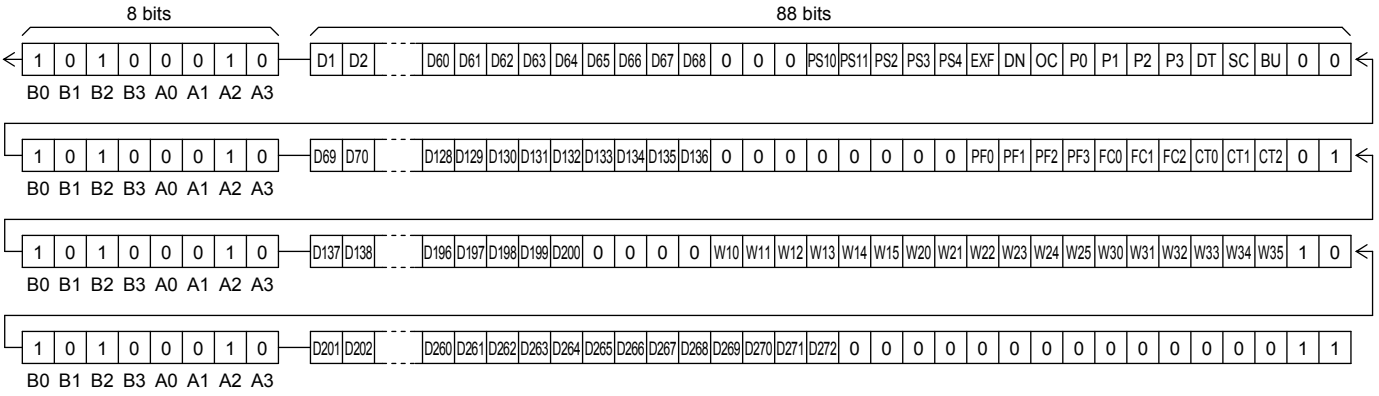
Note: DD is the direction data

- CCB address …… “45H”
- D1 to D207 …….. Display data
- DN …… S68 pin and S69/OSCI pin state setting control data
- OC …… Internal oscillator operating mode/external clock operating mode switching control data
- P0 to P3 …… Segment output port/general-purpose output port switching control data
- DT …… 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
- SC …… Segment on/off control data
- BU …… Normal mode/power-saving mode control data
- FC0 to FC2 …….. Common/segment output waveform frame frequency setting control data
- CT0 to CT2 …….. Display contrast setting control data

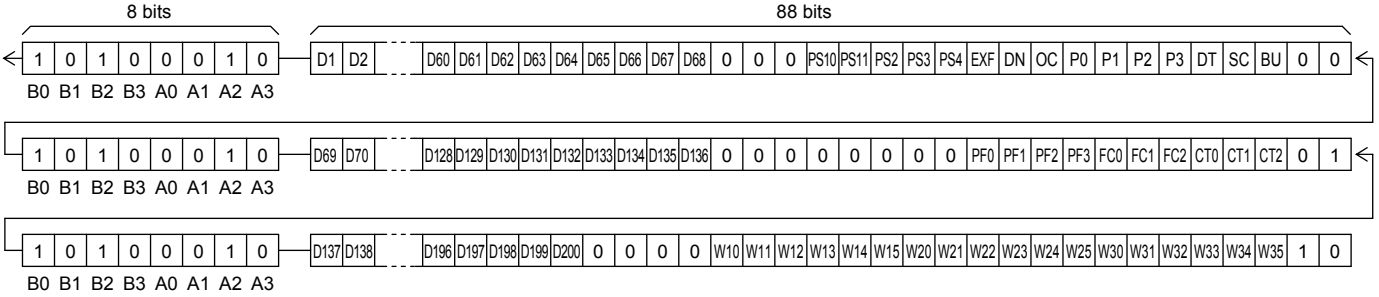
Serial Data Transfer Example

(1) 1/4 duty

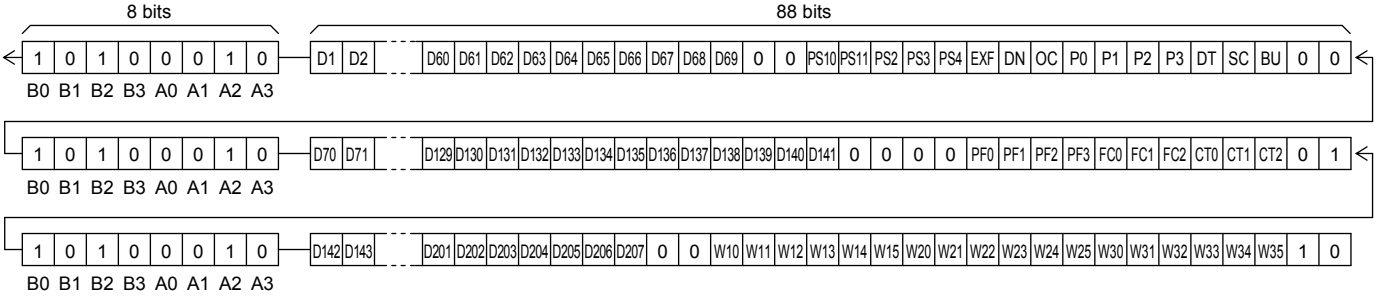
- When 201 or more segments are used
  All 352 bits of serial data must be sent.



- When fewer than 201 segments are used
  The 264 bits of serial data must be sent.
  However, the serial data shown below (the D1 to D200 display data and the control data) must always be sent.

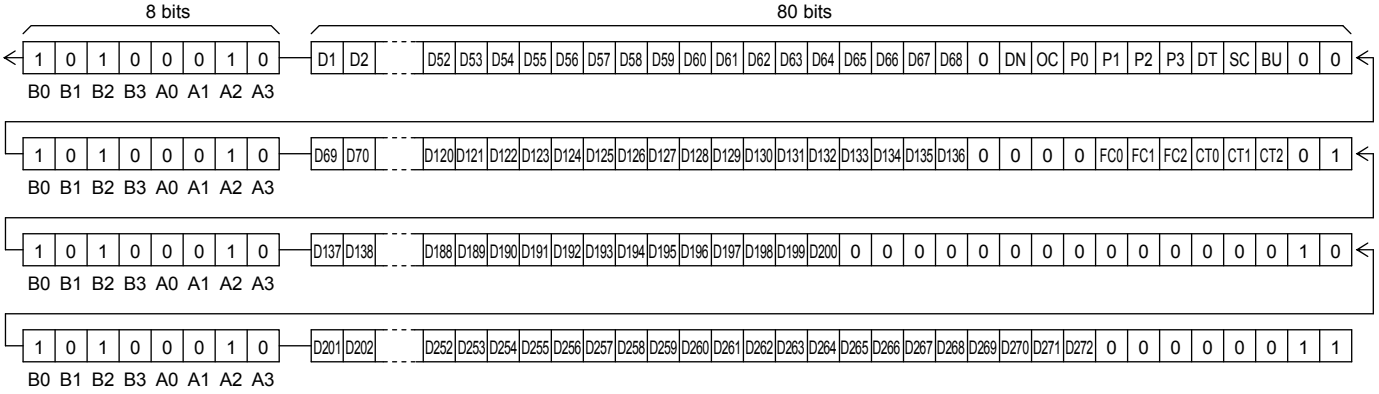


2. 1/3 duty
   All 264 bits of serial data must be sent.

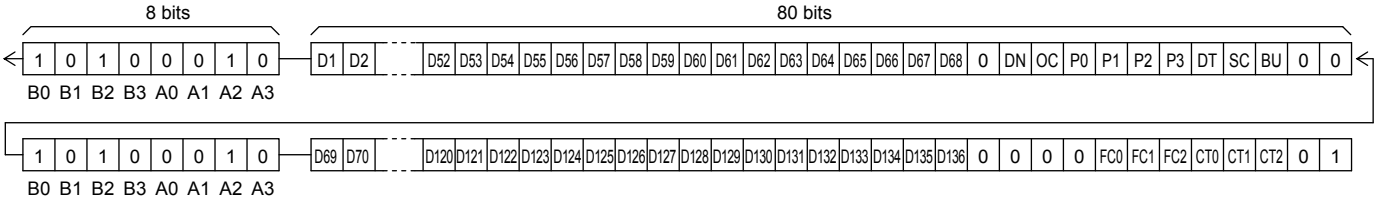


3. 1/4 duty (Simple mode transfer)

- When 201 or more segments are used
  All 320 bits of serial data must be sent.

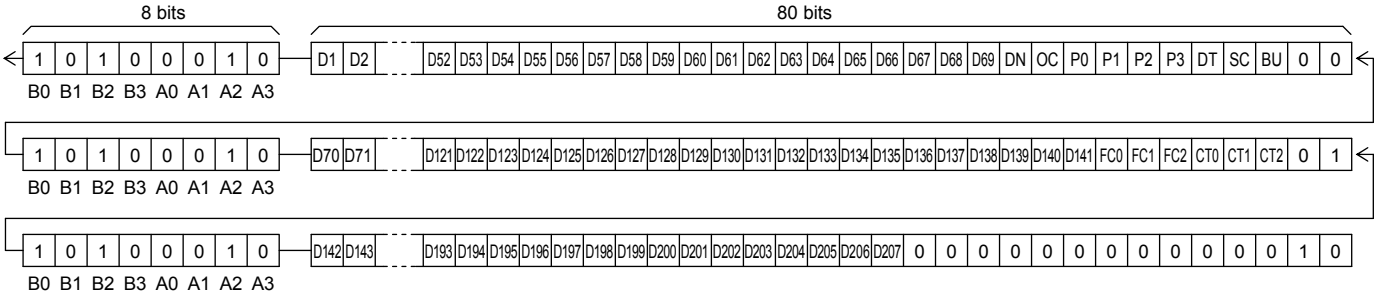


- When fewer than 201 segments are used
  Either 160 or 240 bits of serial data must be sent, depending on the number of segments to be used.
  However, the serial data shown below (the D1 to D136 display data and the control data) must always be sent.

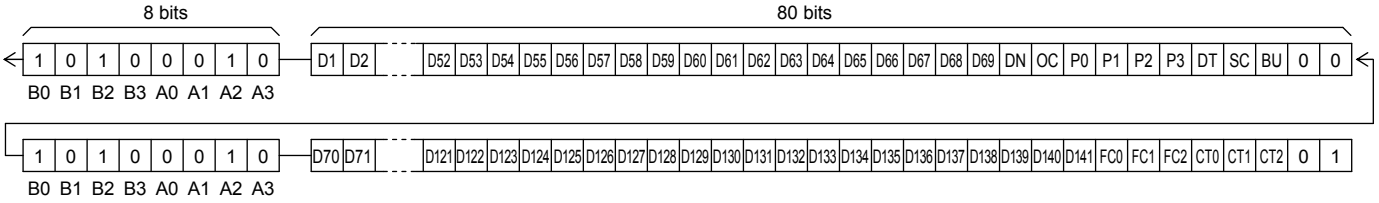


4. 1/3duty (Simple mode transfer)

- When 142 or more segments are used
  All 240 bits of serial data must be sent.



- When fewer than 142 segments are used
  The 160 bits of serial data must be sent.
  However, the serial data shown below (the D1 to D141 display data and the control data) must always be sent.



Control Data Functions

(1) PS10 and PS11, PS2 to PS4 … General-purpose output port (P1 to P4) function setting control data

These control data bits set the general-purpose output function (High or low level output), clock output function or PWM output function of the P1 output pin, and the general-purpose output function (High or low level output) or PWM output function of the P2 to P4 output pins.

However, be careful of being unable to set a PWM output function when the external clock operating frequency is set the $f_{CK}2$=38[kHz] typ (EXF="1") in external clock operating mode (OC= "1").

In addition, be careful of setting of the general-purpose output function (High or low level output) in the case of the simple mode transfer forcibly.

PS10	PS11	General-purpose output port (P1) function
0	0	General-purpose output function (High or low level output)
1	0	Clock output function (Clock frequency : fosc/2, $f_{CK}/2$)
0	1	Clock output function (Clock frequency : fosc/8, $f_{CK}/8$)
1	1	PWM output function (Support for PWM data W10 to W15)

PS2	General-purpose output port (P2) function
0	General-purpose output function (High or low level output)
1	PWM output function (Support for PWM data W20 to W25)

PS3	General-purpose output port (P3) function
0	General-purpose output function (High or low level output)
1	PWM output function (Support for PWM data W30 to W35)

PS4	General-purpose output port (P4) function
0	General-purpose output function (High or low level output)
1	PWM output function (Support for PWM data W10 to W15)

(2) EXF … External clock operating frequency setting control data

This control data bit sets the operating frequency of the external clock which input into the OSCI pin, when the external clock operating mode (OC="1") is set. However, be careful of setting the $f_{CK}1$=300[kHz]typ when the external clock operating mode (OC="1") is set in the case of the simple mode transfer forcibly. In addition, this data is effective only when external clock operating mode (OC= "1") is set.

EXF	External clock operating frequency f_{CK}[kHz]
0	$f_{CK}1$=300[kHz] typ
1	$f_{CK}2$=38[kHz] typ

(3) DN … S68 pin and S69/OSCI pin state setting control data

This control data bit sets state of the S68 pin and the S69/OSCI pin.

DN	Number of display segments		Pin state	
	1/4 duty	1/3 duty	S68	S69/OSCI
0	Up to 264 segments	Up to 201 segment	"L"(V_{SS})	"L"(V_{SS})/OSCI
1	Up to 272 segments	Up to 207 segment	S68	S69/OSCI

Note: "L" (V_{SS}) : Low (V_{SS}) level output

S68 : Segment output

"L" (V_{SS})/OSCI : Low (V_{SS}) level output in internal oscillator operating mode (OC=0)
External clock input in external clock operating mode (OC=1)

S69/OSCI : Segment output in internal oscillator operating mode (OC=0)
External clock input in external clock operating mode (OC=1)

(4) OC … Internal oscillator operating mode/external clock operating mode switching control data
This control data bit selects either the internal oscillator operating mode or external clock operating mode.

OC	Fundamental clock operating mode	I/O pin (S69/OSCI) state
0	Internal oscillator operating mode	S69
1	External clock operating mode	OSCI

Note: S69 : Segment output
OSCI : External clock input

(5) P0 to P3 … Segment output port/general-purpose output port switching control data
These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S8/P8 output pins.

Control data				Output pin state							
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8

Note1: Sn(n=1 to 8): Segment output ports
Pn(n=1 to 8): General-purpose output ports
Note2: When are setting (P0,P1,P2,P3)=(1,0,0,1), (1,0,1,0), (1,0,1,1) and (1,1,X,X), the all P1/S1 to P8/S8 output pins selects the segment output port. X: don't care

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports (general-purpose output function).

Output pin	Correspondence display data	
	1/4 duty	1/3 duty
S1/P1	D1	D1
S2/P2	D5	D4
S3/P3	D9	D7
S4/P4	D13	D10
S5/P5	D17	D13
S6/P6	D21	D16
S7/P7	D25	D19
S8/P8	D29	D22

For example, if the circuit is operated in 1/4 duty and the S4/P4 output pin is selected to be a general-purpose output port and is set general-purpose output function, the S4/P4 output pin will output a high level when the display data D13 is 1, and will output a low level when D13 is 0.

(6) DT … 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive switching control data
This control data bit selects either 1/4-duty 1/3-bias drive or 1/3-duty 1/3-bias drive.

DT	Drive scheme	The COM4/S67 pin state
0	1/4-duty 1/3-bias drive	COM4
1	1/3-duty 1/3-bias drive	S67

Note: COM4 : Common output
S67 : Segment output

(7) SC … Segment on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

(8) BU … Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power saving mode In this mode, the internal oscillator circuit stops oscillation (the S69/OSCI pin is configured for segment output) if the IC is in the internal oscillator operating mode (OC=0) and the IC stops receiving external clock signals (the S69/OSCI pin is configured for external clock input) if the IC is in the external clock operating mode (OC=1). The common and segment output pins go to the V_{SS} level. However, the S1/P1 to S8/P8 output pins can be used as general-purpose output ports under the control of the data bits P0 to P3. (The general-purpose output port P1 to P4 can not be used as clock output or PWM output).

(9) PF0 to PF3 … PWM output waveform frame frequency setting control data

These control data bits set the frame frequency of the PWM output waveforms. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the $f_{CK}2$=38[kHz] typ (EXF="1") in external clock operating mode (OC= "1") or when the serial data transfer is the simple mode transfer, these control data bits become invalid.

Control data				PWM output waveform frame frequency fp[Hz]	
PF0	PF1	PF2	PF3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz] typ)
0	0	0	0	fosc/1536	$f_{CK}1$/1536
1	0	0	0	fosc/1408	$f_{CK}1$/1408
0	1	0	0	fosc/1280	$f_{CK}1$/1280
1	1	0	0	fosc/1152	$f_{CK}1$/1152
0	0	1	0	fosc/1024	$f_{CK}1$/1024
1	0	1	0	fosc/896	$f_{CK}1$/896
0	1	1	0	fosc/768	$f_{CK}1$/768
1	1	1	0	fosc/640	$f_{CK}1$/640
0	0	0	1	fosc/512	$f_{CK}1$/512
1	0	0	1	fosc/384	$f_{CK}1$/384
0	1	0	1	fosc/256	$f_{CK}1$/256

Note : When is setting (PF0,PF1,PF2,PF3)=(1,1,0,1) and (X,X,1,1), the frame frequency is same as frame frequency at the time of the (PF0,PF1,PF2,PF3)=(1,0,1,0) setting (fosc/896, $f_{CK}1$/896).

X: don't care

(10) FC0 to FC2 … Common/segment output waveform fram frequency control data

These control data bits set the frame frequency of the common and segment output waveforms.

Control data			Common/segment output waveform frame frequency fo[Hz]		
FC0	FC1	FC2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK}2$=38[kHz] typ)
1	1	0	fosc/6144	$f_{CK}1$/6144	$f_{CK}2$/768
1	1	1	fosc/4608	$f_{CK}1$/4608	$f_{CK}2$/576
0	0	0	fosc/3072	$f_{CK}1$/3072	$f_{CK}2$/384
0	0	1	fosc/2304	$f_{CK}1$/2304	$f_{CK}2$/288
0	1	0	fosc/1536	$f_{CK}1$/1536	$f_{CK}2$/192
0	1	1	fosc/1152	$f_{CK}1$/1152	$f_{CK}2$/144
1	0	0	fosc/768	$f_{CK}1$/768	$f_{CK}2$/96

Note: When is setting (FC0,FC1,FC2)=(1,0,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,0,0) setting (fosc/3072, fCK1/3072, fCK2/384).

(11) CT0 to CT2 … Display contrast setting control data

These control data bits set display contrast.

CT0 to CT2: Sets the display contrast (7 steps)

CT0	CT1	CT2	LCD drive 3/3 bias voltage $V_{DD}0$ level
0	0	0	$1.00V_{DD}=V_{DD}-(0.05V_{DD}\times0)$
1	0	0	$0.95V_{DD}=V_{DD}-(0.05V_{DD}\times1)$
0	1	0	$0.90V_{DD}=V_{DD}-(0.05V_{DD}\times2)$
1	1	0	$0.85V_{DD}=V_{DD}-(0.05V_{DD}\times3)$
0	0	1	$0.80V_{DD}=V_{DD}-(0.05V_{DD}\times4)$
1	0	1	$0.75V_{DD}=V_{DD}-(0.05V_{DD}\times5)$
0	1	1	$0.70V_{DD}=V_{DD}-(0.05V_{DD}\times6)$

Note: When is setting (CT0,CT1,CT2)=(1,1,1), the LCD drive 3/3 bias voltage $V_{DD}0$ level is $1.00V_{DD}$.

Note that although the display contrast can be adjusted by operating the built-in display contrast adjustment circuit, it can also be adjusted by modifying the supply pin V_{DD} voltage level.

(12) W10 to W15, W20 to W25, W30 to W35 …… PWM data of the PWM output

These control data bits set the pulse width of the PWM output P1 to P4. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the $f_{CK}2$=38[kHz] typ (EXF="1") in external clock operating mode (OC= "1") or when the serial data transfer is the simple mode transfer, these control data bits become invalid.

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Pulse width of PWM output
0	0	0	0	0	0	(1/64)×Tp
1	0	0	0	0	0	(2/64)×Tp
0	1	0	0	0	0	(3/64)×Tp
1	1	0	0	0	0	(4/64)×Tp
0	0	1	0	0	0	(5/64)×Tp
1	0	1	0	0	0	(6/64)×Tp
0	1	1	0	0	0	(7/64)×Tp
1	1	1	0	0	0	(8/64)×Tp
0	0	0	1	0	0	(9/64)×Tp
1	0	0	1	0	0	(10/64)×Tp
0	1	0	1	0	0	(11/64)×Tp
1	1	0	1	0	0	(12/64)×Tp
0	0	1	1	0	0	(13/64)×Tp
1	0	1	1	0	0	(14/64)×Tp
0	1	1	1	0	0	(15/64)×Tp
1	1	1	1	0	0	(16/64)×Tp
0	0	0	0	1	0	(17/64)×Tp
1	0	0	0	1	0	(18/64)×Tp
0	1	0	0	1	0	(19/64)×Tp
1	1	0	0	1	0	(20/64)×Tp
0	0	1	0	1	0	(21/64)×Tp
1	0	1	0	1	0	(22/64)×Tp
0	1	1	0	1	0	(23/64)×Tp
1	1	1	0	1	0	(24/64)×Tp
0	0	0	1	1	0	(25/64)×Tp
1	0	0	1	1	0	(26/64)×Tp
0	1	0	1	1	0	(27/64)×Tp
1	1	0	1	1	0	(28/64)×Tp
0	0	1	1	1	0	(29/64)×Tp
1	0	1	1	1	0	(30/64)×Tp
0	1	1	1	1	0	(31/64)×Tp
1	1	1	1	1	0	(32/64)×Tp

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Pulse width of PWM output
0	0	0	0	0	1	(33/64)×Tp
1	0	0	0	0	1	(34/64)×Tp
0	1	0	0	0	1	(35/64)×Tp
1	1	0	0	0	1	(36/64)×Tp
0	0	1	0	0	1	(37/64)×Tp
1	0	1	0	0	1	(38/64)×Tp
0	1	1	0	0	1	(39/64)×Tp
1	1	1	0	0	1	(40/64)×Tp
0	0	0	1	0	1	(41/64)×Tp
1	0	0	1	0	1	(42/64)×Tp
0	1	0	1	0	1	(43/64)×Tp
1	1	0	1	0	1	(44/64)×Tp
0	0	1	1	0	1	(45/64)×Tp
1	0	1	1	0	1	(46/64)×Tp
0	1	1	1	0	1	(47/64)×Tp
1	1	1	1	0	1	(48/64)×Tp
0	0	0	0	1	1	(49/64)×Tp
1	0	0	0	1	1	(50/64)×Tp
0	1	0	0	1	1	(51/64)×Tp
1	1	0	0	1	1	(52/64)×Tp
0	0	1	0	1	1	(53/64)×Tp
1	0	1	0	1	1	(54/64)×Tp
0	1	1	0	1	1	(55/64)×Tp
1	1	1	0	1	1	(56/64)×Tp
0	0	0	1	1	1	(57/64)×Tp
1	0	0	1	1	1	(58/64)×Tp
0	1	0	1	1	1	(59/64)×Tp
1	1	0	1	1	1	(60/64)×Tp
0	0	1	1	1	1	(61/64)×Tp
1	0	1	1	1	1	(62/64)×Tp
0	1	1	1	1	1	(63/64)×Tp
1	1	1	1	1	1	(64/64)×Tp

Note: W10 to W15 … PWM data of the output pin S1/P1 and S4/P4
W20 to W25 … PWM data of the output pin S2/P2
W30 to W35 … PWM data of the output pin S3/P3

$$Tp = \frac{1}{fp}$$

Display Data and Output Pin Correspondence (1/4 Duty)

Output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5/P5	D17	D18	D19	D20
S6/P6	D21	D22	D23	D24
S7/P7	D25	D26	D27	D28
S8/P8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136

Output pin	COM1	COM2	COM3	COM4
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
S54	D213	D214	D215	D216
S55	D217	D218	D219	D220
S56	D221	D222	D223	D224
S57	D225	D226	D227	D228
S58	D229	D230	D231	D232
S59	D233	D234	D235	D236
S60	D237	D238	D239	D240
S61	D241	D242	D243	D244
S62	D245	D246	D247	D248
S63	D249	D250	D251	D252
S64	D253	D254	D255	D256
S65	D257	D258	D259	D260
S66	D261	D262	D263	D264
S68	D265	D266	D267	D268
S69/OSCI	D269	D270	D271	D272

Note: This table assumes that pins S1/P1 to S8/P8 and S69/OSCI are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

Display data				Output pin (S21) state
D81	D82	D83	D84	
0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	0	0	1	The LCD segment corresponding to COM4 is on.
0	0	1	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	The LCD segment corresponding to COM3 and COM4 are on.
0	1	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	The LCD segment corresponding to COM2 and COM4 are on.
0	1	1	0	The LCD segment corresponding to COM2 and COM3 are on.
0	1	1	1	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	The LCD segment corresponding to COM1 and COM4 are on.
1	0	1	0	The LCD segment corresponding to COM1 and COM3 are on.
1	0	1	1	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	The LCD segment corresponding to COM1 and COM2 are on.
1	1	0	1	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

Display Data and Output Pin Correspondence (1/3 Duty)

Output pin	COM1	COM2	COM3
S1/P1	D1	D2	D3
S2/P2	D4	D5	D6
S3/P3	D7	D8	D9
S4/P4	D10	D11	D12
S5/P5	D13	D14	D15
S6/P6	D16	D17	D18
S7/P7	D19	D20	D21
S8/P8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105

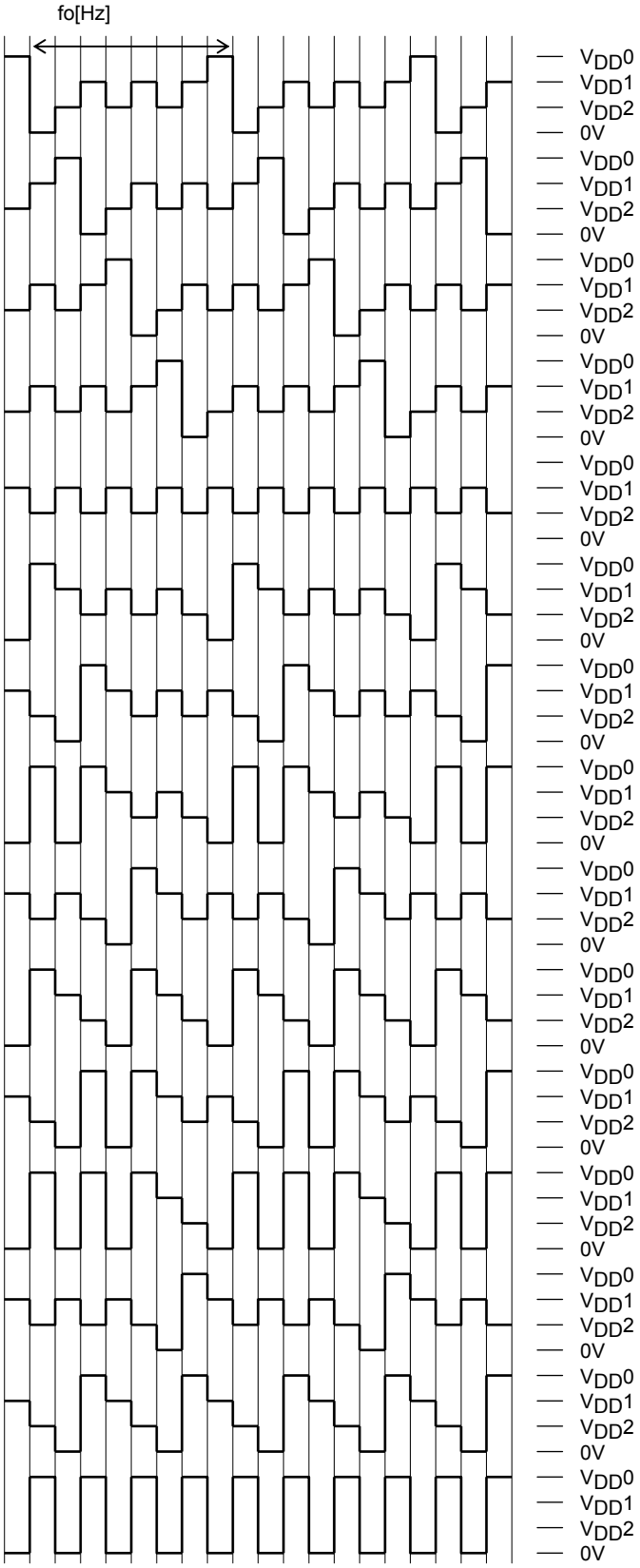
Output pin	COM1	COM2	COM3
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
S54	D160	D161	D162
S55	D163	D164	D165
S56	D166	D167	D168
S57	D169	D170	D171
S58	D172	D173	D174
S59	D175	D176	D177
S60	D178	D179	D180
S61	D181	D182	D183
S62	D184	D185	D186
S63	D187	D188	D189
S64	D190	D191	D192
S65	D193	D194	D195
S66	D196	D197	D198
S67/COM4	D199	D200	D201
S68	D202	D203	D204
S69/OSCI	D205	D206	D207

Note: This table assumes that pins S1/P1 to S8/P8, S67/COM4 and S69/OSCI are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

Display data			Output pin (S21) state
D61	D62	D63	
0	0	0	The LCD segments corresponding to COM1, COM2, and COM3 are off.
0	0	1	The LCD segment corresponding to COM3 is on.
0	1	0	The LCD segment corresponding to COM2 is on.
0	1	1	The LCD segment corresponding to COM2 and COM3 are on.
1	0	0	The LCD segment corresponding to COM1 is on.
1	0	1	The LCD segment corresponding to COM1 and COM3 are on.
1	1	0	The LCD segment corresponding to COM1 and COM2 are on.
1	1	1	The LCD segments corresponding to COM1, COM2, and COM3 are on.

Output Waveforms (1/4-Duty 1/3-Bias Drive Scheme)



LCD driver output when all LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.

LCD driver output when only LCD segments corresponding to COM1 are on.

LCD driver output when only LCD segments corresponding to COM2 are on.

LCD driver output when LCD segments corresponding to COM1 and COM2 are on.

LCD driver output when only LCD segments corresponding to COM3 are on.

LCD driver output when LCD segments corresponding to COM1 and COM3 are on.

LCD driver output when LCD segments corresponding to COM2 and COM3 are on.

LCD driver output when LCD segments corresponding to COM1, COM2, and COM3 are on.

LCD driver output when only LCD segments corresponding to COM4 are on.

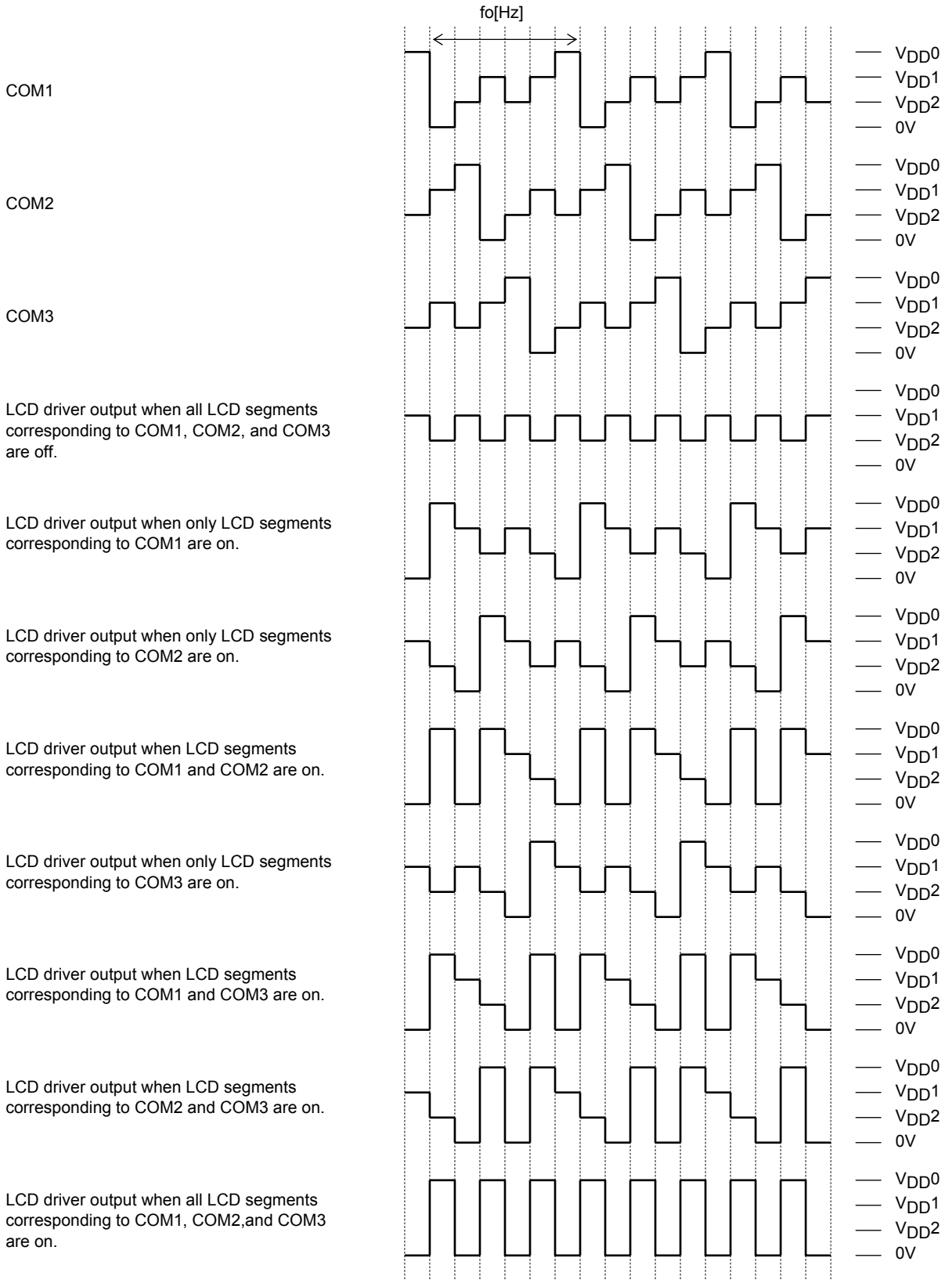
LCD driver output when LCD segments corresponding to COM2 and COM4 are on.

LCD driver output when all LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

Control data			Common/segment output waveform frame frequency fo[Hz]		
FC0	FC1	FC2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK}2$=38[kHz] typ)
1	1	0	fosc/6144	$f_{CK}1/6144$	$f_{CK}2/768$
1	1	1	fosc/4608	$f_{CK}1/4608$	$f_{CK}2/576$
0	0	0	fosc/3072	$f_{CK}1/3072$	$f_{CK}2/384$
0	0	1	fosc/2304	$f_{CK}1/2304$	$f_{CK}2/288$
0	1	0	fosc/1536	$f_{CK}1/1536$	$f_{CK}2/192$
0	1	1	fosc/1152	$f_{CK}1/1152$	$f_{CK}2/144$
1	0	0	fosc/768	$f_{CK}1/768$	$f_{CK}2/96$

Note: When is setting (FC0,FC1,FC2)=(1,0,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,0,0) setting (fosc/3072, $f_{CK}1/3072$, $f_{CK}2/384$).

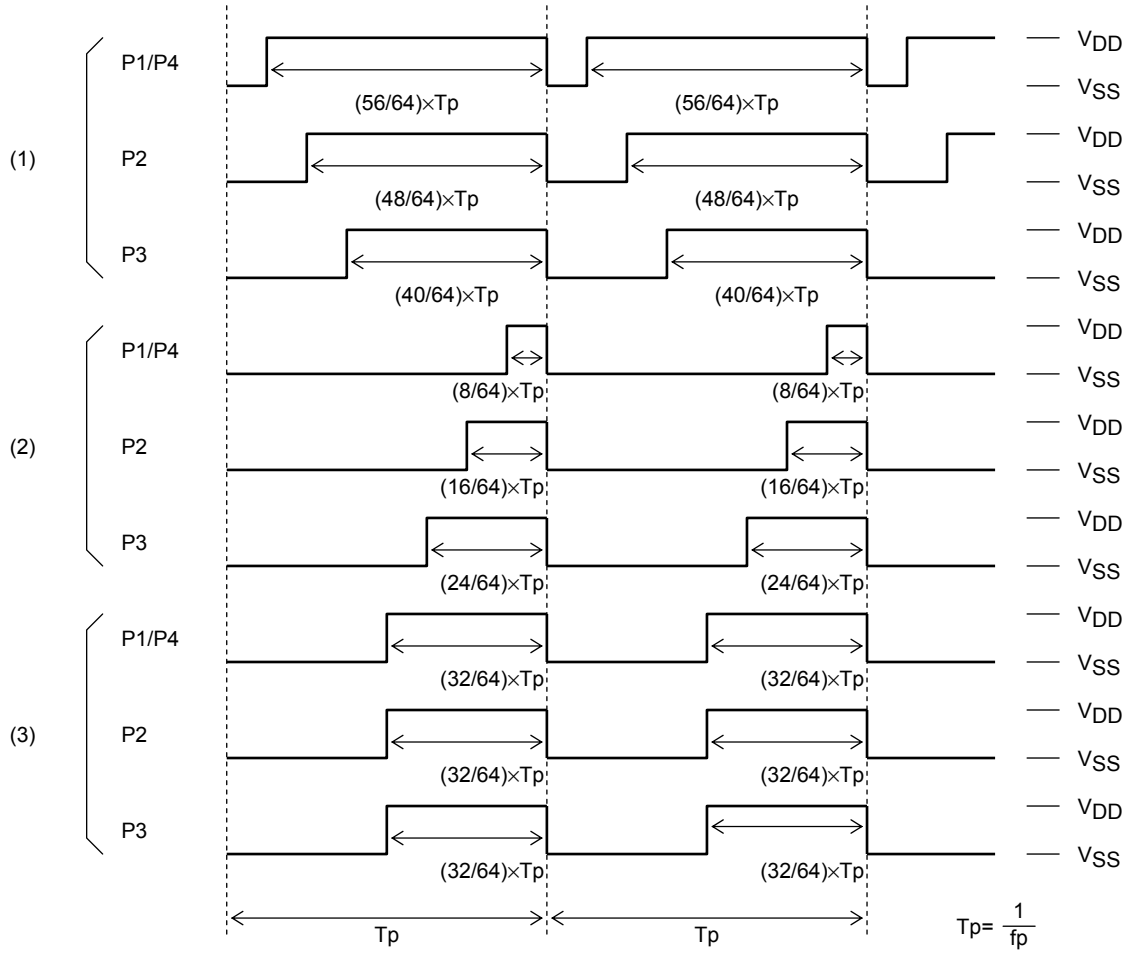
Output Waveforms (1/3-Duty 1/3-Bias Drive Scheme)



Control data			Common/segment output waveform frame frequency fo[Hz]		
FC0	FC1	FC2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK}2$=38[kHz] typ)
1	1	0	fosc/6144	$f_{CK}1/6144$	$f_{CK}2/768$
1	1	1	fosc/4608	$f_{CK}1/4608$	$f_{CK}2/576$
0	0	0	fosc/3072	$f_{CK}1/3072$	$f_{CK}2/384$
0	0	1	fosc/2304	$f_{CK}1/2304$	$f_{CK}2/288$
0	1	0	fosc/1536	$f_{CK}1/1536$	$f_{CK}2/192$
0	1	1	fosc/1152	$f_{CK}1/1152$	$f_{CK}2/144$
1	0	0	fosc/768	$f_{CK}1/768$	$f_{CK}2/96$

Note: When is setting (FC0,FC1,FC2)=(1,0,1), the frame frequency is same as frame frequency at the time of the (FC0,FC1,FC2)=(0,0,0) setting (fosc/3072, $f_{CK}1/3072$, $f_{CK}2/384$).

PWM output port waveforms

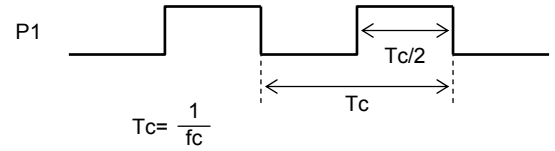


Control data																		PWM output waveforms
W10	W11	W12	W13	W14	W15	W20	W21	W22	W23	W24	W25	W30	W31	W32	W33	W34	W35	
1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0	0	1	(1)
1	1	1	0	0	0	1	1	1	1	0	0	1	1	1	0	1	0	(2)
1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	(3)

Control data				PWM output waveform frame frequency fp[Hz]	
PF0	PF1	PF2	PF3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, f_{CK}1=300[kHz] typ)
0	0	0	0	fosc/1536	f_{CK}1/1536
1	0	0	0	fosc/1408	f_{CK}1/1408
0	1	0	0	fosc/1280	f_{CK}1/1280
1	1	0	0	fosc/1152	f_{CK}1/1152
0	0	1	0	fosc/1024	f_{CK}1/1024
1	0	1	0	fosc/896	f_{CK}1/896
0	1	1	0	fosc/768	f_{CK}1/768
1	1	1	0	fosc/640	f_{CK}1/640
0	0	0	1	fosc/512	f_{CK}1/512
1	0	0	1	fosc/384	f_{CK}1/384
0	1	0	1	fosc/256	f_{CK}1/256

Note: When is setting (PF0,PF1,PF2,PF3)=(1,1,0,1) and (X,X,1,1), the frame frequency is same as frame frequency at the time of the (PF0,PF1,PF2,PF3)=(1,0,1,0) setting (fosc/896, f_{CK}1/896). X: don't care

Clock output waveforms

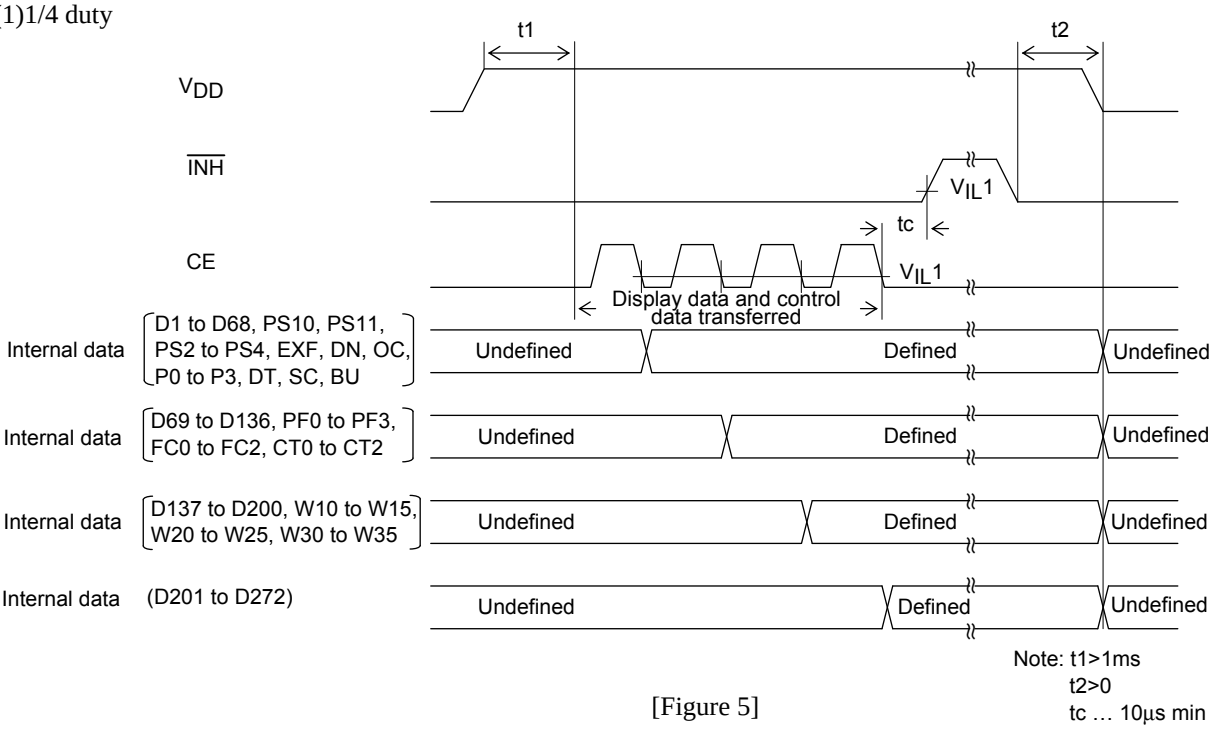


Control data		Clock frequency of clock output P1 fc(=1/Tc)[Hz]
PS10	PS11	
1	0	Clock output function (fosc/2, f_{CK}/2)
0	1	Clock output function (fosc/8, f_{CK}/8)

Display Control and the $\overline{INH}$ Pin

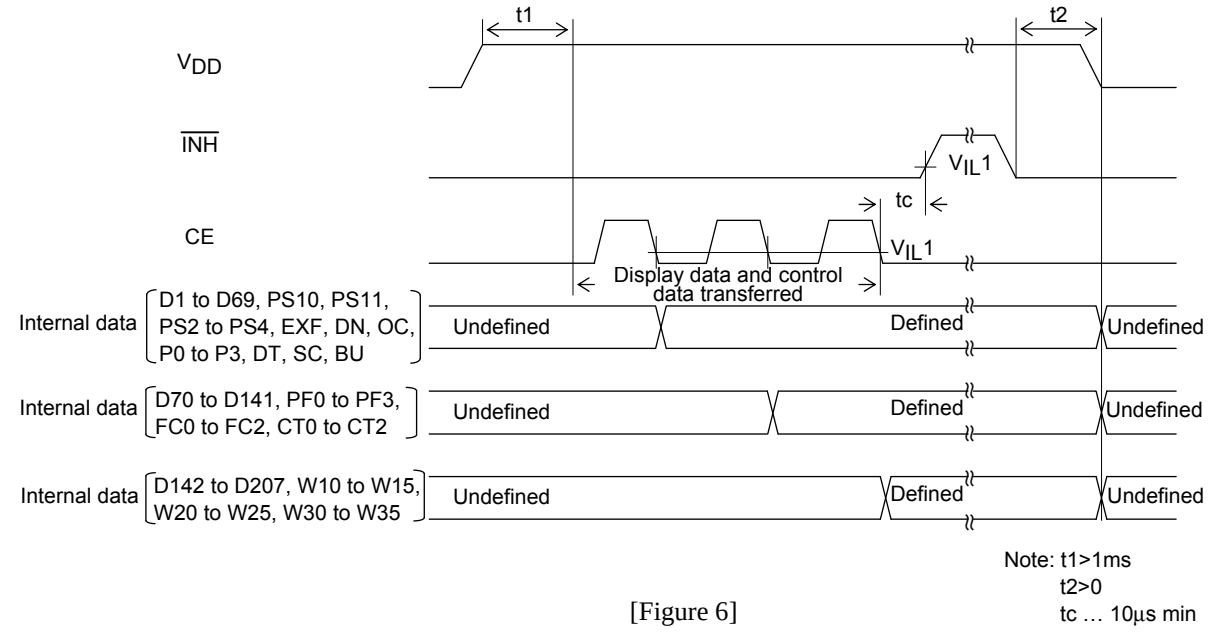
Since the LSI internal data (1/4 duty : the display data D1 to D272 and the control data, 1/3 duty : the display data D1 to D207 and the control data) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S8/P8, S9 to S66, COM1 to COM3, COM4/S67, S68, and S69/OSCI pins to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed. This procedure prevents meaningless display at power on (See Figure 5, Figure 6, Figure 7 and Figure 8.)

(1)1/4 duty



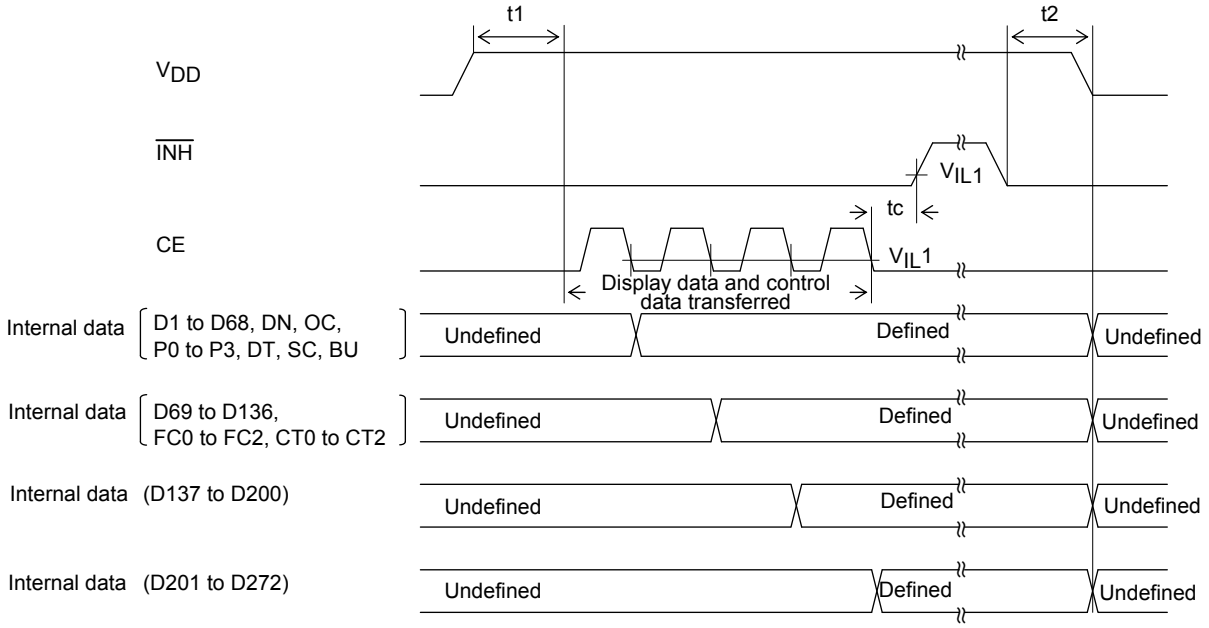
[Figure 5]

(2) 1/3 duty



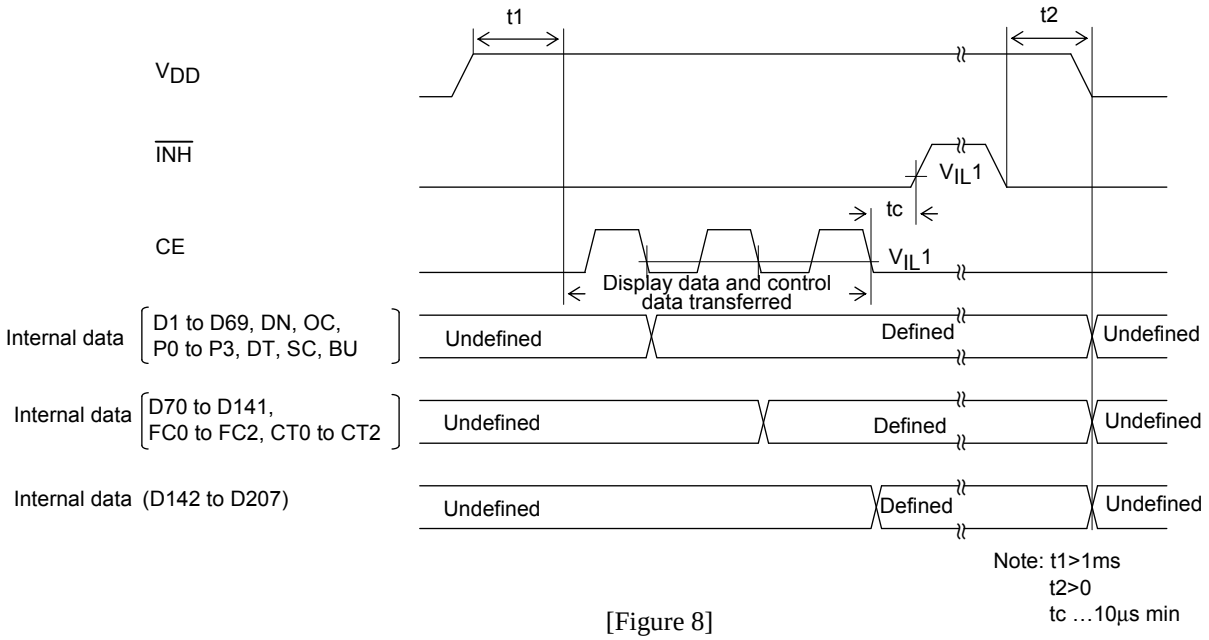
[Figure 6]

(3)1/4 duty (Simple mode transfer)



[Figure 7]

(4)1/3 duty (Simple mode transfer)



[Figure 8]

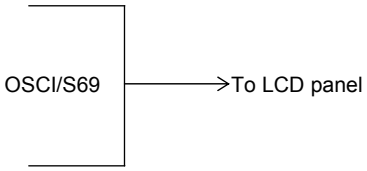
Notes on Controller Transfer of Display Data

When using the LC75879PT in 1/4 duty, applications transfer the display data (D1 to D272) in four operations, and in 1/3 duty, they transfer the display data (D1 to D207) in three operations. In either case, applications should transfer all of the display data within 30 ms to maintain the quality of displayed image.

S69/OSCI Pin Peripheral Circuit

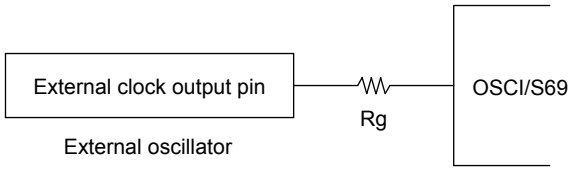
(1) Internal oscillator operating mode (control data OC=0)

Connect the S69/OSCI pin to the LCD panel when the internal oscillator operating mode is selected.



(2) External clock operating mode (control data OC=1)

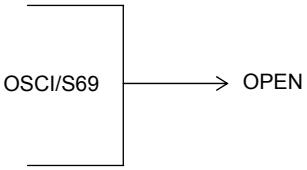
When the external clock operating mode is selected, insert a current protection resistor Rg (2.2 to 22kΩ) between the S69/OSCI pin and external clock output pin (external oscillator). Determine the value of the resistance according to the allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.



Note: Allowable current value at external clock output pin > $\frac{V_{DD}}{Rg}$

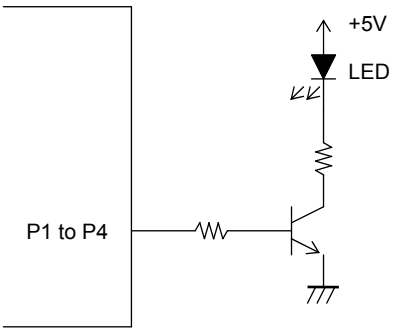
(3) Unused pin treatment

When the S69/OSCI pin is not to be used, select the internal oscillator operating mode (setting control data OC to 0) to keep the pin open.



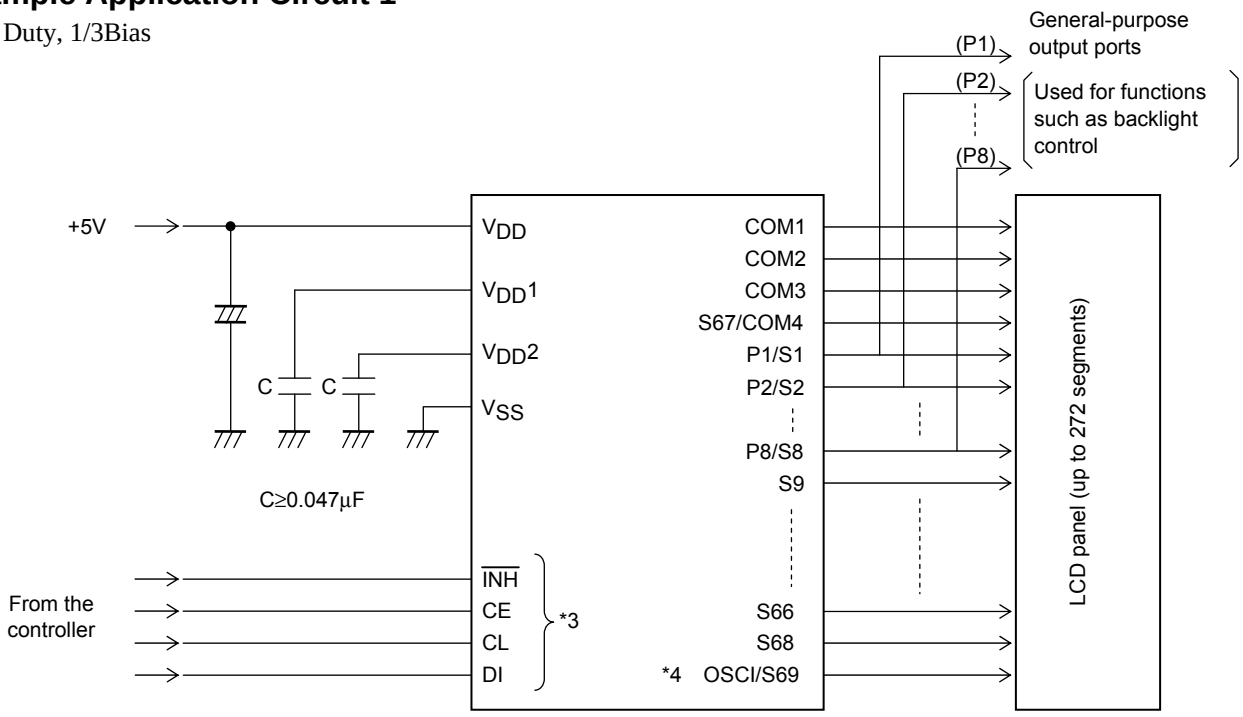
P1 to P4 pin peripheral circuit

It is recommended the circuit shown below be used to adjust the brightness of the LED backlight using the PWM output P1 to P4



Sample Application Circuit 1

1/4 Duty, 1/3Bias

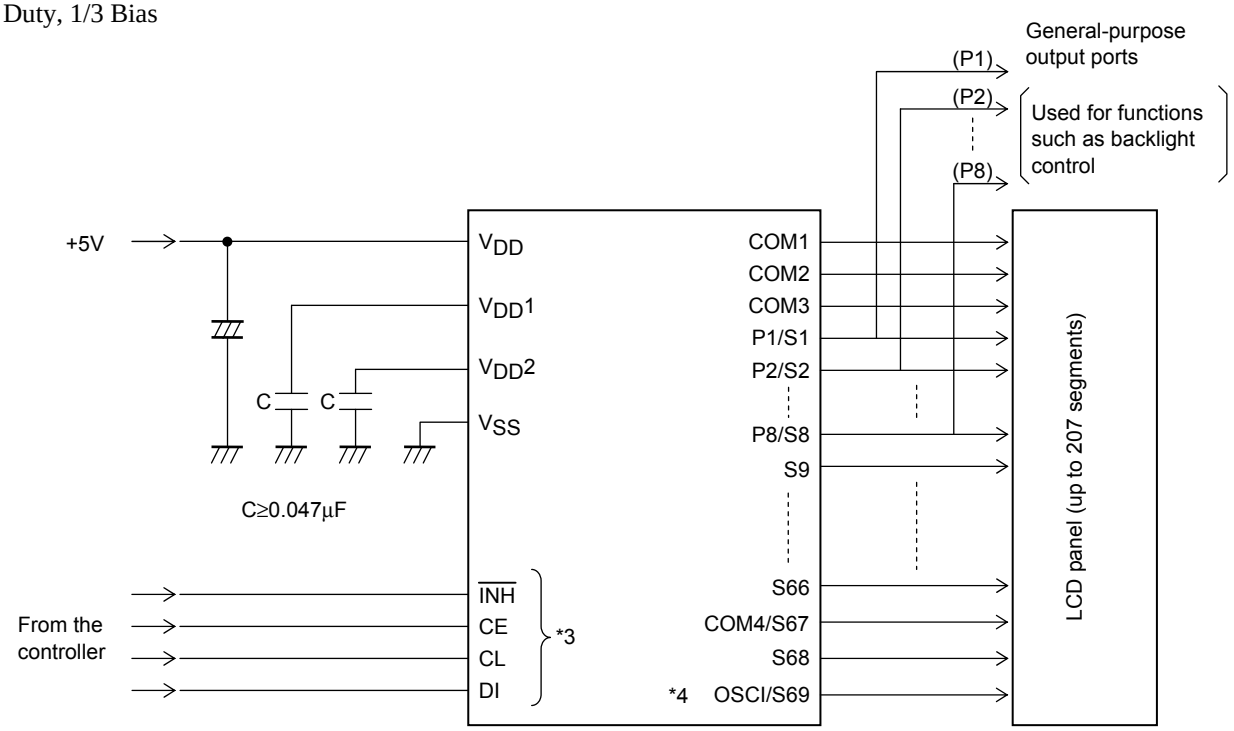


*3 The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3.3V or 5V.

*4 Connect the S69/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor Rg (2.2 to 22kΩ) between the S69/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode (see "S69/OSCI Pin Peripheral Circuit").

Sample Application Circuit 2

1/3 Duty, 1/3 Bias



*3 The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3.3V or 5V.

*4 Connect the S69/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor Rg (2.2 to 22kΩ) between the S69/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode (see "S69/OSCI Pin Peripheral Circuit")

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