Ordering number : ENA0429

SANYO Semiconductors
DATA SHEET

CMOS IC

LC75835W — 1/3, 1/4-Duty General-Purpose LCD Display Driver

Overview

The LC75835W is a 1/3, 1/4 duty general-purpose LCD display driver that can be used for displaying segments for mobile devices and other such products under the control of a microcontroller. In addition to being able to directly drive up to 136 LCD segments, the LC75835W can also control up to 16 general-purpose output ports. It incorporates an oscillation circuit that reduces the external resistors and capacitors used for oscillation.

Features

- Either 1/4 or 1/3 duty can be selected with the serial control data.
  1/4 duty drive: Up to 136 segments can be driven
  1/3 duty drive: Up to 105 segments can be driven
- Either 1/3 or 1/2 bias can be selected with the serial control data.
- On, off, or blinking for each segment can be set with the serial control data.
- Serial data control of display switching in 40-bit units.
  (As a general rule, the display can be switched in 12 segment-units.)
- Serial data control of current on/off to the LCD drive bias voltage generation divider resistors.
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port functions.
- Buzzer control signals (1 channel) can be output from the general-purpose output port.
- Serial data control of the frame frequency of the common and segment output waveforms.
- Serial data control of the segment blinking frequency.
- Serial data control of switching between the internal oscillator operating mode and external clock operating mode.
- Serial data input supports CCB* format communication with the system controller.
- Independent V_{LCD} for the LCD driver block (V_{LCD} can be set to any voltage in the range 2.7 to 5.5 volts without regard to the logic block power supply V_{DD}).
- The $\overline{INH}$ pin allows the display to be forced to the off state.
- Incorporation of an oscillator circuit

- CCB is a trademark of SANYO Electric Co., Ltd.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	-0.3 to +4.5	V
	V_{LCD} max	V_{LCD}	-0.3 to +6.5	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$, OSCI	-0.3 to +4.5	V
	$V_{IN}2$	$V_{LCD}1$, $V_{LCD}2$	-0.3 to V_{LCD}+0.3	
Output voltage	V_{OUT}	S1 to S35, COM1 to COM4, P1 to P16	-0.3 to V_{LCD}+0.3	V
Output current	$I_{OUT}1$	S1 to S35	300	μA
	$I_{OUT}2$	COM1 to COM4	3	mA
	$I_{OUT}3$	P1 to P16 *1	5	
Allowable power dissipation	Pd max	Ta = 75°C	100	mW
Operating temperature	Topr		-30 to +75	°C
Storage temperature	Tstg		-55 to +125	°C

Note: *1 The sum of output current through P1 to P16 must be 40mA or less.

Allowable Operating Ranges at Ta = -30 to +75°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		3.6	V
	V_{LCD}	V_{LCD}	2.7		5.5	
Input voltage	$V_{LCD}1$	$V_{LCD}1$		2/3V_{LCD}	V_{LCD}	V
	$V_{LCD}2$	$V_{LCD}2$		1/3V_{LCD}	V_{LCD}	
Input high-level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.7V_{DD}		3.6	V
	$V_{IH}2$	OSCI	0.7V_{DD}		3.6	
Input low-level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$	0		0.2V_{DD}	V
	$V_{IL}2$	OSCI	0		0.2V_{DD}	
External clock operating frequency	f_{CK}	OSCI external clock operating mode [Figure 4]	15	32.8	65	kHz
External clock duty cycle	D_{CK}	OSCI external clock operating mode [Figure 4]	30	50	70	%
Data setup time	tds	CL, DI [Figure 2][Figure 3]	160			ns
Data hold time	tdh	CL, DI [Figure 2][Figure 3]	160			ns
CE wait time	tcp	CE, CL [Figure 2][Figure 3]	160			ns
CE setup time	tcs	CE, CL [Figure 2][Figure 3]	160			ns
CE hold time	tch	CE, CL [Figure 2][Figure 3]	160			ns
High-level clock pulse width	tϕH	CL [Figure 2][Figure 3]	160			ns
Low-level clock pulse width	tϕL	CL [Figure 2][Figure 3]	160			ns
Rise time	tr	CE, CL, DI [Figure 2][Figure 3]		160		ns
Fall time	tf	CE, CL, DI [Figure 2][Figure 3]		160		ns
$\overline{INH}$ switching time	tc	$\overline{INH}$, CE [Figure 5][Figure 6]	10			μs

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$			$0.1V_{DD}$		V
Input high-level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 3.6V			1.0	μA
	$I_{IH}2$	OSCI	V_I = 3.6V			1.0	
Input low-level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0V	-1.0			μA
	$I_{IL}2$	OSCI	V_I = 0V	-1.0			
Output high-level voltage	$V_{OH}1$	S1 to S35	I_O = -20μA	V_{LCD}-0.9			V
	$V_{OH}2$	COM1 to COM4	I_O = -100μA	V_{LCD}-0.9			
	$V_{OH}3$	P1 to P16	I_O = -1mA	V_{LCD}-0.9			
Output low-level voltage	$V_{OL}1$	S1 to S35	I_O = 20μA			0.9	V
	$V_{OL}2$	COM1 to COM4	I_O = 100μA			0.9	
	$V_{OL}3$	P1 to P16	I_O = 1mA			0.9	
Output middle-level voltage *2	$V_{MID}1$	COM1 to COM4	1/2 bias I_O = ±100μA	$1/2V_{LCD}$ -0.9		$1/2V_{LCD}$ +0.9	V
	$V_{MID}2$	S1 to S35	1/3 bias I_O = ±20μA	$2/3V_{LCD}$ -0.9		$2/3V_{LCD}$ +0.9	
	$V_{MID}3$	S1 to S35	1/3 bias I_O = ±20μA	$1/3V_{LCD}$ -0.9		$1/3V_{LCD}$ +0.9	
	$V_{MID}4$	COM1 to COM4	1/3 bias I_O = ±100μA	$2/3V_{LCD}$ -0.9		$2/3V_{LCD}$ +0.9	
	$V_{MID}5$	COM1 to COM4	1/3 bias I_O = ±100μA	$1/3V_{LCD}$ -0.9		$1/3V_{LCD}$ +0.9	
LCD drive bias voltage	$V_{LCD}1$	$V_{LCD}1$	1/3 bias I_I = ±0μA Current supply to bias voltage generation divider resistors Outputs open	$2/3V_{LCD}$ -0.03V_{LCD}	$2/3V_{LCD}$	$2/3V_{LCD}$ +0.03V_{LCD}	V
	$V_{LCD}2$	$V_{LCD}2$	1/3 bias I_I = ±0μA Current supply to bias voltage generation divider resistors Outputs open	$1/3V_{LCD}$ -0.03V_{LCD}	$1/3V_{LCD}$	$1/3V_{LCD}$ +0.03V_{LCD}	
	$V_{LCD}12$	$V_{LCD}1$, $V_{LCD}2$	1/2 bias I_I = ±0μA Current supply to bias voltage generation divider resistors Outputs open	$1/2V_{LCD}$ -0.03V_{LCD}	$1/2V_{LCD}$	$1/2V_{LCD}$ +0.03V_{LCD}	
Oscillator frequency	fosc	Internal oscillator circuit	Internal oscillator operating mode	236	295	354	kHz
Current drain	$I_{DD}1$	V_{DD}	Power-saving mode			1	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 3.3V normal mode External clock operating mode *3		5	10	
	$I_{DD}3$	V_{DD}	V_{DD} = 3.3V normal mode External clock operating mode *3 Serial data transfer *4		90	180	
	$I_{DD}4$	V_{DD}	V_{DD} = 3.3V normal mode Internal oscillator operating mode		50	100	
	$I_{DD}5$	VDD	V_{DD} = 3.3V normal mode Internal oscillator operating mode Serial data transfer *4		135	270	
	$I_{LCD}1$	V_{LCD}	Power-saving mode			1	
	$I_{LCD}2$	V_{LCD}	V_{LCD} = 5.0V output open Normal mode, 1/2 bias		85	170	
	$I_{LCD}3$	V_{LCD}	V_{LCD} = 5.0V output open Normal mode, 1/3 bias		55	110	
	$I_{LCD}4$	V_{LCD}	V_{LCD} = 5.0V output open Normal mode, current to bias voltage generation divider resistors shut off		10	20	

Note: *2 Excluding the bias voltage generation divider resistors (R_{LCD} = 30kΩ typ.) built in the $V_{LCD}1$ and $V_{LCD}2$. (See Figure 1.)

Note: *3 External clock operating mode (f_{CK} = 32.8kHz, $V_{IH}2 = V_{DD}$, $V_{IL}2$ = 0V, rise/fall time = 20ns)

Note: *4 Serial data transfer (data transfer frequency 2MHz, $V_{IH}1 = V_{DD}$, $V_{IL}1$ = 0V, rise/fall time = 20ns)

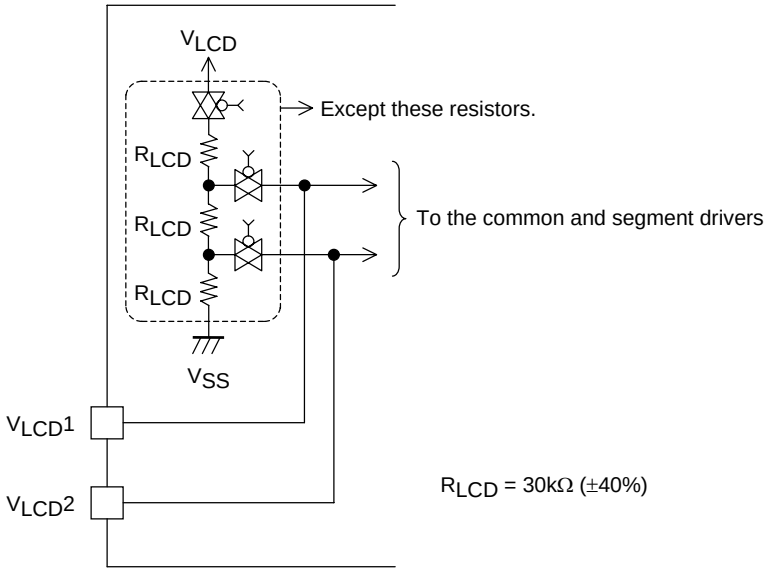


Figure 1

1. When CL is stopped at the low level

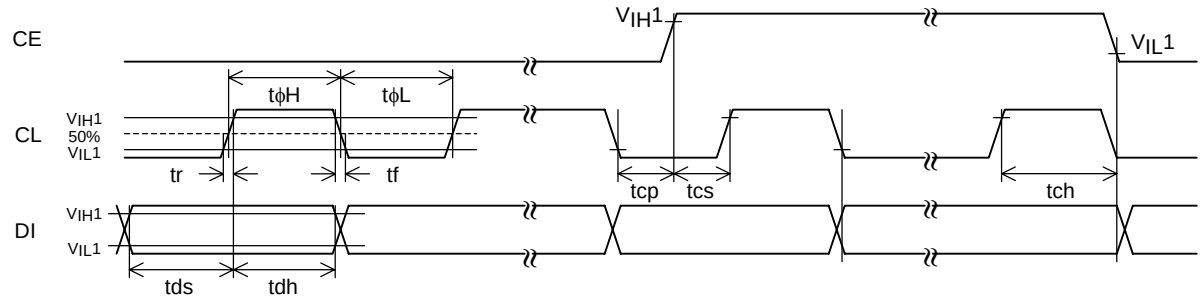


Figure 2

2. When CL is stopped at the high level

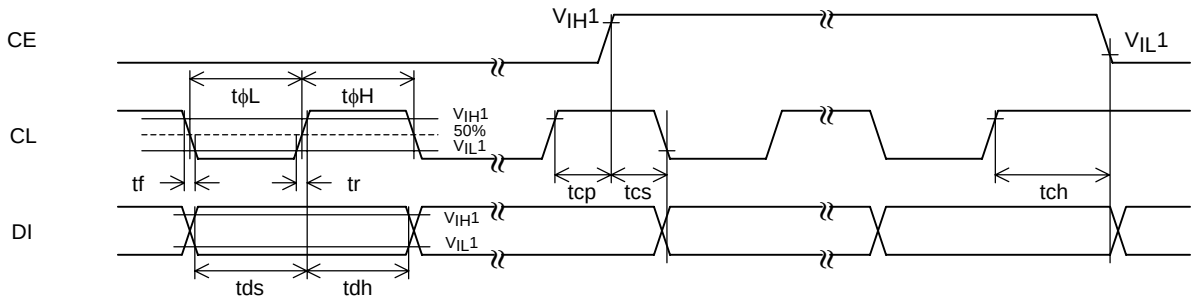
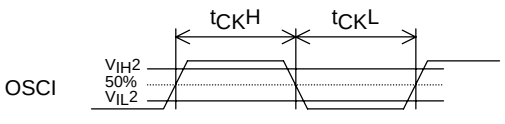


Figure 3

3. OSCI pin clock timing in external clock operating mode



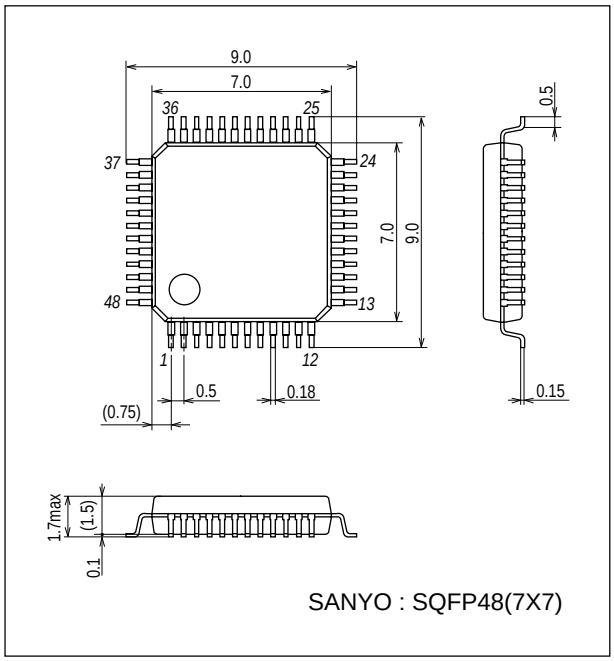
$$f_{CK} = \frac{1}{t_{CK}H + t_{CK}L} \quad [kHz]$$

$$D_{CK} = \frac{t_{CK}H}{t_{CK}H + t_{CK}L} \times 100[\%]$$

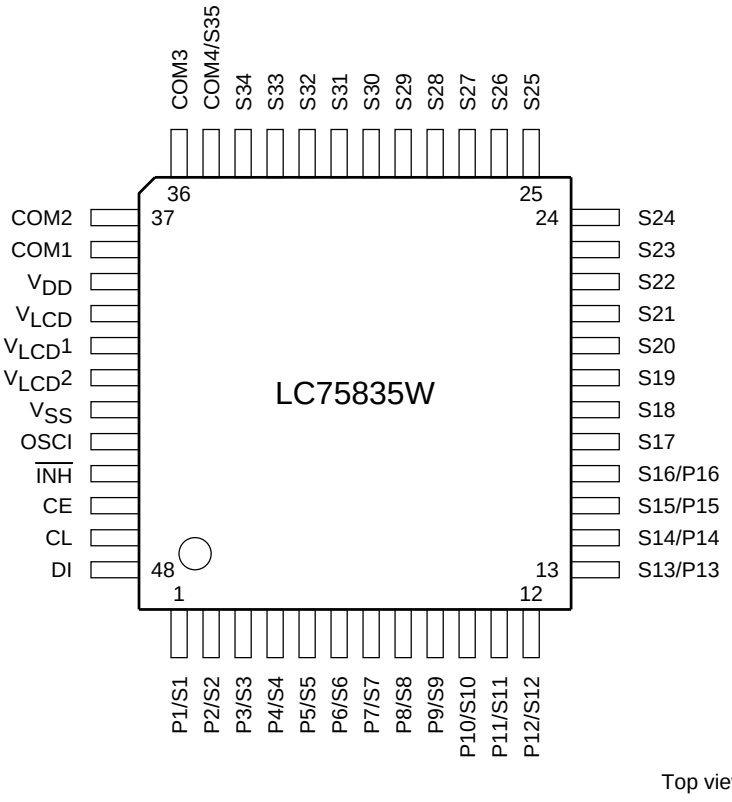
Figure 4

Package Dimensions

unit : mm (typ)
3163B

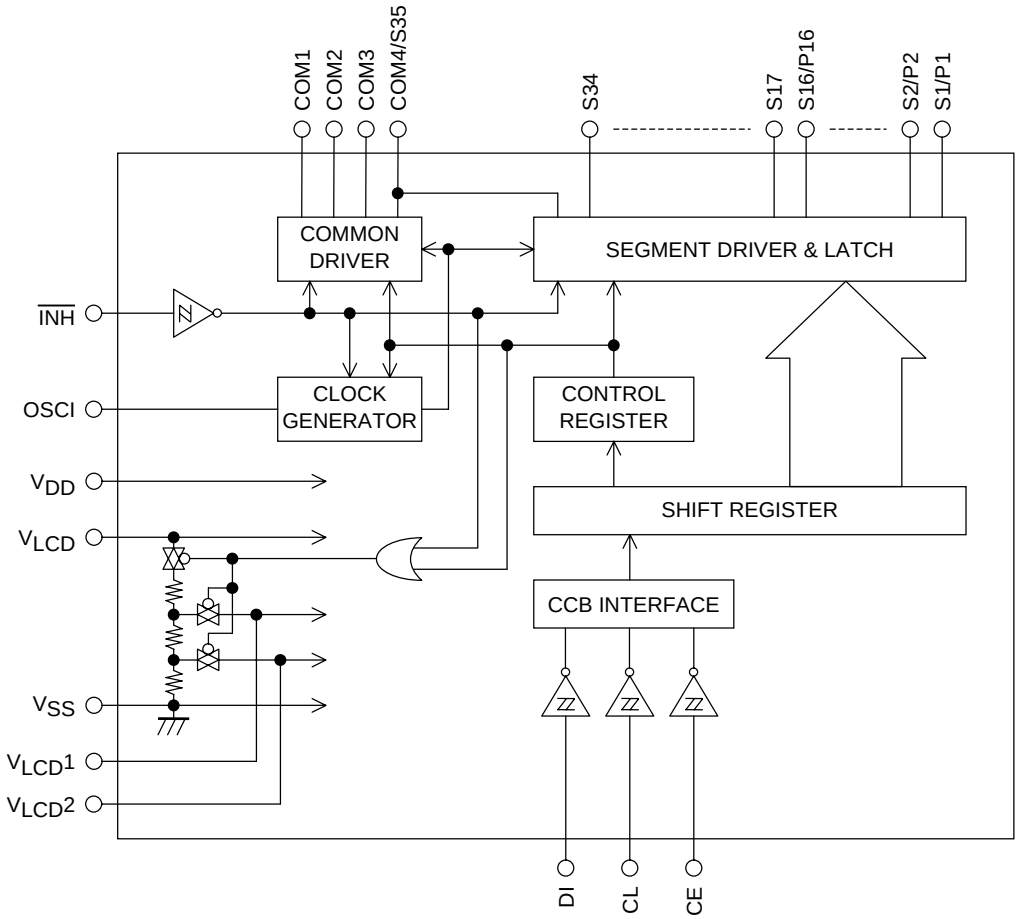


Pin Assignment



Top view

Block Diagram



Pin Functions

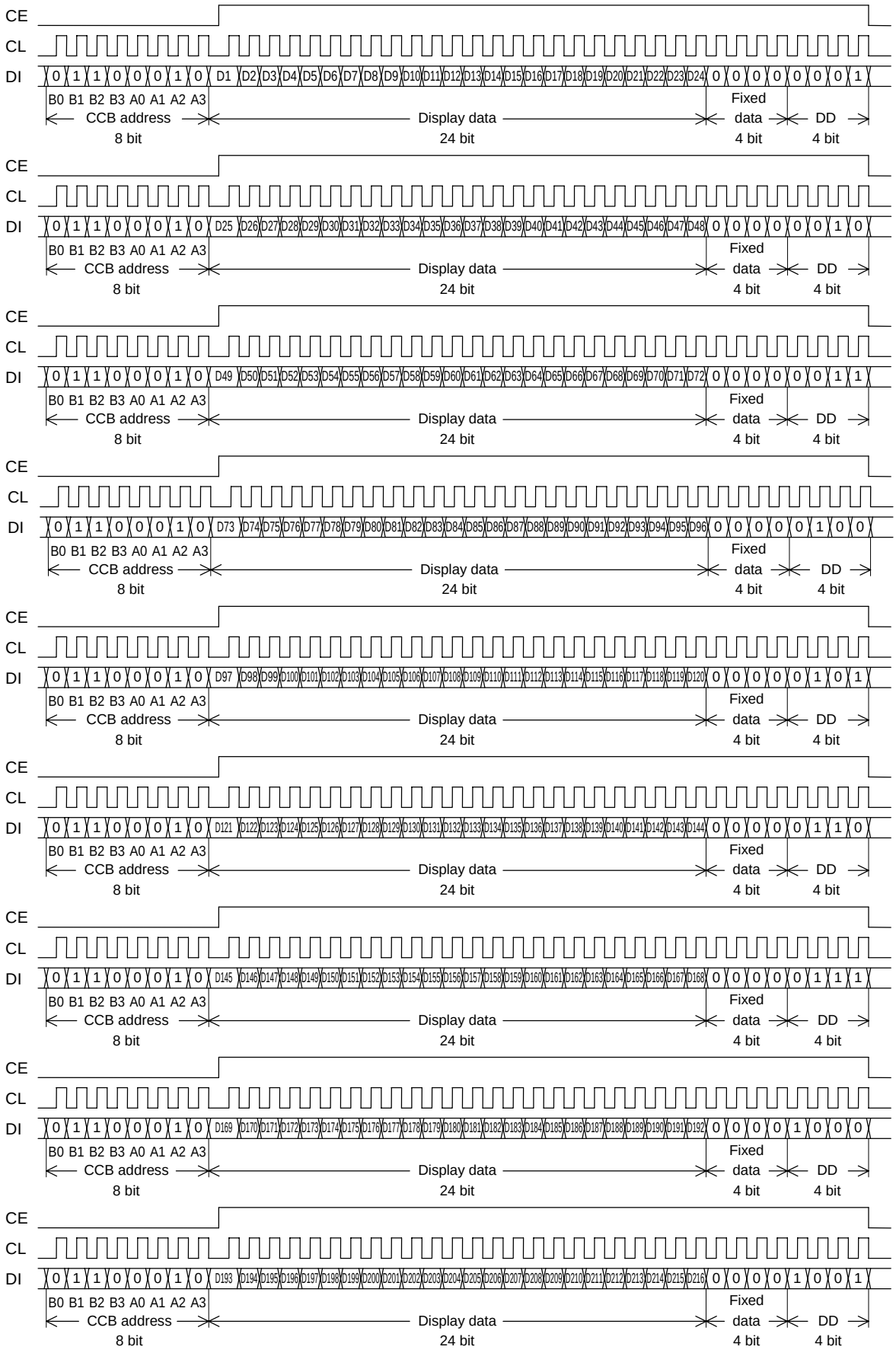
Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S16/P16 S17 to S34	1 to 16 17 to 34	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S16/P16 pins can be used as general-purpose output ports when so set up by the control data.	-	O	OPEN
COM1 to COM3 COM4/S35	38 to 36 35	Common driver output pins. The frame frequency is fo [Hz]. COM4/S35 can be used as segment output in 1/3 duty mode.	-	O	OPEN
OSCI	44	External clock input pin. A 15 to 65kHz clock must be supplied to this pin in external clock operating mode. This pin must be connected to ground in internal oscillator operating mode.	-	I	GND
CE CL DI	46 47 48	Serial data transfer inputs. Must be connected to the controller. CE: Chip enable CL: Synchronization clock DI: Transfer data	H ↑ -	I I I	GND
$\overline{INH}$	45	Display off control input • $\overline{INH}$ = low (V_{SS}) ...Display forced off S1/P1 to S16/P16 = low (V_{SS}) (These pins are forcibly set to the general-purpose output port and held at the VSS level.) S17 to S34 = low (V_{SS}) COM1 to COM3 = low (V_{SS}) COM4/S35 = low (V_{SS}) Shuts off current to the LCD drive bias voltage generation divider resistors. Stop the internal oscillation circuit. • $\overline{INH}$ = high (V_{DD})...Display on However, serial data transfer is possible when the display is forced off.	L	I	GND
$V_{LCD}1$	41	Used to apply the LCD drive 2/3 bias voltage externally. Connect this pin to $V_{LCD}2$ when using a 1/2-bias drive scheme.	-	I	OPEN
$V_{LCD}2$	42	Used to apply the LCD drive 1/3 bias voltage externally. Connect this pin to $V_{LCD}1$ when using a 1/2-bias drive scheme.	-	I	OPEN
V_{DD}	39	Power supply pin for the logic circuit block. A power voltage of 2.7V to 3.6V must be applied to this pin.	-	-	-
V_{LCD}	40	Power supply pin for the LCD driver block. A power voltage of 2.7V to 5.5 V must be applied to this pin.	-	-	-
V_{SS}	43	Power supply pin. Must be connected to ground.	-	-	-

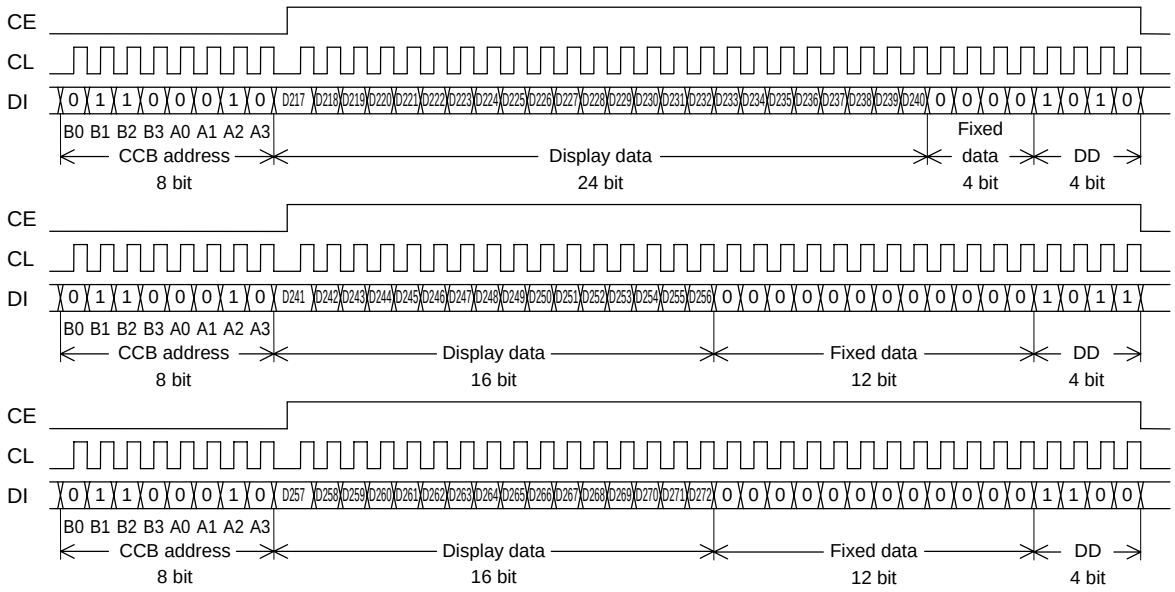
Serial Data Transfer Formats

(1) 1/4 duty

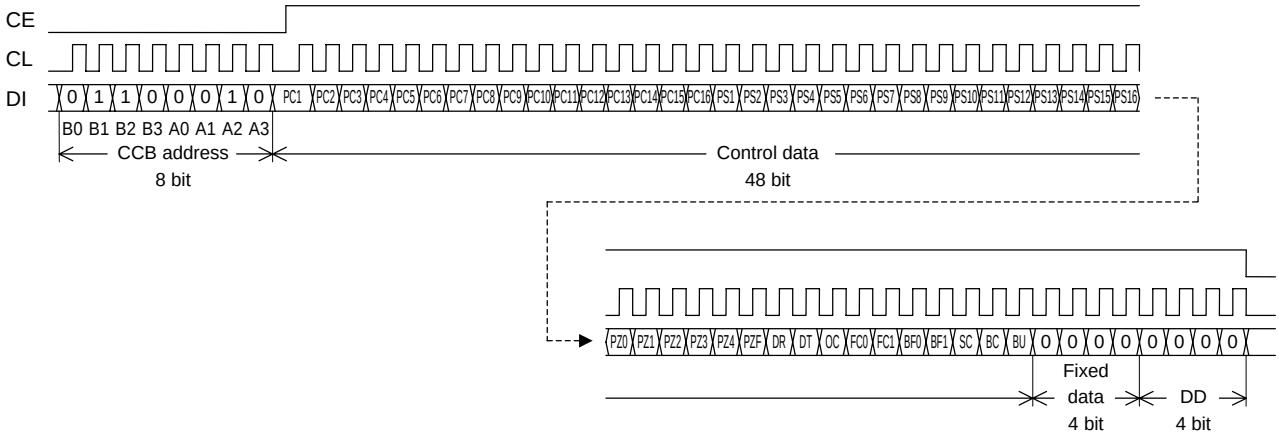
1. When CL is stopped at the low level

- When the display data is transferred





• When the control data is transferred

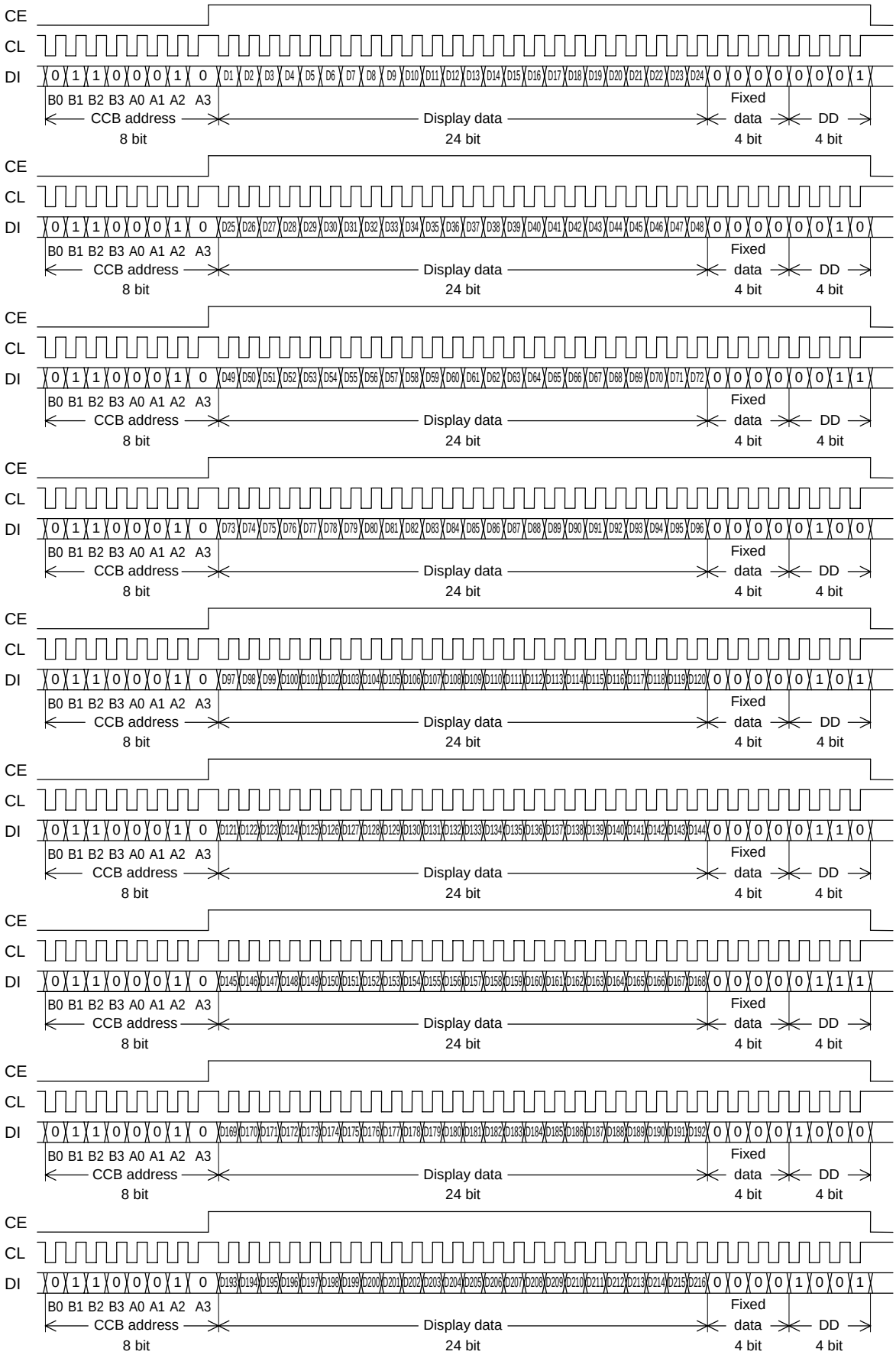


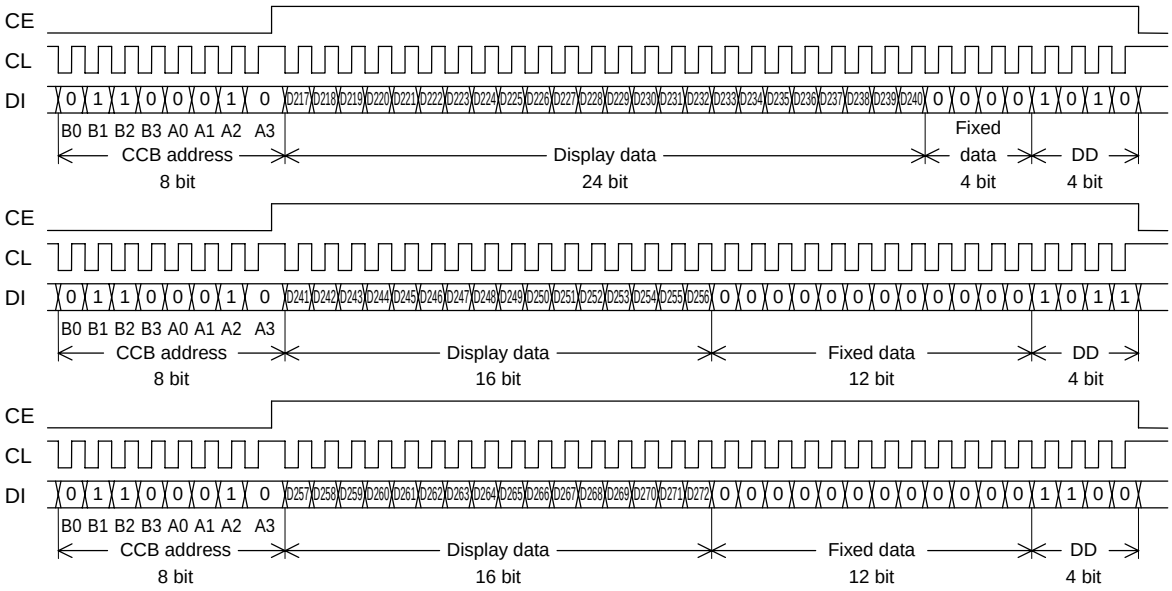
Note: DD is the direction data.

• CCB address ..... "46H"
• D1 to D272 ..... Display data
• PC1 to PC16..... General-purpose output port state setting data
• PS1 to PS16 ..... Segment output port/general-purpose output port switching control data
• PZ0 to PZ4 ..... Buzzer control signal output selection data
• PZF ..... Buzzer control signal frequency setting control data
• DR ..... 1/3-bias drive or 1/2-bias drive switching control data
• DT ..... 1/4-duty drive or 1/3-duty drive switching control data
• OC ..... Internal oscillator operating mode/external clock operating mode switching control data
• FC0, FC1 ..... Common/segment output waveform frame frequency setting control data
• BF0, BF1 ..... Segment blinking frequency setting control data
• SC ..... Segment on/off control data
• BC ..... LCD drive bias voltage generation divider resistor current on/off control data
• BU ..... Normal mode/power-saving mode control data

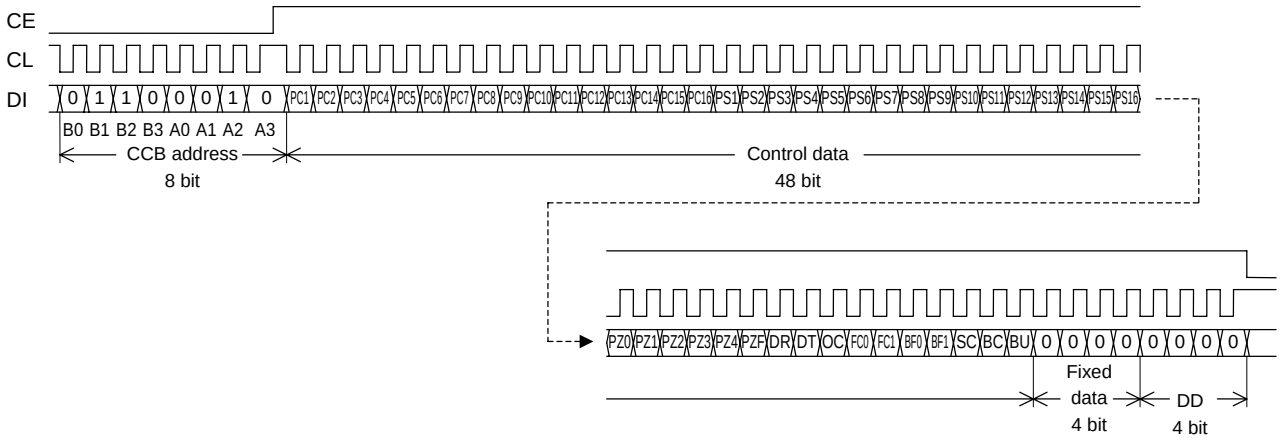
2. When CL is stopped at the high level

- When the display data is transferred





• When the control data is transferred



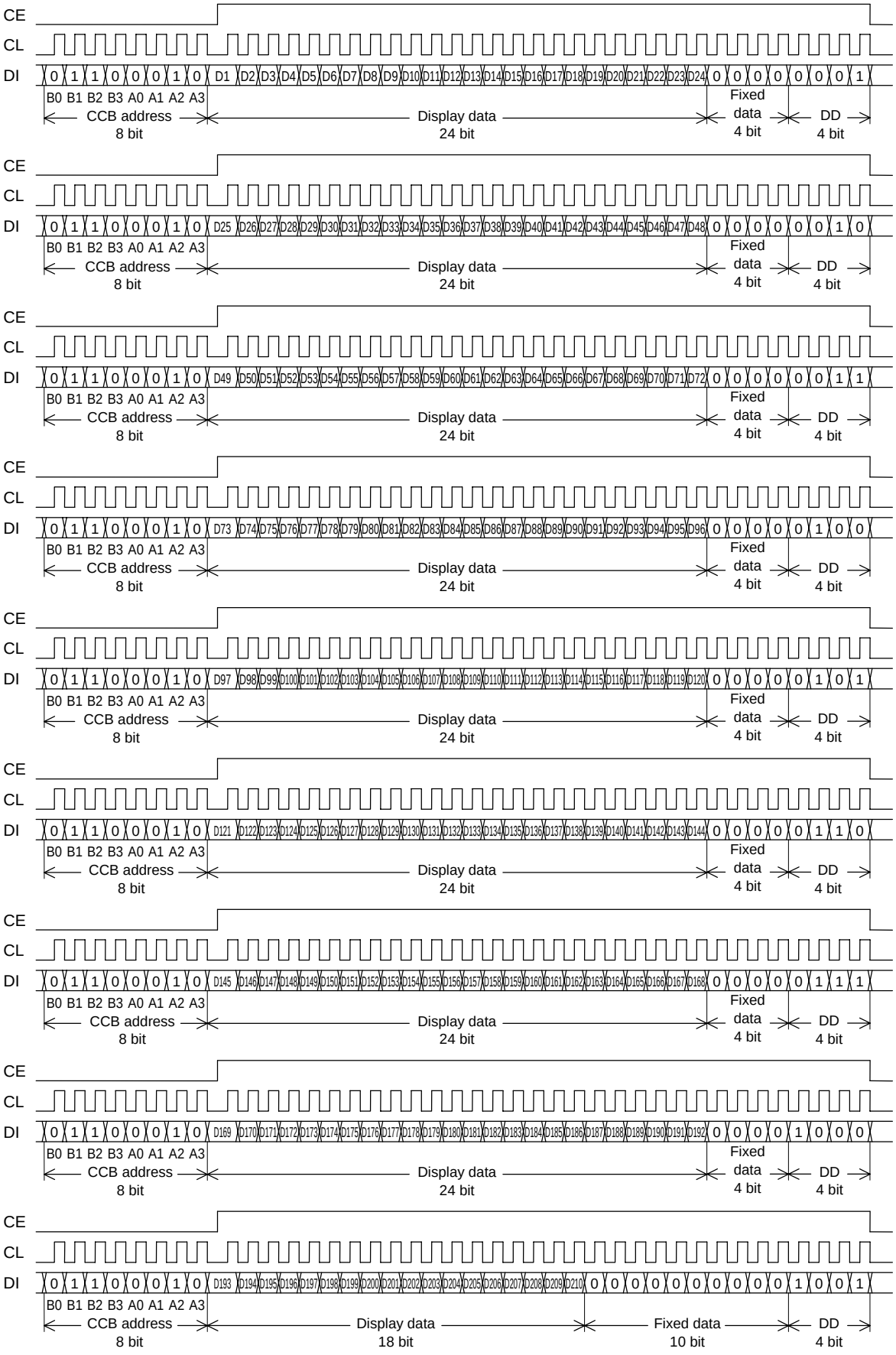
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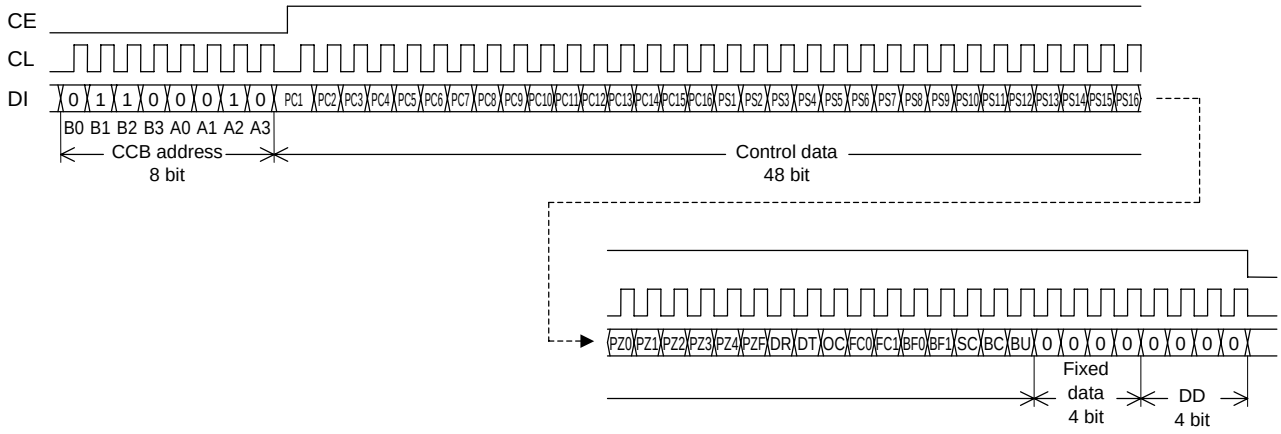
(2) 1/3 duty

1. When CL is stopped at the low level

- When the display data is transferred



• When the control data is transferred

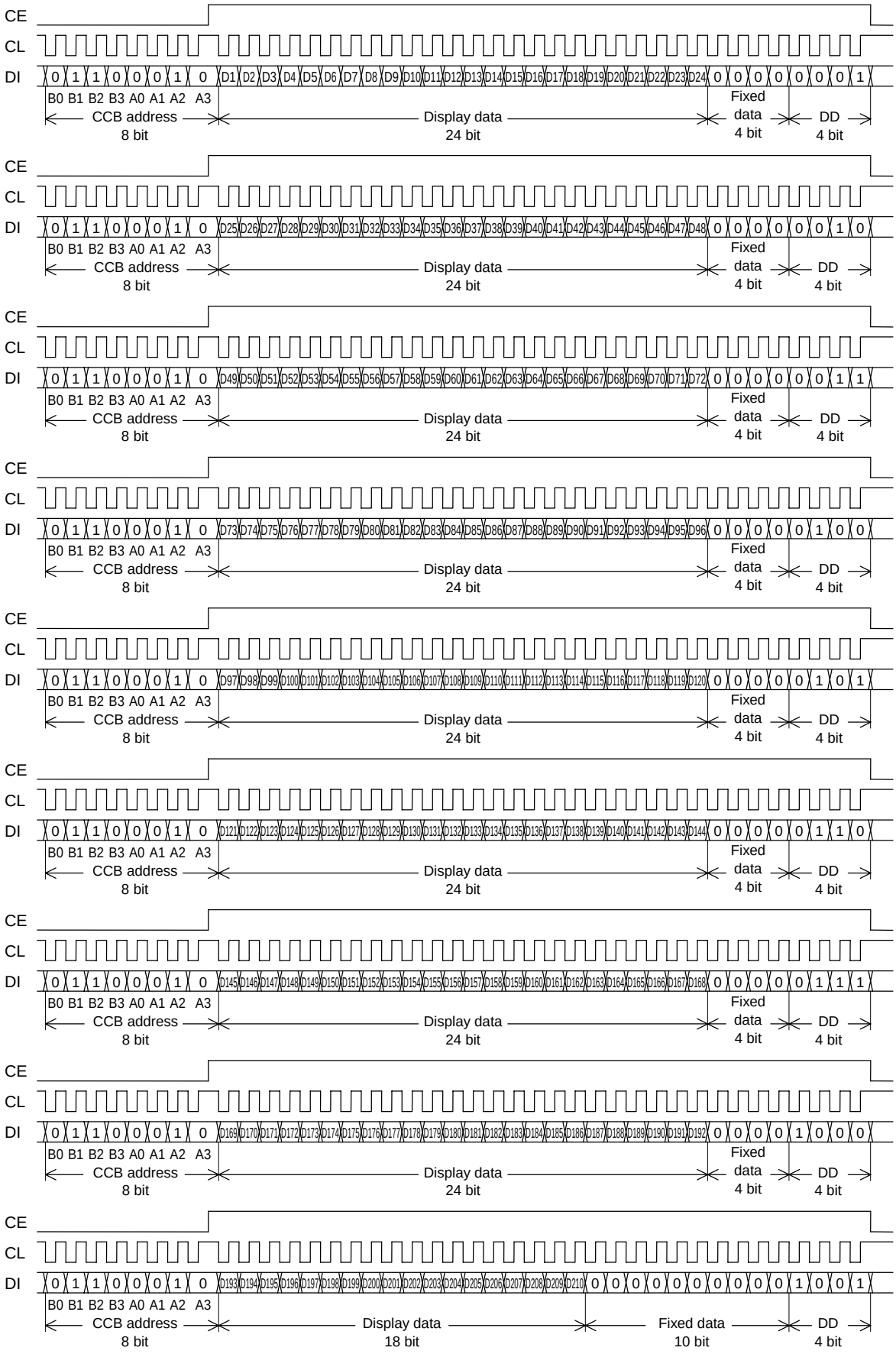


Note: DD is the direction data.

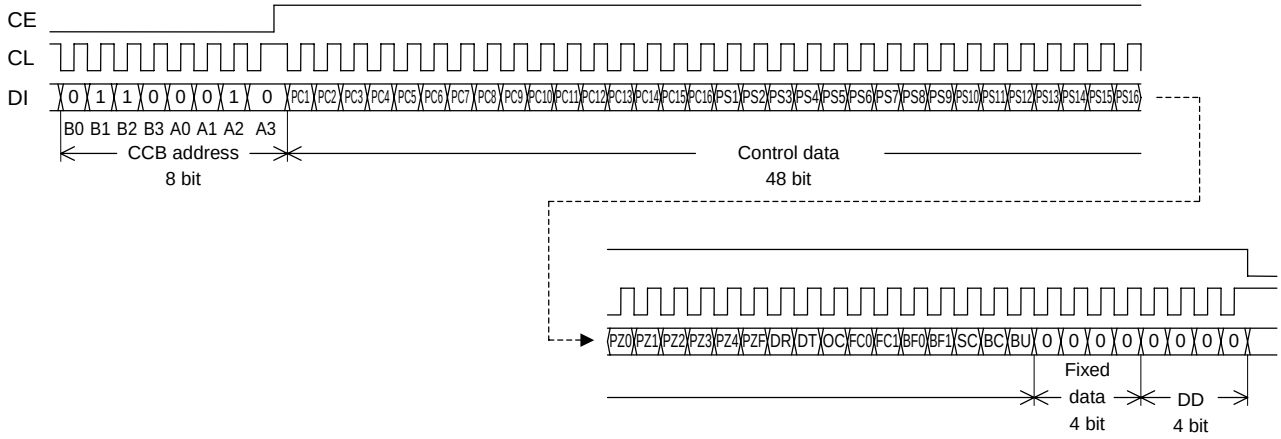
• CCB address ..... "46H"
• D1 to D210 ..... Display data
• PC1 to PC16..... General-purpose output port state setting data
• PS1 to PS16 ..... Segment output port/general-purpose output port switching control data
• PZ0 to PZ4 ..... Buzzer control signal output selection data
• PZF ..... Buzzer control signal frequency setting control data
• DR ..... 1/3-bias drive or 1/2-bias drive switching control data
• DT ..... 1/4-duty drive or 1/3-duty drive switching control data
• OC ..... Internal oscillator operating mode/external clock operating mode switching control data
• FC0, FC1 ..... Common/segment output waveform frame frequency setting control data
• BF0, BF1 ..... Segment blinking frequency setting control data
• SC ..... Segment on/off control data
• BC ..... LCD drive bias voltage generation divider resistor current on/off control data
• BU ..... Normal mode/power-saving mode control data

2. When CL is stopped at the high level

- When the display data is transferred



• When the control data is transferred



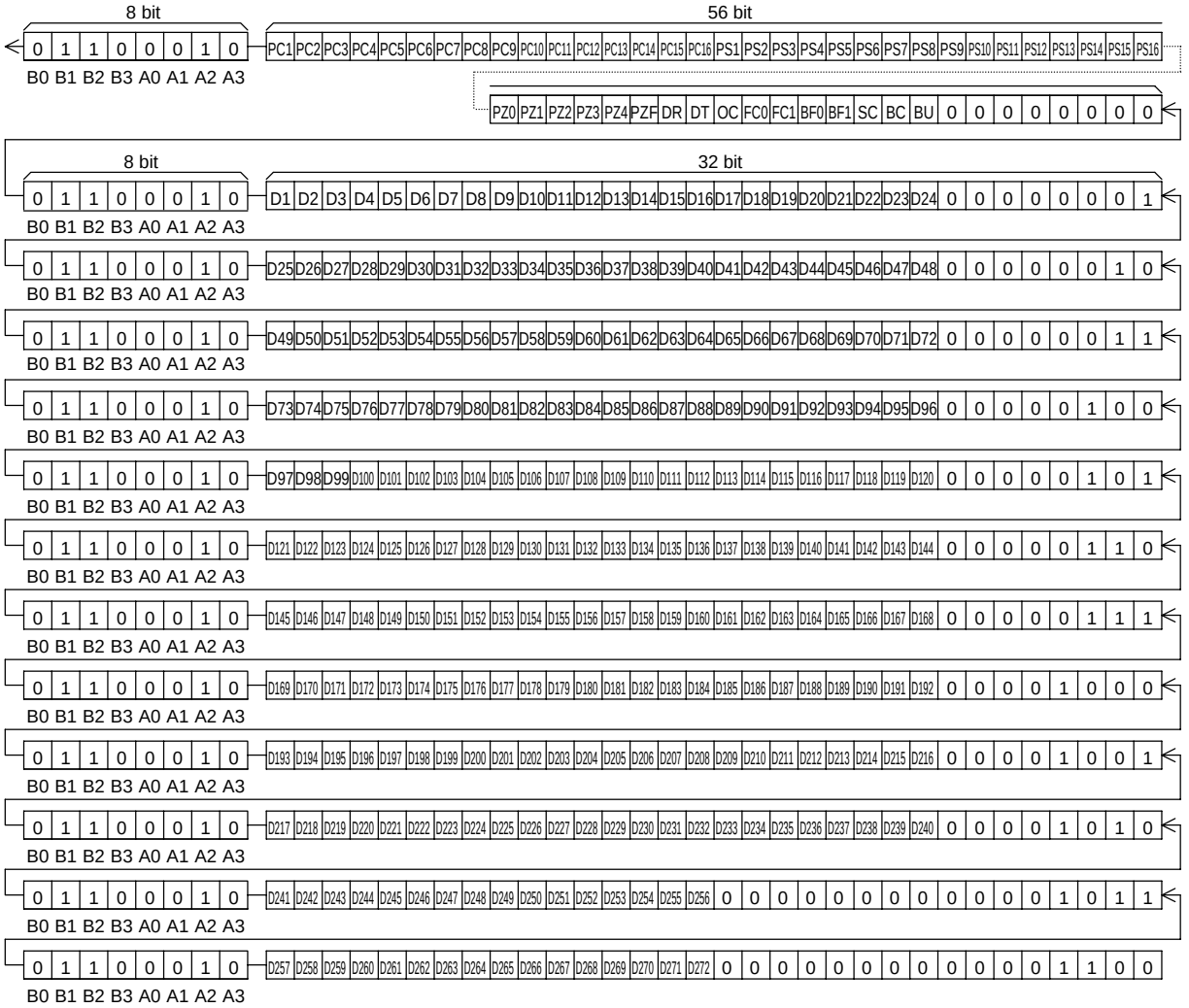
Note: DD is the direction data.

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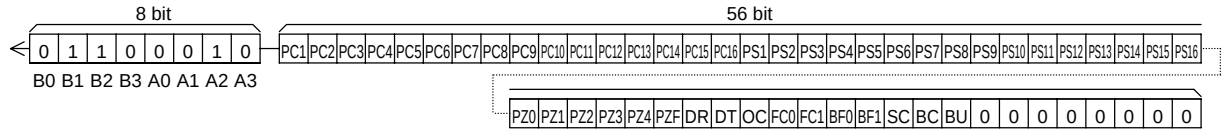
Serial Data Transfer Example

(1) 1/4 duty

- When 129 or more segments are used
  All 544 bits of serial data (including CCB address) must be sent.



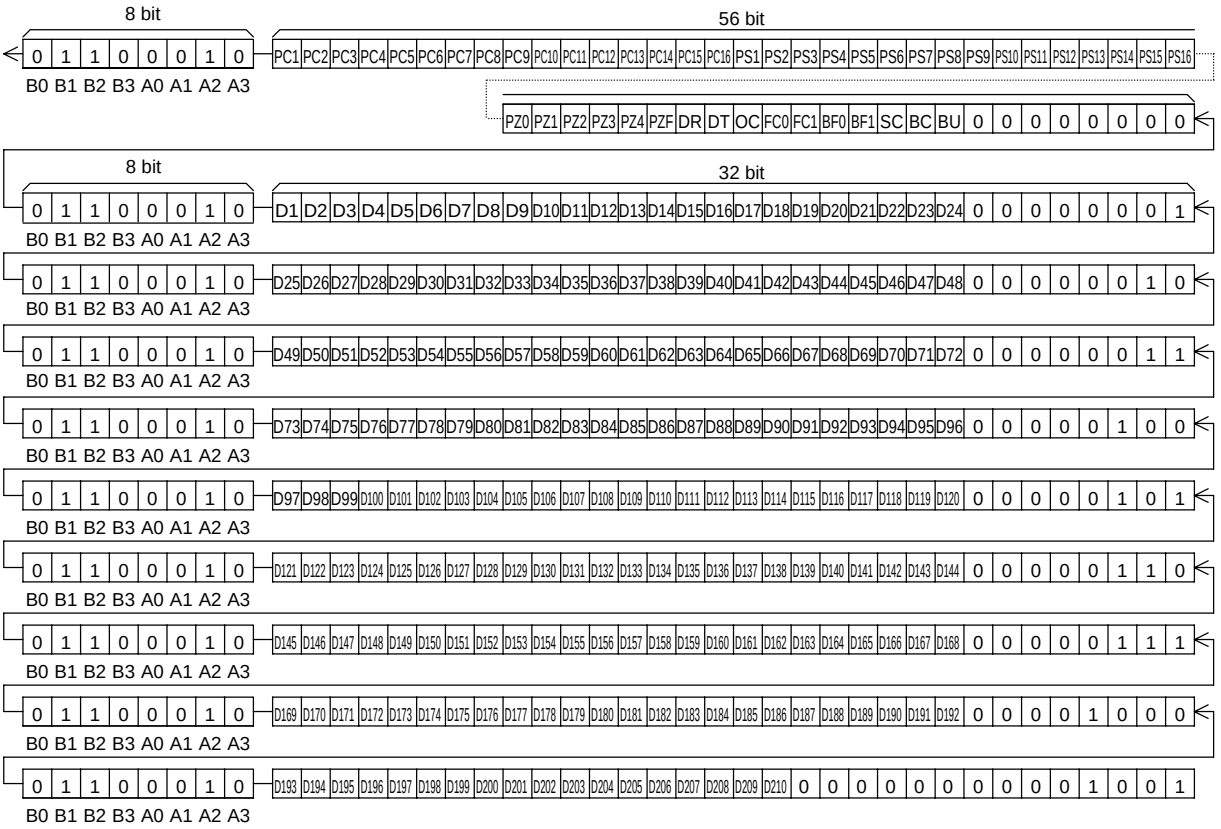
- When fewer than 129 segments are used
  Depending on the number of segments used, 104 bits, 144 bits, 184 bits, 224 bits, 264 bits, 304 bits, 344 bits, 384 bits, 424 bits, 464 bits or 504 bits (including the CCB address) must be sent as serial data. However, the serial data (control data) shown in the figure below must be sent without fail.



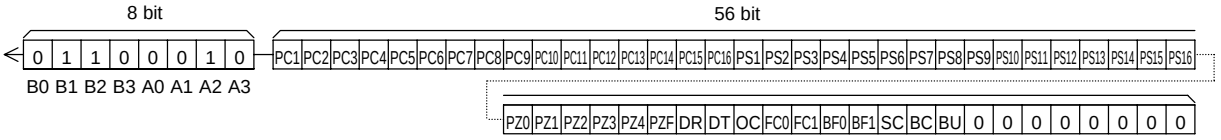
Note: After the above serial data is sent, the contents of the display data can be changed by transferring only the serial data (CCB addresses, display data, fixed data, and direction data) including the display data to be changed in 40-bit units.

(2) 1/3 duty

- When 97 or more segments are used
  All 424 bits of serial data (including CCB addresses) must be sent.



- When fewer than 97 segments are used
  Depending on the number of segments used, 104 bits, 144 bits, 184 bits, 224 bits, 264 bits, 304 bits, 344 bits or 384 bits (including the CCB address) must be sent as serial data. However, the serial data (control data) shown in the figure below must be sent without fail.



Note: After the above serial data is sent, the contents of the display data can be changed by transferring only the serial data (CCB addresses, display data, fixed data, and direction data) including the display data to be changed in 40-bit units.

Control Data Functions

1. PC1 to PC16: General-purpose output port state setting data

This control data is used to set the "H" and "L" status of general-purpose output ports P1 to P16.

Output pin	P1	P2	P3	P4	P5	P6	P7	P8
Control data	PC1	PC2	PC3	PC4	PC5	PC6	PC7	PC8

Output pin	P9	P10	P11	P12	P13	P14	P15	P16
Control data	PC9	PC10	PC11	PC12	PC13	PC14	PC15	PC16

Notes: PCn = "1": "H" (V_{LCD}) is output from output pin Pn (n = 1 to 16).
PCn = "0": "L" (V_{SS}) is output from output pin Pn (n = 1 to 16).

If, for instance, output pins S4/P4 and S5/P5 have been selected as the general-purpose output ports at PC4 = "1" and PC5 = "0", "H" (V_{LCD}) is output from output pin P4 and "L" (V_{SS}) is output from output pin P5.

2. PS1 to PS16: Segment output port/general-purpose output port switching control data

This control data is used to switch between segment output ports and general-purpose output ports for the S1/P1 to S16/P16 output pins.

Output pin	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8
Control data	PS1	PS2	PS3	PS4	PS5	PS6	PS7	PS8

Output pin	S9/P9	S10/P10	S11/P11	S12/P12	S13/P13	S14/P14	S15/P15	S16/P16
Control data	PS9	PS10	PS11	PS12	PS13	PS14	PS15	PS16

Notes: PSn = "1": General-purpose output port Pn is selected for output pin Sn/Pn (n = 1 to 16).
PSn = "0": Segment output port Sn is selected for output pin Sn/Pn (n = 1 to 16).

If, for instance, PS1 to PS3 = "0", PS4, PS5 = "1" and PS6 to PS16 = "0", general-purpose output ports are selected for output pins S4/P4 and S5/P5 and segment output ports are selected for output pins S1/P1 to S3/P3 and S6/P6 to S16/P16.

3. PZ0 to PZ4: Buzzer control signal output selection data

This control data is used to select the general-purpose output ports from which the buzzer control signals (square waves with a 50% duty ratio) are output.

Control data					General-purpose output ports from which buzzer control signals are output
PZ0	PZ1	PZ2	PZ3	PZ4	
1	0	0	0	0	P1
0	1	0	0	0	P2
1	1	0	0	0	P3
0	0	1	0	0	P4
1	0	1	0	0	P5
0	1	1	0	0	P6
1	1	1	0	0	P7
0	0	0	1	0	P8

Control data					General-purpose output ports from which buzzer control signals are output
PZ0	PZ1	PZ2	PZ3	PZ4	
1	0	0	1	0	P9
0	1	0	1	0	P10
1	1	0	1	0	P11
0	0	1	1	0	P12
1	0	1	1	0	P13
0	1	1	1	0	P14
1	1	1	1	0	P15
0	0	0	0	1	P16

Note: Data other than the data listed above must be set if the buzzer control signals are not to be output.
For example, set (PZ0, PZ1, PZ2, PZ3, PZ4) = (0, 0, 0, 0, 0).

4. PZF: Buzzer control signal frequency setting control data

This control data bit sets the frequency of the buzzer control signals (square waves with a 50% duty ratio).

PZF	Buzzer control signal frequency fz [Hz]
0	fosc/144, f_{CK}/16
1	fosc/72, f_{CK}/8

Note: fosc: Internal oscillation frequency (295 [kHz] typ.), f_{CK}: External clock operating frequency (32.8 [kHz] typ.)

5. DR: 1/3 bias drive or 1/2 bias drive switching control data
   This control data bit selects either 1/3 bias drive or 1/2 bias drive.

DR	Bias drive scheme
0	1/3 bias drive
1	1/2 bias drive

6. DT: 1/4 duty drive or 1/3 duty drive switching control data
   This control data bit selects either 1/4 duty drive or 1/3 duty drive.

DT	Duty drive scheme	Output pin (COM4/S35) status
0	1/4 duty drive	COM4 (common output)
1	1/3 duty drive	S35 (segment output)

7. OC: Internal oscillator operating mode/external clock operating mode switching control data
   This control data bit selects either internal oscillator operating mode or external clock operating mode.

OC	Basic clock operation mode	Input pin (OSCI) status
0	Internal oscillator operating mode	Must be connected to GND.
1	External clock operating mode	The clock signal (15 to 65 [kHz]) must be input from an external source.

8. FC0, FC1: Common/segment output waveform frame frequency setting control data
   These control data bits set the frame frequency for common and segment output waveforms.

Control data		Frame frequency fo [Hz]	
FC0	FC1	1/4 duty drive	1/3 duty drive
0	0	fosc/5760, f_{CK}/640	fosc/5670, f_{CK}/630
1	0	fosc/4608, f_{CK}/512	fosc/4536, f_{CK}/504
0	1	fosc/3456, f_{CK}/384	fosc/3402, f_{CK}/378
1	1	fosc/2304, f_{CK}/256	fosc/2268, f_{CK}/252

   Note: fosc: Internal oscillation frequency (295 [kHz] typ.), f_{CK}: External clock operating frequency (32.8 [kHz] typ.)

9. BF0, BF1: Segment blinking frequency setting control data
   Theses control data bits control the segment blinking frequency.

Control data		Segment blinking frequency fb [Hz]
BF0	BF1	
0	0	fosc/184320, f_{CK}/20480
1	0	fosc/147456, f_{CK}/16384
0	1	fosc/110592, f_{CK}/12288
1	1	fosc/73728, f_{CK}/8192

   Note: fosc: Internal oscillation frequency (295 [kHz] typ.), f_{CK}: External clock operating frequency (32.8 [kHz] typ.)

10. SC: Segment on/off control data
    This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

    Note that when the segments are turned off by setting SC to “1”, the segments are turned off by outputting segment off waveforms from the segment output pins.

11. BC: LCD drive bias voltage generation divider resistor current on/off control data
    This control data is used to turn on/off the current to the LCD drive bias voltage generation divider resistors.

BC	LCD drive bias voltage generation divider resister state
0	Turns on current to the divider resistors.
1	Turns off current to the divider resistors.

12. BU: Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power-saving mode (In internal oscillator operating mode (OC = “0”), the oscillation of the internal oscillation circuit is stopped; in external clock operating mode (OC = “1”), the acceptance of the external clock is stopped. The common or segment output pins go to the V_{SS} level. In addition, the current to the LCD drive bias voltage generation divider resistors is turned off. However, the output pins S1/P1 to S16/P16 can be used as general-purpose output ports (the output of a buzzer control signal is impossible.) under the control of control data bits PS1 to PS16.)

Display Data and Output Pin Correspondence

1. 1/4 duty

Output pin	COM1		COM2		COM3		COM4	
S1/P1	D1	D2	D3	D4	D5	D6	D7	D8
S2/P2	D9	D10	D11	D12	D13	D14	D15	D16
S3/P3	D17	D18	D19	D20	D21	D22	D23	D24
S4/P4	D25	D26	D27	D28	D29	D30	D31	D32
S5/P5	D33	D34	D35	D36	D37	D38	D39	D40
S6/P6	D41	D42	D43	D44	D45	D46	D47	D48
S7/P7	D49	D50	D51	D52	D53	D54	D55	D56
S8/P8	D57	D58	D59	D60	D61	D62	D63	D64
S9/P9	D65	D66	D67	D68	D69	D70	D71	D72
S10/P10	D73	D74	D75	D76	D77	D78	D79	D80
S11/P11	D81	D82	D83	D84	D85	D86	D87	D88
S12/P12	D89	D90	D91	D92	D93	D94	D95	D96
S13/P13	D97	D98	D99	D100	D101	D102	D103	D104
S14/P14	D105	D106	D107	D108	D109	D110	D111	D112
S15/P15	D113	D114	D115	D116	D117	D118	D119	D120
S16/P16	D121	D122	D123	D124	D125	D126	D127	D128
S17	D129	D130	D131	D132	D133	D134	D135	D136
S18	D137	D138	D139	D140	D141	D142	D143	D144
S19	D145	D146	D147	D148	D149	D150	D151	D152
S20	D153	D154	D155	D156	D157	D158	D159	D160
S21	D161	D162	D163	D164	D165	D166	D167	D168
S22	D169	D170	D171	D172	D173	D174	D175	D176
S23	D177	D178	D179	D180	D181	D182	D183	D184
S24	D185	D186	D187	D188	D189	D190	D191	D192
S25	D193	D194	D195	D196	D197	D198	D199	D200
S26	D201	D202	D203	D204	D205	D206	D207	D208
S27	D209	D210	D211	D212	D213	D214	D215	D216
S28	D217	D218	D219	D220	D221	D222	D223	D224
S29	D225	D226	D227	D228	D229	D230	D231	D232
S30	D233	D234	D235	D236	D237	D238	D239	D240
S31	D241	D242	D243	D244	D245	D246	D247	D248
S32	D249	D250	D251	D252	D253	D254	D255	D256
S33	D257	D258	D259	D260	D261	D262	D263	D264
S34	D265	D266	D267	D268	D269	D270	D271	D272

Note: The applies to the case where the S1/P1 to S16/P16 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S11 output pin.

Display data								Segment output pin (S11) state
D81	D82	D83	D84	D85	D86	D87	D88	
0	0	0	0	0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
1	0	1	0	1	0	1	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.
X	1	X	1	X	1	X	1	The LCD segments for COM1, COM2, COM3, and COM4 are blinking.
1	0	0	0	0	0	0	0	The LCD segment corresponding to COM1 is on. The LCD segments corresponding to COM2, COM3, and COM4 are off.
X	1	0	0	0	0	0	0	The LCD segment for COM1 is blinking. The LCD segments corresponding to COM2, COM3, and COM4 are off.
0	0	1	0	0	0	0	0	The LCD segment corresponding to COM2 is on. The LCD segments corresponding to COM1, COM3, and COM4 are off.
0	0	X	1	0	0	0	0	The LCD segment for COM2 is blinking. The LCD segments corresponding to COM1, COM3, and COM4 are off.
0	0	0	0	1	0	0	0	The LCD segment corresponding to COM3 is on. The LCD segments corresponding to COM1, COM2, and COM4 are off.
0	0	0	0	X	1	0	0	The LCD segment for COM3 is blinking. The LCD segments corresponding to COM1, COM2, and COM4 are off.
0	0	0	0	0	0	1	0	The LCD segment corresponding to COM4 is on. The LCD segments corresponding to COM1, COM2, and COM3 are off.
0	0	0	0	0	0	X	1	The LCD segment for COM4 is blinking. The LCD segments corresponding to COM1, COM2, and COM3 are off.
1	0	1	0	0	0	0	0	The LCD segments corresponding to COM1 and COM2 are on. The LCD segments corresponding to COM3 and COM4 are off.
0	0	1	0	1	0	0	0	The LCD segments corresponding to COM2 and COM3 are on. The LCD segments corresponding to COM1 and COM4 are off.
0	0	0	0	1	0	1	0	The LCD segments corresponding to COM3 and COM4 are on. The LCD segments corresponding to COM1 and COM2 are off.
1	0	0	0	0	0	1	0	The LCD segments corresponding to COM1 and COM4 are on. The LCD segments corresponding to COM2 and COM3 are off.
1	0	X	1	0	0	0	0	The LCD segment corresponding to COM1 is on. The LCD segment for COM2 is blinking. The LCD segments corresponding to COM3 and COM4 are off.
0	0	1	0	X	1	0	0	The LCD segment corresponding to COM2 is on. The LCD segment for COM3 is blinking. The LCD segments corresponding to COM1 and COM4 are off.
0	0	0	0	1	0	X	1	The LCD segment corresponding to COM3 is on. The LCD segment for COM4 is blinking. The LCD segments corresponding to COM1 and COM2 are off.
X	1	0	0	0	0	1	0	The LCD segment corresponding to COM4 is on. The LCD segment for COM1 is blinking. The LCD segments corresponding to COM2 and COM3 are off.

Note: X: don’t care

2. 1/3 duty

Output pin	COM1		COM2		COM3	
S1/P1	D1	D2	D3	D4	D5	D6
S2/P2	D7	D8	D9	D10	D11	D12
S3/P3	D13	D14	D15	D16	D17	D18
S4/P4	D19	D20	D21	D22	D23	D24
S5/P5	D25	D26	D27	D28	D29	D30
S6/P6	D31	D32	D33	D34	D35	D36
S7/P7	D37	D38	D39	D40	D41	D42
S8/P8	D43	D44	D45	D46	D47	D48
S9/P9	D49	D50	D51	D52	D53	D54
S10/P10	D55	D56	D57	D58	D59	D60
S11/P11	D61	D62	D63	D64	D65	D66
S12/P12	D67	D68	D69	D70	D71	D72
S13/P13	D73	D74	D75	D76	D77	D78
S14/P14	D79	D80	D81	D82	D83	D84
S15/P15	D85	D86	D87	D88	D89	D90
S16/P16	D91	D92	D93	D94	D95	D96
S17	D97	D98	D99	D100	D101	D102
S18	D103	D104	D105	D106	D107	D108
S19	D109	D110	D111	D112	D113	D114
S20	D115	D116	D117	D118	D119	D120
S21	D121	D122	D123	D124	D125	D126
S22	D127	D128	D129	D130	D131	D132
S23	D133	D134	D135	D136	D137	D138
S24	D139	D140	D141	D142	D143	D144
S25	D145	D146	D147	D148	D149	D150
S26	D151	D152	D153	D154	D155	D156
S27	D157	D158	D159	D160	D161	D162
S28	D163	D164	D165	D166	D167	D168
S29	D169	D170	D171	D172	D173	D174
S30	D175	D176	D177	D178	D179	D180
S31	D181	D182	D183	D184	D185	D186
S32	D187	D188	D189	D190	D191	D192
S33	D193	D194	D195	D196	D197	D198
S34	D199	D200	D201	D202	D203	D204
S35/COM4	D205	D206	D207	D208	D209	D210

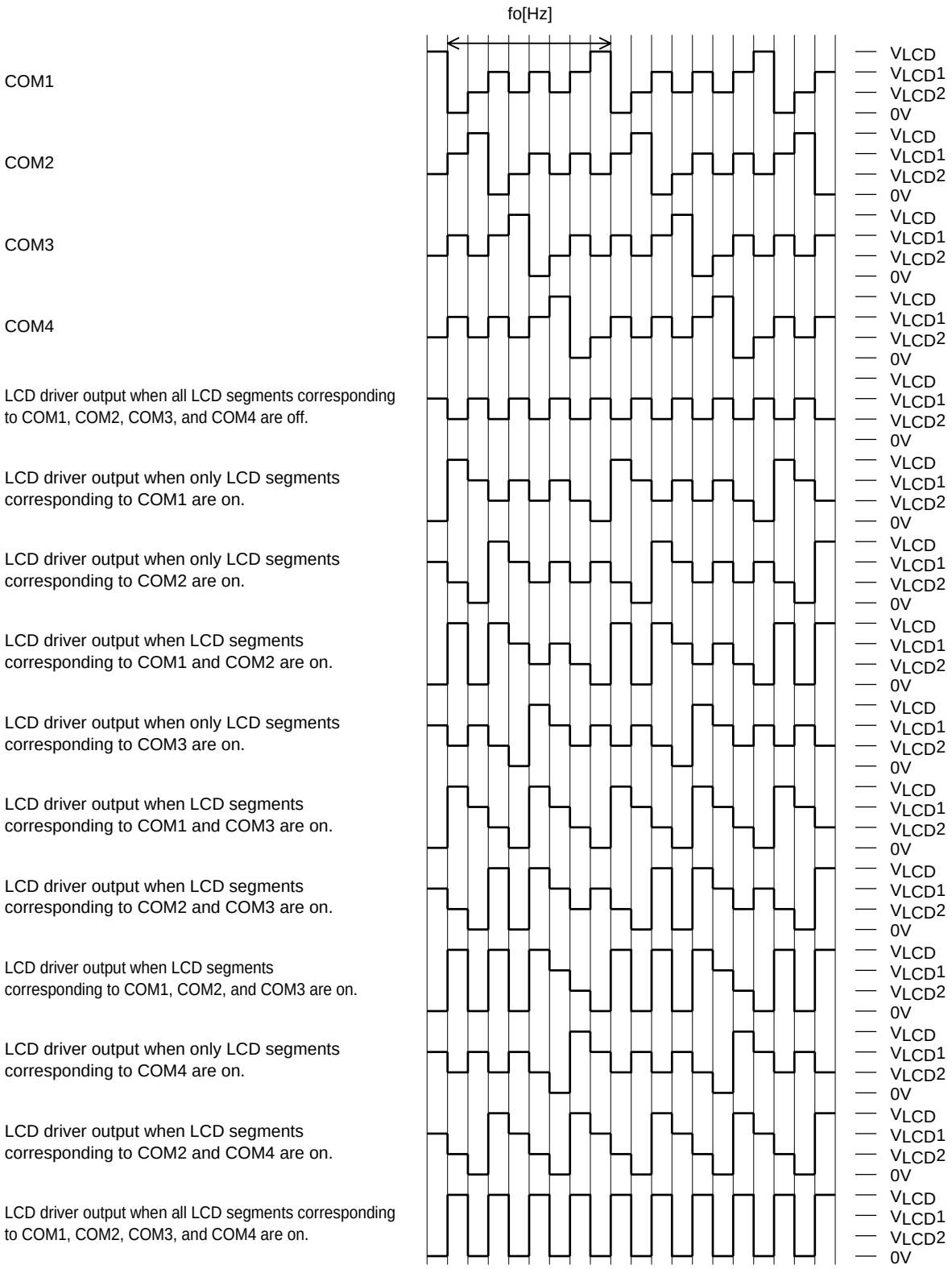
Note: The applies to the case where the S1/P1 to S16/P16 and S35/COM4 output pins are set to be segment output ports.

For example, the table below lists the segment output states for the S11 output pin.

Display data						Segment output pin (S11) state
D61	D62	D63	D64	D65	D66	
0	0	0	0	0	0	The LCD segments corresponding to COM1, COM2, and COM3 are off.
1	0	1	0	1	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
X	1	X	1	X	1	The LCD segments for COM1, COM2, and COM3 are blinking.
1	0	0	0	0	0	The LCD segment corresponding to COM1 is on. The LCD segments corresponding to COM2 and COM3 are off.
X	1	0	0	0	0	The LCD segment for COM1 is blinking. The LCD segments corresponding to COM2 and COM3 are off.
0	0	1	0	0	0	The LCD segment corresponding to COM2 is on. The LCD segments corresponding to COM1 and COM3 are off.
0	0	X	1	0	0	The LCD segment for COM2 is blinking. The LCD segments corresponding to COM1 and COM3 are off.
0	0	0	0	1	0	The LCD segment corresponding to COM3 is on. The LCD segments corresponding to COM1 and COM2 are off.
0	0	0	0	X	1	The LCD segment for COM3 is blinking. The LCD segments corresponding to COM1 and COM2 are off.
1	0	1	0	0	0	The LCD segments corresponding to COM1 and COM2 are on. The LCD segment corresponding to COM3 is off.
0	0	1	0	1	0	The LCD segments corresponding to COM2 and COM3 are on. The LCD segment corresponding to COM1 is off.
1	0	0	0	1	0	The LCD segments corresponding to COM1 and COM3 are on. The LCD segment corresponding to COM2 is off.
1	0	X	1	0	0	The LCD segment corresponding to COM1 is on. The LCD segment for COM2 is blinking. The LCD segment corresponding to COM3 is off.
0	0	1	0	X	1	The LCD segment corresponding to COM2 is on. The LCD segment for COM3 is blinking. The LCD segment corresponding to COM1 is off.
X	1	0	0	1	0	The LCD segment corresponding to COM3 is on. The LCD segment for COM1 is blinking. The LCD segment corresponding to COM2 is off.

Note: X: don’t care

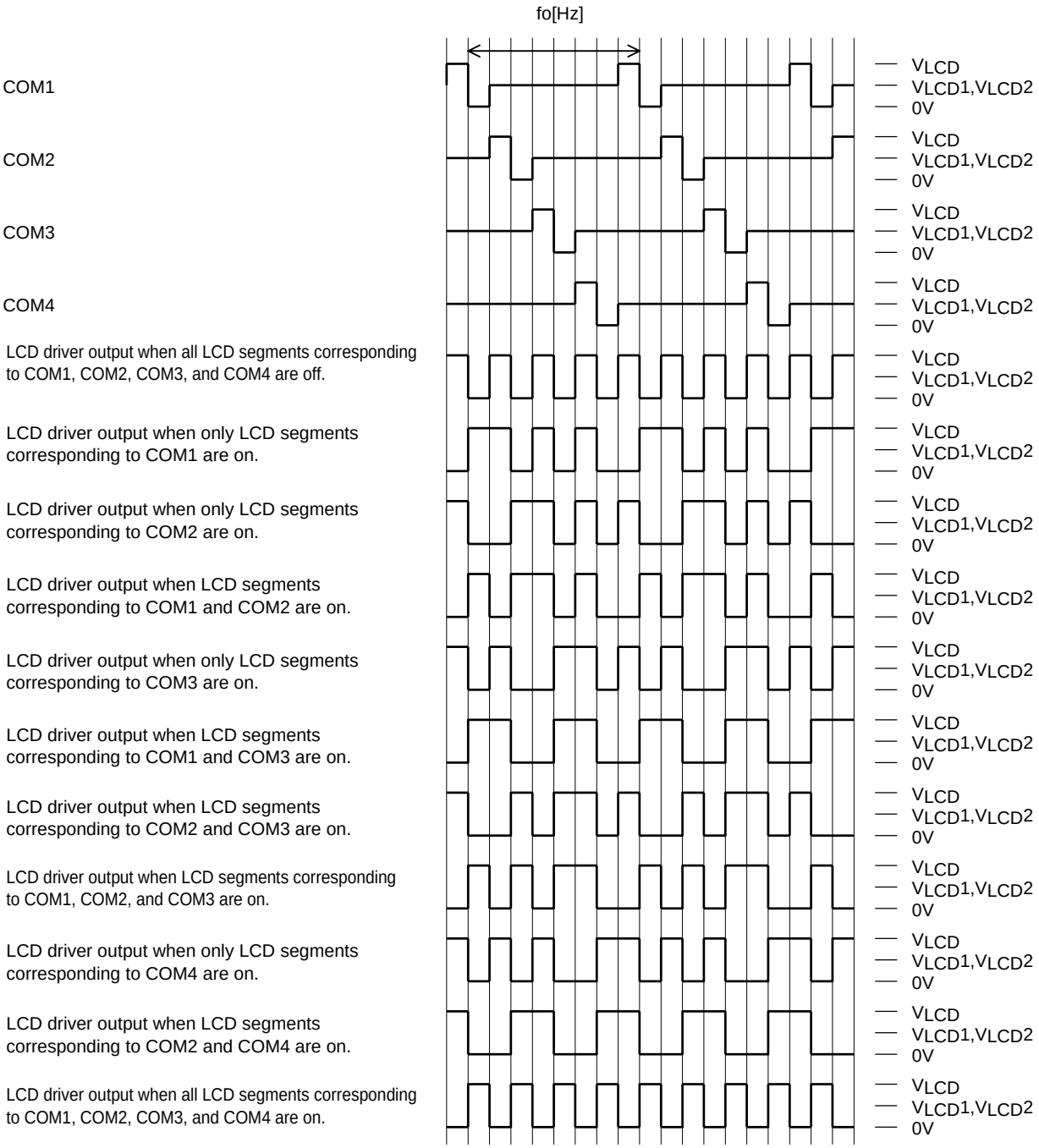
Output Waveforms (1/4-Duty 1/3-Bias Drive Scheme)



Control data		Frame frequency fo [Hz]
FC0	FC1	
0	0	fosc/5760, f_{CK}/640
1	0	fosc/4608, f_{CK}/512
0	1	fosc/3456, f_{CK}/384
1	1	fosc/2304, f_{CK}/256

Note: fosc: Internal oscillation frequency (295 [kHz] typ.), f_{CK}: External clock operating frequency (32.8 [kHz] typ.)

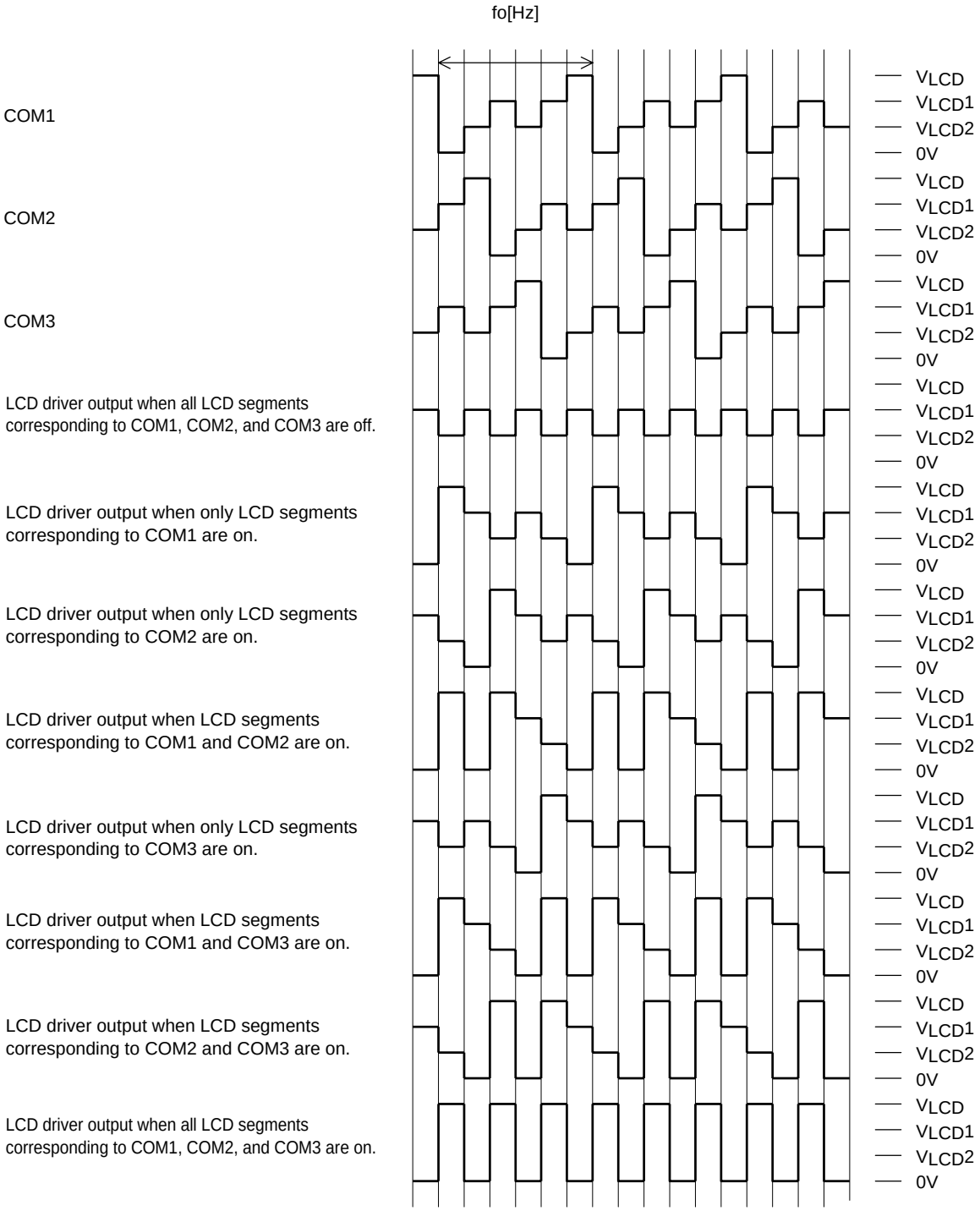
Output Waveforms (1/4-Duty 1/2-Bias Drive Scheme)



Control data		Frame frequency fo [Hz]
FC0	FC1	
0	0	fosc/5760, f_{CK}/640
1	0	fosc/4608, f_{CK}/512
0	1	fosc/3456, f_{CK}/384
1	1	fosc/2304, f_{CK}/256

Note: fosc: Internal oscillation frequency (295 [kHz] typ.), f_{CK}: External clock operating frequency (32.8 [kHz] typ.)

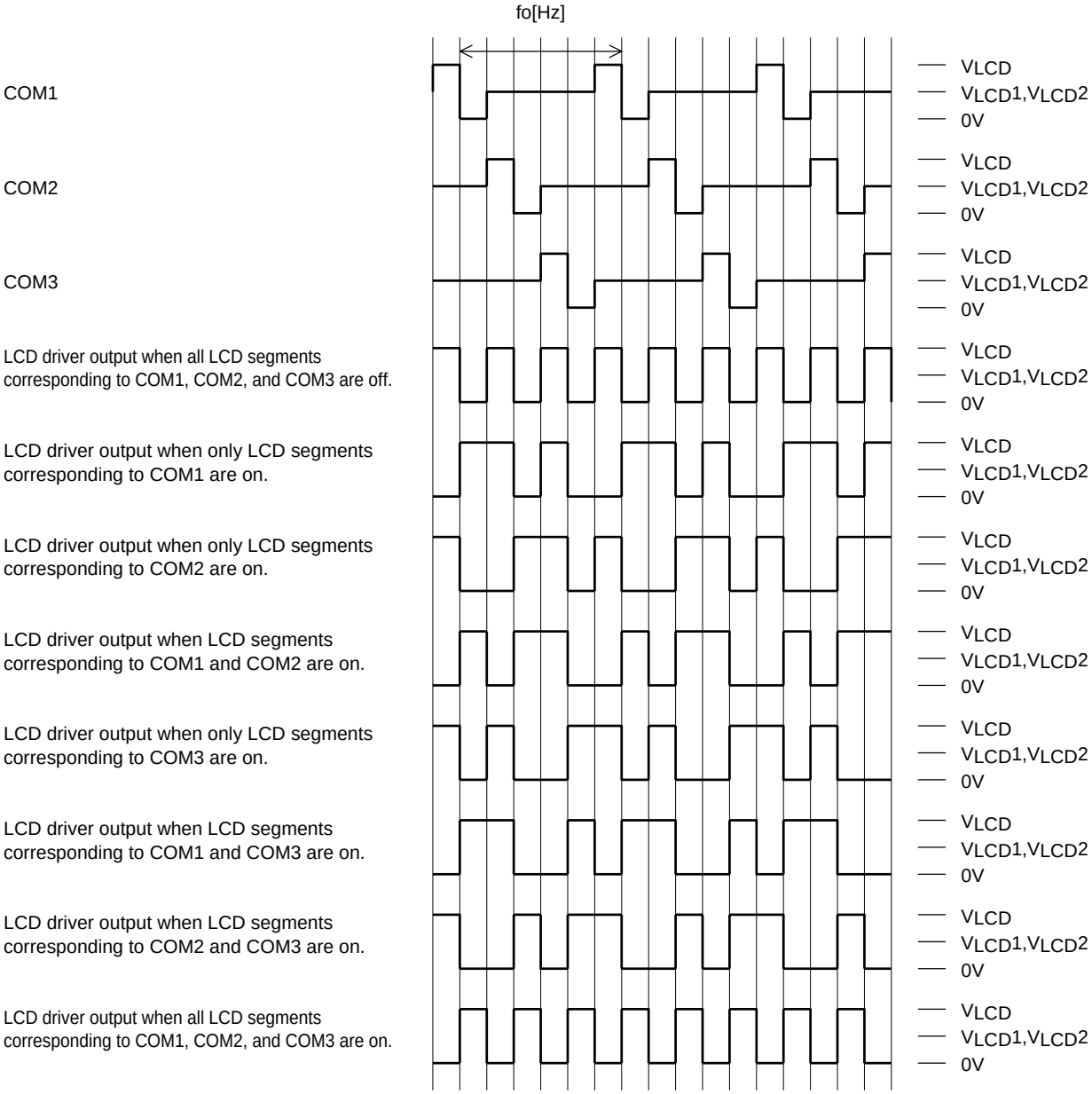
Output Waveforms (1/3-Duty 1/3-Bias Drive Scheme)



Control data		Frame frequency fo [Hz]
FC0	FC1	
0	0	fosc/5670, f_{CK}/630
1	0	fosc/4536, f_{CK}/504
0	1	fosc/3402, f_{CK}/378
1	1	fosc/2268, f_{CK}/252

Note: fosc: Internal oscillation frequency (295 [kHz] typ.), f_{CK}: External clock operating frequency (32.8 [kHz] typ.)

Output Waveforms (1/3-Duty 1/2-Bias Drive Scheme)



Control data		Frame frequency fo [Hz]
FC0	FC1	
0	0	fosc/5670, f_{CK}/630
1	0	fosc/4536, f_{CK}/504
0	1	fosc/3402, f_{CK}/378
1	1	fosc/2268, f_{CK}/252

Note: fosc: Internal oscillation frequency (295 [kHz] typ.), f_{CK}: External clock operating frequency (32.8 [kHz] typ.)

The $\overline{\text{INH}}$ pin and Display Control

Since the IC internal data (1/4 duty: the display data D1 to D272 and the control data, 1/3 duty: the display data D1 to D210 and the control data) is undefined when power is first applied, applications should set the $\overline{\text{INH}}$ pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S16/P16, S17 to S34, COM1 to COM3, and COM4/S35 to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{\text{INH}}$ pin high after the data transfer has completed. This procedure prevents meaningless displays at power on. (See Figures 5 and 6.)

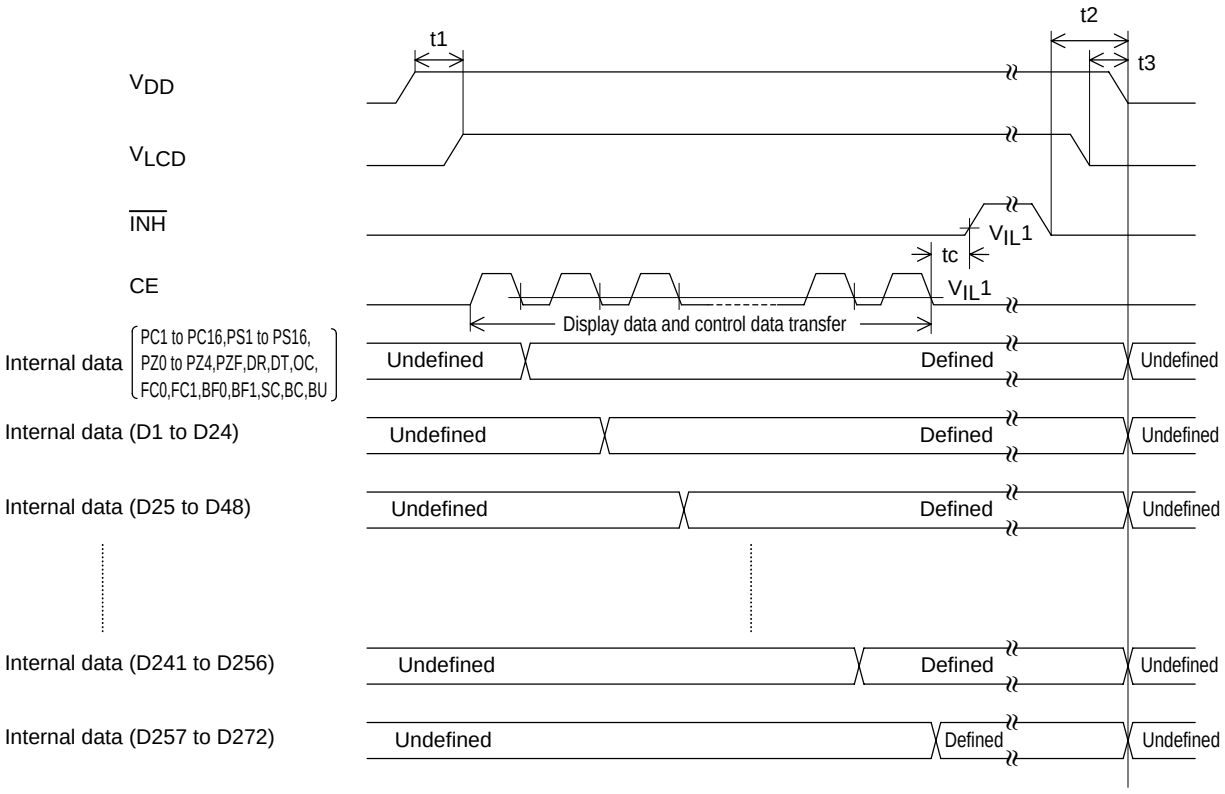
Notes on the Power On/Off Sequences

Applications should observe the following sequences when turning the LC75835W power on and off.
(See Figures 5 and 6)

- At power on: Logic block power supply (V_{DD}) on → LCD driver block power supply (V_{LCD}) on
- At power off: LCD driver block power supply (V_{LCD}) off → Logic block power supply (V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

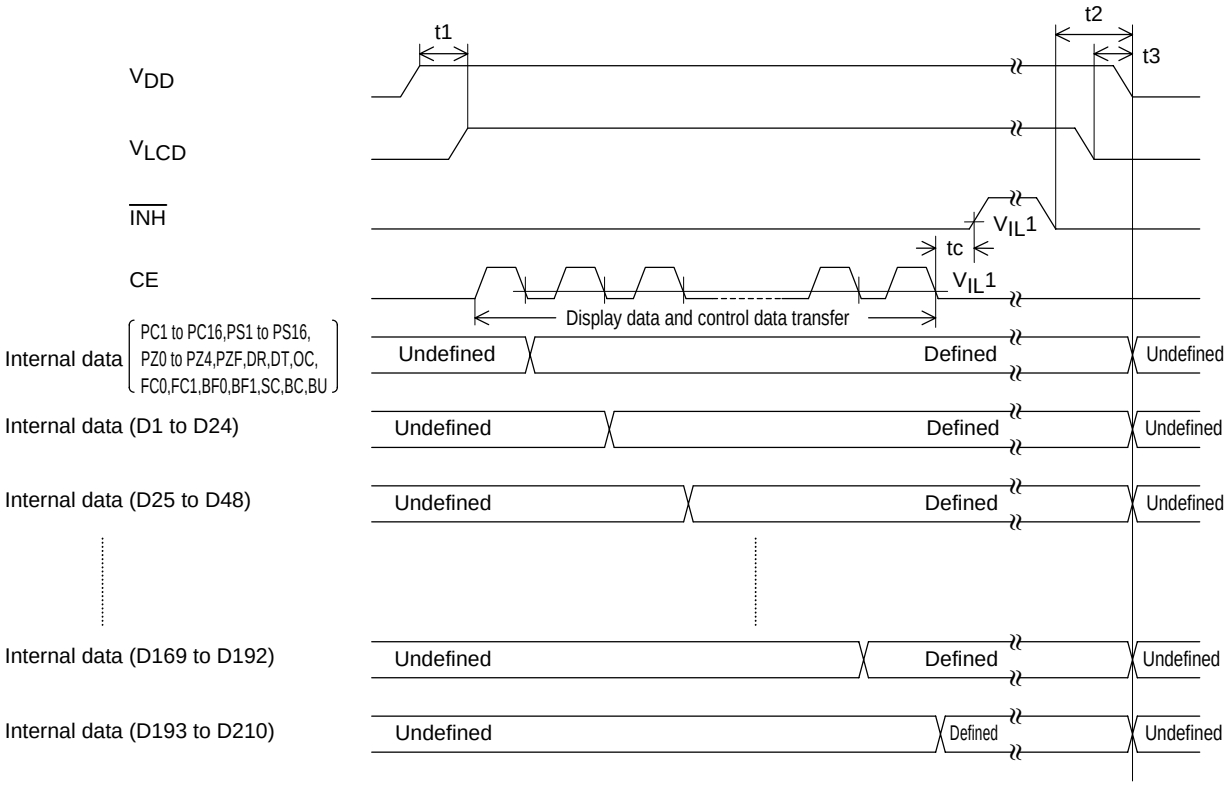
1. 1/4 duty



Note: t1≥0
t2>0
t3≥0 (t2>t3)
tc···10μs min

Figure 5

2. 1/3 duty



Note: t1≥0
t2>0
t3≥0 (t2>t3)
tc···10μs min

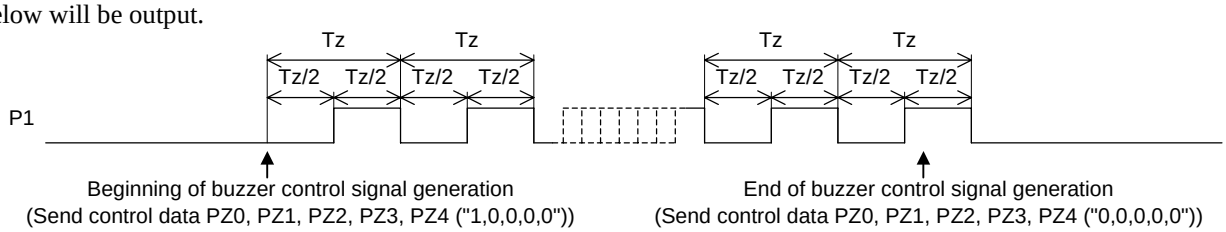
Figure 6

Notes on Controller Transfer of Display Data

Since the LC75835W accepts the display data (D1 to D272) divided into 12 separate transfer operations when using 1/4 duty drive scheme and data (D1 to D210) divided into 9 separate transfer operations when using 1/3 duty drive scheme, we recommend that the applications transfer all of the display data within a period of less than 30ms to prevent observable degradation of display quality.

Generation of Buzzer Control Signal

A square wave with a 50% duty ratio is output from the general-purpose output port selected for the output of the buzzer control signal between the start and end of the buzzer control signal output. If, for example, general-purpose output port P1 has been selected as the output of the buzzer control signal (PC1 = “0”, PS1 = “1”), the waveform shown below will be output.

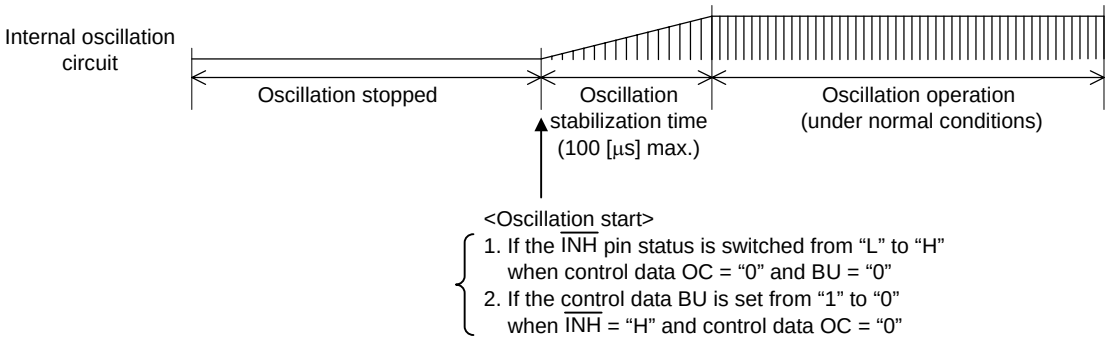


Control data PZF	Buzzer control signal frequency fz(=1/Tz)[Hz]
0	fosc/144, f_{CK}/16
1	fosc/72, f_{CK}/8

Note: fosc: Internal oscillation frequency (295 [kHz] typ.), f_{CK}: External clock operating frequency (32.8 [kHz] typ.)

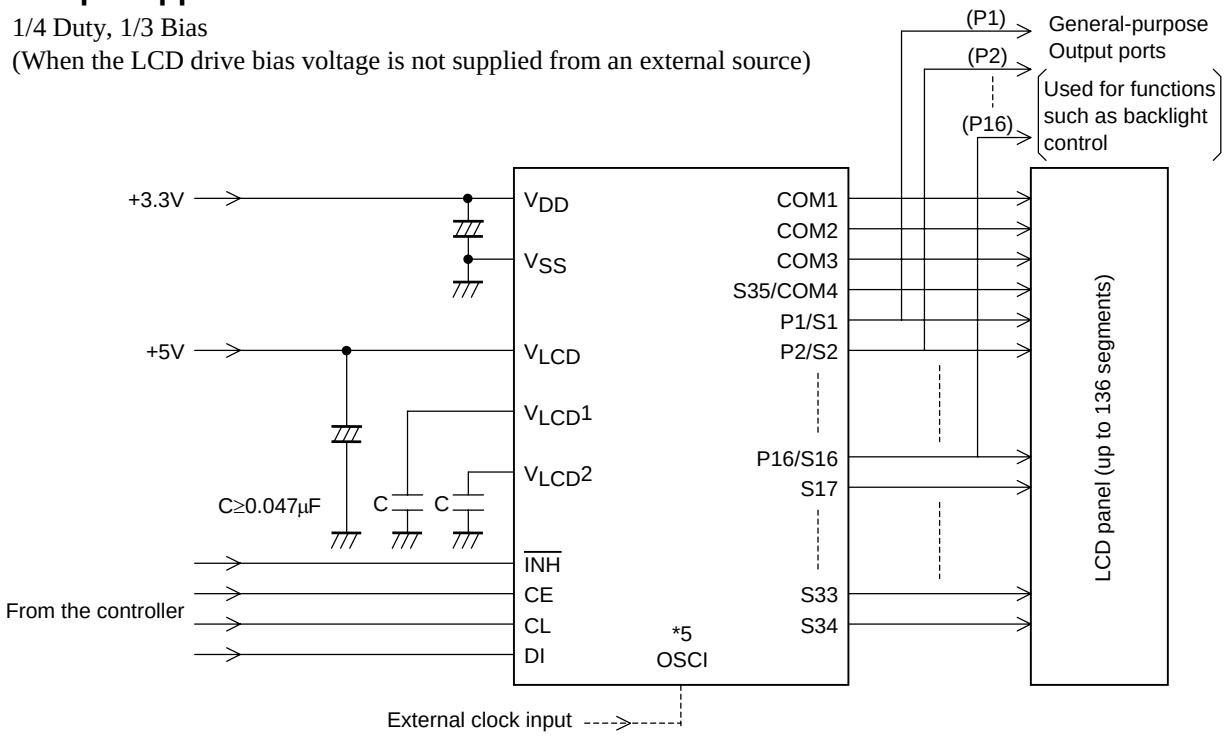
Oscillation Stabilization Time of the Internal Oscillation Circuit

It must be noted that the oscillation of the internal oscillation circuit is unstable for a maximum of 100μs (oscillation stabilization time) after oscillation has started.



Sample Application Circuit 1

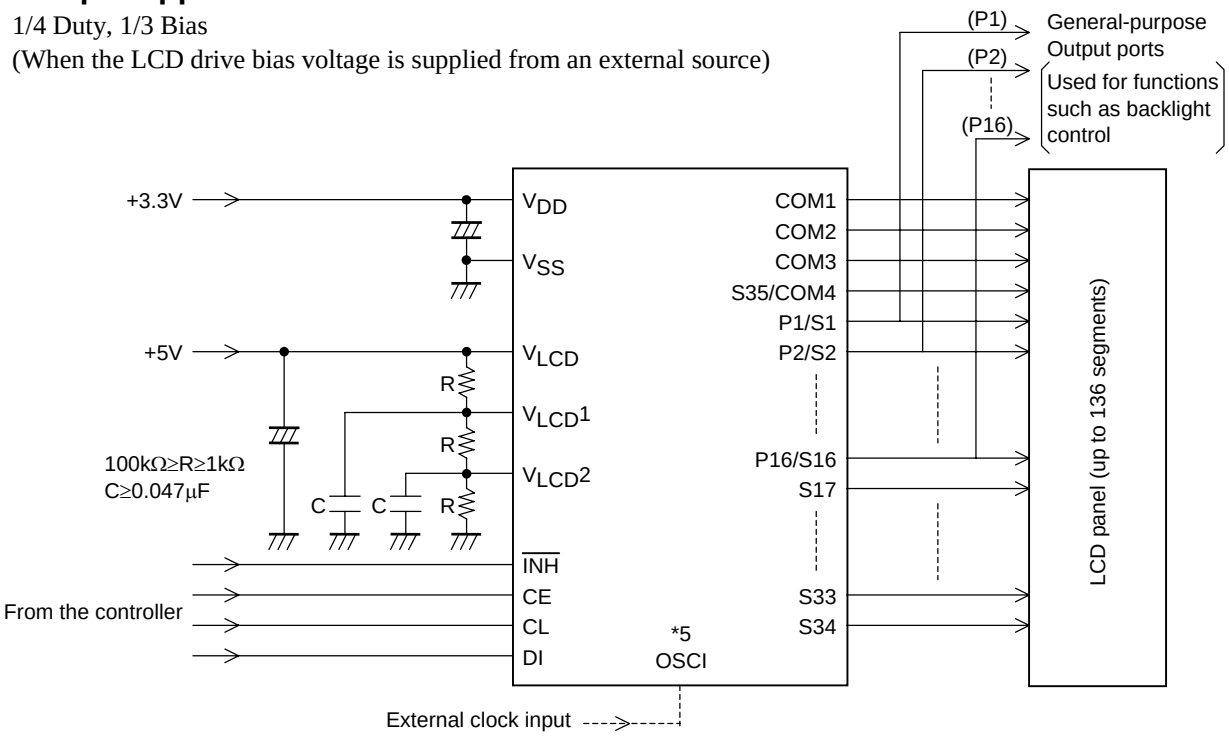
1/4 Duty, 1/3 Bias
(When the LCD drive bias voltage is not supplied from an external source)



*5: The OSCI pin must be connected to GND when the internal oscillator operating mode (OC = “0”) has been selected; the clock must be input from an external source when the external clock operating mode (OC = “1”) has been selected.
*6: Control data BC must be set to “0”.

Sample Application Circuit 2

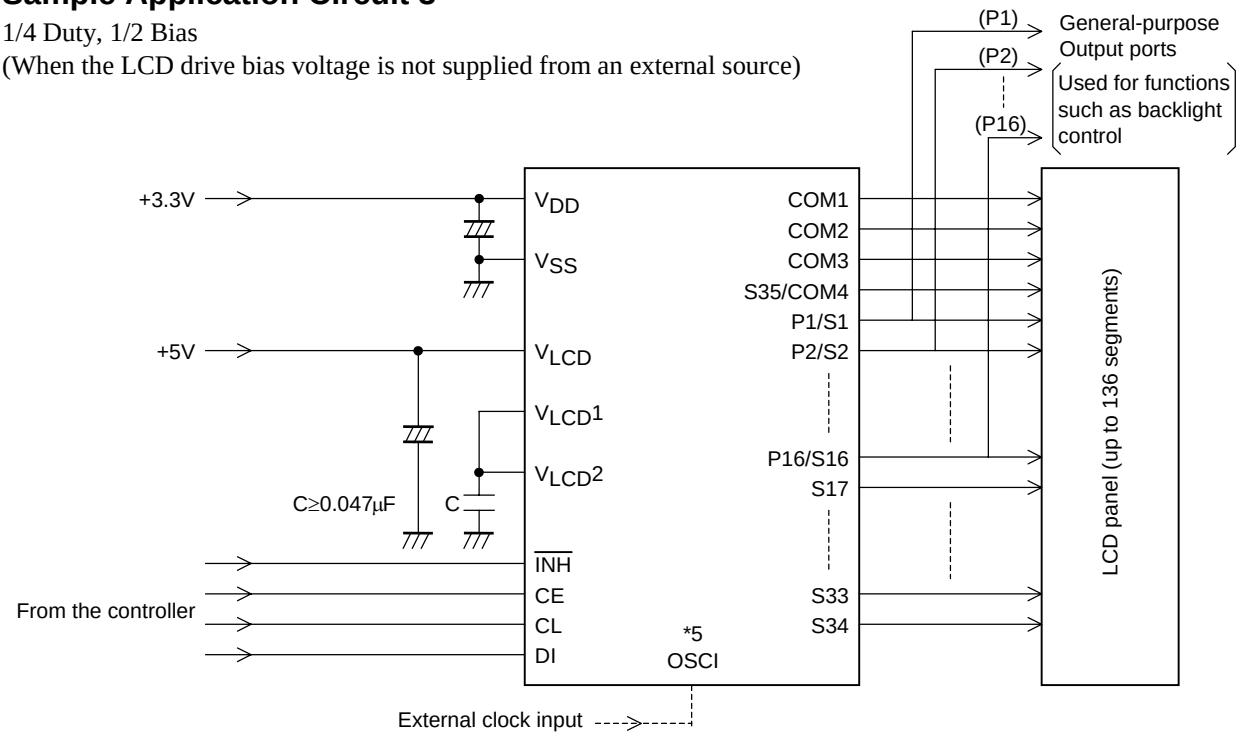
1/4 Duty, 1/3 Bias
(When the LCD drive bias voltage is supplied from an external source)



*5: The OSCI pin must be connected to GND when the internal oscillator operating mode (OC = “0”) has been selected; the clock must be input from an external source when the external clock operating mode (OC = “1”) has been selected.
*6: Control data BC must be set to “1”.

Sample Application Circuit 3

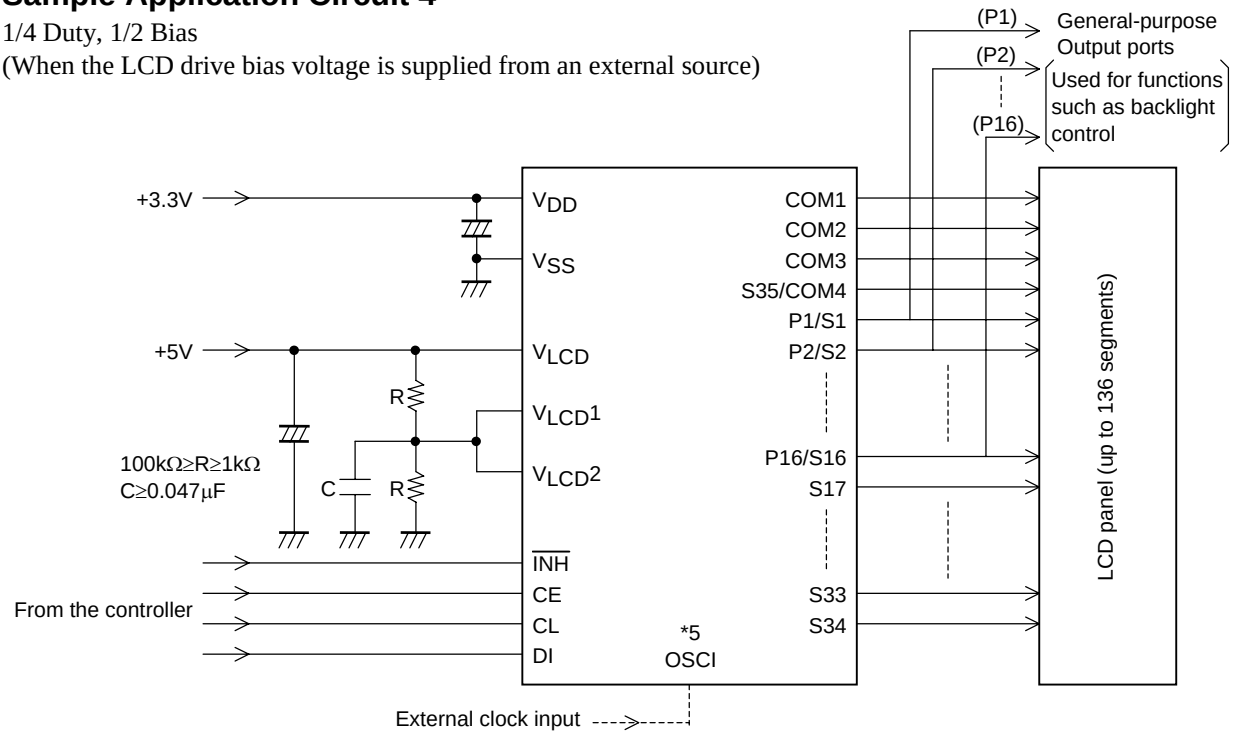
1/4 Duty, 1/2 Bias
(When the LCD drive bias voltage is not supplied from an external source)



*5: The OSCI pin must be connected to GND when the internal oscillator operating mode (OC = “0”) has been selected; the clock must be input from an external source when the external clock operating mode (OC = “1”) has been selected.
*6: Control data BC must be set to “0”.

Sample Application Circuit 4

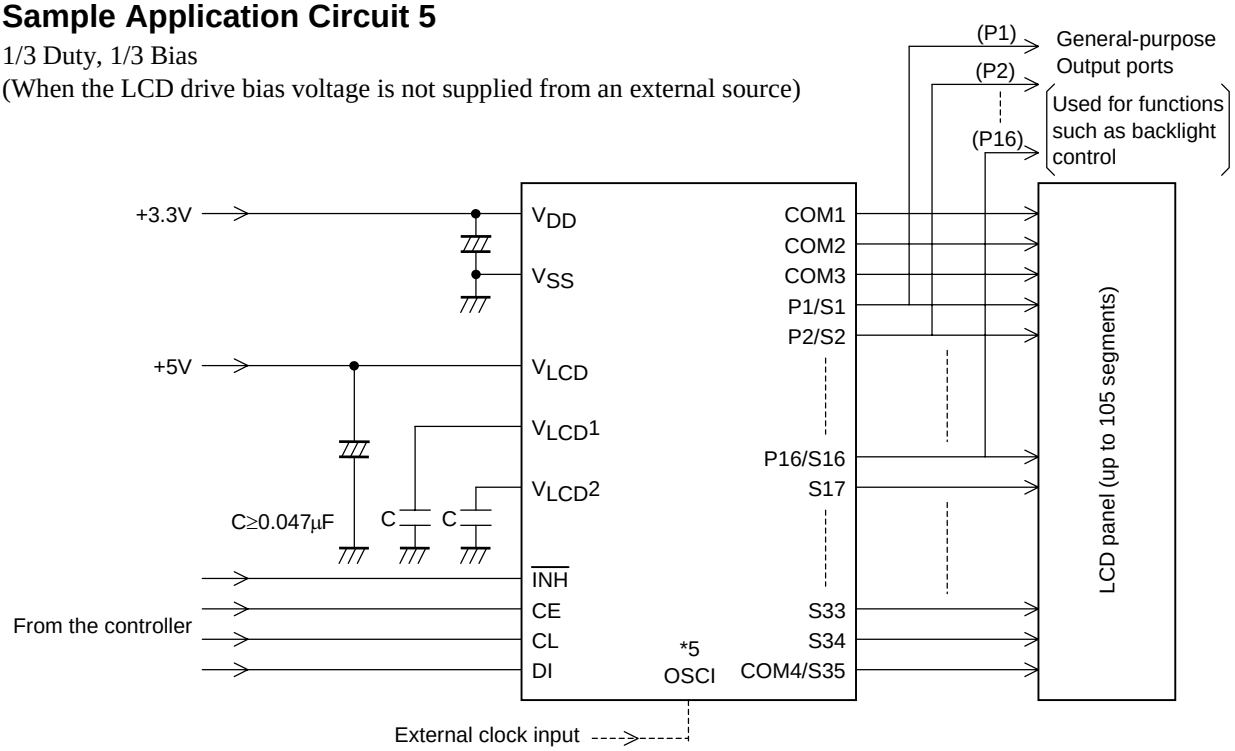
1/4 Duty, 1/2 Bias
(When the LCD drive bias voltage is supplied from an external source)



*5: The OSCI pin must be connected to GND when the internal oscillator operating mode (OC = “0”) has been selected; the clock must be input from an external source when the external clock operating mode (OC = “1”) has been selected.
*6: Control data BC must be set to “1”.

Sample Application Circuit 5

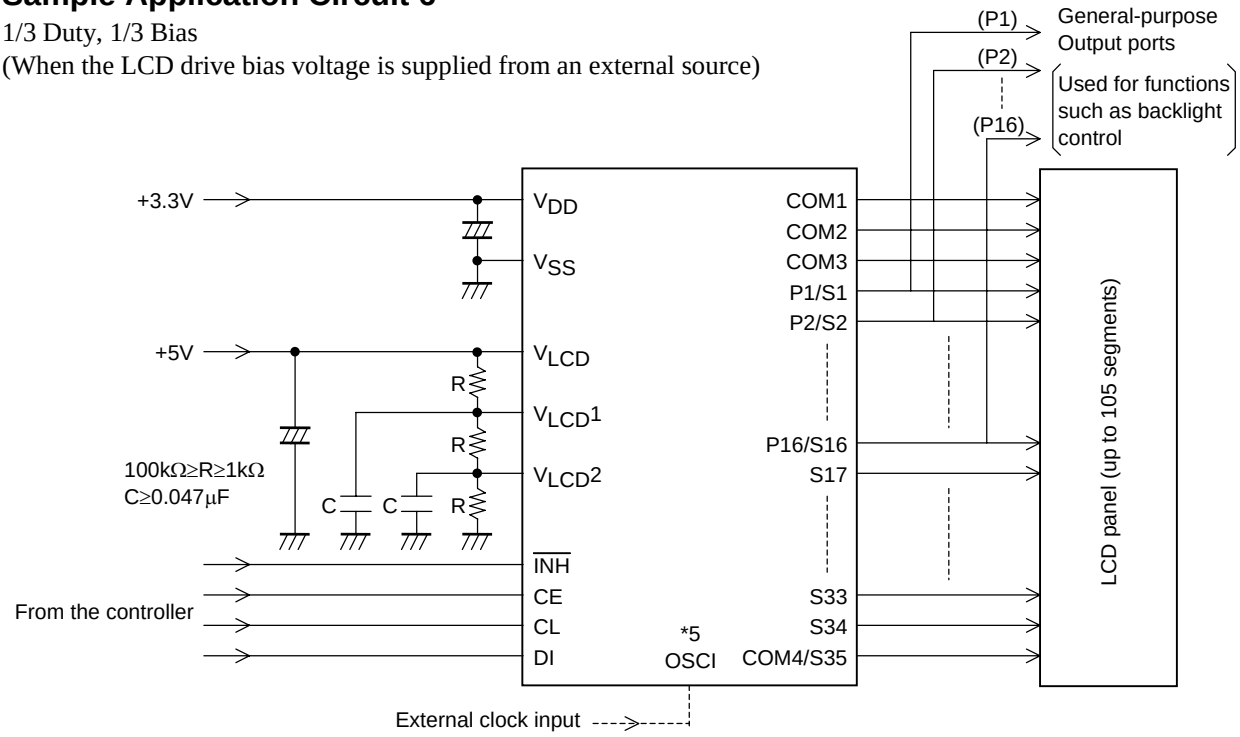
1/3 Duty, 1/3 Bias
(When the LCD drive bias voltage is not supplied from an external source)



*5: The OSCI pin must be connected to GND when the internal oscillator operating mode (OC = "0") has been selected; the clock must be input from an external source when the external clock operating mode (OC = "1") has been selected.
*6: Control data BC must be set to "0".

Sample Application Circuit 6

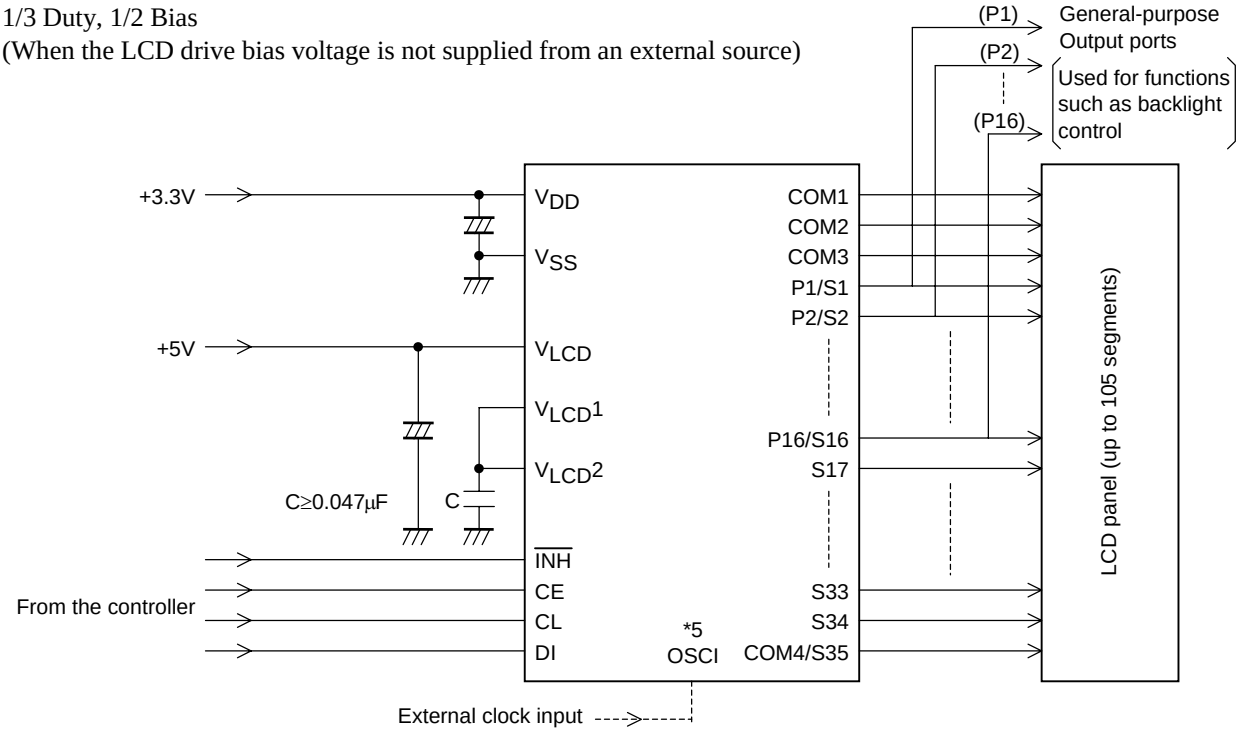
1/3 Duty, 1/3 Bias
(When the LCD drive bias voltage is supplied from an external source)



*5: The OSCI pin must be connected to GND when the internal oscillator operating mode (OC = "0") has been selected; the clock must be input from an external source when the external clock operating mode (OC = "1") has been selected.
*6: Control data BC must be set to "1".

Sample Application Circuit 7

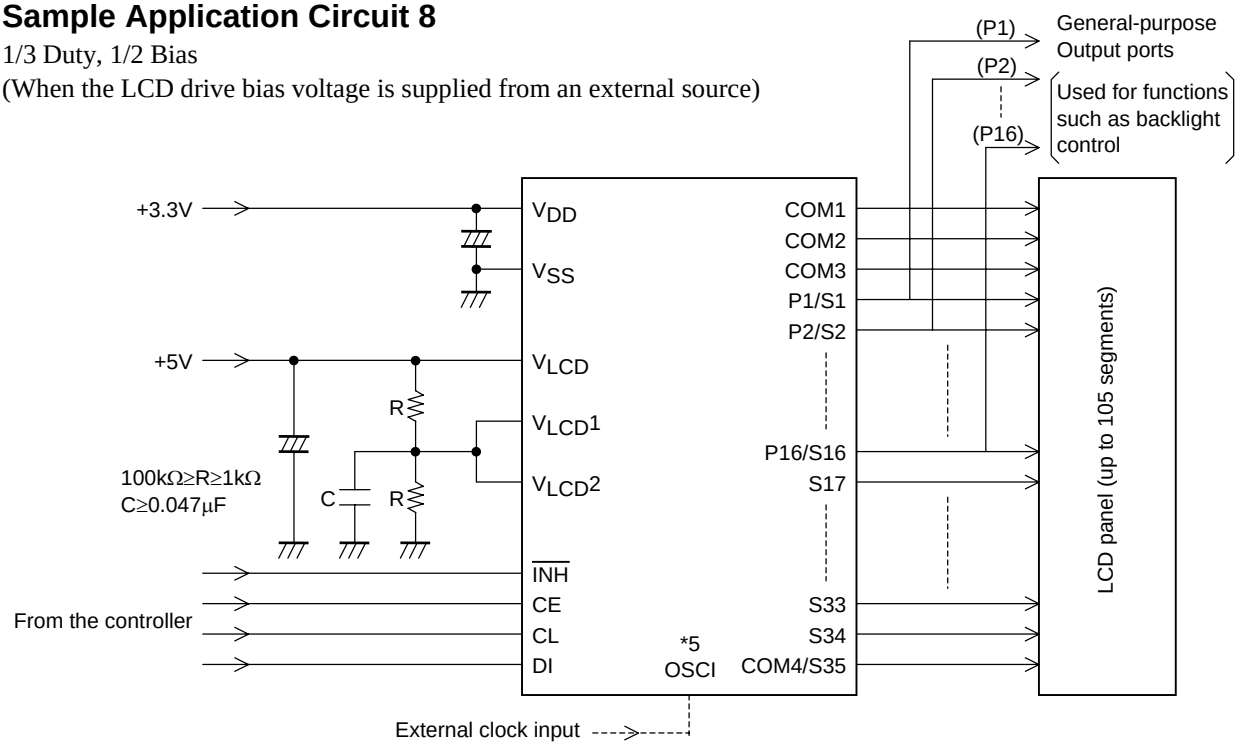
1/3 Duty, 1/2 Bias
(When the LCD drive bias voltage is not supplied from an external source)



*5: The OSCI pin must be connected to GND when the internal oscillator operating mode (OC = “0”) has been selected; the clock must be input from an external source when the external clock operating mode (OC = “1”) has been selected.
*6: Control data BC must be set to “0”.

Sample Application Circuit 8

1/3 Duty, 1/2 Bias
(When the LCD drive bias voltage is supplied from an external source)



*5: The OSCI pin must be connected to GND when the internal oscillator operating mode (OC = “0”) has been selected; the clock must be input from an external source when the external clock operating mode (OC = “1”) has been selected.
*6: Control data BC must be set to “1”.

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