LC75700T

Key Scanning IC

ON Semiconductor®

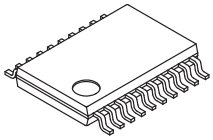
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Overview

The LC75700T is a key scanning LSI that accepts input from up to 30 keys and can control up to four general purpose output ports. Therefore it can reduce the number of lines to the front panel in application systems.

Features

- Key input function for up to 30 keys.
- General-purpose output ports for up to four pins.
- A key scan is performed only when a key is pressed, and thus power dissipation is reduced.
- Serial data I/O supports CCB* format communication with the system controller.
- Switching between the key scan output port and general purpose output port functions can be controlled by the control data.
- The $\overline{\text{RES}}$ pin is provided. This pin disables key scanning, and forces the general-purpose output ports to the low level.
- RC oscillator circuit



TSSOP20 4.4x6.5 / TSSOP20 (225 mil)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75700T-MPB-E	TSSOP20(225mil) (Pb-Free)	70 / Fan-Fold
LC75700T-TLM-E	TSSOP20(225mil) (Pb-Free)	2000 / Tape &Reel
LC75700TS-MPB-E	TSSOP20(225mil) (Pb-Free)	70 / Fan-Fold
LC75700TS-TLM-E	TSSOP20(225mil) (Pb-Free)	2000 / Tape &Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

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Publication Order Number :
LC75700T/D

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{IN}1	CE, CL, DI, $\overline{RES}$	–0.3 to +7.0	V
	V_{IN}2	OSC, KI1 to KI5	–0.3 to V_{DD} + 0.3	
Output voltage	V_{OUT}1	DO	–0.3 to +7.0	V
	V_{OUT}2	OSC, KS1 to KS6, P1 to P4	–0.3 to V_{DD} + 0.3	
Output current	I_{OUT}1	KS1 to KS6	1	mA
	I_{OUT}2	P1 to P4	5	
Allowable power dissipation	Pd max	Ta = 85°C	150	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7	5.0	5.5	V
Input high level voltage	V_{IH}1	CE, CL, DI, $\overline{RES}$	0.8 V_{DD}		5.5	V
	V_{IH}2	KI1 to KI5	0.6 V_{DD}		V_{DD}	
Input low level voltage	V_{IL}	CE, CL, DI, $\overline{RES}$, KI1 to KI5	0		0.2 V_{DD}	V
Recommended external resistance	Rosc	OSC		39		kΩ
Recommended external capacitance	Cosc	OSC		1000		pF
Guaranteed oscillator range	fosc	OSC	19	38	76	kHz
Low level clock pulse width	tøL	CL See figure 1.	160			ns
High level clock pulse width	tøH	CL See figure 1.	160			ns
Data setup time	tds	DI, CL See figure 1.	160			ns
Data hold time	tdh	DI, CL See figure 1.	160			ns
CE wait time	tcp	CE, CL See figure 1.	160			ns
CE setup time	tcs	CE, CL See figure 1.	160			ns
CE hold time	tch	CE, CL See figure 1.	160			ns
DO output delay time	tdc	DO R_{PU} = 4.7 kΩ, C_L = 10 pF*1 See figure 1.			1.5	µs
DO rise time	tdr	DO R_{PU} = 4.7 kΩ, C_L = 10 pF*1 See figure 1.			1.5	µs

Note: *1. Since DO is an open-drain output, these times depend on the values of the pull-up resistor R_{PU} and the load capacitance C_L.

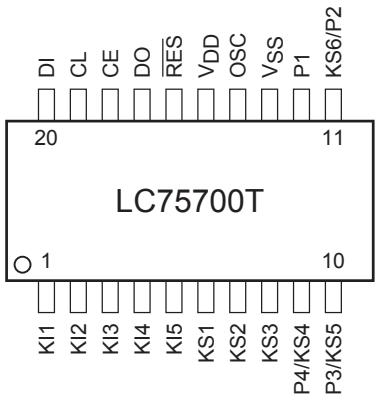
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
Hysteresis	VH	CE, CL, DI, $\overline{RES}$, KI1 to KI5			0.1 V_{DD}		V
Input high level current	I_{IH}	CE, CL, DI, $\overline{RES}$	V_I = 5.5 V			5	µA
Input low level current	I_{IL}	CE, CL, DI, $\overline{RES}$	V_I = 0 V	–5			µA
Input floating voltage	V_{IF}	KI1 to KI5				0.05 V_{DD}	V
Pull-down resistance	R_{PD}	KI1 to KI5	V_{DD} = 5.0 V	50	100	250	kΩ
			V_{DD} = 3.0 V	100	200	500	
Output off leakage current	I_{OFFH}	DO	V_O = 5.5 V			6	µA
Output high level voltage	$V_{OH}1$	KS1 to KS6	V_{DD} = 3.6 V to 5.5 V I_O = –500 µA	V_{DD} – 1.0	V_{DD} – 0.5	V_{DD} – 0.2	V
			V_{DD} = 2.7 V to 3.6 V I_O = –250 µA	V_{DD} – 0.8	V_{DD} – 0.4	V_{DD} – 0.1	
	$V_{OH}2$	P1 to P4	I_O = –1 mA	V_{DD} – 0.9			
Output low level voltage	$V_{OL}1$	KS1 to KS6	V_{DD} = 3.6 V to 5.5 V I_O = 25 µA	0.2	0.5	1.5	V
			V_{DD} = 2.7 V to 3.6 V I_O = 12.5 µA	0.1	0.4	1.2	
	$V_{OL}2$	P1 to P4	I_O = 1 mA			0.9	
	$V_{OL}3$	DO	I_O = 1 mA		0.1	0.5	
Oscillator frequency	fosc	OSC	Rosc = 39 kΩ Cosc = 1000 pF	30.4	38	45.6	kHz
Current drain	$I_{DD}1$	V_{DD}	Key scan standby state			5	µA
	$I_{DD}2$	V_{DD}	V_{DD} = 5.5 V Output open fosc = 38 kHz		200	400	

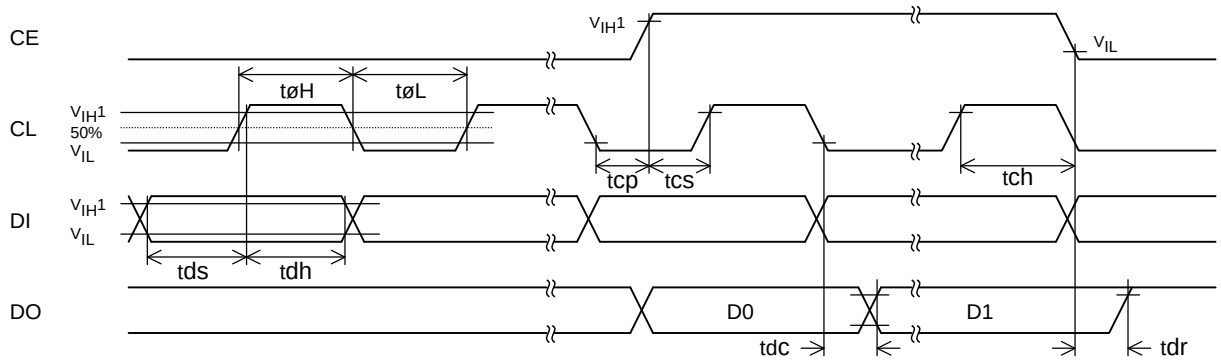
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Pin Assignment



Top view

1. When CL is stopped at the low level



2. When CL is stopped at the high level

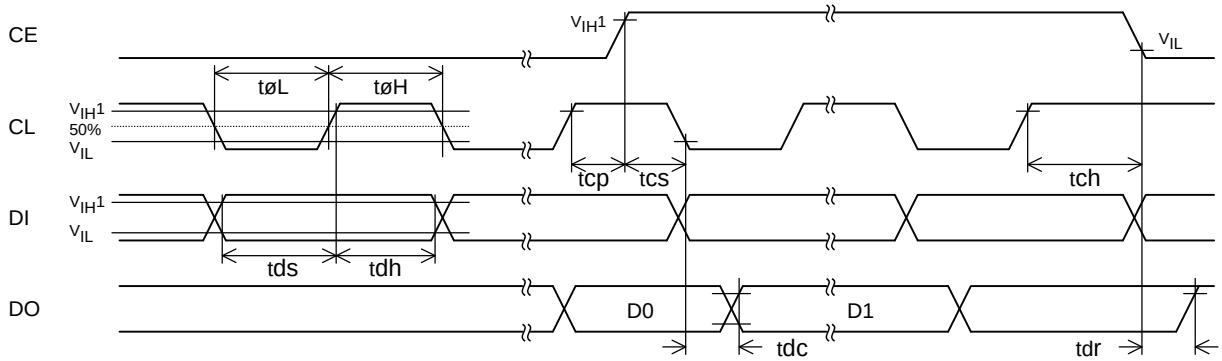
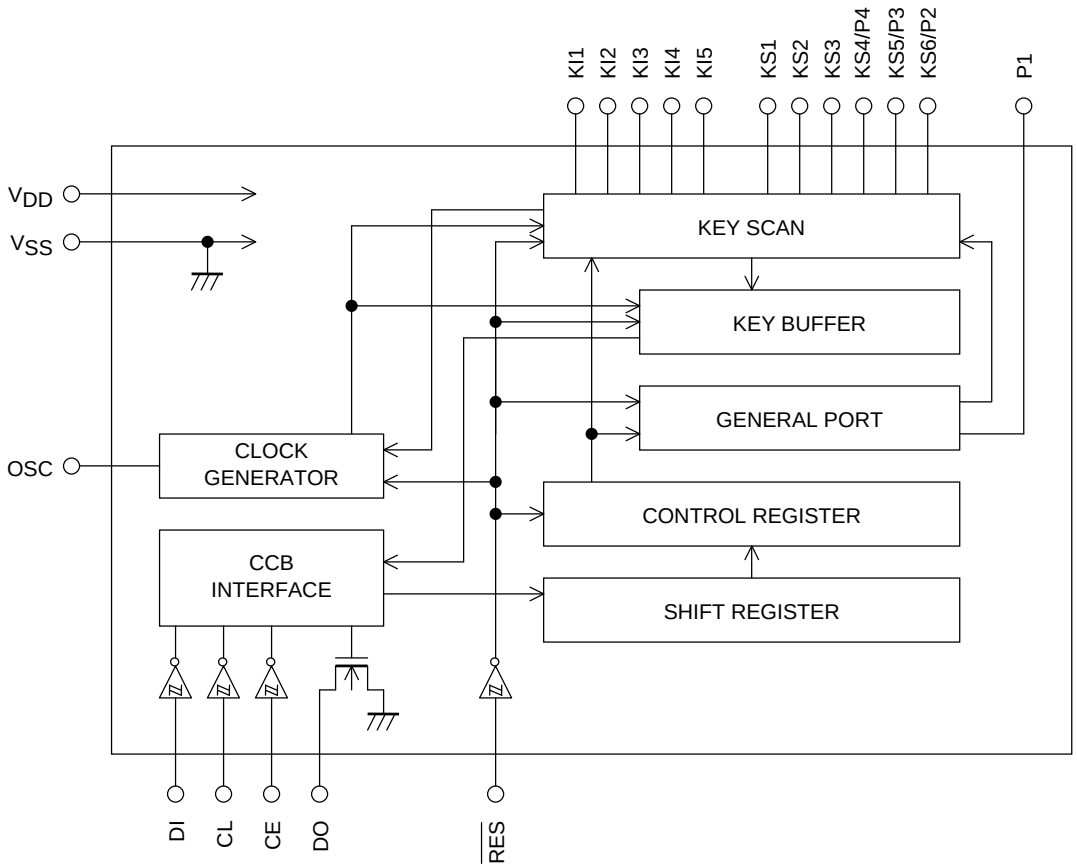


Figure 1

Block Diagram

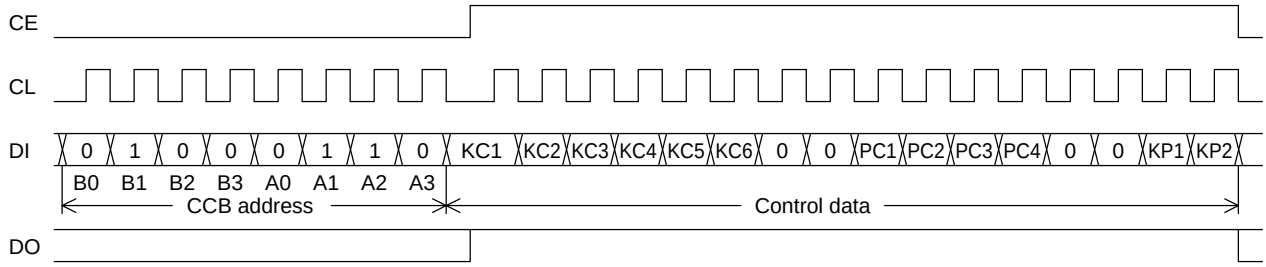


Pin Functions

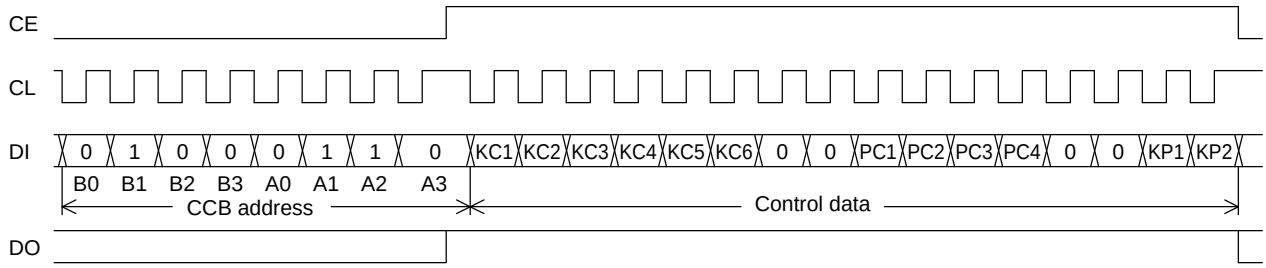
Pin	Pin No.	Function	Active	I/O	Handling when unused
KI1 to KI5	1 to 5	Key scan inputs. These pins have built-in pull-down resistors.	H	I	GND
KS1 to KS3	6 to 8	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to from a key matrix.	—	0	Open
KS4/P4 to KS6/P2	9 to 11	Key scan outputs and general-purpose output ports shared-function pins. These pins can be set the key scan output ports or the general-purpose output ports by the control data “KP1 and KP2”.	—	0	Open
P1	12	The P1 is general-purpose output ports.	—	0	Open
OSC	14	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor at this pin.	—	I/O	V_{DD}
$\overline{RES}$	16	Reset input. that re-initializes the LSI internal states. This pin must be used. • When $\overline{RES}$ is low (V_{SS}) — Key scanning disabled: KS1 to KS3 = low (V_{SS}). — Key scan outputs and general output ports shared-function pins: KS4/P4 to KS6/P2 = low (V_{SS}). — General-purpose output port: P1 = low (V_{SS}). — All the key data is reset to low. • When $\overline{RES}$ is high (V_{DD}) — The states of the pins as key scan output pins or general-purpose output ports, must be set with the control data. — And key scanning is a enabled. Note that serial data must be transferred when $\overline{RES}$ is high.	L	I	GND
CE	18	Serial data interface. Connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE: Chip enable CL: Synchronization clock DI: Transfer data DO: Output data	H	I	GND
CL	19		↑	I	
DI	20		—	I	
DO	17		—	O	Open
V_{DD}	15	Power supply. A voltage of between 2.7 V and 5.5 V must be supplied.	—	—	—
V_{SS}	13	Ground. Must be connected to the system ground.	—	—	—

Serial Data Input

1. When CL is stopped at the low level



2. When CL is stopped at the high level



- CCB address: 62H
- KC1 to KC6: Key scan output state setting data
- PC1 to PC4: General-purpose output port state setting data
- KP1, KP2: Selection data between the key scan output ports and the general-purpose output ports.

Control Data Functions

1.KP1, KP2: Selection data between the key scan output ports and the general-purpose output ports.
These control data bits switch the functions of the KS4/P4 to KS6/P2 output pins between the key scan output port and the general-purpose output port.

KP1	KP2	Output pins			Maximum number of key inputs	Number of general-purpose output ports (+ P1)
		KS4/P4	KS5/P3	KS6/P2		
0	0	KS4	KS5	KS6	30	0 (+1)
1	0	KS4	KS5	P2	25	1 (+1)
0	1	KS4	P3	P2	20	2 (+1)
1	1	P4	P3	P2	15	3 (+1)

Note: KSn (n = 4 to 6): Key scan output ports
Pn (n = 4 to 2): General-purpose output ports

2.KC1 to KC6: Key scan output state setting data
These control data bits set the states of the key scan output pins KS1 to KS6.

Output pins	KS1	KS2	KS3	KS4	KS5	KS6
Key scan output state setting data	KC1	KC2	KC3	KC4	KC5	KC6

For example, if the KS4/P4 to KS6/P2 output pins are set to function as key scan output ports, when KC1 to KC3 are set to 1 and KC4 to KC6 are set to 0, in the key scan standby state, the KS1 to KS3 output pins will output the high level (V_{DD}) and the KS4 to KS6 pins will output the low level (V_{SS}). Note that key scan output signals are not output from output pins that are set to the low level.

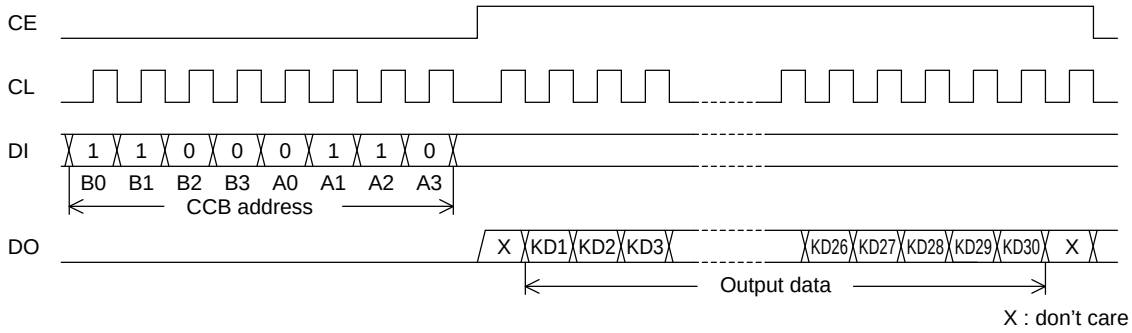
3.PC1 to PC4: General-purpose output port state setting data
These control data bits set the states of the general-purpose output ports P1 to P4.

Output pins	P1	P2	P3	P4
General-purpose output port state setting data	PC1	PC2	PC3	PC4

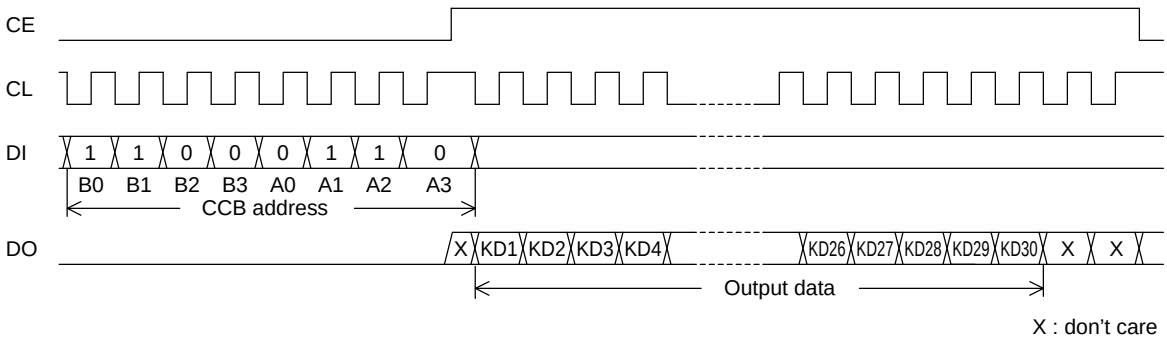
For example, if the KS4/P4 to KS6/P2 output pins are set to function as general-purpose output ports, when PC1 and PC2 are set to 1, and PC3 and PC4 are set to 0, the P1 and P2 output pins will output the high level (V_{DD}), and P3 and P4 will output the low level (V_{SS}).

Serial Data Output

1. When CL is stopped at the low level



2. When CL is stopped at the high level



- CCB address: 63H
- KD1 to KD30: Key data

Note: If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) will be invalid.

Output Data

1.KD1 to KD30: Key data

When a key matrix of up to 30 keys is formed from the KS1 to KS6 key scan output pins and the KI1 to KI5 key scan input pins and one of those key is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

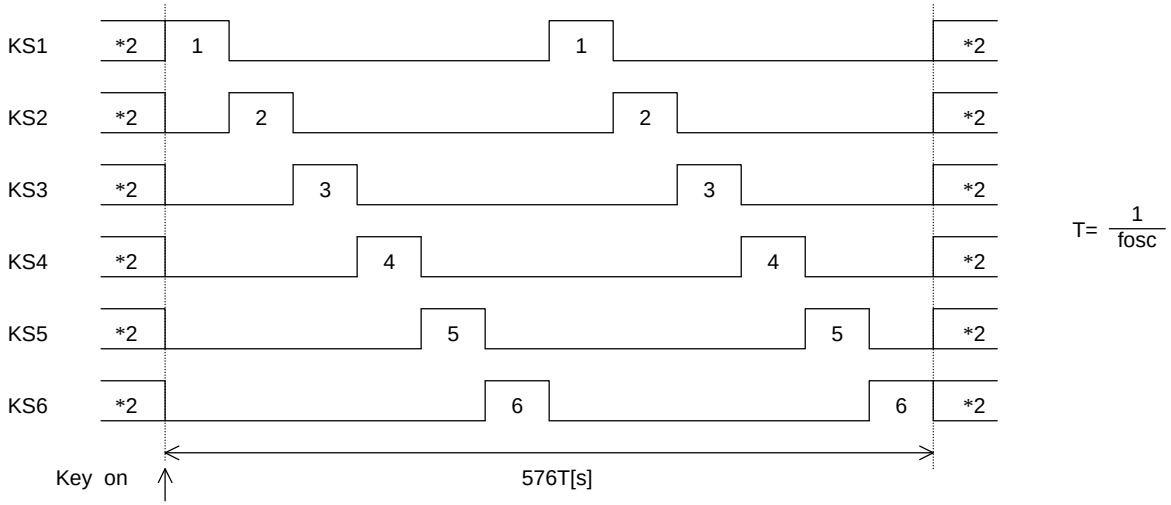
	KI1	KI2	KI3	KI4	KI5
KS1	KD1	KD2	KD3	KD4	KD5
KS2	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

When the KS4/P4 to KS6/P2 output pins are set to function as the general-purpose output ports with the control data "KP1 and KP2", and a key matrix of up to 15 keys is formed from the KS1 to KS3 output pins and the KI1 to KI5 input pins, the KD16 to KD30 key data bits will be set to 0.

Key Scan Operation Functions

1.Key scan timing

The key scan period is 288T (s). To reliably determine the on/off state of the keys, this LSI scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 615T (s) after starting a key scan. If the key data does not agree and a key was pressed at that point, it scans the keys again. Thus this LSI cannot detect a key press shorter than 615T (s).



*2. Not that the high/low states of these pins are determined by the control data, and that key scan output signals are not output from pins that are set to low .

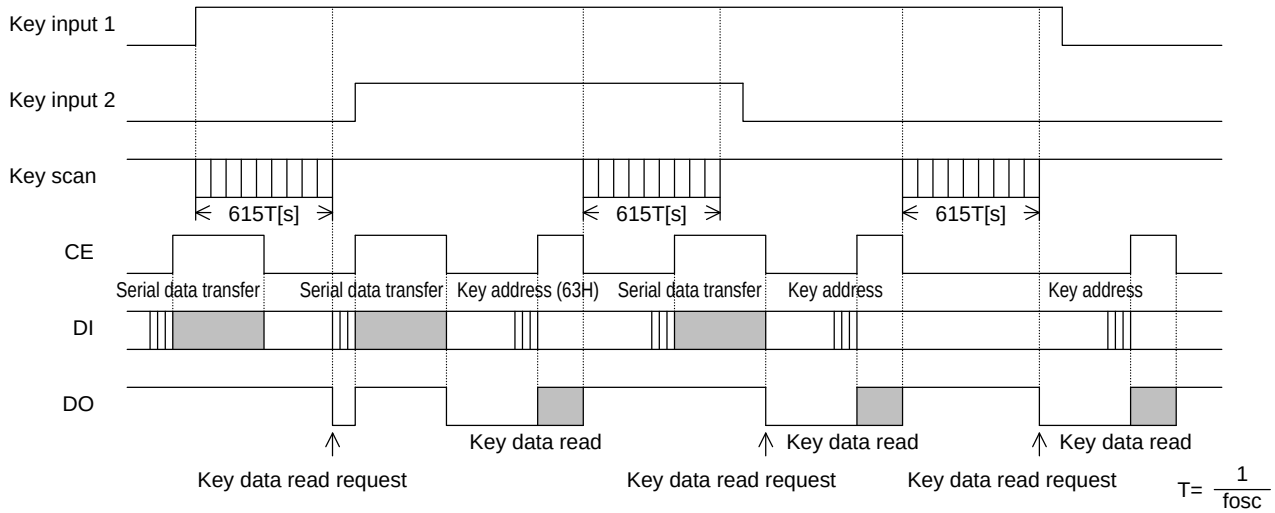
2.Key scan operation

•The pins KS1 to KS6 are set to the high or low state by the control data.

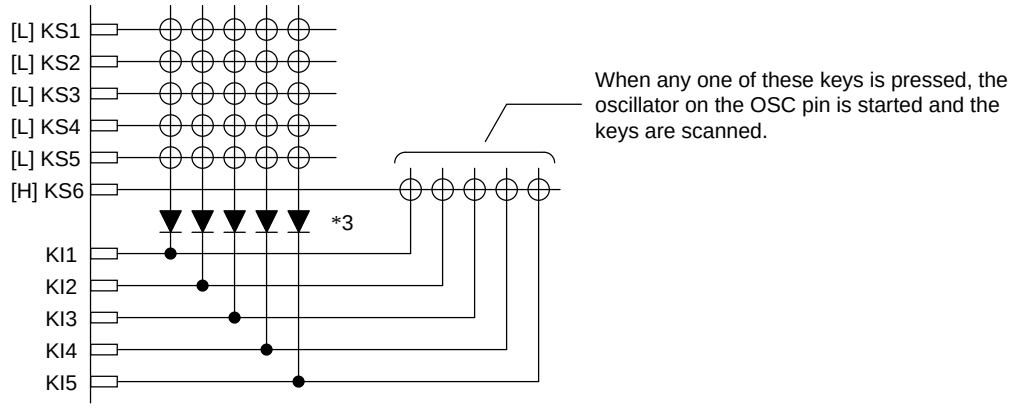
•If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.

•If a key is pressed for longer than 615T (s) (where T = 1/fosc) this LSI outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, Do will be set high.

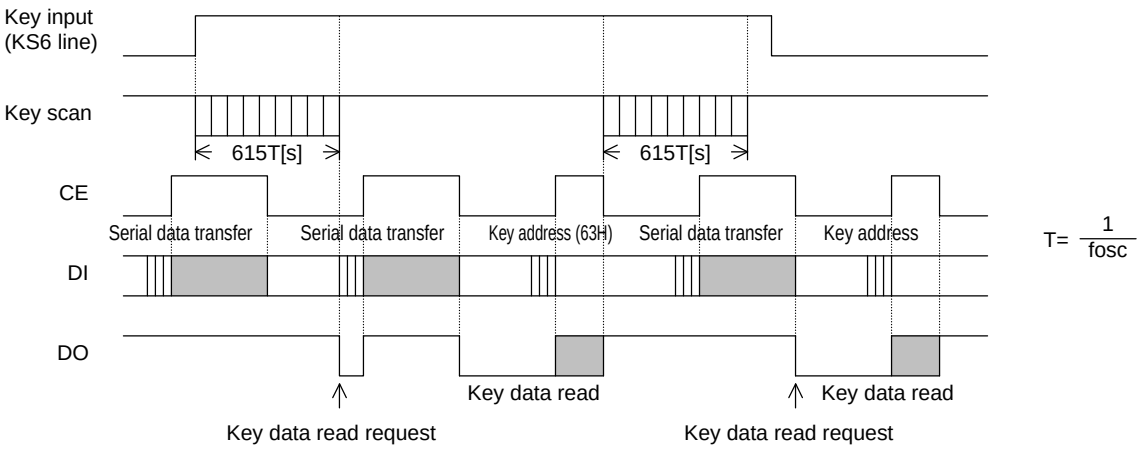
•After the controller reads the key data, the key data read request is cleared (DO is set high) and this LSI performs another key scan. Also note that DO being an open-drain output, requires a pull-up resistor (between 1 kΩ and 10 kΩ) .



Example: When control data “KP1 and KP2 = 0, KC1 to KC5 = 0, KC6 = 1” are executed.
(i.e.key scanning with only KS6 high.)



*3. These diodes are required to reliabled recognize multiple key presses of keys on the KS6 line when state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal keys on the KS1 to KS5 lines are pressed at the same time.



Multiple Key Presses

Although this LSI is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key.Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

System Reset

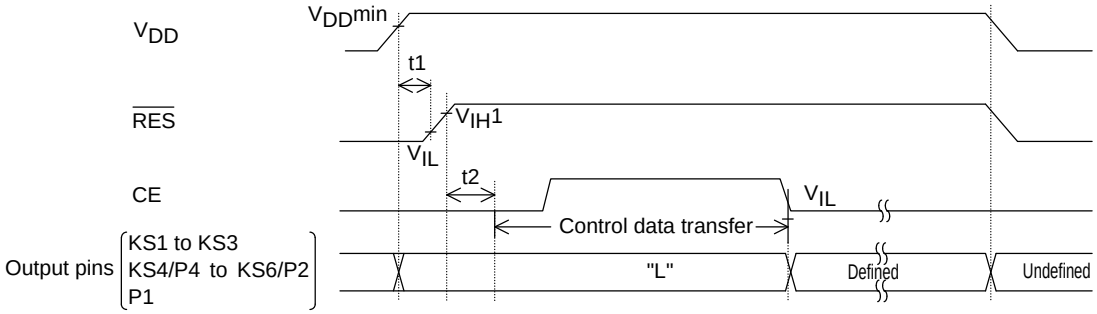
When the power is first applied, the state of function is undefined, so it must be initialized by $\overline{RES}$ = “L”

1.Reset methods

This LSI stopprts the reset methods described below.

When a system reset is applied, key scanning is disabeled, the key data is reset, and the general-purpose output ports are set to and held at the low level (V_{SS}).

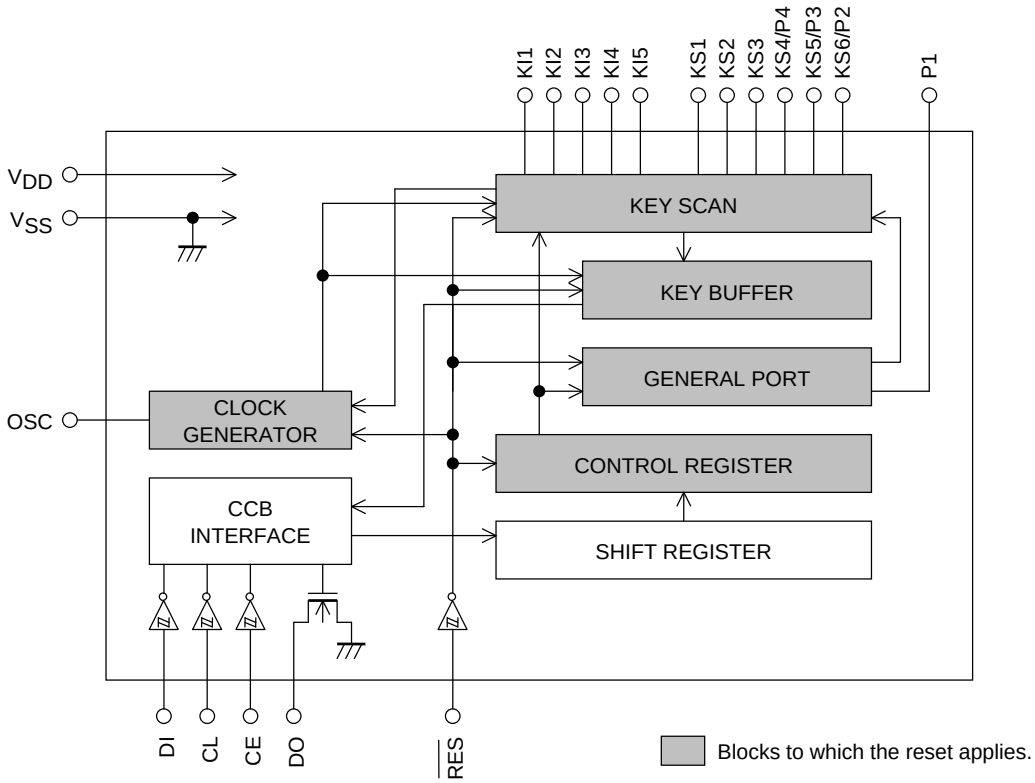
Set $\overline{RES}$ = “H” after the $\overline{RES}$ = “L” period. And key scanning become possible by the control data are transferred.



Notes: t1 ≥ 10 μs
t2 ≥ 10 μs

2.Internal block states during the reset period.

- CLOCK GENERATOR
  Reset is applied and the basic clock is stopped. (The oscillator on the OSC pin is stopped.)
- KEY SCAN, KEY BUFFER
  Reset is applied, the circuit is set to the initial state, and at the same time the key scan operation is disabled.
  And all the key data is set to Low. Then, when the control data are transferred, the key scanning operation is enabled.
- GENERAL PORT
  Reset is applied and the outputs of P1 to P4 are all set to the low level.
- CCB INTERFACE, SHIFT REGISTER, CONTROL REGISTER
  When a reset is applied, The CONTROL REGISTER is forcibly initialized internally. Then, when control data are transferred, the LSI operates according to the control data.

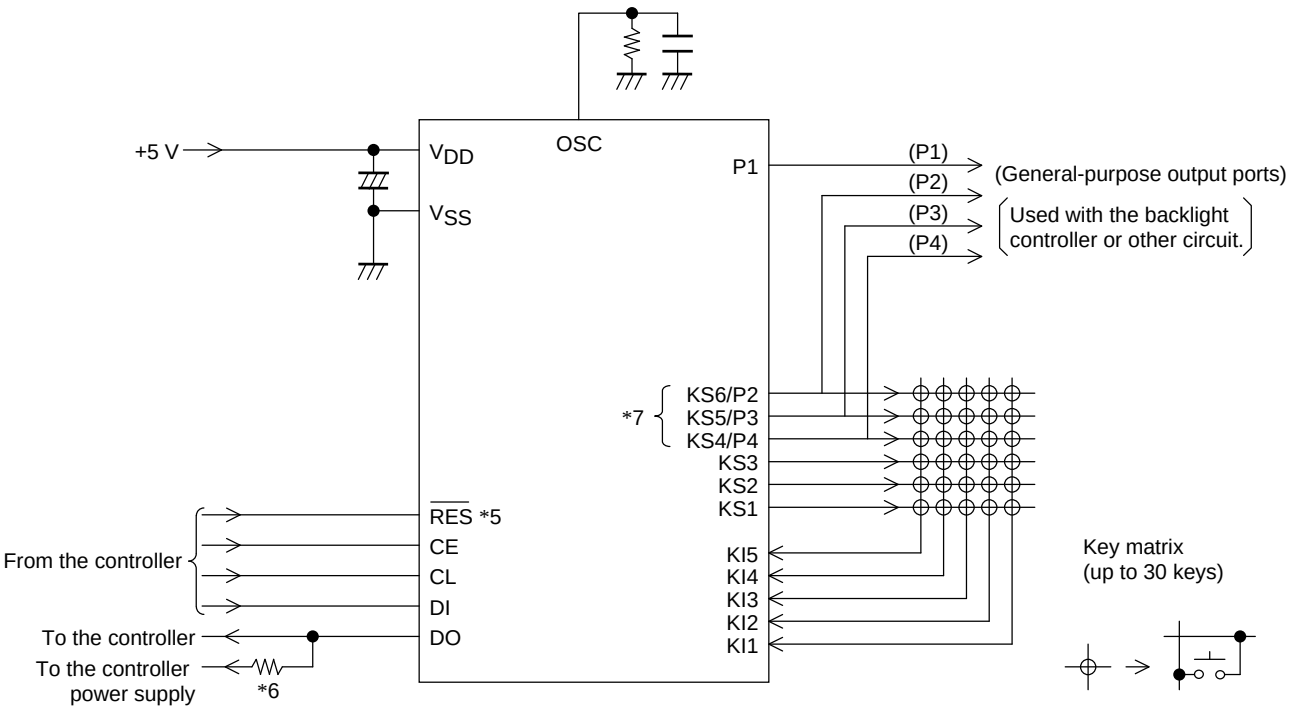


3. Output pin states during a reset

Output pins	State during a reset
KS1 to KS3	L
KS4/P4 to KS6/P2	L
P1	L
DO	H *4

*4. Since this output pin is an open-drain output, a pull-up resistor of between 1 and 10 kΩ is required. This pin remains high during the reset period even if a key data read operation is performed.

Sample Application Circuit

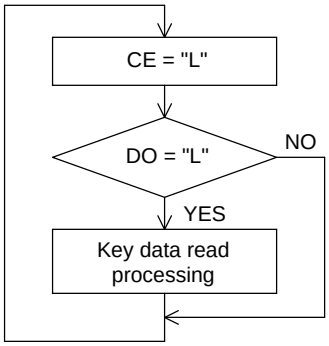


Note: *5. When the power is first applied, it must be initialized by $\overline{RES}$ = "L".
*6. The DO pin,being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 and 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
*7. Each of The KS4/P4 to KS6/P2 pins must be set to either the key scan output port or the general-purpose output port.

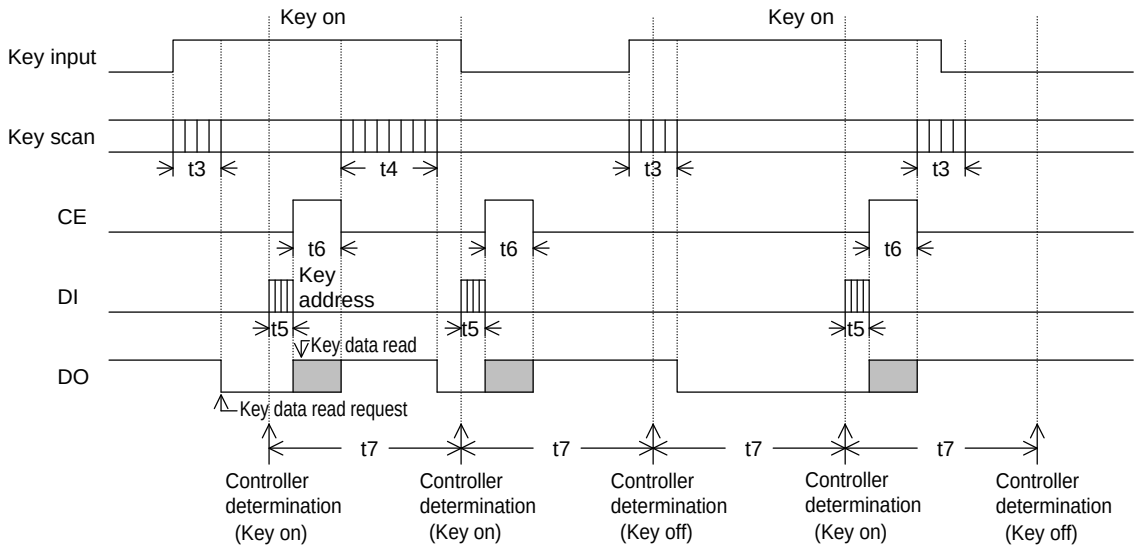
Notes on the controller key data read techniques

1. Timer based key data acquisition

(1) Flowchart



(2) Timing chart



t3: Key scan execution time when the key data agreed for two key scans (615T (s))
t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230T(s))
t5: Key address (63H) transfer time
t6: Key data read time

$$T = \frac{1}{fosc}$$

(3) Explanation

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t7 period without fail. If DO is low, the controller recognizes that a key has been pressed and executed the key data read operation.

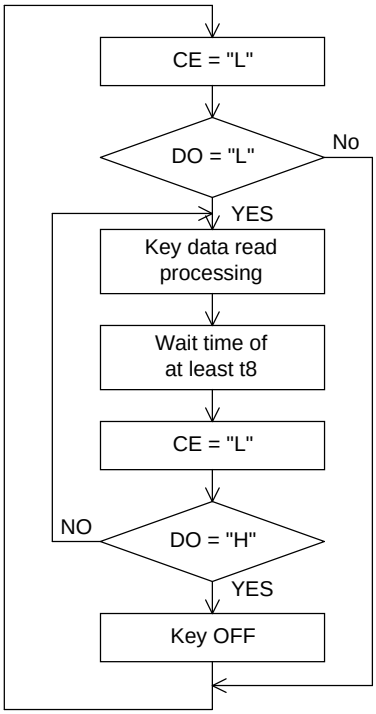
The period t7 in this technique must satisfy the following condition.

$t7 > t4 + t5 + t6$

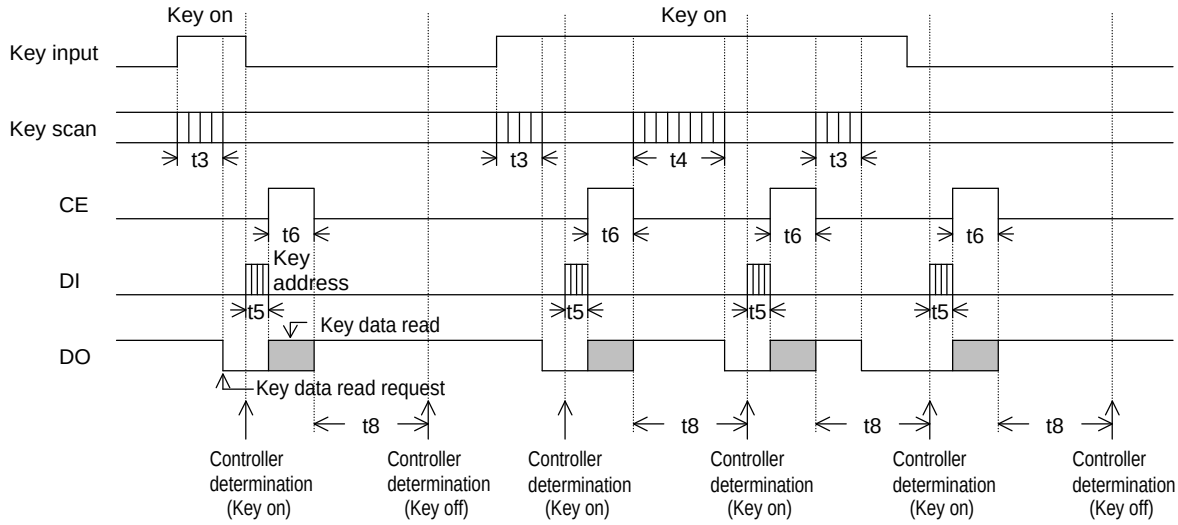
<u>If a keydata read operation is executed when DO is high, the read key data (KD1 to KD30) will be invalid.</u>

2. Interrupt based key data acquisition

(1) Flowchart



(2) Timing chart



t3: Key scan execution time when the key data agreed for two key scans (615T (s))
t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230T(s))
t5: Key address (63H) transfer time
t6: Key data read time

$$T = \frac{1}{fosc}$$

(3) Explanation

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t8 has elapsed by checking the DO state when CE is low and reading the key data.

The period t8 in this technique must satisfy the following condition.

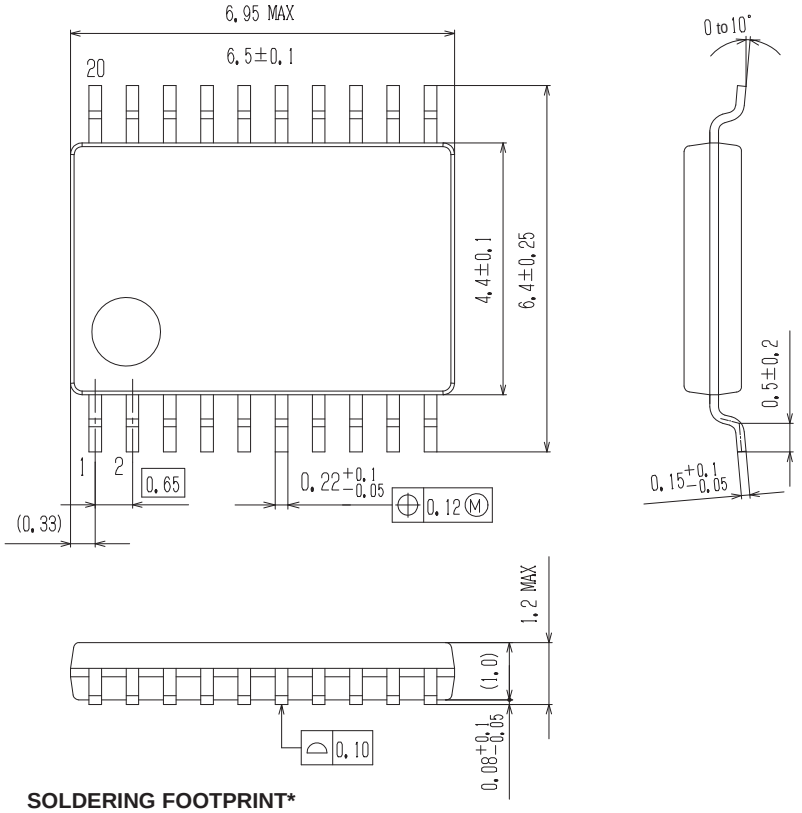
t8 > t4

If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) will be invalid.

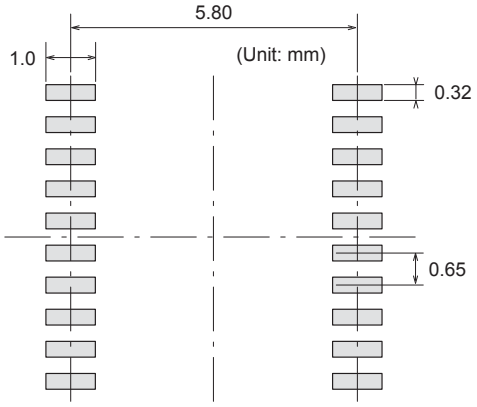
PACKAGE DIMENSIONS

unit : mm

TSSOP20 4.4x6.5 / TSSOP20 (225 mil)
CASE 948AX
ISSUE A



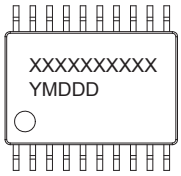
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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