Ordering number: EN4431A

CMOS LSI

LC73861, LC73862

DTMF Receiver LSI

Overview

The LC73861 and LC73862 are DTMF signal detector receiver that incorporates all the necessary filters for telephone answering machines.

Features

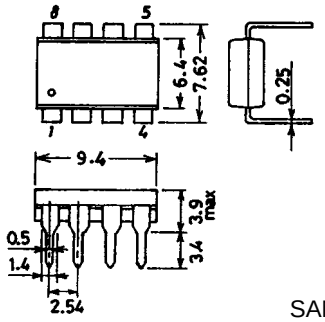
- 16-DTMF tone signal decoder
- DTMF receiver with all necessary filters built-in
  - Dial tone filter
  - High-group bandpass filter
  - Low-group bandpass filter
- Extended dynamic range
- Serial data output
- Microcontroller guard-time compatible
- 4.5 to 5.5 V operating supply voltage range

Package Dimensions

unit : mm

3001B-DIP8

[LC73861, LC73862]



SANYO : DIP8

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.0	V
Maximum input voltage	V_{IN} max		–0.3 to V_{DD} +0.3	V
Maximum input current	I_{IN} max		–10 to +10	mA
Maximum output voltage	V_{OUT} max		–0.3 to V_{DD} +0.3	V
Allowable power dissipation	Pd max	Ta ≦ 85°C	500	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

Allowable Operating Conditions at Ta = –40°C to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating supply voltage	V_{DD}		4.5		5.5	V
High-level input voltage	V_{IH}	ACK pin	0.7V_{DD}			V
Low-level input voltage	V_{IL}	ACK pin			0.3V_{DD}	V

DC Electrical Characteristics at Ta = 25°C ± 2°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating supply current	I_{DD}(op)			3	7	mA
High-level output current	I_{OH}	V_{OUT} = 4.6 V, SD and EST pins			–0.4	mA
Low-level output current	I_{OL}	V_{OUT} = 0.4 V, SD and EST pins	1			mA
Input impedance	Zin	INPUT pin	10			kΩ

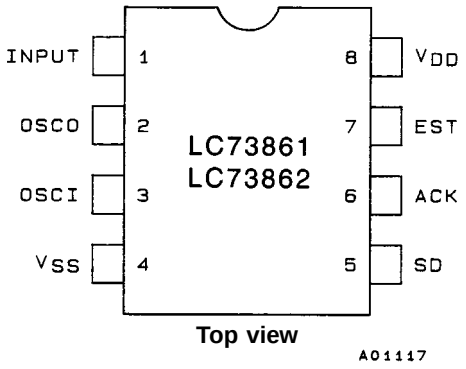
AC Electrical Characteristics at Ta = 25°C ± 2°C, V_{DD} = 5 V, V_{SS} = 0 V, f_{OSC} = 4.194304 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Valid input signal level		See notes 1, 2, 3, 5, 6 and 9.	–49.5		0	dBm
Positive twist accept		See notes 2, 3, 4, 9 and 11.		6		dB
Frequency deviation accept		See notes 2, 3, 5 and 9.	±1.5% ±2			Hz
Frequency deviation reject		See notes 2, 3 and 5.	±3.5			%
Third tone tolerance		See notes 2, 3, 4, 5, 9 and 10.		–16		dB
Dial tone tolerance		See notes 2, 3, 4, 5, 8, 9 and 10.		22		dB
Noise tolerance		See notes 2, 3, 4, 5, 7, 9 and 10.		–12		dB
Tone present detect time	t_{DP}	See Timing Chart.	3		20	ms
Tone absent detect time	t_{DA}	See Timing Chart.	0.5		20	ms
Data shift rate					1	MHz
Data output delay time	t_{PAD}	See Timing Chart.		100		ns
Setup time delay	t_{DL}	See Timing Chart.	0			ns
Data hold time	t_{DH}	See Timing Chart.	30			ns
Oscillator frequency	f_{OSC}	LC73861	4.190109	4.194304	4.198498	MHz
		LC73862	3.5759	3.5795	3.5831	MHz
Load capacitance	C_{XO}	OSCI and OSCO			30	pF

Notes

1. 0 dBm = 1 mW power when driving a 600 Ω load.
2. All 16 DTMF signal frequencies.
3. 40 ms DTMF signal period and 40 ms pause period.
4. Nominal DTMF frequency.
5. Low-frequency group and High-frequency group signal levels are the same.
6. DTMF signal frequency deviation is within ±1.5% ±2 Hz.
7. Bandwidth limited (0 to 3 kHz) Gaussian noise.
8. 350 Hz and 440 Hz dial tone frequencies.
9. Error rate of less than 1 in 10,000.
10. Referenced to the lowest frequency component of the DTMF signal.
11. Twist = High-frequency group tone level ÷ Low-frequency group tone level.

Pin Assignment



Top view

Pin Description

Number	Name	I/O	Description
1	INPUT	I	Input coupling capacitor required. Biased internally to $V_{DD}/2$.
2	OSCO	O	An oscillating circuit is formed by connecting a 4.194304 MHz (LC73861) / 3.579545 MHz (LC73826) oscillator and a capacitor (if needed) between these pins. (To determine whether an external capacitor is needed or not, contact the manufacturer of the oscillator.)
3	OSCI	I	
4	V_{SS}		Supply pin, normally 0 V
5	SD	O	Outputs 4-bit serial decoded DTMF output, least significant bit first.
6	ACK	I	The ACK pin is used to shift out data to the SD pin. Four pulses are needed in order to shift out the 4-bit DTMF code. The data is latched by the shift register before the rising edge of the first pulse.
7	EST	O	Indicates the presence of a DTMF signal when HIGH. (This pin can be monitored and after a short delay, data can be accessed by 4 pulses to ACK.)
8	V_{DD}	O	Supply pin, normally 4.5 V to 5.5 V

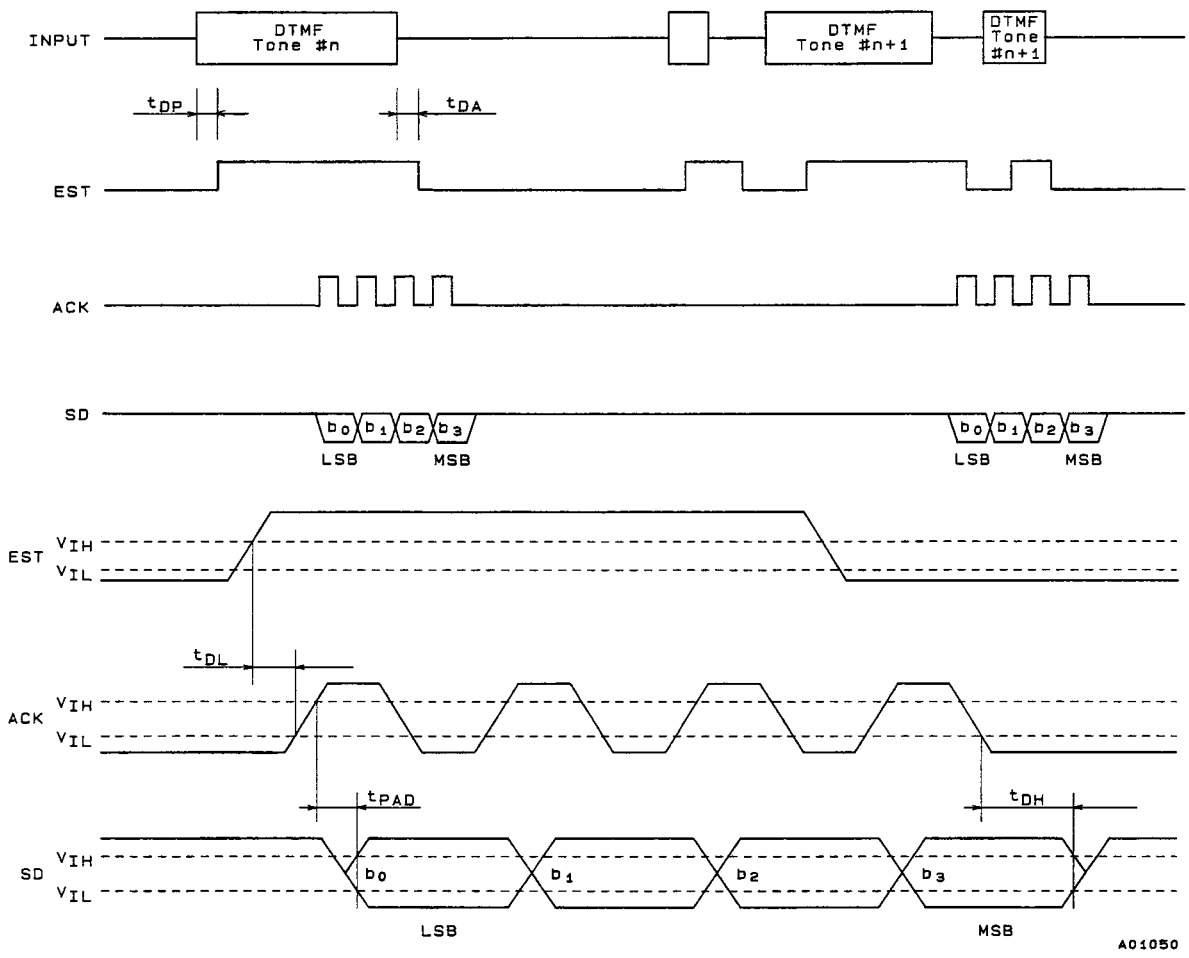
Output Code Table

F_L	F_H	KEY	b3	b2	b1	b0
697	1209	1	L	L	L	H
697	1336	2	L	L	H	L
697	1477	3	L	L	H	H
770	1209	4	L	H	L	L
770	1336	5	L	H	L	H
770	1477	6	L	H	H	L
852	1209	7	L	H	H	H
852	1336	8	H	L	L	L
852	1477	9	H	L	L	H
941	1336	0	H	L	H	L
941	1209	*	H	L	H	H
941	1477	#	H	H	L	L
697	1633	A	H	H	L	H
770	1633	B	H	H	H	L
852	1633	C	H	H	H	H
941	1633	D	L	L	L	L

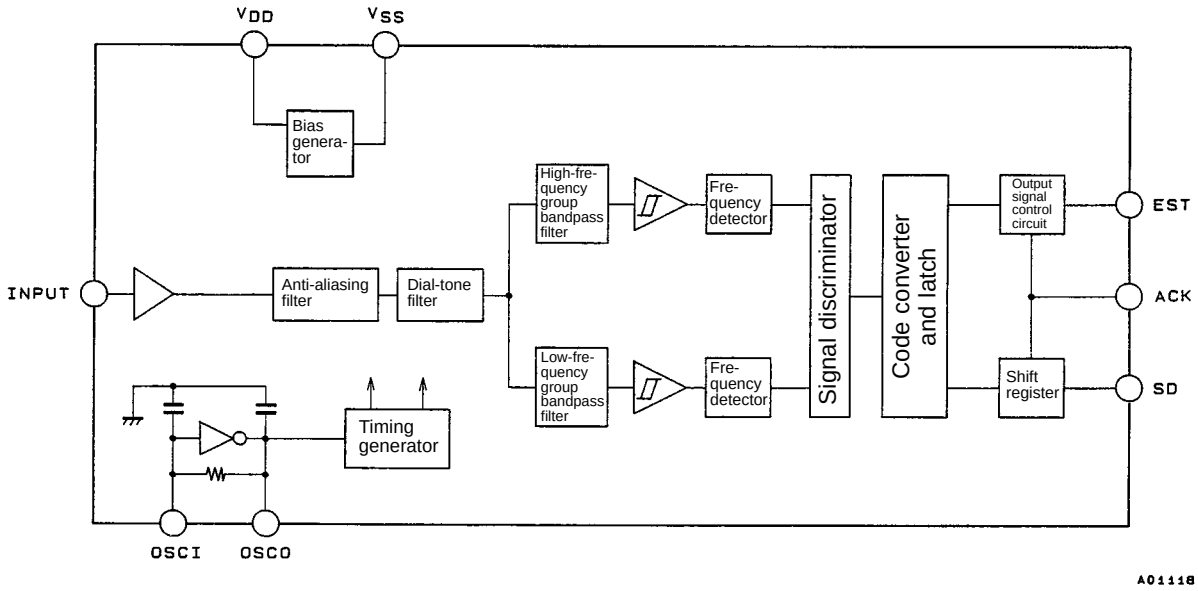
DTMF Dialing Matrix

	C1	C2	C3	C4
R1	1	2	3	A
R2	4	5	6	B
R3	7	8	9	C
R4	*	0	#	D

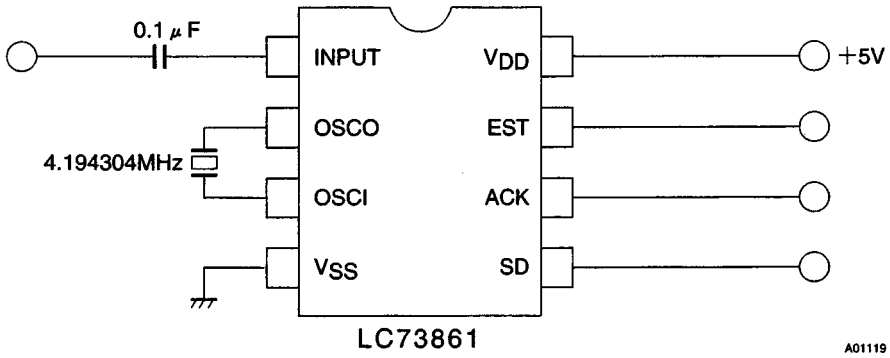
Timing Chart

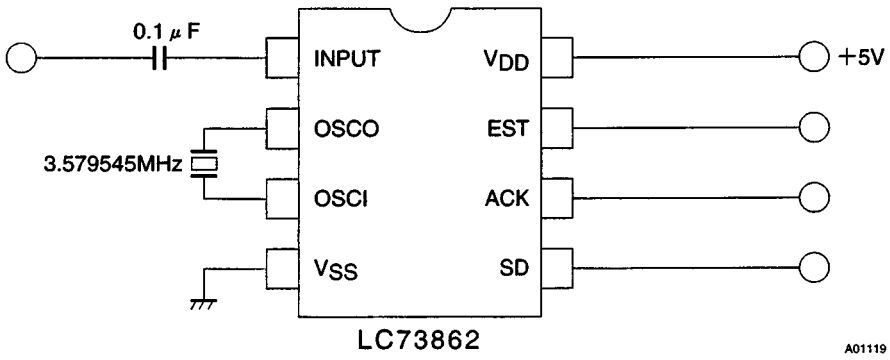


Equivalent Block Diagram



Test Circuit / Sample Application Circuit





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