Ordering number : ENA1744

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

# LC72725KVS — CMOS IC RDS(RBDS) Demodulation IC

## Overview

The LC72725KVS is ICs that implement the signal processing required by the European Broadcasting Union RDS (Radio Data System) standard and by the US NRSC (National Radio System Committee) RBDS (Radio Broadcast Data System) standard. These ICs include band-pass filter, demodulator,and data buffer on chip. RDS data can be read out from this on-chip memory by external clock input in slave operation mode.

## Functions

- Bandpass filter : Switched capacitor filter (SCF)
- RDS Demodulation : 57KHz carrier and RDS data clock regeneration, biphase decode, differential decode.
- Buffer : 128 bit (about 100ms) can be restored in the on-chip data buffer.
- Data output : Master or slave output mode can be selected.
- RDS-ID : Detect RDS signal which can be reset by RST signal input.
- Standby control : Crystal oscillator can be stopped.
- Fully adjustment free
- Low Voltage

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# Specifications

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}d = V_{SS}a = 0V$

| Parameter | Symbol | Pin Name | Conditions | Ratings | Unit |
|---|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}d$, $V_{DD}a$ | $V_{DD}a \leq V_{DD}d+0.3V$ | -0.3 to +6.5 | V |
| Maximum input voltage | $V_{IN}1$ max | TEST, MODE, RST | | -0.3 to +6.5 | V |
| | $V_{IN}2$ max | XIN, RDCL | | -0.3 to $V_{DD}d$+0.3 | V |
| | $V_{IN}3$ max | MPXIN, CIN | | -0.3 to $V_{DD}a$+0.3 | V |
| Maximum output voltage | $V_O1$ max | RDS-ID(READY) | | -0.3 to +6.5 | V |
| | $V_O2$ max | XOUT, RDDA, RDCL | | -0.3 to $V_{DD}d$+0.3 | V |
| | $V_O3$ max | FLOUT | | -0.3 to $V_{DD}a$+0.3 | V |
| Maximum output current | $I_O1$ max | XOUT, FLOUT, RDDA, RDCL | | +3.0 | mA |
| | $I_O2$ max | RDS-ID(READY) | | +20.0 | mA |
| Allowable power dissipation | Pd max | | (Ta≤85°C) | 100 | mW |
| Operating temperature | Topr | | $V_{DD}$ = 3.0V to 5.5V | -40 to +85 | °C |
| Storage temperature | Tstg | | | -40 to +125 | °C |

## Allowable Operating Ranges at Ta = -40 to +85°C, $V_{SS}d = V_{SS}a = 0V$, $V_{DD}d = V_{DD}a$ = 3.0V to 5.5V

| Parameter | Symbol | Pin Name | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| Supply voltage | $V_{DD}$ | $V_{DD}d$, $V_{DD}a$ | Ta = -40 to +85°C | 3.0 | | 5.5 | V |
| Input high-level voltage | $V_{IH}1$ | TEST, MODE, RST | | 0.7$V_{DD}d$ | | 6.5 | V |
| | $V_{IH}2$ | RDCL | | 0.7$V_{DD}d$ | | $V_{DD}d$ | V |
| Input low-level voltage | $V_{IL}$ | TEST, MODE, RST, RDCL | | 0 | | 0.3$V_{DD}d$ | V |
| Output voltage | $V_O1$ | RDDA, RDCL | | | | $V_{DD}d$ | V |
| | $V_O2$ | RDS-ID(READY) | | | | 6.5 | V |
| Input amplitude | $V_{IN}$ | MPXIN | f = 57±2kHz | 1.6 | | 50 | mVrms |
| | VXIN | XIN | | 400 | | 1500 | mVrms |
| Guaranteed crystal oscillator frequencies | Xtal | XIN, XOUT | CI≤120Ω | | 4.332 | | MHz |
| Crystal oscillator operating range | TXtal | XIN, XOUT | Fo = 4.332MHz | | | ±100 | ppm |
| RDCL setup time | tCS | RDCL, RDDA | | 0 | | | µs |
| RDCL high-level time | tCH | RDCL | | 0.75 | | | µs |
| RDCL low-level time | tCL | RDCL | | 0.75 | | | µs |
| Data output time | tDC | RDCL, RDDA | | | | 0.75 | µs |
| READY output time | tRC | RDCL, READY | | | | 0.75 | µs |
| READY low-level time | tRL | READY | | | | 107 | ms |

**Electrical Characteristics** at Ta = -40 to +85°C, $V_{SS}d = V_{SS}a = 0V$, $V_{DD}d = V_{DD}a = 3.0V$ to 5.5V

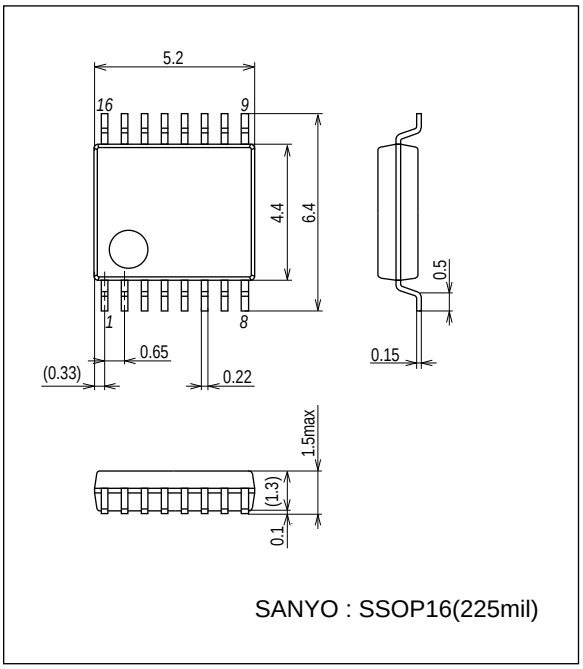
| Parameter | Symbol | Pin Name | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| Internal feedback resistance | Rf | XIN | | | 1.0 | | MΩ |
| Hysteresis | VHIS | TEST, MODE, RST, RDCL | | | $0.1V_{DD}d$ | | V |
| Output low-level voltage | $V_{OL}1$ | RDDA, RDCL | I = 2mA | | | 0.4 | V |
| | $V_{OL}2$ | RDS-ID(READY) | I = 8mA | | | 0.4 | V |
| Output high-level voltage | $V_{OH}$ | RDDA, RDCL | I = -2mA | $V_{DD}d$-0.54 | | | V |
| Input high-level current | $I_{IH}1$ | TEST, MODE, RST, RDCL | $V_I$ = 6.5V | | | 5.0 | μA |
| | $I_{IH}2$ | XIN | $V_I = V_{DD}d$ | 2.0 | | 11 | μA |
| Input low-level current | $I_{IL}1$ | TEST, MODE, RST, RDCL | $V_I$ = 0V | | | 5.0 | μA |
| | $I_{IL}2$ | XIN | $V_I$ = 0V | 2.0 | | 11 | μA |
| Output off leakage current | IOFF | RDS-ID(READY) | $V_O$ = 6.5V | | | 5.0 | μA |
| Current drain | $I_{DD}$ | $V_{DD}d+V_{DD}a$ | $V_{DD}d+V_{DD}a$ ($V_{DD}d = V_{DD}a$ = 3.3V) | 1.5 | 2.5 | 3.5 | mA |

**Bandpass Filter Characteristics** at Ta = 25°C, $V_{SS}d = V_{SS}a = 0V$, $V_{DD}d = V_{DD}a = 3.0V$ to 5.5V

| Parameter | Symbol | Pin Name | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| Input resistance | Rmpxin | MPXIN-$V_{SS}a$ | f = 57kHz | | 100 | | kΩ |
| | Rcin | CIN-$V_{SS}a$ | f = 57kHz | | 100 | | kΩ |
| Center frequency | fc | FLOUT | | 56.5 | 57.0 | 57.5 | kHz |
| -3dB band width | BW-3dB | FLOUT | | 2.5 | 3.0 | 3.5 | kHz |
| Gain | Gain | MPXIN-FLOUT | f = 57kHz | 28 | 31 | 34 | dB |
| Stop band attenuation | Att1 | FLOUT | Δf = ±7kHz | 30 | | | dB |
| | Att2 | FLOUT | f<45kHz, f>70kHz | 40 | | | dB |
| | Att3 | FLOUT | f<20kHz | 50 | | | dB |
| Reference voltage output | Vref | Vref | $V_{DD}a$ = 3V | | 1.5 | | V |

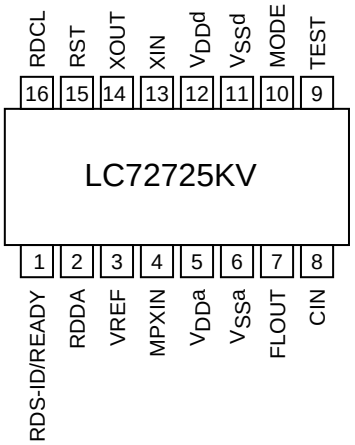
## Package Dimensions

unit : mm (typ)
3178B



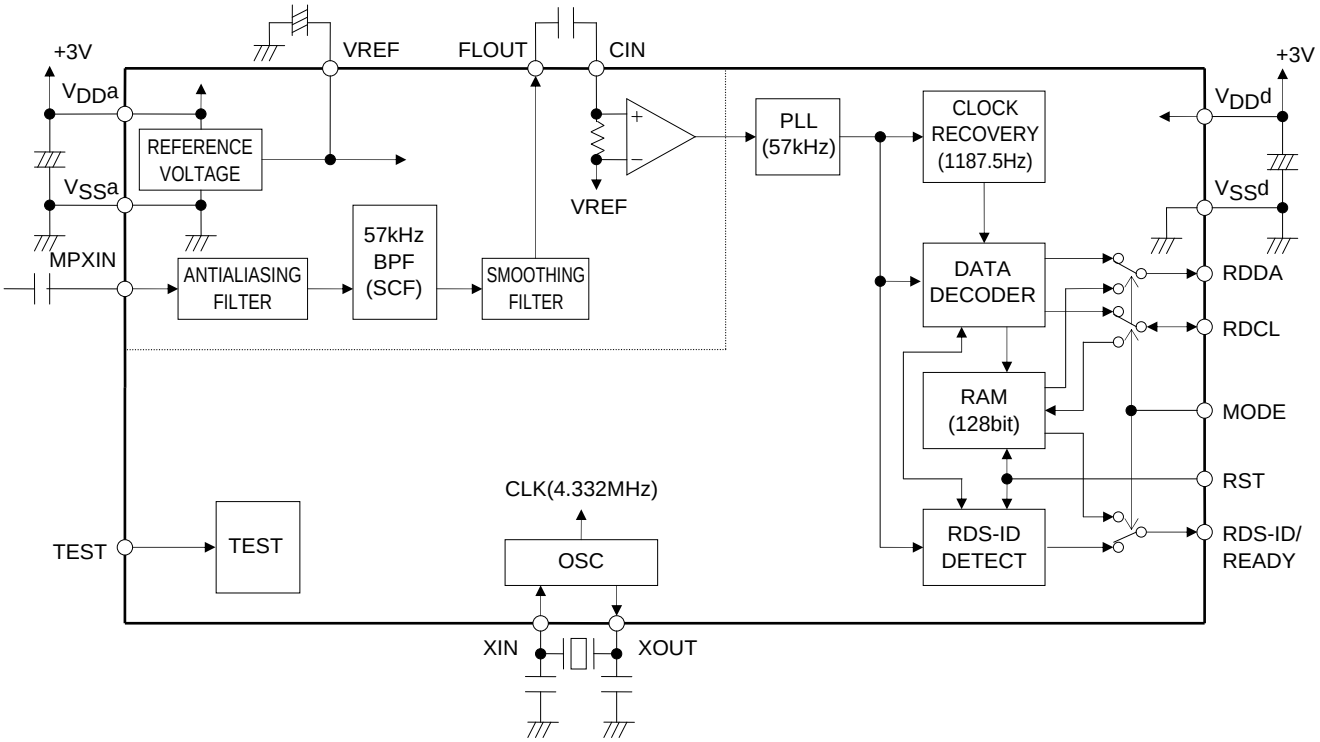

SANYO : SSOP16(225mil)

## Pin Assignment

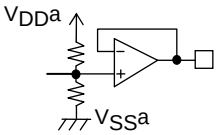
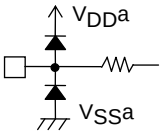
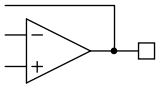
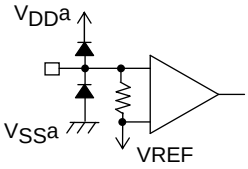
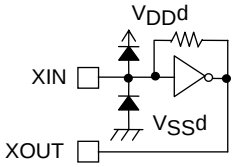
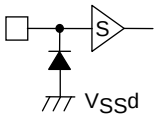
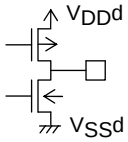
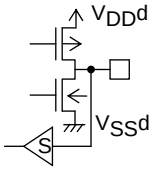
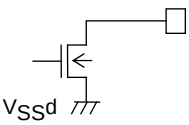



Top view

## Block Diagram



## Pin Descriptions

| Pin No. | Pin Name | I/O | Function | Pin Circuit |
|---|---|---|---|---|
| 3 | VREF | Output | Reference voltage output ($V_{DD}a/2$) |   |
| 4 | MPXIN | Input | Baseband (multiplexed) signal input |   |
| 7 | FLOUT | Output | Subcarrier output (filter output) |  |
| 8 | CIN | Input | Subcarrier input (comparator input) |   |
| 5 | $V_{DD}a$ | - | Analog system power supply (+3V) | - |
| 6 | $V_{SS}a$ | - | Analog system ground | - |
| 14 | XOUT | Output | Crystal oscillator output (4.332MHz) |   |
| 13 | XIN | Input | Crystal oscillator input<br>(external reference signal input) | |
| 9 | TEST | | Test input |   |
| 10 | MODE | | Read out mode (0:master, 1:slave) | |
| 15 | RST | | RDS-ID/RAM reset (active high) | |
| 2 | RDDA | Output | RDS data output |   |
| 16 | RDCL | I/O | RDS clock output (master mode) /<br>RDS read out clock input (slave mode) |   |
| 1 | RDS-ID/<br>READY | Output | RDS reliability data output<br>(High:data with high RDS reliability<br>Low: data with low RDS reliability)<br>READY output (active high) |   |
| 12 | $V_{DD}d$ | - | Digital system power supply (+3V) | - |
| 11 | $V_{SS}d$ | - | Digital system ground | - |

## Input/Output Data Format

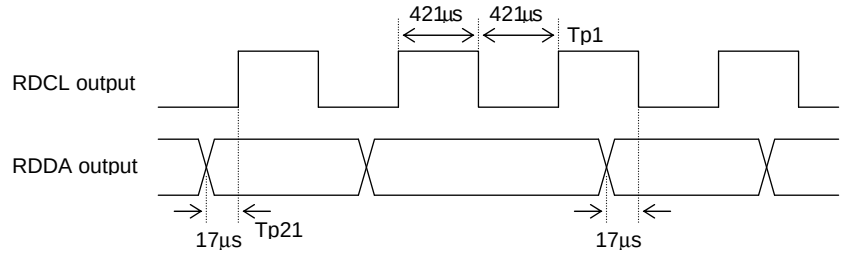
| TEST | MODE | Circuit Operation Mode | RDCL Pin | RDS-ID/READY Pin |
|---|---|---|---|---|
| 0 | 0 | Master read out mode | Clock output | RDS-ID output |
| 0 | 1 | Slave read out mode | Clock input | READY output |
| 1 | 0 | Standby mode (crystal oscillator stopped) | - | - |
| 1 | 1 | IC test mode which is not available to user applications. | - | - |

| | RST Pin |
|---|---|
| RST = 0 | Normal operation |
| RST = 1 | RDS-ID • demodulation circuit clear + READY • memory clear (when slave mode) |

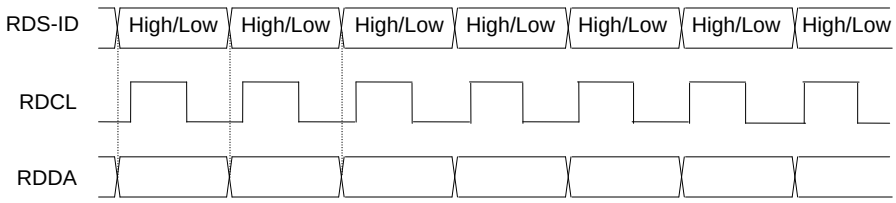
| | RDS-ID/READY Pin |
|---|---|
| Master mode | RDS-ID output (Active-high) |
| Slave mode | READY output (Active-high) |

Note: RDS-ID(READY) pin is an n-channel open-drain output, and requires an external pull-up resistor to output data.

## RDCL/RDDA Output Timing in Master Mode

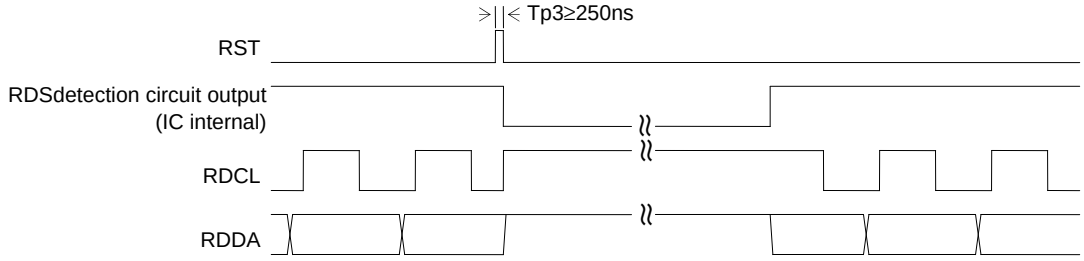



## RDS-ID Output Timing



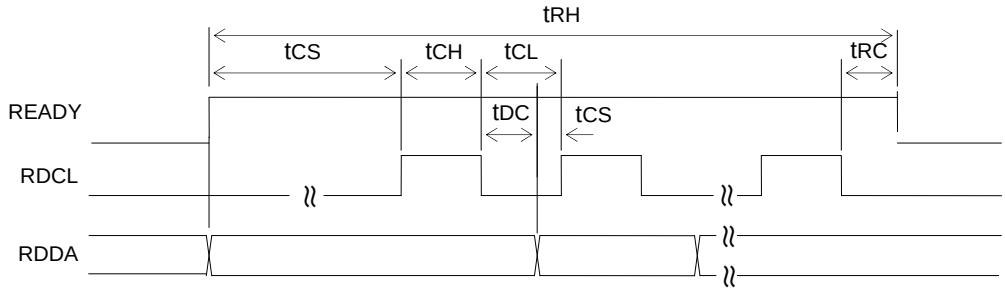

Note: RDS-ID is High: data with high RDS reliability, Low: data with low RDS reliability

## RST Operation in Master Mode




Note: RDCL and RDDA outputs keep high level after input of RST until RDS detection circuit output is detected.

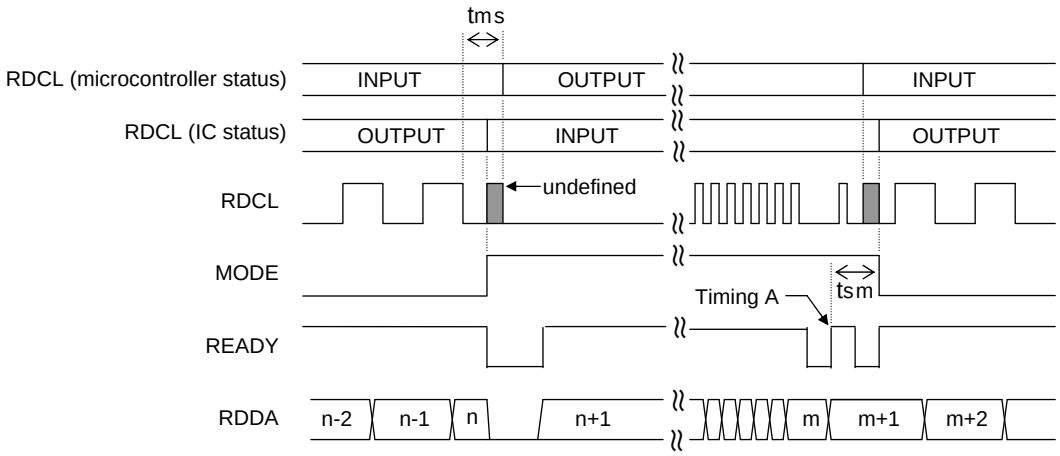
## RDCL Operation in Slave Mode



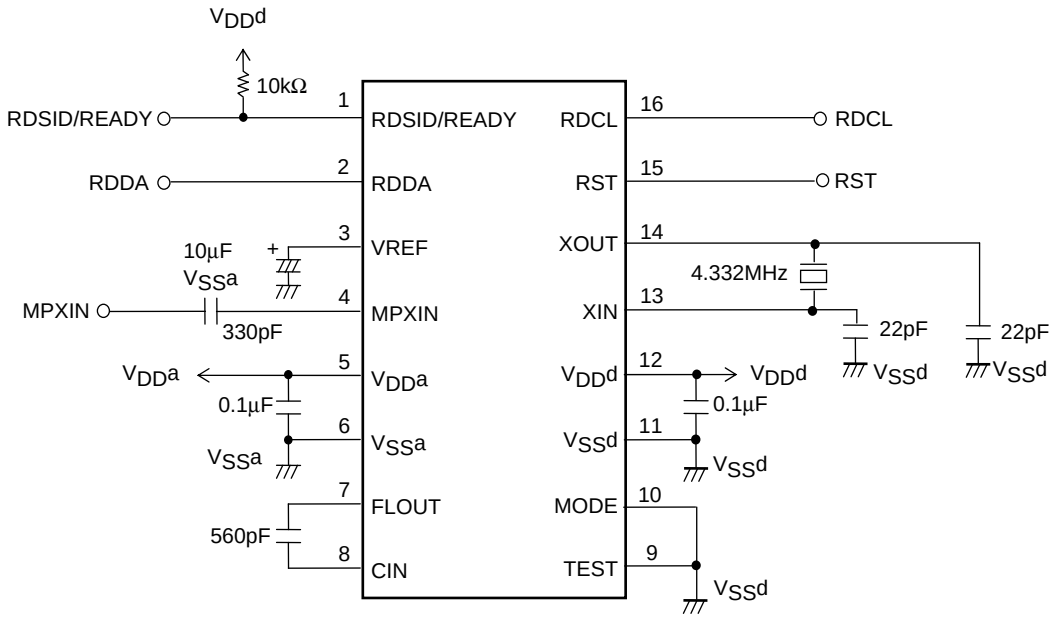

| Parameter | Symbol | Pin Name | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| RDCL setup time | tCS | RDCL,RDDA | | 0 | | | µs |
| RDCL high-level time | tCH | RDCL | | 0.75 | | | µs |
| RDCL low-level time | tCL | RDCL | | 0.75 | | | µs |
| Data output time | tDC | RDCL,RDDA | | | | 0.75 | µs |
| READY output time | tRC | RDCL,READY | | | | 0.75 | µs |
| READY high-level time | tRH | READY | | | | 107 | ms |

Notes: 1. RDCL input must be started after READY signal goes high. When READY signal is low, RDCL must be low level.

2. READY status must be checked after tRC time from RDCL is set low. If the READY status is high, then next read cycle can be continued. If the READY status is low, next RDCL clock input must be stopped.
3. If the above condition is satisfied, RDS data (RDDA) can be read out at both rising and falling edge of RDCL.
4. READY signal goes low after the last data is read out from on-chip memory. If one RDS data is stored in the memory, READY signal goes high again.
5. When the reception channel is changed, a memory and READY reset must be applied using RST input. If a reset is not applied, reception data from the previous channel may remain in memory. If RST input is applied, reception data is not stored in memory until the first RDS-ID is detected, and READY output goes high after the first RDS-ID is detected. After the first RDS-ID is detected, reception data is stored even if RDS-ID is not detected.
6. The readout mode may be switched between master and slave modes during readout.
   Applications must observe the following points to assure data continuity during this operation.
   1) Data acquisition timing in master made
      Data must be read on the falling edge of RDCL
   2) Timing of the switch from master mode to slave mode
      After the RDCL output goes low and the RDDA data has been acquired, the application must set MODE high immediately.
      Then, the microcontroller starts output by setting the RDCL signal low.
      The microcontroller RDCL output must start within 840µs (tms) after RDCL went low.
      In this case, if the last data read in master mode was data item n, then data starting with item n+1 will be written to memory.
   3) Timing of the switch from slave mode to master mode
      After all data has been read from memory and READY has gone high, the application must then wait until READY goes low once again the next time (timing A in the figure), immediately read out one bit of data and input the RDCL clock.
      Then, at the point READY goes high, the microcontroller must terminate RDCL output and then set MODE low.
      The application must switch MODE to low within 840µs (tms) after READY goes low (timing A in the figure).



## Sample Application Connection Circuit (for master mode operation)




Note: If the RST pin is unused, it must be connected to ground.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