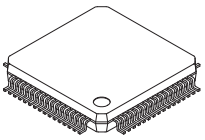
# LC72717PW

# Mobile FM Multiplex Broadcast (DARC) Receiver IC

ON Semiconductor®

www.onsemi.com



SPQFP64 10x10 / SQFP64

## Overview

The LC72717PW is a data demodulation LSI for receiving FM multiplex broadcasts for mobile reception in the DARC format. This LSI includes an on-chip bandpass filter for extracting the DARC signal from the FM baseband signal. It also supports ITU-R recommended FM multiplex frame structures (methods A, A', B, and C) and can implement a compact, multifunction DARC reception system.

The LC72717PW's package, pin assignment and electrical characteristics are same as the LC72715PW (VICS-LSI). Functionally, the LC72717PW is a product that VICS function is removed from the LC72715PW.

The LC72717PW is also control-compatible with the LC72711LW.

Note that a contract with the NHK Engineering System, Inc. may be required to produce DARC compatible products in case, please contact with the NHK Engineering System, Inc.

## Functions

- Adjustment-free 76 kHz SCF bandpass filter
- Supports all FM multiplex frame structures (methods A, A', B and C) under CPU control.
- MSK delay detection system based on a 1T delay.
- Error correction function based on a 2T delay (in the MSK detection stage)
- Digital PLL based clock regeneration function
- Shift-register 1T and 2T delay circuits
- Block and frame synchronization detection circuits
- Functions for setting the number of allowable BIC errors and the number of synchronization protection operations.
- Error correction using (272, 190) codes
- Built-in layer 4 CRC code checking circuit
- On-chip frame memory and memory control circuit for vertical correction
- 7.2 MHz crystal oscillator circuit
- Two power saving modes: STNBY and EC STOP
- Applications can use either a parallel CPU interface (DMA) or a CCB* serial interface.
- Supply voltage: 2.7 V to 3.6 V

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

## ORDERING INFORMATION

See detailed ordering and shipping information on page 27 of this data sheet.

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June 2017 - Rev. 3

Publication Order Number :
LC72717PW/D

## Specifications

### Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ | | −0.3 to +4.0 | V |
| Input voltage | $V_{IN}1$ | A0/CL, A1/CE, A2/DI, RST, STNBY ($V_{DD}$ is equal to 2.7 V or more.) | −0.3 to +5.6 | V |
| | | A0/CL, A1/CE, A2/DI, RST, STNBY ($V_{DD}$ is less than 2.7 V.) | −0.3 to $V_{DD}$+0.3 | V |
| | $V_{IN}2$ | Input pin other than $V_{IN}1$ | −0.3 to $V_{DD}$+0.3 | V |
| Output voltage | $V_{OUT}$ | Output pin | −0.3 to $V_{DD}$+0.3 | V |
| Output current | $I_{OUT}1$ | INT, RDY, DREQ, D0 to D15, DO | 0 to 2.0 | mA |
| | $I_{OUT}2$ | Output pin other than $I_{OUT}1$ | 0 to 1.0 | mA |
| Allowable output current (total) | ITTL | Total for all the output pins | 10 | mA |
| Allowable power dissipation | Pd max | | 200 | mW |
| Operating temperature | Topr | Ta ≤ 85°C | −40 to +85 | °C |
| Storage temperature | Tstg | | −55 to +125 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### Allowable Operating Ranges at Ta = −40°C to +85°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pin Name | Type | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | min | typ | max | |
| Supply voltage | $V_{DD}$ | | | | 2.7 | | 3.6 | V |
| Input high-level voltage | $V_{IH}1$ | A0/CL, A1/CE, A2/DI, RST, STNBY | Schmitt | | $0.7V_{DD}$ | | 5.5 | V |
| | $V_{IH}2$ | IOCNT1, IOCNT2, DACK, D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS | Schmitt | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH}3$ | SP, BUSWD, TIN, TPC1, TPC2, TOSEL1, TOSEL2 | | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| Input low-level voltage | $V_{IL}1$ | A0/CL, A1/CE, A2/DI, RST, STNBY | Schmitt | | 0.0 | | $0.3V_{DD}$ | V |
| | $V_{IL}2$ | IOCNT1, IOCNT2, DACK, D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS | Schmitt | | 0.0 | | $0.3V_{DD}$ | V |
| | $V_{IL}3$ | SP, BUSWD, TIN, TPC1, TPC2, TOSEL1, TOSEL2 | | | 0.0 | | $0.3V_{DD}$ | V |
| Oscillation frequency | FOSC | XIN, XOUT | Oscillation circuit | Within ±250 ppm | | 7.2 | | MHz |
| XIN input sensitivity | VXI | XIN | | Capacitive coupling | 400 | | | mVrms |
| Input amplitude | VMPX1 | MPXIN | SCF | 100% demodulation composite $V_{DD}$ = 3.3 V | 120 | | 500 | mVrms |
| | VMPX2 | MPXIN | SCF | 100% demodulation composite $V_{DD}$ = 2.7 V | 120 | | 450 | mVrms |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Electrical Characteristics** at Ta = −40°C to +85°C, $V_{DD}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0 V

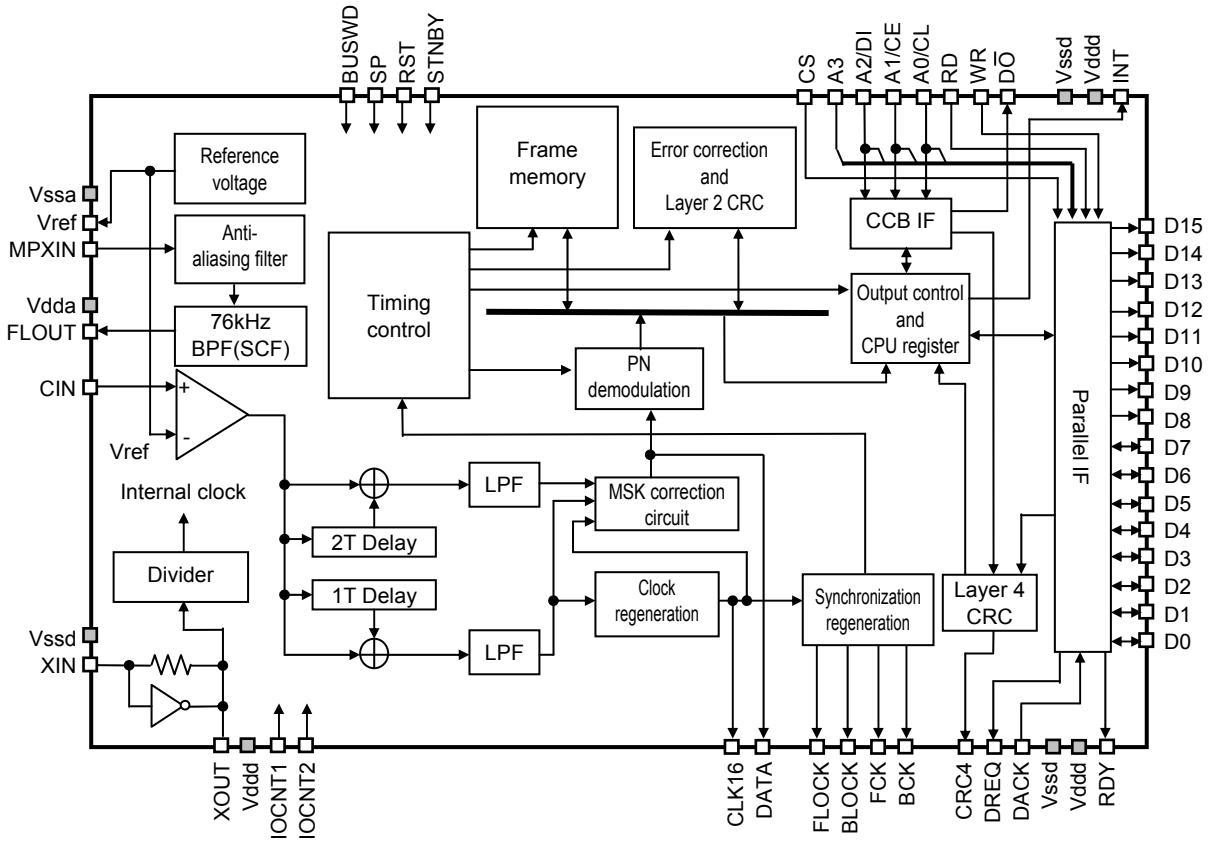
| Parameter | Symbol | Pin Name | Type | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | min | typ | max | |
| Input high-level current | $I_{IH}1$ | A0/CL, A1/CE, A2/DI, RST, STNBY | Schmitt | | | | 1.0 | μA |
| | $I_{IH}2$ | IOCNT1, IOCNT2, DACK D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS | Schmitt | | | | 1.0 | μA |
| | $I_{IH}3$ | SP, BUSWD, TIN, TPC1, TPC2, TOSEL1, TOSEL2 | | | | | 1.0 | μA |
| Input low-level current | $I_{IL}1$ | A0/CL, A1/CE, A2/DI, RST, STNBY | Schmitt | | −1.0 | | | μA |
| | $I_{IL}2$ | IOCNT1, IOCNT2, DACK D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS | Schmitt | | −1.0 | | | μA |
| | $I_{IL}3$ | SP, BUSWD, TIN, TPC1, TPC2, TOSEL1, TOSEL2 | | | −1.0 | | | μA |
| Output high-level voltage | $V_{OH}1$ | CLK16, DATA, FLOCK, BLOCK, FCK, BCK, CRC4 | CMOS | $I_{OH}$ = −1 mA | $V_{DD}$−0.4 | | | V |
| | $V_{OH}2$ | DREQ, RDY, D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, INT | CMOS | $I_{OH}$ = −2 mA | $V_{DD}$−0.4 | | | V |
| Output low-level voltage | $V_{OL}1$ | CLK16, DATA, FLOCK, BLOCK, FCK, BCK, CRC4 | CMOS | $I_{OL}$ = 1 mA | | | 0.4 | V |
| | $V_{OL}2$ | DREQ, RDY, D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, INT | CMOS | $I_{OL}$ = 2 mA | | | 0.4 | V |
| | $V_{OL}3$ | DO | Nch-Open Drain | $I_{OL}$ = 2 mA | | | 0.4 | V |
| Output leakage current | IOFF | DO | | $V_O = V_{DD}$ | | | 1.0 | μA |
| Hysteresis voltage | VHYS | A0/CL, A1/CE, A2/DI, RST, STNBY, IOCNT1, IOCNT2, DACK, D0, D1, D2, D3, D4, D5, D6, D7, WR, RD, A3, CS | | | | $0.1V_{DD}$ | | V |
| Internal feedback resistance | RF | XIN, XOUT | | | | 1.0 | | MΩ |
| Current drain | $I_{DD}$ | | | | | 6 | 12 | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Bandpass Filter Characteristics** at Ta = 25°C, $V_{DD}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Input resistance | RMPX | | | 50 | | kΩ |
| Reference supply voltage output | VREF | Vref, Vdda = 3 V | | 1.5 | | V |
| BPF center frequency | FC | FLOUT | | 76.0 | | kHz |
| −3 dB band width | FBW | FLOUT | | 19.0 | | kHz |
| Group-delay in band width | DGD | FLOUT | | | ±7.5 | μs |
| Gain | Gain | FLOUT-MPXIN, f = 76 kHz | | 20 | | dB |
| Attenuation characteristic | ATT1 | FLOUT, f = 50 kHz | 25 | | | dB |
| | ATT2 | FLOUT, f = 100 kHz | 15 | | | dB |
| | ATT3 | FLOUT, f = 30 kHz | 50 | | | dB |
| | ATT4 | FLOUT, f = 150 kHz | 50 | | | dB |

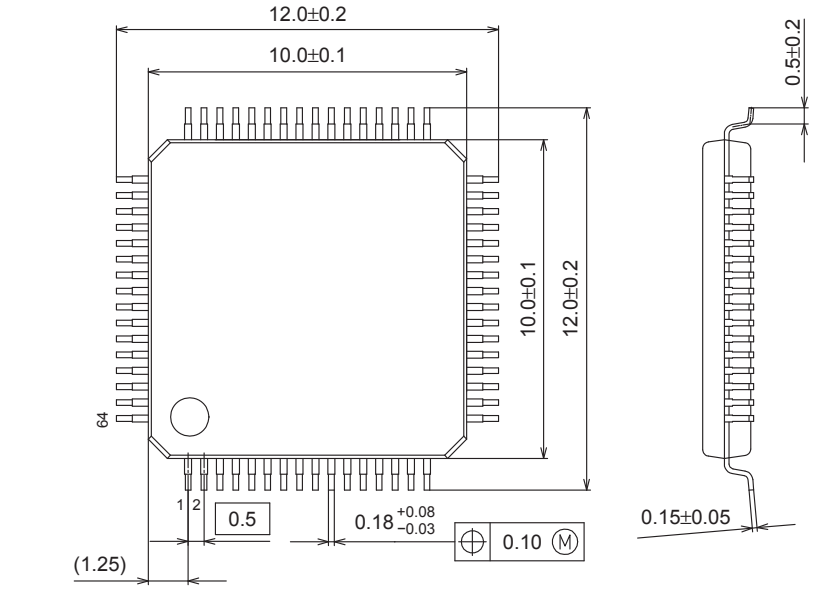
**Block Diagram**

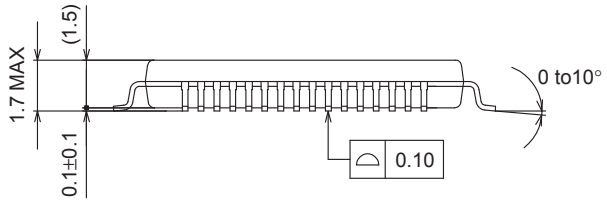


## Package Dimensions

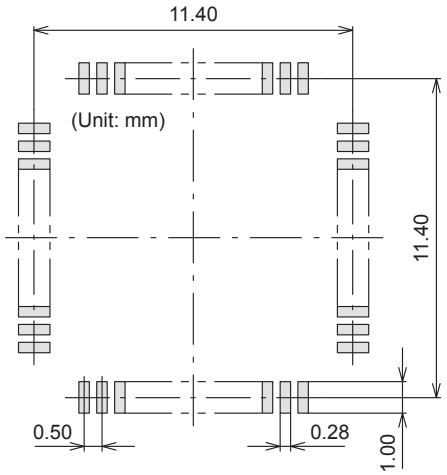
unit : mm

**SPQFP64 10x10 / SQFP64**
CASE 131AK
ISSUE A

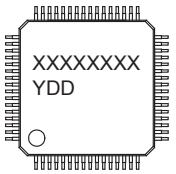


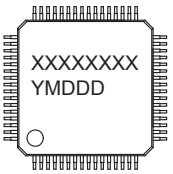

**SOLDERING FOOTPRINT***




**GENERIC MARKING DIAGRAM***




XXXXX = Specific Device Code
Y = Year
DD = Additional Traceability Data



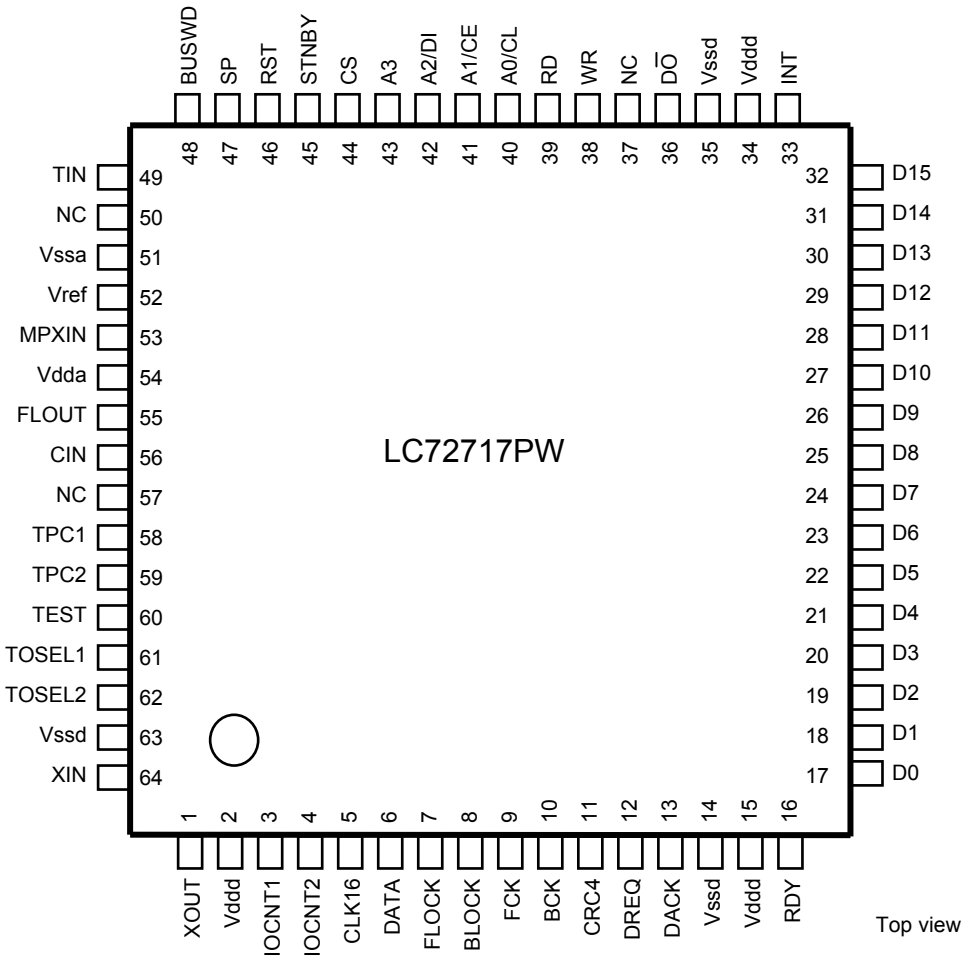

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## Pin Assignment




## List of Pin Functions

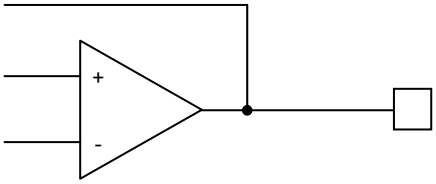
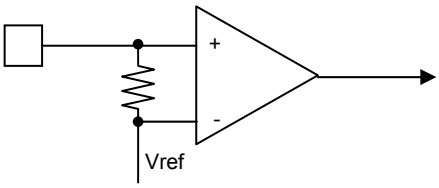
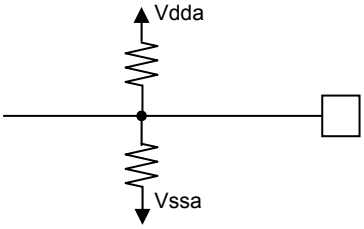
| Pin No. | Name of Pin | IO Form | State with RST="L" | Description of Functions |
|---|---|---|---|---|
| 1 | XOUT | O | Oscillation | Pin for system clock (crystal oscillator) |
| 2 | Vddd | - | - | Digital power pin |
| 3 | IOCNT1 | I | Input | Data bus I/O control 1 input pin (Parallel IF)<br>* Connect to Vssd when CCB IF (SP=H) is to be used. |
| 4 | IOCNT2 | I | Input | Data bus I/O control 2 input pin (Parallel IF)<br>* Connect to Vssd when CCB IF (SP=H) is to be used. |
| 5 | CLK16 | O | L | Clock regeneration monitor pin |
| 6 | DATA | O | L | Demodulation data monitor pin |
| 7 | FLOCK | O | L | Frame synchronization flag output pin (H: synchronized) |
| 8 | BLOCK | O | L | Block synchronization flag output pin (H: synchronized) |
| 9 | FCK | O | L | Frame start signal output pin |
| 10 | BCK | O | L | Block start signal output pin |
| 11 | CRC4 | O | H | Layer 4 CRC check result output pin |
| 12 | DREQ | O | H | DMA REQ signal output pin (parallel IF) |
| 13 | DACK | I | Input | DMA ACK signal input pin (parallel IF)<br>* Connect to Vddd when CCB IF (SP=H) is to be used. |
| 14 | Vssd | - | - | Digital GND pin |
| 15 | Vddd | - | - | Digital power pin |
| 16 | RDY | O | H | Read data READY signal output pin (parallel IF) |

Continued on next page.

Continued from preceding page.

| Pin No. | Name of Pin | IO Form | State with RST="L" | Description of Functions |
|---|---|---|---|---|
| 17 | D0 | I/O | Input | Data bus 0 to 7 I/O pins (parallel IF)<br>Bus width switched to 8 bits or 16 bits according to the BUSWD setting<br>* Connect to Vssd when CCB IF (SP=H) is to be used. |
| 18 | D1 | I/O | Input | |
| 19 | D2 | I/O | Input | |
| 20 | D3 | I/O | Input | |
| 21 | D4 | I/O | Input | |
| 22 | D5 | I/O | Input | |
| 23 | D6 | I/O | Input | |
| 24 | D7 | I/O | Input | |
| 25 | D8 | O | Hi-Z | Data bus 8 to 15 output pins (parallel IF)<br>* Output OFF for 8 bit bus width (BUSWD=L) |
| 26 | D9 | O | Hi-Z | |
| 27 | D10 | O | Hi-Z | |
| 28 | D11 | O | Hi-Z | |
| 29 | D12 | O | Hi-Z | |
| 30 | D13 | O | Hi-Z | |
| 31 | D14 | O | Hi-Z | |
| 32 | D15 | O | Hi-Z | |
| 33 | INT | O | H | Interrupt output pin for external CPU |
| 34 | Vddd | - | - | Digital power pin |
| 35 | Vssd | - | - | Digital GND pin |
| 36 | $D\overline{O}$ | O | Hi-Z(H) | $D\overline{O}$ output pin (CCB IF) |
| 37 | NC | - | - | NC pin (This pin must be open.) |
| 38 | WR | I | Input | Write control signal input pin (parallel IF)<br>* Connect to Vddd when CCB IF (SP=H) is to be used. |
| 39 | RD | I | Input | Read control signal input pin (parallel IF)<br>* Connect to Vddd when CCB IF (SP=H) is to be used. |
| 40 | A0/CL | I | Input | CL input pin (CCB IF)/ address input pin 0 (parallel IF) |
| 41 | A1/CE | I | Input | CE input pin (CCB IF)/ address input pin 1 (parallel IF) |
| 42 | A2/DI | I | Input | DI input pin (CCB IF)/ address input pin 2 (parallel IF) |
| 43 | A3 | I | Input | Address input pin 3 (parallel IF)<br>* Connect to Vssd when CCB IF (SP=H) is to be used. |
| 44 | CS | I | Input | Chip selector input pin (parallel IF)<br>* Connect to Vddd when CCB IF (SP=H) is to be used. |
| 45 | STNBY | I | Input | Standby mode input pin (H: standby) |
| 46 | RST | I | Input | System reset input pin (L: reset) |
| 47 | SP | I | Input | CCB/parallel setting input pin (H: CCB, L: parallel) |
| 48 | BUSWD | I | Input | Data bus width setting input pin (L: 8 bits, H: 16 bits) |
| 49 | TIN | I | Input | Test input pin (This pin must be connected to Vssd.) |
| 50 | NC | - | - | NC pin (This pin must be open.) |
| 51 | Vssa | - | - | Analog GND pin |
| 52 | Vref | AO | Vdda/2 | Reference voltage output pin (Vdda/2) |
| 53 | MPXIN | AI | Input | Baseband (multiplex) signal input pin |
| 54 | Vdda | - | - | Analog power pin |
| 55 | FLOUT | AO | Vdda/2 | Subcarrier output pin (76kHz BPF output) |
| 56 | CIN | AI | Input | Subcarrier input pin (comparator input) |
| 57 | NC | - | - | NC pin (This pin must be open.) |
| 58 | TPC1 | I | Input | Test input pin (This pin must be connected to Vssd.) |
| 59 | TPC2 | I | Input | Test input pin (This pin must be connected to Vssd.) |
| 60 | TEST | I | Input | Test mode setting pin (This pin must be connected to Vssd.) |
| 61 | TOSEL1 | I | Input | Test input pin (This pin must be connected to Vssd.) |
| 62 | TOSEL2 | I | Input | Test input pin (This pin must be connected to Vssd.) |
| 63 | Vssd | - | - | Digital GND pin |
| 64 | XIN | I | Oscillation | System clock pin (crystal oscillator/external clock input) |

## Internal Equivalent Circuit of Analog Pins

| Name of pin<br>Pin number in parentheses | Internal equivalent circuit |
|---|---|
| MPXIN(53) |  |
| FLOUT(55) |  |
| CIN(56) |  |
| Vref(52) |  |

### CPU Interface <CCB Mode>

CCB (Computer Control Bus), which is the ON Semiconductor original serial bus format for ON Semiconductor's acoustic LSIs, performs data input and output.
The CCB address is transmitted with CE= "L", acknowledging the CCB I/O mode when CE is set to "H".

(1) List of CCB modes

| CCB address | | | | | | | | | I/O mode | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| Hexadecimal | B0 | B1 | B2 | B3 | A0 | A1 | A2 | A3 | | |
| FAh | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | Input | 16-bit control data input |
| FBh | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | Output | Output of data corresponding to the input clock (CL) portion |
| FCh | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | Input | Layer 4 CRC check circuit data input (on the 8-bit units) |
| Fad | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | Output | Output of the register only |

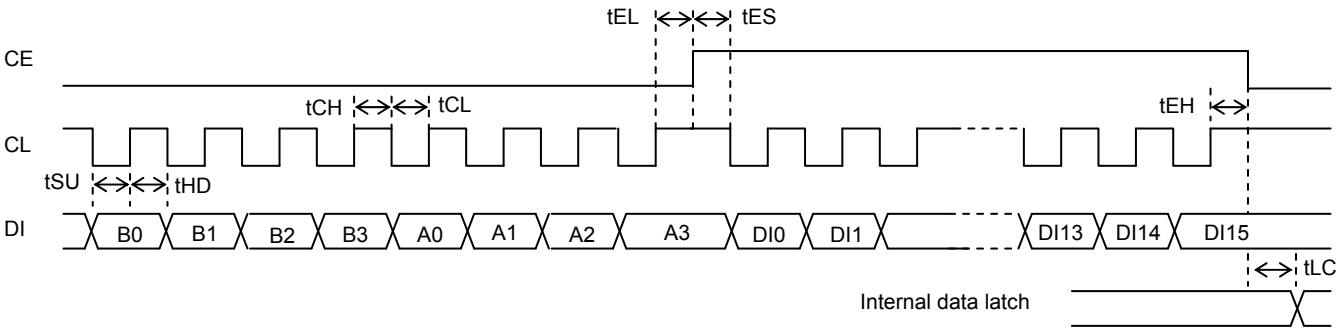
(2) Data input (CCB address FAh)

This is to set data to the LSI internal register. DI input includes both CCB address FAh and 16-bit data (DI0 to DI15) are input.

Assignment of each bit is as shown in the table below. Though DI12 to DI15 are invalid data, it is necessary to enter the arbitrary data so that the total of 16 bits can be obtained. For the contents of each register and register address, refer to the chapter of CPU registers.

(Note that writing into the layer 4 CRC check register will be described later (for the CCB address, use FCh.))

| (LSB) | | | Input data (8-bit) | | | | (MSB) | Register address | | | | Invalid data |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DI0 | DI1 | DI2 | DI3 | DI4 | DI5 | DI6 | DI7 | DI8 | DI9 | DI10 | DI11 | DI12 to DI15 |
| BIT0 | BIT1 | BIT2 | BIT3 | BIT4 | BIT5 | BIT6 | BIT7 | BIT0 | BIT1 | BIT2 | BIT3 | BIT4 to BIT7 |



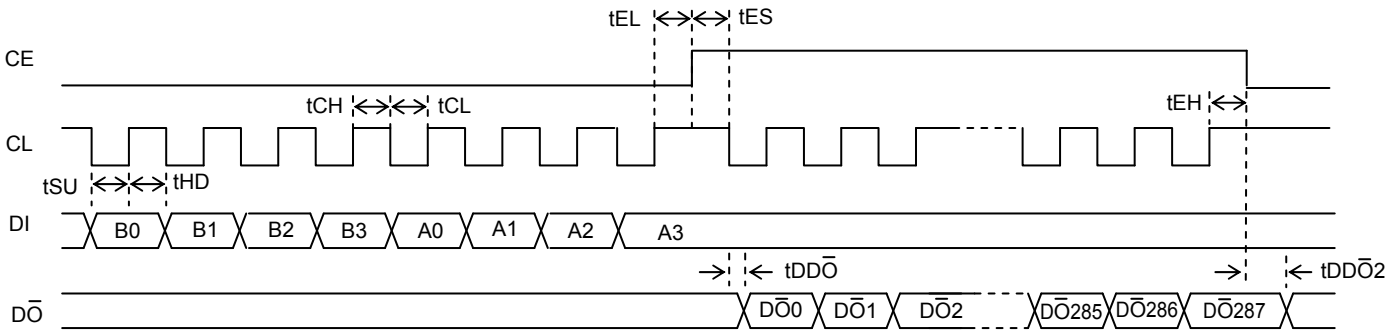

(3) Output of the corrected data (CCB address FBh)

The corrected packet data is output from LSI. The CCB address, FBh, is input in DI.

The valid data to be output is maximum 288 bits. If the clock input (CL input) is interrupted halfway to set CE to the "L" level, data output is not troubled by the next interrupt.

①The maximum data to be output is 288 bits (36 bytes) and the leading two bytes, to which the status register (STAT) contents and the block number register (BLNO) contents are added, are output.
②STAT and BLNO, which are the register contents outputs, are output respectively with LSB first.
③The corrected data is output sequentially beginning with the leading bit in data of one block.
④The BIC code is not output.
⑤In case of data reading for multiple times by one interrupt signal (INT), the output data is not guaranteed.

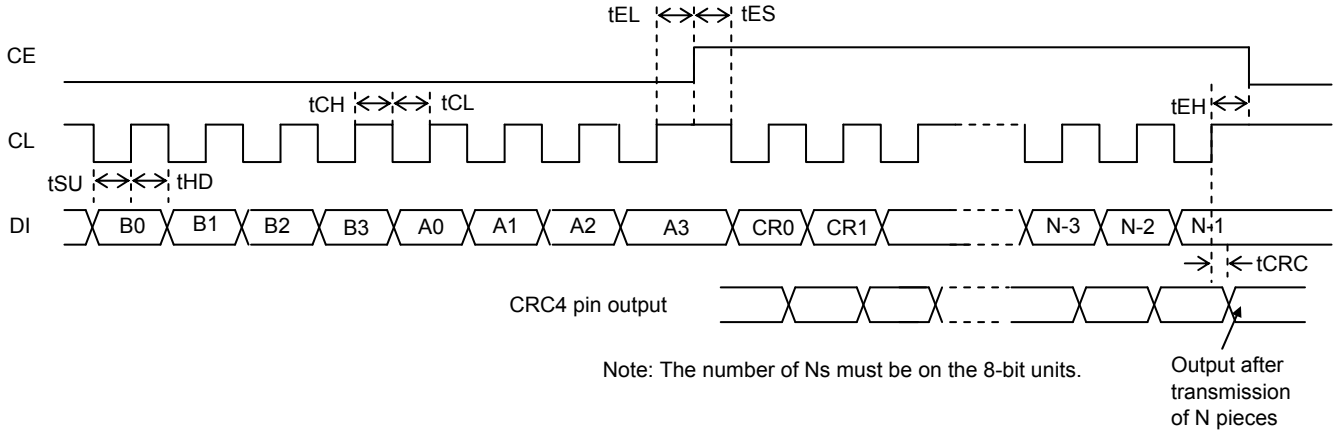
| STAT (8) | BLN0 (8) | Data block (176) | | Error-corrected data | Layer 2 CRC (14) | Parity (82) |
|---|---|---|---|---|---|---|
| $D\overline{O}0$ to $D\overline{O}7$ | $D\overline{O}8$ to $D\overline{O}15$ | $D\overline{O}16$ | to | $D\overline{O}191$ | $D\overline{O}192$ to $D\overline{O}205$ | $D\overline{O}206$ to $D\overline{O}287$ |




(4) Layer 4 CRC check circuit (CCB address FCh)

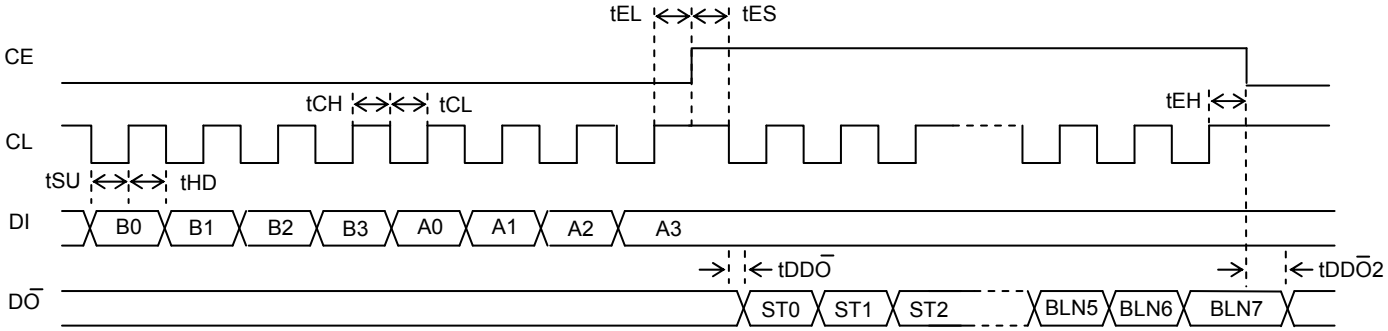
This is a function to detect the error in the data group (Layer 4 CRC), transmitting the data group of specified number of bytes, via the CCB interface, to LSI. The CCB address is FCh. In this case, it is not necessary to send register address.

The length of data group to be transmitted is on the 8-bit units. Here is not any upper limit (such as N pieces in the figure below) for the length of data to be transmitted at a time and data transmission can be divided into multiple times.




(5) Register output (CCB address Fad)

This is the dedicated register that can read only the status register (STAT) and block number register (BLNO) in LSI. To DI, the CCB address (Fad) is input. Data is output in order of the status register and the block number register.



| Symbol | Parameter | min | typ | max | unit |
|---|---|---|---|---|---|
| tCL | Clock “L” level time | 0.7 | | | μs |
| tCH | Clock “H” level time | 0.7 | | | μs |
| tSU | Data setup time | 0.7 | | | μs |
| tHD | Data hold time | 0.7 | | | μs |
| tEL | CE wait time | 0.7 | | | μs |
| tES | CE setup time | 0.7 | | | μs |
| tEH | CE hold time | 0.7 | | | μs |
| tLC | Data latch change time | | | 0.7 | μs |
| tDDO*1 | DO data output time | 135 | | 320 | ns |
| TDDO2 | DO data output off time | 135 | | | ns |
| tCRC | CRC4 change period | | | 0.7 | μs |

*1 DO data output change time from the “H” level to the “L” level. Output change time from the “L” level to the “H” level is determined by the external pull-up resistance value and load capacitance value.

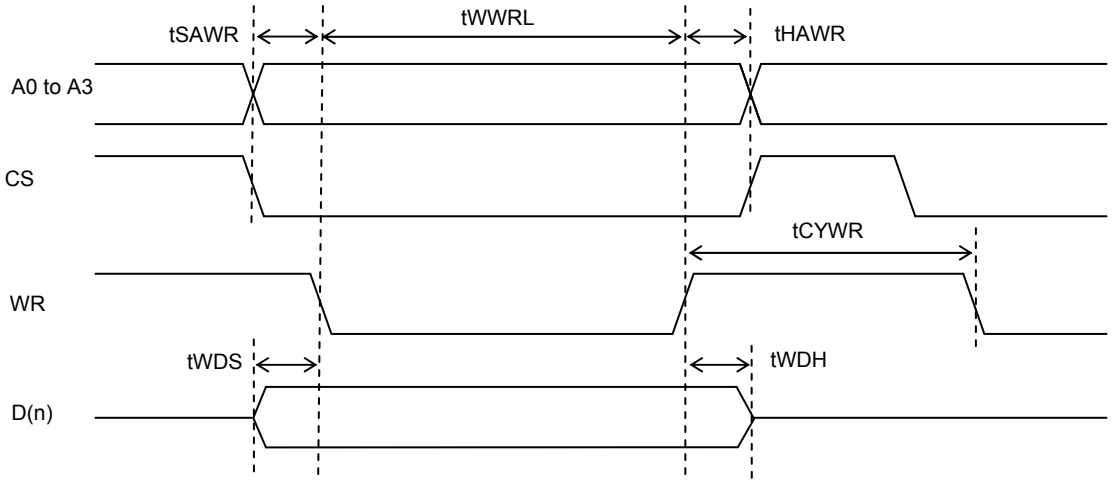
### CPU Interface <Parallel Mode>

This LSI can perform control via the parallel interface, in addition to the CCB interface. To use the parallel interface, it is necessary to set the SP pin = L. The data bus width can be selected with the BUSWD pin. (BUSWD pin - L: 8 bits, H: 16 bits)
The DMA transmission method can also be selected according to the setting of control register.

(1) Data input (register setting)

Data is set to the register in LSI. For accessing, input the register address to A0 to A3 pins and the write data to the D(n) pin.

Set the CS pin = L, and then the WR pin = L. Subsequently, by setting the WR pin = H and the CS pin = H after the tWWRL period, the data can be set to the register. It is necessary to keep an interval of tCYWR or more before the next data input.

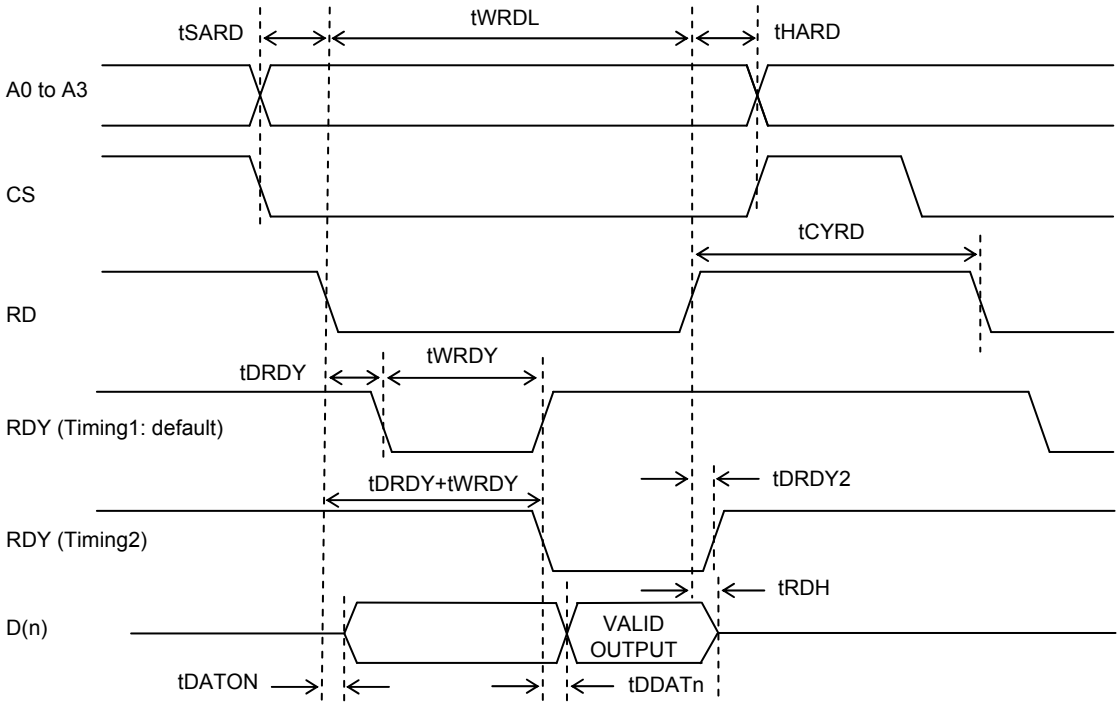


(2) Register output

This is to read data from the register in LSI. Only the status register (STAT) and block number register (BLNO) in LSI can be read.

For accessing, input the register address in A0 to A3, set the CS pin = L, and then the RD pin = L. This causes the RDY pin to change from “H” to “L”. Then, data is output from the D(n) pin after the RDY pin becomes “H”. It is necessary to keep an interval of tCYRD or more before the next data output. (n: 0-7 for BUSWD=L and 0 – 15 for BUSWD=H.)

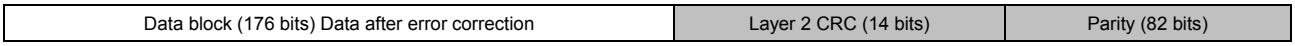
By setting bit 3 (RDY) = 1 of the control register 2, the RDY pin output method can be changed. In this case, the RDY pin changes from “H” to “L” in the timing enabling output of the acquired data and the pin returns to “H” after the end of data output (shown as Timing 2 in the figure).



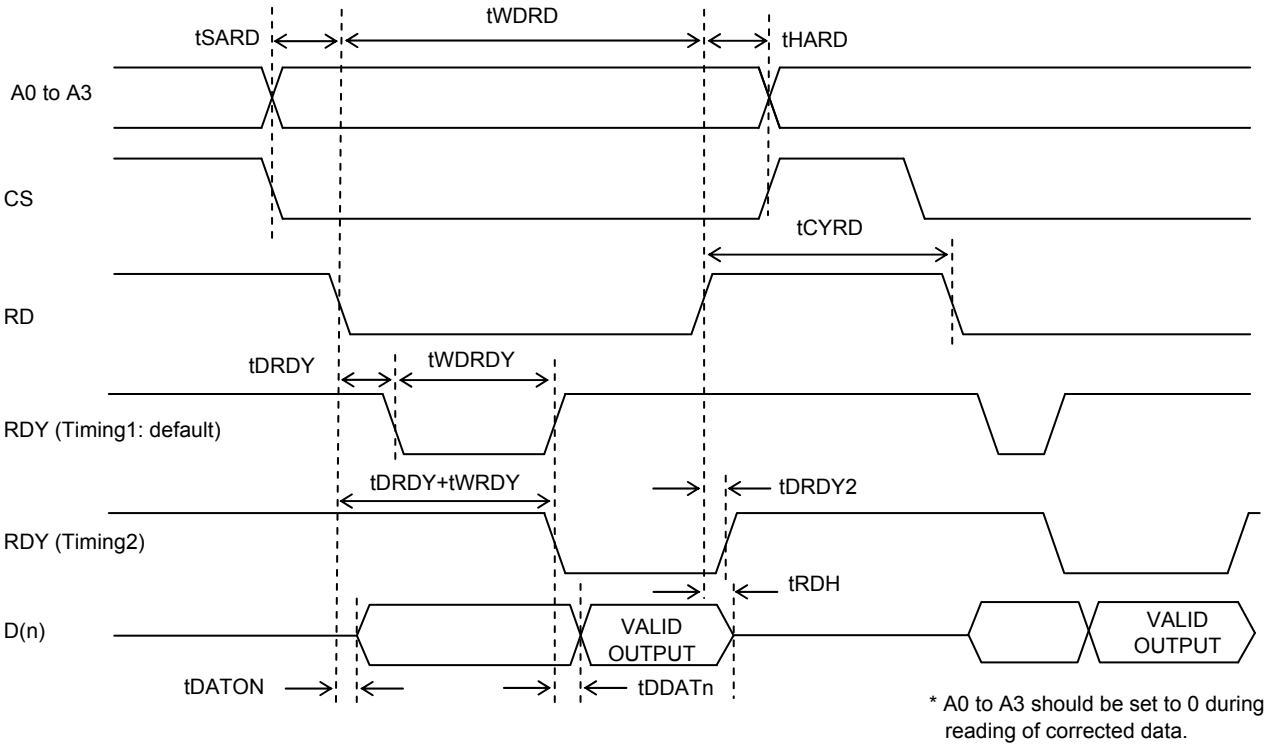
(3) Corrected data output

This is to output the packet data after correction processing from LSI. The total length of output data is 176 bits (22 Bytes) only, and the Layer 2 CRC data (14 bits) and parity data (82 bits) are not output. The corrected data is output, on either the 8-bit or 16-bit units, sequentially from the leading data among those in one packet. The BIC code is not output.

The accessing method is the same as for the register output and the address “0” is input to A0 to A3 pins. Since this is different from the register output in the timing conditions during access, the timing chart is shown here separately from the register output. The RDY signal output method can also be selected similarly.




Structure of a Single Data Packet (Total length 272 bits: BIC not included)




(4) Layer 4 CRC check output

This is a function to detect error of data group (layer 4 CRC). The CRC4 pin = “H” or bit1 (CRC4) = 1 of the status register after writing of the data group into the layer 4 CRC register means that there is no error. The accessing method is the same as for the data input when setting up an internal register, and the address “6h” of the layer 4 CRC register is input into the register address.

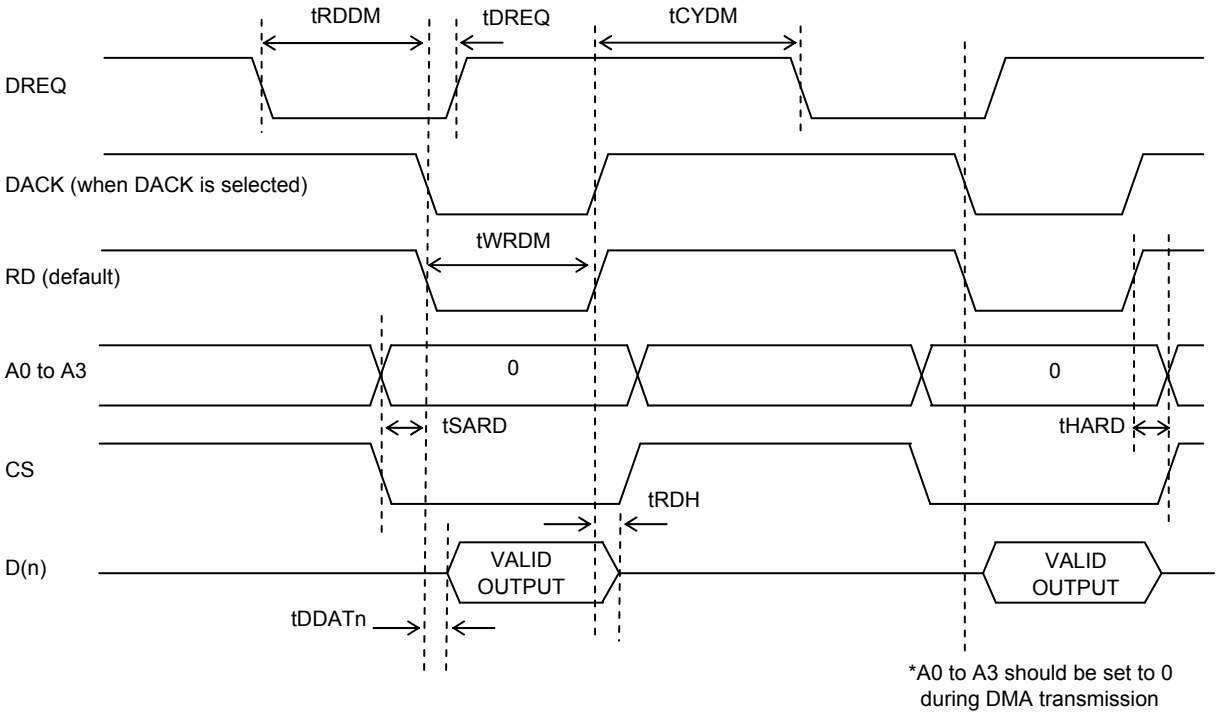
Note: WR cycle wait for writing in layer 4CRC register differs from the time of the data input of other register setup.

(5) DMA transmission output

Setting bit0 (DMA) = 1 of control register 2 causes the DMA mode, allowing the corrected data to be output in the DMA method.

For accessing, input the address “0h” to A0 to A3 pins after falling of the DREQ output pin, setting the CS pin = L, and then the RD pin = L. After the DREQ pin = H, data is acquired from the D(n) pin. Then, the wait state occurs for the tCYDM period or longer till the DREQ pin becomes “L”. In the DMA mode, only 8 bits can be selected for the data bus width. (n: 0 to 7 for BUSWD=L. Do not set BUSWD=H because it may cause fault.)

The DACK pin can be used instead of the RD pin for DMA transmission. In this case, it is necessary to set bit1 (DMA_RD) = 1 of the control register 2. It is also possible to change the polarity of DREQ and DACK pins. In this case, it is necessary to set bit4 (DREQ) = 1 and bit5 (DACK) = 1 of the control register 2.




| Symbol | Parameter | min | typ | max | unit |
|---|---|---|---|---|---|
| tSARD | Address and CS to RD setup | 20 | | | ns |
| tHARD *1 | RD to address and CS hold | 0 | | | ns |
| tWRDL | RD “L” level width | 340 | | | ns |
| tCYRD | RD cycle wait | 150 | | | ns |
| tWRDY | RDY width (at register output) | 60 | | 210 | ns |
| tRDH | RD data hold | 0 | | 40 | ns |
| tSAWR | Address and CS to WR setup | 20 | | | ns |
| tHAWR | WR to address and CS hold | 20 | | | ns |
| tCYWR | WR cycle wait | 150 | | | ns |
| | WR cycle wait(When writing data in Layer 4CRC register) | 1200 | | | ns |
| tWWRL | WR “L” level width | 200 | | | ns |
| tWDS | WR data setup | 0 | | | ns |
| tWDH | WR data hold | 20 | | | ns |
| tDRDY | RDY output delay | 0 | | 40 | ns |
| tDRDY2 | RDY output delay 2 | 0 | | 40 | ns |
| tWDRD | RD width at output of corrected data BUSWD=L (8bit) | 340 | | | ns |
| | RD width at output of corrected data BUSWD=H (16bit) | 620 | | | ns |
| tWDRDY | RDY width at output of corrected data BUSWD=L (8bit) | 60 | | 210 | ns |
| | RDY width at output of corrected data BUSWD=H (16bit) | 300 | | 490 | ns |
| tRDDM | DMA start time | 20 | | | ns |
| tDREQ | DACK to DREQ delay | | | 260 | ns |
| tDATON | DATn output start time | 0 | | 40 | ns |
| tDDATn | DATn output delay | 0 | | 40 | ns |
| tCYDM | DMA cycle wait | | | 420 | ns |
| tWRDM | RD “L” level width at DMA transmission output | 300 | | | ns |

*1 Specified up to the earliest negating of A0 to A3 and CS

## CPU Registers

This LSI has both write registers and read registers. Access to the registers is made via CCB IF or parallel IF. Switching of access mode is made with the SP pin. (CCB IF: SP=H, Parallel IF: SP=L)

(1) Write registers

Setting any data to ‘0h’ or ‘7h’ or larger address of Write-registers is prohibited. Do not set any data to these addresses.

• List of write registers

| ADR | R/W | Register Name | Description |
|---|---|---|---|
| 0h | - | - | Reserved (setting prohibited) |
| 1h | W | BIC | Allowable number of BIC errors |
| 2h | W | SYNCB | Block synchronization: error protection count |
| 3h | W | SYNCF | Frame synchronization: error protection count |
| 4h | W | CTL1 | Control register 1 |
| 5h | W | CTL2 | Control register 2 |
| 6h | W | CRC4 | Layer 4 CRC register (for the parallel IF only. CCB to use the dedicated address) |
| 7h and beyond | - | - | Reserved (setting prohibited) |

• 1h <BIC>: Number of allowable BIC errors <Write Only>

Register to set the allowable number of BIC error bits for determination of synchronization

| ADR | Register Name | Bit | Name | Description | Reset |
|---|---|---|---|---|---|
| 1h | BIC | 7-4 | BIC_F | Forward protection value (initial value 2)<br>Sets the allowable number of BIC error bits (when synchronized). | 0010b |
| | | 3-0 | BIC_B | Backward protection value (initial value 2)<br>Sets the number of allowable BIC error bits (when not synchronized). | 0010b |

When the block synchronization determination output (BLOCK) is to be used determination of whether or not there is any FM multiplex data, it is recommended to set the allowable number of BIC errors during backward protection to ‘0001b’ or ‘0000b’.

• 2h <SYNCB>: Block synchronization: error protection count <Write Only>

Register to set the number of block synchronization protections for determination of block synchronization.

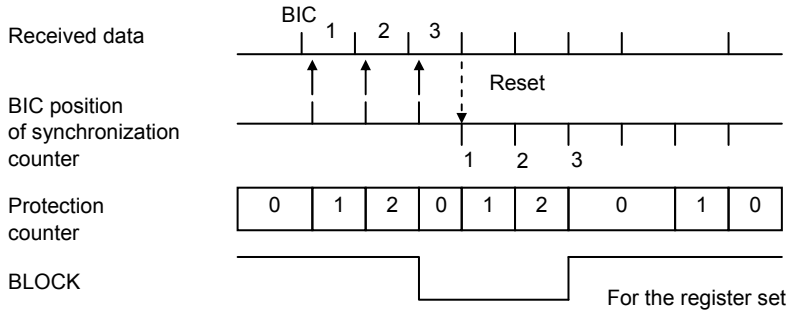
| ADR | Register Name | Bit | Name | Description | Reset |
|---|---|---|---|---|---|
| 2h | SYNCB | 7-4 | SYNCB_B | Backward protection value (Register initial value 1: Number of backward protections 2)<br>Number of backward protections = Backward protection value +1 | 0001b |
| | | 3-0 | SYNCB_F | Forward protection value (Register initial value 7: Number of forward protections 8)<br>Number of forward protections = Forward protection value +1 | 0111b |

To change the set value, it is necessary to set the value determined by deducting 1 from the desired number of protections.

The number of forward and backward protections can be set separately. The conditions for counting the number of protections are as follows:

- Number of backward protections (not synchronized): BLOCK=L)
  When the timing of the free-run counter for LSI internal synchronization agrees with that of received BIC, the protection counter is incremented by 1. Similarly, when the timing between the LSI internal counter and the received BIC is lost, the protection counter is cleared to zero. The count timing is the timing of the LSI internal counter.
- Number of forward protections (synchronized: BLOCK=H)
  Contrarily to the case of backward protection, the number of protections is counted up when the timing of LSI internal free-run counter is deviated from the received BIC detection timing. The number of protections is cleared to zero when they agree.

The figure below shows the agreement/disagreement between the LSI internal timing and received BIC timing and the relationship between the protection counter value and BLOCK signal.
For the number of forward/backward protections of 3, the protection counter value at a timing of BLOCK signal changeover is 2, that is, smaller by 1. The number of protections is determined in the internal circuit by comparing the register set value for the number of forward/backward protections and the protection counter. Accordingly, the register set value must be set to the value smaller than the desired number of protections by 1.
For example, when the number of both forward and backward protections is 3 as shown below, it is necessary to set '22h'. If the set value is '00h', the number of protections becomes 1 by definition for forward and backward protections. However, the operation becomes the same as for the state without the protection circuit.
When the block synchronization flag output (BLOCK) is to be used for determination whether or not there is FM multiplex data, it is recommended to reset the value severer than the initial value.




For the register set value of 22h:
the number of both the forward and backward protections become 3.

- 3h <SYNCF>: Frame synchronization: error protection count <Write Only>
  Register to set the number of frame synchronization protections for determination of frame synchronization

| ADR | Register Name | Bit | Name | Description | Reset |
|---|---|---|---|---|---|
| 3h | SYNCF | 7-4 | SYNCF_B | Backward protection value<br>(Register initial value 1: Number of backward protections 2)<br>Number of backward protections = Backward protection value +1 | 0001b |
| | | 3-0 | SYNCF_F | Forward protection value<br>(Register initial value 7: Number of forward protections 8)<br>Number of forward protections = Forward protection value +1 | 0111b |

To change the set value, it is necessary to set the value determined by deducting 1 from the desired number of protections. This LSI detects BIC peculiar change points exist at four points in one frame and increases/decreases the counts of protection counter by determining agreement/disagreement with the timing counter for LSI internal frame synchronization.

• 4h <CTL1>: Control register 1 <Write Only>

Register to control the block reset ON/OFF, function activation/stop, and the data output method.

| ADR | Register Name | Bit | Name | Description | Reset |
|---|---|---|---|---|---|
| 4h | CTL1 | 7 | CRC4_RST | Layer 4 CRC check circuit reset setting<br>1: Reset ON 0: Reset OFF<br>To cancel reset, it is necessary to set 0. | 0 |
| | | 6 | DO̅ _MOVE | Sets the DO̅ pin output method changeover<br>0: Hi-Z state retained in states other than data output<br>1: Changes in an interlocked manner with the INT signal *6 | 0 |
| | | 5 | INT_MOVE | Sets changeover of corrected data output method *4<br>0: Outputs only data received at completion of correction & layer 2 CRC completion as well as during synchronization<br>1: Outputs all of data | 0 |
| | | 4 | SYNC_RST | Synchronization regeneration circuit reset setting *1<br>1: Reset ON 0: Reset OFF<br>0 to be set to cancel reset | 0 |
| | | 3 | EC_STOP | Error correction function down setting *2<br>0: All functions activated<br>1: Only MSK detector circuit and synchronization regeneration circuit activated | 0 |
| | | 2 | VEC_HALT | Vertical error correction function down function *3<br>0: Executes vertical error correction and second horizontal correction.<br>1: Does not execute vertical error correction and second horizontal correction. | 0 |
| | | 1 | RTIB | Real-time information block setting *5<br>0: Real-time information blocks present.<br>1: No-real-time information block. | 0 |
| | | 0 | FRAME | Frame setting<br>0: Specifies method B.<br>1: Specifies method A. | 0 |

*1 With SYNC_RST=1, the synchronization status and the synchronization protection status are cleared, resulting in the unsynchronized state. This function enables rapid pull-in of frame synchronization when the frame synchronization of new tuned and received data is deviated during tuning of a radio receiver. In this case, registers such as the number of allowable BIC errors, the number of block forward/backward protections, and the number of frame forward/backward protections are not initialized. During reset, the INT signal is not output and the DO pin becomes the HI-Z output.

*2 With EC_STOP=1, all of operations and data output related to error correction is shut down. MSK demodulation, synchronization circuits, serial data input, and layer 4 CRC circuit remain operative.

*3 With VEC_HALT=1 setting, all of LSI operation related to vertical correction and second horizontal correction are shut down. Only the data after first horizontal correction is output.

*4 Since the output mode will be modified depending on the setting of the VEC_OUT flag or the result of horizontal error correction, refer to the “List of operation modes” section for detail.

*5 In the ITU-R recommended frame structure method A, a total of 12 data blocks can be inserted in the parity data area (the area that consists of 82 consecutive blocks of parity packets). If this IC is used ina system that has no real-time information blocks (RTIB), this flag must be set.

Note that if this flag is changed, frame synchronization is retained in the synchronized state for the time corresponding to the forward protection count, and then switches to the unsynchronized state. To quickly reestablish frame synchronization, applications must reset the synchronization circuit using the SYNC_RST flag.

*6 About the relationship between INT and DO̅, refer to the “Output Format with DO̅_MOVE=1”section in the “Error Correction” chapter.

• 5h <CTL2>: Control register 2 <Write Only>

Register to control the parallel IF setting, vertically-corrected data output method, etc.

| ADR | Register Name | Bit | Name | Description | Reset |
|---|---|---|---|---|---|
| 5h | CTL2 | 7 | Reserved | Either keep an initial value or set it to 0. | 0 |
| | | 6 | BLK_RST | Block synchronization circuit reset setting *1<br>1: Reset ON 0: Reset OFF<br>0 to be set to cancel reset | 0 |
| | | 5 | DACK | DACK signal polarity setting (effective for SP=L only)<br>0: Negative logic for DACK signal polarity<br>1: Positive logic for DACK signal polarity | 0 |
| | | 4 | DREQ | DREQ signal polarity setting (effective for SP=L only)<br>0: Negative logic for DREQ signal polarity<br>1: Positive logic for DREQ signal polarity | 0 |
| | | 3 | RDY | RDY signal timing setting (effective for SP=L only)<br>0: Outputs the RDY signal in the timing 1.<br>1: Outputs the RDY signal in the timing 2. | 0 |
| | | 2 | VEC_OUT | Vertically error corrected data output method changeover setting *2<br>0: No vertically error corrected output if vertical error correction has not been made<br>1: All data output even when vertical error correction has not been made | 0 |
| | | 1 | DMA_RD | DMA read control signal selection setting (effective for SP=L only)<br>0: RD signal used<br>1: DACK signal used | 0 |
| | | 0 | DMA | DMA transmission function enable setting (effective for SP=L only)<br>0: DMA transmission not used for reading of corrected data<br>1: DMA transmission used for reading of corrected data | 0 |

*1 With BLK_RST=1, the block synchronization state and block synchronization protection counter value are cleared. But this does not affect the functions related to frame synchronization.

*2 With VEC_OUT=1, one frame of data completely free from error. The data similar to the horizontally-corrected data is output in the timing of output of vertically-corrected data even when vertical correction has not been made.

• 6h <CRC4>: Layer 4 CRC register <Write Only>

Register for data group writing to check the layer 4 CRC.

Used on with the parallel IF. The dedicated CCB address is to be used for CCB IF.

| ADR | Register Name | Bit | Name | Description | Reset |
|---|---|---|---|---|---|
| 6h | CRC4 | 7 | CRCDAT7 | Layer 4 CRC check data setting<br>By writing value consecutively into this register, the layer 4 CRC check of data group comprising multiple bytes can be made.<br><br>The CRC checked results can be known by checking the CRC4 flag in the status register or CRC4 pin output. | 0 |
| | | 6 | CRCDAT6 | | 0 |
| | | 5 | CRCDAT5 | | 0 |
| | | 4 | CRCDAT4 | | 0 |
| | | 3 | CRCDAT3 | | 0 |
| | | 2 | CRCDAT2 | | 0 |
| | | 1 | CRCDAT1 | | 0 |
| | | 0 | CRCDAT0 | | 0 |

(2) Read registers

• List of read registers

| ADR | R/W | Register Name | Description |
|---|---|---|---|
| 0h | R | PDATO | Input this address into A0 to A3 after reading of error-corrected data |
| 1h | R | STAT | Status register |
| 2h | R | BLNO | Block number register |
| 3h and beyond | - | - | Reserved |

Parallel mode: To read registers, send address shown in the list of read registers.
CCB mode: To read registers, send assigned CCB address (FBh or Fad). It is not necessary to send address shown in the list of read registers.

• 1h <STAT>: Status register <Read Only>
Register to confirm various states

| ADR | Register Name | Bit | Name | Description | Reset |
|---|---|---|---|---|---|
| 1h | STAT | 7 | VH | Determination on vertically error corrected data<br>0: Data for which only horizontal correction is performed<br>1: Data for which vertical and second horizontal correction after horizontal correction are performed | 0 |
| | | 6 | BLK | Block synchronization state<br>0: Data that is received when block synchronization is not established<br>1: Data that is received when block synchronization is established | 0 |
| | | 5 | FRM | Frame synchronization state<br>0: Data that is received when frame synchronization is not established<br>1: Data that is received when frame synchronization is established | 0 |
| | | 4 | ERR | Error correction state<br>0: Data whose correction is completed and for which error is not detected by the layer 2 CRC check<br>1: Data whose correction is impossible or for which error is detected by the layer 2 CRC check. | 0 |
| | | 3 | PRI | Determination of parity block<br>0: Data that is estimated to be data block by the frame synchronization circuit<br>1: Data that is estimated to be parity block by the frame synchronization circuit | 0 |
| | | 2 | HEAD | Frame head determination<br>1: Data that is estimated to be the frame head block by the frame synchronization circuit<br>0: Data other than above | 0 |
| | | 1 | CRC4 | Layer 4 CRC check result<br>0: Error in layer 4 CRC check result<br>1: No error in layer 4 CRC check result | 1 |
| | | 0 | RTIB | Real-time information block state<br>1: Indicates the data is a real-time information block.(This bit is valid only in method A'.)<br>0: The others | 0 |

The value in the "Reset" column is the readable value immediately after canceling the reset.

• 2h <BLNO>: Block Number register <Read Only>
Register to confirm the output data block Number

| ADR | Register Name | Bit | Name | Description | Reset |
|---|---|---|---|---|---|
| 2h | BLNO | 7 | BLN7 | Indicates the block Number or parity block Number of output data | 0 |
| | | 6 | BLN6 | | 0 |
| | | 5 | BLN5 | Data block Number 0 to 189 | 0 |
| | | 4 | BLN4 | Parity block Number 0 to 81 | 0 |
| | | 3 | BLN3 | | 0 |
| | | 2 | BLN2 | | 0 |
| | | 1 | BLN1 | | 0 |
| | | 0 | BLN0 | | 0 |

The value in the “Reset” column is the readable value immediately after canceling the reset.

• Data renewal timing of read register
The timing for rewriting of read register (STAT, BLNO) data is the timing for changing of INT from H to L.

• Read procedure of corrected data
Normally, the status register is first read because of occurrence of interrupt to check the condition of corrected output data that is output by the interrupt signal, determining whether or not read is necessary. For example, read is not made till the next interrupt if the error correction result is NG and read is not necessary.
For CCB IF, data read is made at the CCB address, ‘FBh’, and determination is made by means of the status information added by 16 bits to see if the subsequent data is to be read. When interrupting read, set the CE signal to “L”.
It is possible to read the register in a manner a synchronous with the interrupt signal when INT_MOVE is set to “1”. For example, to check the current receiving state, read the status register to check BLK (data received during block synchronization) and FRM (data received during frame synchronization). In this case, read data is more close to the current receiving state, when VH=0 (data subject to horizontal correction only) information is used.

• Layer 4 CRC check
To perform layer 4 CRC check, the data group to be checked is transmitted. After transmission, it is determined that the data group is free from error if the CRC4 pin becomes the H-level output or the status register CRC4 (layer 4 CRC check result) is ‘1’.
The CRC4 pin or CRC4 flag of status register is either “H” or “1” when all bits of check register in LSI are “0”. To perform layer 4 CRC check using this function, it is necessary to initialize the CRC check register in LSI before transmission of one group of one data group. Initialization is made by setting the CRC4_RST (layer 4 CRC check circuit reset) of control register to ‘1’.
Subsequently, to transmit the layer 4 CRC check data, set CRC4_RST back to 0 to cancel reset.

The generating polynomial of CRC code is as follows: $G(X) = X^{16} + X^{12} + X^5 + 1$

## Error Correction

(1) Error Correction and Output Conditions of Error-corrected Data (in the default state)

The received data is subject to error detection by the layer 2 CRC and error correction by the (272,190) code for each one block (272 bits). At the end of correction, preparation for transmission to CPU is made and the INT signal is output. This is called “horizontal correction”.

In the default state, this INT signal is output only when the output data concerned meets all of three conditions as follows:

①Data whose error correction is completed and for which layer 2 CRC detects no error
②Data received during block and frame synchronizations
③Data in the data packet
*Depending on the register mode setting, horizontally-corrected data may be output regardless of conditions of ① to ③ above.

When horizontal correction cannot cover completely, correction by the product code is made frame by frame. For data that cannot be horizontally corrected, the second horizontal correction is made.
This series of operations is called “vertical correction”. Conditions for the data obtained from vertically-corrected output are as follows in the default state:

①Data that cannot be corrected by horizontal correction, but that has been completely corrected by the vertical correction
②Data in the data packet

Accordingly, horizontally-corrected data is not output. Packet data that cannot be corrected horizontally or vertically is not output. The parity packet data after vertical correction is not output either.
Vertical correction is applied to the whole packet data that have been received during frame synchronization, and is executed when horizontal correction cannot correct all packet (block) data. Vertical correction is not made when the error-free data is received for one frame or when the received data is not synchronous in flame synchronization during reception. For the packet whose error has been corrected by horizontal correction and any error-free packet, vertical correction is not made to prevent faulty correction.
In the default setting, the applicable vertically-corrected output is not output when vertical correction has not been made.

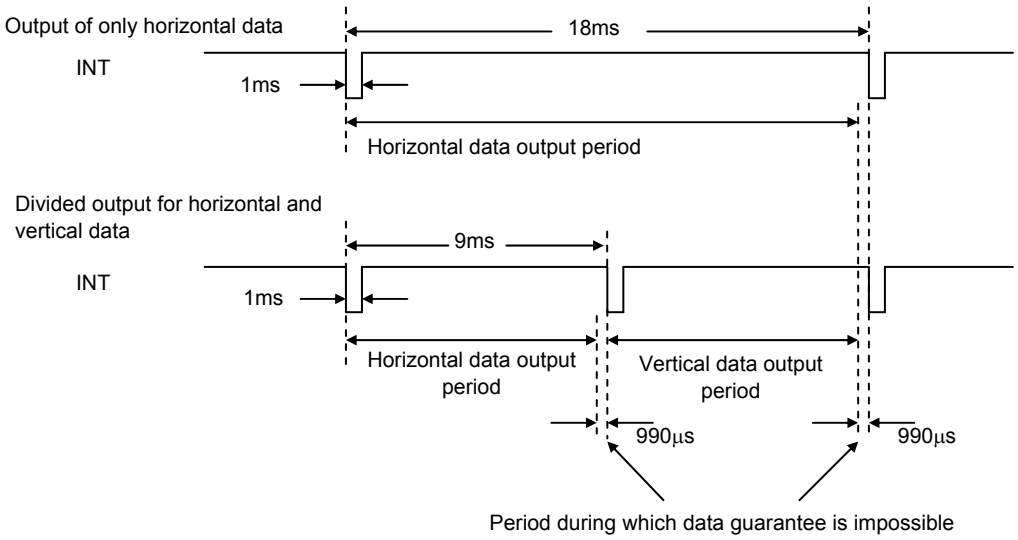
* Depending on the register mode setting, the vertically-corrected data may be output regardless of whether or not vertical correction is to be made.

(2) Error-corrected Data Output Timing (Basic Restrictions)

Data received by LSI is corrected error and written sequentially without any interruption into the output data buffer memory. Since this data buffer memory has a capacity for one-block data, the corrected data before reading is over-written by the next data if data read is delayed. In consequence, it is essential to read data according to the timing stipulations shown below.

This LSI specifies the output timing for each of horizontally and vertically corrected data as follows:

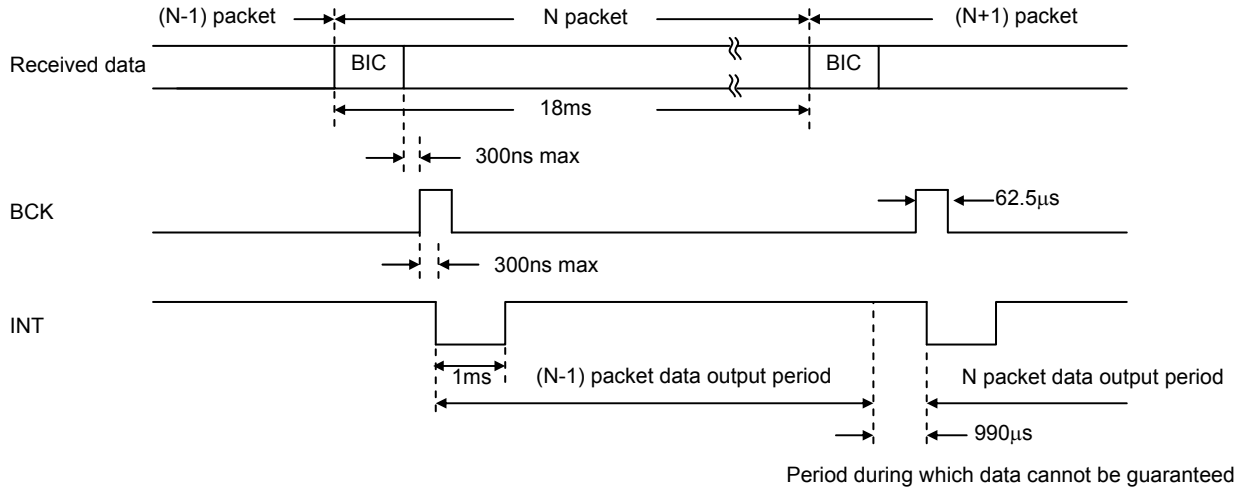
①Upon completion of preparation for the output data, LSI lowers the INT pin to “L” as a request for transmission.
②Data output has the period during which only horizontal data can be read and the period during which horizontal and vertical data are read according to the time division.
③Complete data transmission within about 8ms after INT = “L”. When only the horizontally-corrected data can be output, data transmission is possible for about 17ms. Even when CPU is in the course of reading, the output buffer is overwritten by the next output data once the specified time period is expired.
④The data amount that can be read by one horizontal and vertical transmission request (INT) is one block only. Vertically-corrected data is output sequentially beginning with the first block after completion of vertical correction, but the data of parity block is not output.



(3) Horizontally-corrected Data Output Timing (Relationship With The Received Data)

The timing relationship between the received data and interrupt control signal (INT) for horizontary-corrected data output is shown. But the delay from the actual received signal caused by demodulation in the MSK demodulation block is ignored.

Block synchronization is established by determining the BIC code. Data of the Nth packet can be output during receiving of the next (N + 1) packet data.



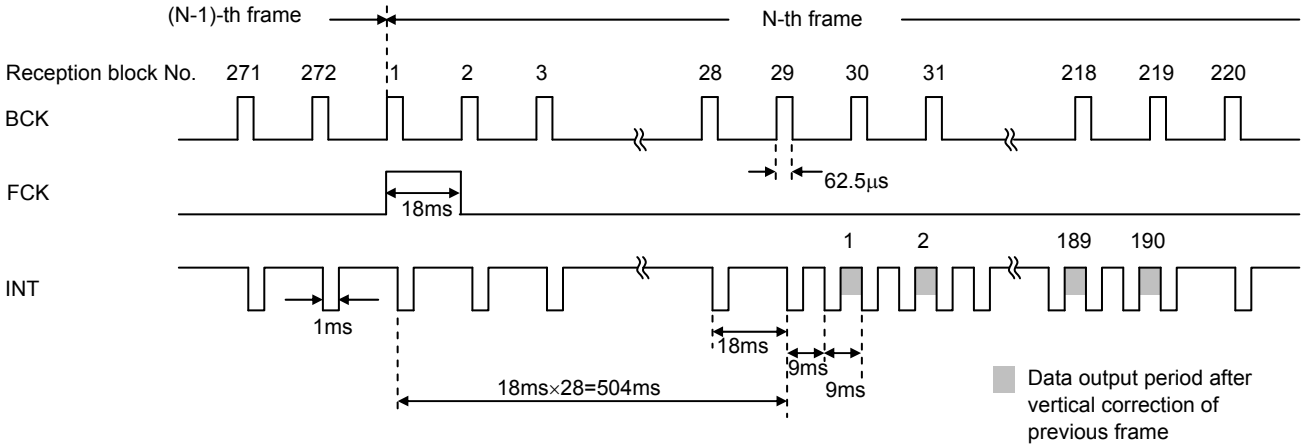

(4) Vertically-corrected Data Output Timing

Vertical correction is made when the data of one frame is stored in the memory, frame synchronization has been established, and when horizontal correction cannot correct all of packet data. Vertical correction start timing is the head of a frame. During receiving of the first to 28$^{th}$ packets of the N-th frame, horizontal correction of each packet is made, transferring data to the CPU interface. Using the idling time in this period, vertical correction of the previous (N-1)-th frame data is made.

Vertically-corrected data is output for the amount equivalent to 190 blocks sequentially beginning with reception of the 29$^{th}$ packet (block), in such a manner that one block data is output each time one block is received. Only data of data block in the FM multiplex broadcasting frame is output.

The final 190$^{th}$ block is output during reception of the 218$^{th}$ block.

In the vertically-corrected data output timing, the packet data corrected by vertical correction is not output (INT not issued). However, vertical correction data output order is not shortened for the amount equivalent to the packet data that is not output. For example, if the first to 100$^{th}$ data packets have been horizontally corrected, the 101$^{st}$ vertically corrected packet data is output, not at the reception point of the block Number 29 $^{th}$, but at the 129$^{th}$ packet data reception point.



(5) List of Operation Modes

Depending on the set value of INT_MOVE (bit 5 of control register 1) and VEC_OUT (bit 2 of control register 2), the INT signal output timing and output data are modified. In the table below, ○ indicates “output”, × indicates “no output.” and - indicates “none applicable.”

| Parameter | INT_MOVE | VEC_OUT | Horizontal correction result | Horizontally-corrected output | | | Vertically-corrected output | |
|---|---|---|---|---|---|---|---|---|
| | | | | OK data | NG data | Parity | OK data | NG data |
| Default value | 0 | 0 | OK | ○ | - | × | × | - |
| | | | NG | ○ | × | × | ○ *1 | × |
| Mode 1 | 1 | 1 | OK | ○ | - | ○ | ○ *2 | - |
| | | | NG | ○ | ○ | ○ | ○ *2 | ○ |
| Mode 2 | 1 | 0 | OK | ○ | - | ○ | × *3 | - |
| | | | NG | ○ | ○ | ○ | ○ *4 | ○ |
| Mode 3 | 0 | 1 | OK | ○ | - | × | ○ | - |
| | | | NG | ○ | × | × | ○ | × |

*1 Only data whose horizontal correction result is NG and whose vertical correction result is OK is output.

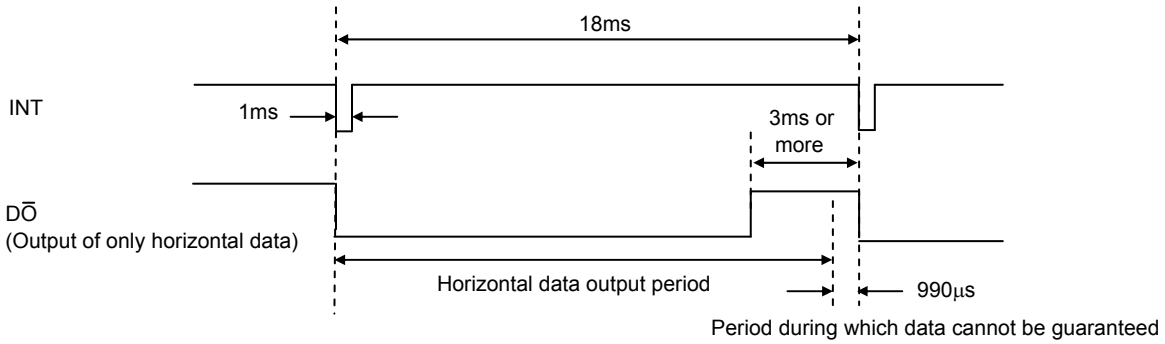
*2 All of vertically-corrected outputs (190 blocks/frame) are output, in both cases of horizontal correction result of OK and NG, regardless of whether the vertical correction result is OK or NG.

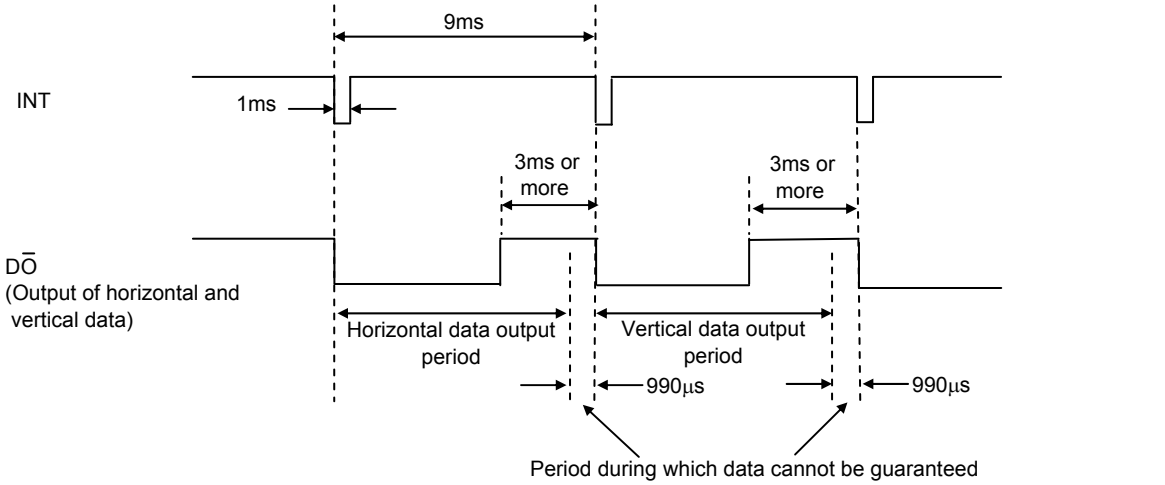
*3 The vertically-corrected data is not output when there is no data that is determined to be NG because all the horizontal correction results are OK.

*4 When there is any data whose horizontal correction result becomes NG, all of vertically-corrected outputs (190 blocks/frame) are output regardless of whether the vertical correction result is OK or NG.

(6) Output Format with $D\overline{O}$_MOVE=1

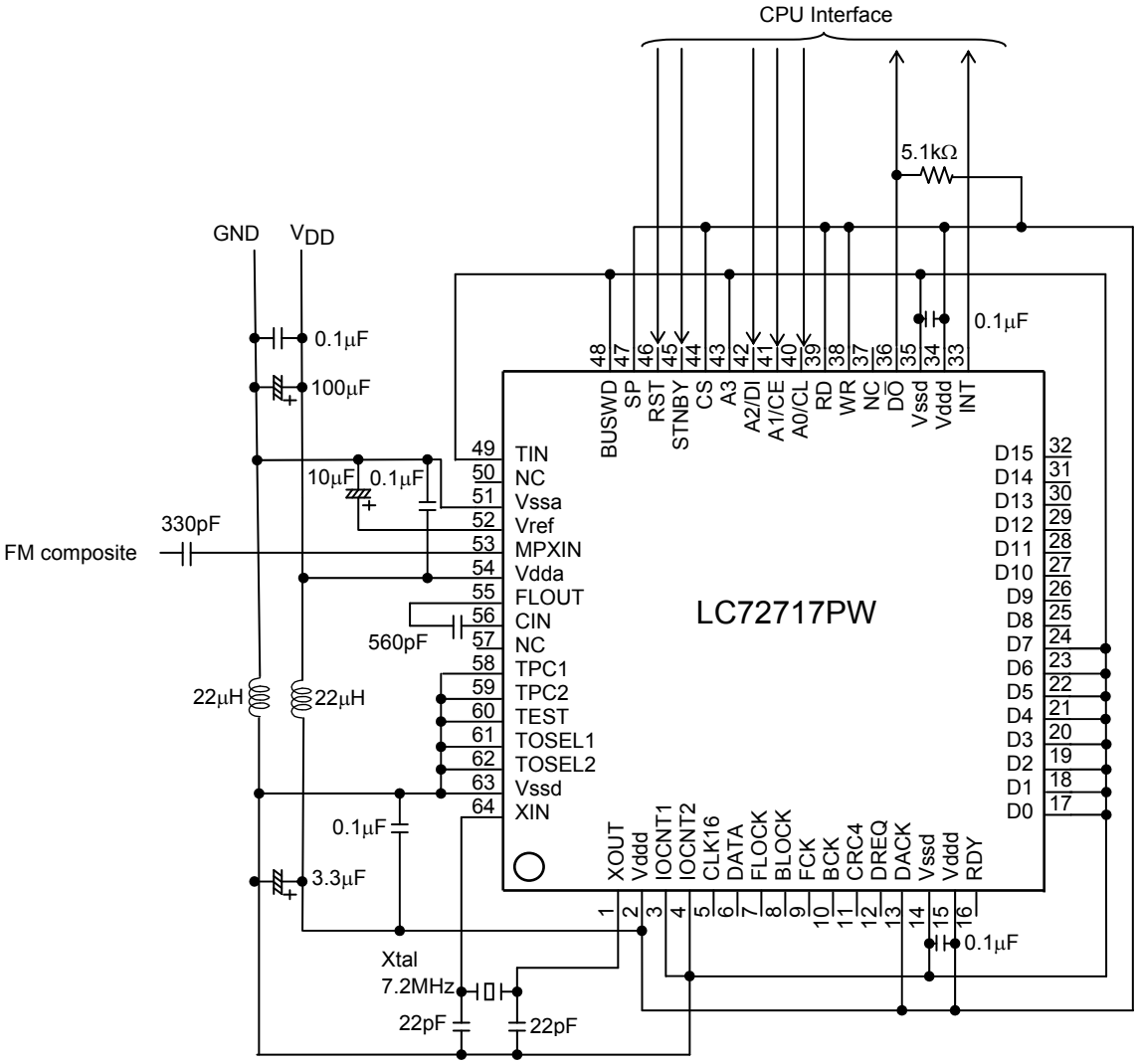
The relationship between INT and $D\overline{O}$ is shown below. $D\overline{O}$ becomes “L” in synchronous with the falling edge of INT, and return to “H” before 3ms or more against the next falling edge of INT. Therefore, when the data read is started while $D\overline{O}$ is “L”, there is margin time 3ms or more against the falling edge of INT. This timing diagram is for the case when the data read is not performed. When the data read is performed, $D\overline{O}$ returns to “H” after completion of read.



### Example of an application circuit diagram

This is an application circuit example when the CCB serial interface is selected, using a microcomputer operating on the supply voltage of 3V.
The $D\overline{O}$ pin must be pulled up by a resistor to the supply voltage.




<Note>

(1)This example of an application circuit is a circuit of reference, and does not guarantee the characteristic.

(2)The capacitance value to be connected to the above crystal oscillator is the reference value.
Before use, confirm by crystal supplier that oscillation is free from trouble using the actual substrate.

(3)A bypass capacitor needs to be connected near the power supply terminal.

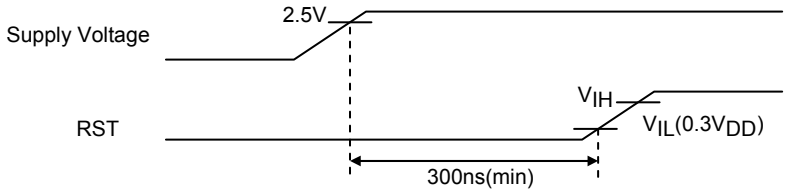
## Cautions

### Operation at Reset and Standby

(1) Reset signal

After crystal was oscillated and stabilized, reset operation is performed by setting the RST pin input level to $V_{IL}$ or less for 300ns or more at the supply voltage ($V_{DD}$) of 2.5V or more. (See the figure below).

Be sure to perform reset operation at power ON.




(2) Pin state at reset

Refer to the list of pin functions.

(3) Reset operation range

The reset signal causes reset inside LSI, causing return to the initial state. Though the crystal oscillation circuit is not stopped, the internal divider circuit is stopped.

(4) Data input after reset

If 300ns or more time has elapsed after completion of reset, the register write control circuit is ready for activation.

(5) Standby mode

Set the STNBY pin to the “H” level, and LSI enters the standby mode. In this mode, all of LSI operations can be stopped. After canceling of STNBY, the time is required till the crystal oscillation circuit becomes stable.

Digital pin output states during standby is the same as for that dueing reset. On the other hand, analog output pins (FLOUT, VREF) are L outputs (Vdda/2 is output during reset).

Similarly to the case of reset, the LSI inside is reset to return to the initial state.

## ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---|---|---|
| LC72717PW-H | SQFP64(10X10)<br>(Pb-Free / Halogen Free) | 500 / Tray Foam |
| LC72717PW-NH | SQFP64(10X10)<br>(Pb-Free / Halogen Free) | 1000 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

- The DARC (Data Radio Channel) FM multiplex broadcast technology was developed by NHK (Japan Broadcasting Corporation).
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- DARC and the logo shown on the right-hand side can be displayed on electronic equipment that uses DARC technology by the conclusion of a contract with NHK-ES.

Please contact NHK Engineering System, Inc. for further details.

Contact information: NHK Engineering System, Inc.
Phone: +81- (0)3-5494-2400 (main)
URL: http://www.nes.or.jp/index.html

DARC
DATA RADIO CHANNEL

*Note
The number of shipments of this LSI will be reported to NHK-ES by our company.
(the number of samples is excluded)

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