Ordering number : ENN6974A

CMOS IC

LC72148V

Electronic Tuning PLL Frequency Synthesizer for Car Stereo Systems

Overview

The LC72148V is a 3 V version of the LC72146 PLL frequency synthesizer that can easily implement a variety of 3 V power supply tuners, including in-car navigation system receivers based on the VICS FM multiplex system.

Functions

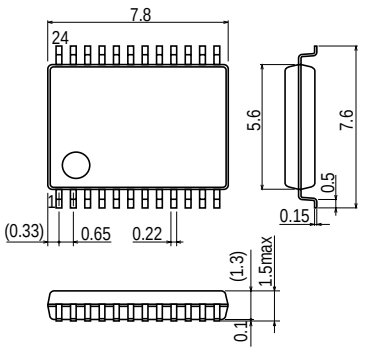
- High-speed programmable divider
  - FMIN: 10 to 180 MHz ··· Pulse swallower technique
  - AMIN: 2 to 40 MHz ··· Pulse swallower technique
    0.5 to 10 MHz ··· Direct division technique
- IF counters
  - HCTR: 0.4 to 25 MHz ··· Frequency measurement
  - LCTR: 10 to 500 kHz ··· Frequency measurement
    1.0 to 20×10^3 Hz ··· Period measurement
- Reference frequency
  - One of 12 reference frequencies can be selected (Crystal resonator: 7.2 or 4.5 MHz)
    1, 3, 5, 9, 10, 3.125, 6.25, 12.5, 25, 30, 50, and 100 kHz
- Phase comparator
  - Provides dead zone control
  - Built-in unlock detection circuit
  - Built-in deadlock clear circuit
  - Sub-charge pump for high-speed locking
- Built-in MOS transistor for implementing an active low-pass filter
- I/O ports: Five general-purpose I/O ports.
  - Input: 7 pins (maximum)
  - Output: 7 pins (maximum. N-channel: 4 pins, CMOS: 3 pins)
  - A clock time base signal (8 Hz) can be output.
- Serial data I/O
  - Supports communication with a controller in the CCB format.
  - Uses the same serial data as the LC72146.
- Operating ranges
  - Supply voltage: 2.7 to 3.6 V
  - Operating temperature: –40 to +85°C
- Package
  - SSOP24

Package Dimensions

unit: mm

3175B-SSOP24

[LC72148V]



SANYO: SSOP24

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

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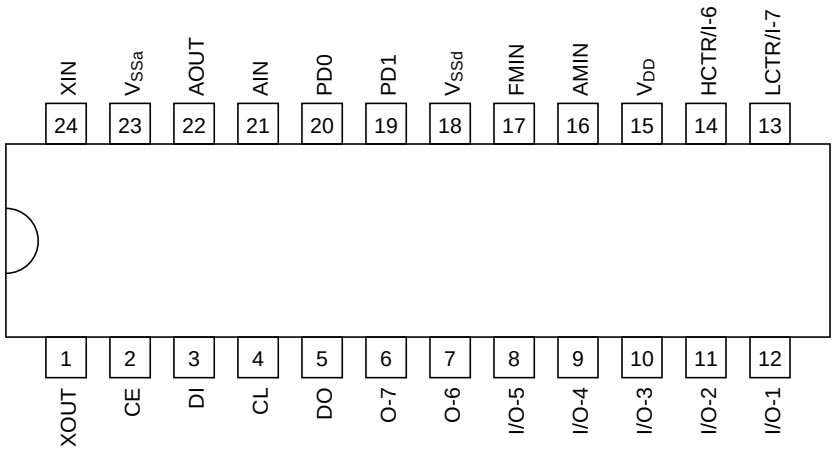
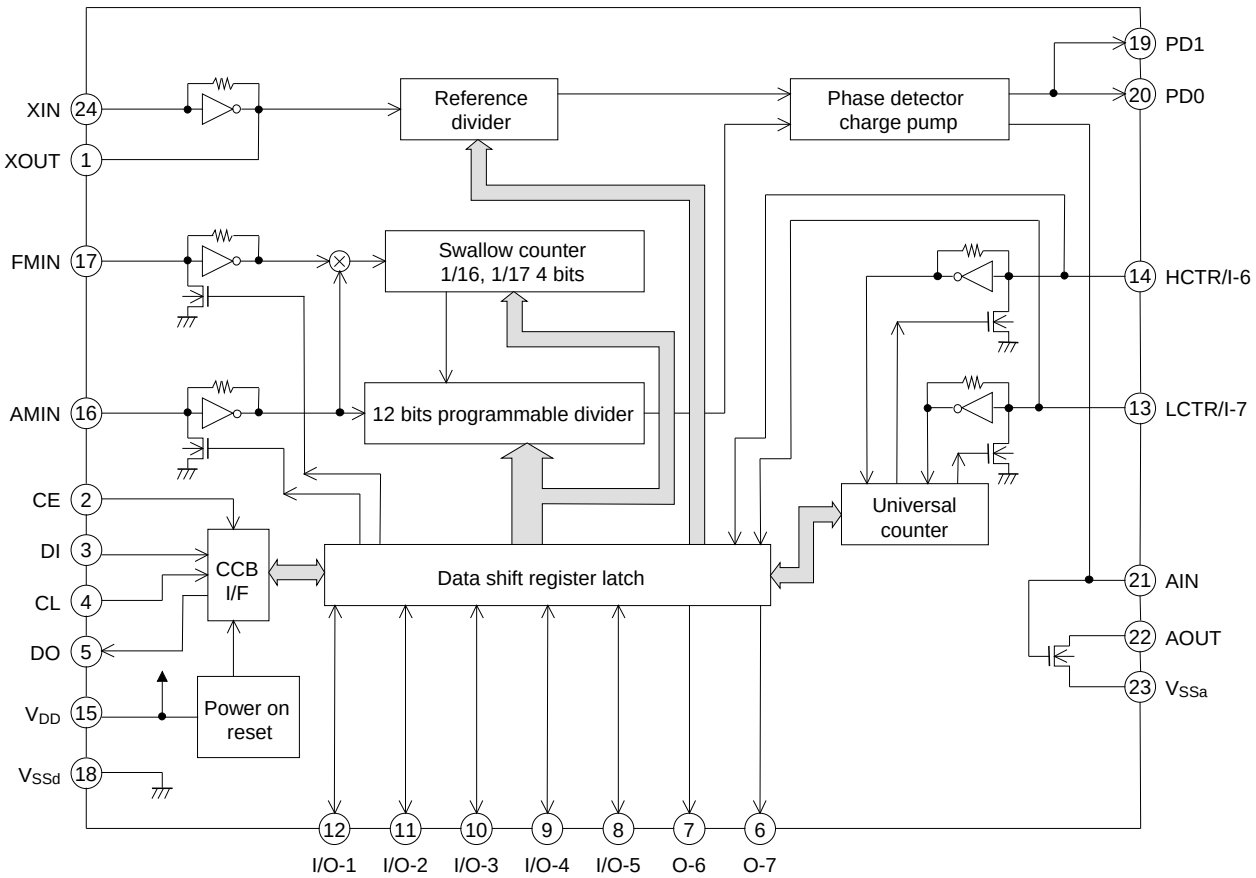
41202RM (OT)/70601RM (OT) No. 6974-

Pin Assignment



Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, Vssd = Vssa = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
Maximum input voltage	$V_{IN}1$ max	CE, CL, DI	–0.3 to +7.0	V
	$V_{IN}2$ max	XIN, FMIN, AMIN, HCTR/I-6, LCTR/I-7, AIN, I/O-4, I/O-5	–0.3 to V_{DD} + 0.3	V
	$V_{IN}3$ max	I/O-1, I/O-2, I/O-3	–0.3 to +15.0	V
Maximum output voltage	V_O1 max	DO	–0.3 to +7.0	V
	V_O2 max	XOUT, I/O-4, I/O-5, O-6, PD0, PD1, AIN	–0.3 to VDD + 0.3	V
	V_O3 max	I/O-1, I/O-2, I/O-3, AOUT, O-7	–0.3 to +15.0	V
Maximum output current	I_O1 max	I/O-4, I/O-5, O-6, O-7	0 to 3.0	mA
	I_O2 max	DO, AOUT	0 to 6.0	mA
	I_O3 max	I/O-1, I/O-2, I/O-3	0 to 10	mA
Allowable power dissipation	Pd max	(Ta ≤ 85°C) SSOP24	140	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Conditions at Ta = 25°C, Vssd = Vssa = 0 V

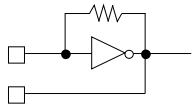
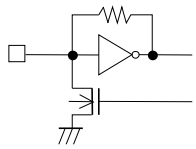
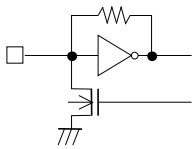
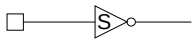
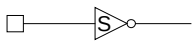
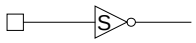
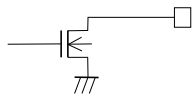
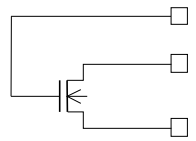
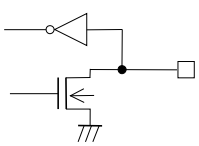
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	V_{DD}	2.7		3.6	V
	$V_{DD}2$	V_{DD}: Serial data retained	1.5			V
High-level input voltage	$V_{IH}1$	CE, CL, DI, I/O-1, I/O-2, I/O-3	0.7 V_{DD}		6.5	V
	$V_{IH}2$	I/O-4, I/O-5, HCTR/I-6, LCTR/I-7	0.7 V_{DD}		V_{DD}	V
	$V_{IH}3$	LCTR/I-7: Pulse waveform	0.7 V_{DD}		V_{DD}	V
Low-level input voltage	$V_{IL}1$	CE, CL, DI, I/O-1 to I/O-5, HCTR/I-6, LCTR/I-7	0		0.3 V_{DD}	V
	$V_{IL}2$	LCTR/I-7: Pulse waveform	0		0.3 V_{DD}	V
Output voltage	V_O1	DO	0		6.5	V
	V_O2	I/O-1, I/O-2, I/O-3, O-7, AOUT	0		13	V
Input frequency	$f_{IN}1$	XIN: $V_{IN}1$ *1	1		8	MHz
	$f_{IN}2$	FMIN: $V_{IN}2$ *1	10		180	MHz
	$f_{IN}3$	AMIN (SNS = 1): $V_{IN}3$ *1	2		40	MHz
	$f_{IN}4$	AMIN (SNS = 0): $V_{IN}4$ *1	0.5		10	MHz
	$f_{IN}5$	HCTR/I-6: $V_{IN}5$ *1	0.4		25	MHz
	$f_{IN}6$	LCTR/I-7: $V_{IN}6$ *1	10		500	kHz
	$f_{IN}7$	LCTR/I-7 *2	1.0		20×10^3	Hz
Input amplitude	$V_{IN}1$	XIN: $f_{IN}1$	200		900	mVrms
	$V_{IN}2$-1	FMIN: f = 10 to 130 MHz	20		900	mVrms
	$V_{IN}2$-2	FMIN: f = 130 to 180 MHz	40		900	mVrms
	$V_{IN}3$	AMIN (SNS = 1): $f_{IN}3$	40		900	mVrms
	$V_{IN}4$	AMIN (SNS = 0): $f_{IN}4$	40		900	mVrms
	$V_{IN}5$-1	HCTR/I-3 (CTC = 0): f = 0.4 to 25 MHz	40		900	mVrms
	$V_{IN}5$-2	HCTR/I-3 (CTC = 1): f = 8 to 12 MHz	70		900	mVrms
	$V_{IN}6$-1	LCTR/I-4 (CTC = 0): f = 10 to 400 kHz	40		900	mVrms
	$V_{IN}6$-2	LCTR/I-4 (CTC = 0): f = 400 to 500 kHz	20		900	mVrms
	VIN6-3	LCTR/I-4 (CTC = 1): f = 400 to 500 kHz	70		900	mVrms
Guaranteed operation range for crystal resonator	X'tal	XIN, XOUT *3	4.0		8.0	MHz

Notes: 1. Sine wave, capacitance coupling
2. Pulse waveform, DC coupling (period measurement)
3. Recommended CI values for the crystal resonator: CI ≤ 120Ω (4.5 MHz) or CI ≤ 70Ω (7.2 MHz)

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Internal feedback resistors	Rf1	XIN		1		MΩ
	Rf2	FMIN		500		kΩ
	Rf3	AMIN		500		kΩ
	Rf4	HCTR/I-6		250		kΩ
	Rf5	LCTR/I-7		250		kΩ
Internal pull-down resistors	Rpd1	FMIN	80	200	600	kΩ
	Rpd2	AMIN	80	200	600	kΩ
Hysteresis	V_{HIS}	CE, CL, DI, LCTR/I-7		0.1 V_{DD}		V
High-level output voltage	$V_{OH}1$	PD0, PD1, I/O-4, I/O-5, O-6, I_O = –0.5 mA	V_{DD} – 0.5			V
		PD0, PD1, I/O-4, I/O-5, O-6, I_O = –1 mA	V_{DD} – 1.0			V
	$V_{OH}2$	AIN, I_O = –5 mA	V_{DD} – 1.0			V
Low-level output voltage	$V_{OL}1$	PD0, PD1, I/O-4, I/O-5, O-6, O-7, I_O = 0.5 mA			0.5	V
		PD0, PD1, I/O-4, I/O-5, O-6, O-7, I_O = 1.0 mA			1.0	V
	$V_{OL}2$	AIN, I_O = 5 mA			1.0	V
	$V_{OL}3$	I/O-1, I/O-2, I/O-3, I_O = 1 mA			0.2	V
		I/O-1, I/O-2, I/O-3, I_O = 2.5 mA			0.5	V
		I/O-1, I/O-2, I/O-3, I_O = 5 mA			1.0	V
		I/O-1, I/O-2, I/O-3, I_O = 9 mA			1.8	V
	$V_{OL}4$	DO, I_O = 5 mA			1.0	V
	$V_{OL}5$	AOUT, I_O = 10 mA, AIN = 2.0 V			1.5	V
High-level input current	$I_{IH}1$	CE, CL, DI, V_I = 6.5 V			5.0	µA
	$I_{IH}2$	I/O-1, I/O-2, I/O-3, V_I = 13 V			5.0	µA
	$I_{IH}3$	I/O-4, I/O-5, HCTR/I-6, LCTR/I-7, V_I = V_{DD}			5.0	µA
	$I_{IH}4$	XIN, V_I = V_{DD}	1.3		8	µA
	$I_{IH}5$	FMIN, AMIN, V_I = V_{DD}	2.5		15	µA
	$I_{IH}6$	HCTR/I-6, LCTR/I-7, V_I = V_{DD}	5.0		30	µA
Low-level input current	$I_{IL}1$	CE, CL, DI, V_I = 0 V			5.0	µA
	$I_{IL}2$	I/O-1, I/O-2, I/O-3, V_I = 0 V			5.0	µA
	$I_{IL}3$	HCTR/I-6, LCTR/I-7, V_I = 0 V			5.0	µA
	$I_{IL}4$	XIN, V_I = 0 V	1.3		8	µA
	$I_{IL}5$	FMIN, AMIN, V_I = 0 V	2.5		15	µA
	$I_{IL}6$	HCTR/I-6, LCTR/I-7, V_I = 0 V	5.0		30	µA
Output off leakage current	$I_{OFF}1$	I/O-1, I/O-2, I/O-3, O-7, AOUT, V_O = 13 V			5.0	µA
	$I_{OFF}2$	DO, V_O = 6.5 V			5.0	µA
High-level three-state off leakage current	I_{OFFH}	PD0, PD1, AIN, V_O = V_{DD}		0.01	200	nA
Low-level three-state off leakage current	I_{OFFL}	PD0, PD1, AIN, V_O = 0 V		0.01	200	nA
Input capacitance	C_{IN}	FMIN		6		pF
Supply current	$I_{DD}1$	V_{DD}, X'tal = 7.2 MHz, $f_{IN}2$ = 180 MHz, $V_{IN}2$ = 40 mVrms, $f_{IN}5$ = 25 MHz, $V_{IN}5$ = 40 mVrms		3	8	mA
	$I_{DD}2$	V_{DD}, With the PLL block stopped. (PLL INHIBIT) With the crystal oscillator operating. (Crystal frequency = 7.2 MHz)		0.5	1.5	mA
	$I_{DD}3$	V_{DD}, With the PLL block stopped. With the crystal oscillator stopped.			10	µA

Pin Functions

Pin No.	Symbol	Type	Function	Pin circuit
24 1	XIN XOUT	X'tal	• Crystal resonator connections (7.2 or 4.5 MHz)	
17	FMIN	Local oscillator signal input	• FMIN is selected when DVS in the serial data input is set to 1. • The input frequency range is 10 to 180 MHz. • The signal is directly transmitted to the swallow counter. • The divisor can be set to a value in the range 272 to 65,535.	
16	AMIN	Local oscillator signal input	• AMIN is selected when DVS in the serial data input is set to 0. • When SNS in the serial data input is set to 1: —The input frequency range is 2 to 40 MHz. —The signal is directly transmitted to the swallow counter. —The divisor can be set to a value in the range 272 to 65,535. • When SNS in the serial data input is set to 0: —The input frequency range is 0.5 to 10 MHz. —The signal is directly transmitted to the 12-bit programmable divider. —The divisor can be set to a value in the range 5 to 4,095.	
2	CE	Chip enable	• This pin must be set to the high level during serial data input (DI) from, or serial data output (DO) to, the LC72148V.	
3	DI	Input data	• Input pin for serial data transmitted from the controller to the LC72148V.	
4	CL	Clock	• Data synchronization clock used during serial data input (DI) from, or serial data output (DO) to, the LC72148V.	
5	DO	Output data	• Data output pin for data output from the LC72148V to the controller. The content of the data output is determined by the ULD, DT0, and DT1 bits in the serial data.	
15	V_{DD}	Power supply	• The LC72148V power supply pin. (V_{DD} = 2.7 to 3.6 V) • The power-on reset circuit operates when power is first applied.	———
18	V_{SSd}	Ground	• Digital system ground for the LC72148V	———
21 22 23	AIN AOUT V_{SSa}	Low-pass filter amplifier transistor	• Connections to the internal n-channel MOS transistor provided to implement an active low-pass filter for the PLL. • A high-speed locking circuit can be implemented by using these pins in conjunction with the built-in sub-charge pump. • See the item describing the structure of the charge pump for details. • Vssa is a dedicated ground pin.	
12 11 10	I/O-1 I/O-2 I/O-3	General-purpose I/O ports	• Input/output shared-function pins • In output mode, the circuits are open-drain outputs. • The I/O direction is determined by I/O-1 to I/O-3 in the serial data. When the data is 0: input port When 1: output port • When specified for use as input ports The input pin states are transmitted from the DO pin to the controller Input state = low : Data = 0 Input state = high : Data = 1 • When specified for use as output ports The output states are determined by OUT1 to OUT3 in the serial data. Data = 0 : low Data = 1 : open • These pins are set to function as input ports by the power-on reset.	

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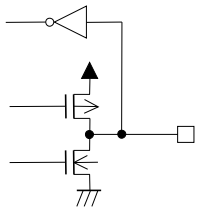
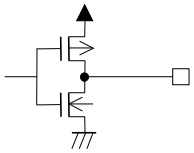
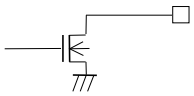
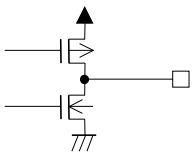
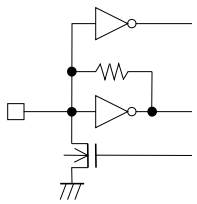
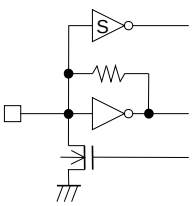
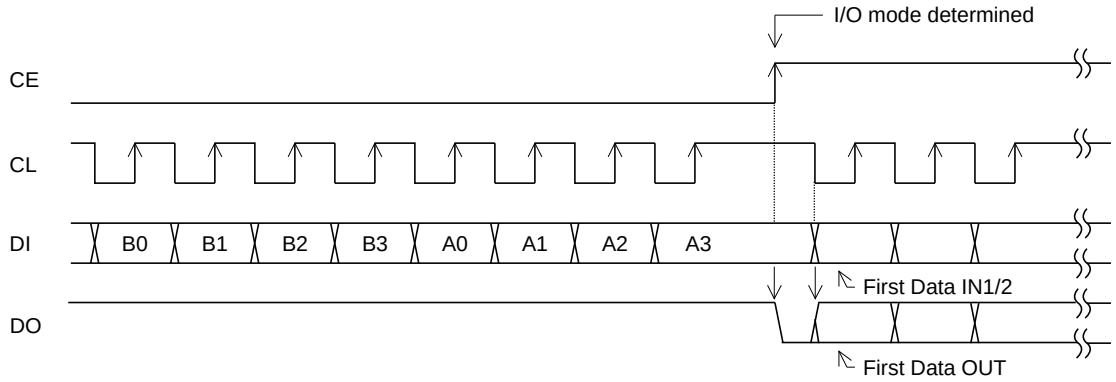
Pin No.	Symbol	Type	Function	Pin circuit
9 8	I/O-4 I/O-5	General-purpose I/O ports	• Input/output shared-function pins • In output mode, the circuits are complementary outputs. • The I/O direction is determined by I/O-4 and I/O-5 in the serial data. When the data is 0: input port When 1: output port • When specified for use as input ports The input pin states are transmitted from the DO pin to the controller Input state = low : Data = 0 Input state = high : Data = 1 • When specified for use as output ports The output states are determined by OUT4 and OUT5 in the serial data. Data = 0 : low Data = 1 : high • These pins are set to function as input ports by the power-on reset.	
7	O-6	Output port	• The OUT6 bit in the serial data is latched and output from O-6.	
6	O-7	Output port	• The OUT7 bit in the serial data is latched and output from O-7. • This pin outputs the 8 Hz clock time base signal when TBC is 1. • This pin is set to the open state by the power-on reset.	
20 19	PD0 PD1	Charge pump output	• PLL charge pump output pins When the frequency created by dividing the local oscillator signal frequency by N is higher than the reference frequency, a high level is output from the PD0 pin, and when lower, a low level is output. When the frequencies match, PD0 goes to the high-impedance state. • PD1 operates in a similar manner.	
14	HCTR/I-6	General-purpose counter	• HCTR is selected when CTS1 in the serial data input is set to 1. —The input frequency range is 0.4 to 25 MHz —The signal is passed through an internal divide-by-two circuit and transmitted to a general-purpose counter. An integrating count can also be performed. —The result is output starting with the MSB of the general-purpose counter from the DO pin. —There are four counting time periods: 4, 8, 32, or 64 ms. —See the item on the general-purpose counter for details. • When H/I-6 in the serial data is set to 0 — This pin functions as an input port, and its state is output from the DO output pin.	
13	LCTR/I-7	General-purpose counter	• LCTR is selected when CTS1 in the serial data input is set to 0. • When CTS0 in the serial data input is set to 1 in the CTS1=0 state. —The circuit operates in frequency measurement mode. —The input frequency range is 10 to 500 kHz. —The signal is transmitted directly to the general-purpose counter. • When CTS0 in the serial data input is set to 0 —The circuit operates in period measurement mode. —The input frequency range is 1 Hz to 20 kHz. —The measurement period can be set to be either 1 period or 2 periods. If 2-period measurement is selected, the input frequency range will be 2 Hz to 40 kHz. —The result is output starting with the MSB of the general-purpose counter from the DO pin. —See the item on the general-purpose counter for details. • When L/I-7 in the serial data input is set to 0. —This pin functions as an input port, and its state is output from the DO output pin.	

Procedures for input and output of serial data

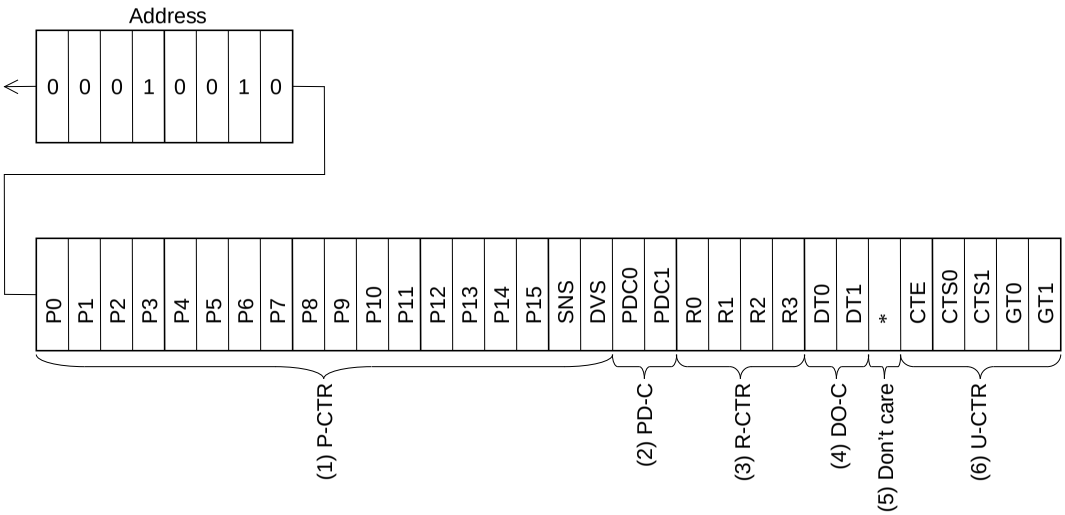
Data is input and output using CCB (Computer Control Bus), which is SANYO's audio IC serial bus format. This IC adopts the 8-bit address version of the CCB format.

	I/O mode	Address								Description
		B0	B1	B2	B3	A0	A1	A2	A3	
1	IN1 (84)	0	0	0	1	0	0	1	0	• Control data input (serial data input) mode • 32 bits of data are input. • See the "Structure of the DI control data (serial data input)" item for the content of the input data.
2	IN2 (94)	1	0	0	1	0	0	1	0	• Control data input (serial data input) mode • 32 bits of data are input. • See the "Structure of the DI control data (serial data input)" item for the content of the input data.
3	OUT (A4)	0	1	0	1	0	0	1	0	• Data output (serial data output) mode • The number of bits of data output is equal to the number of clock cycles. • See the "Structure of the DO output data (serial data output)" item for the content of the output data.

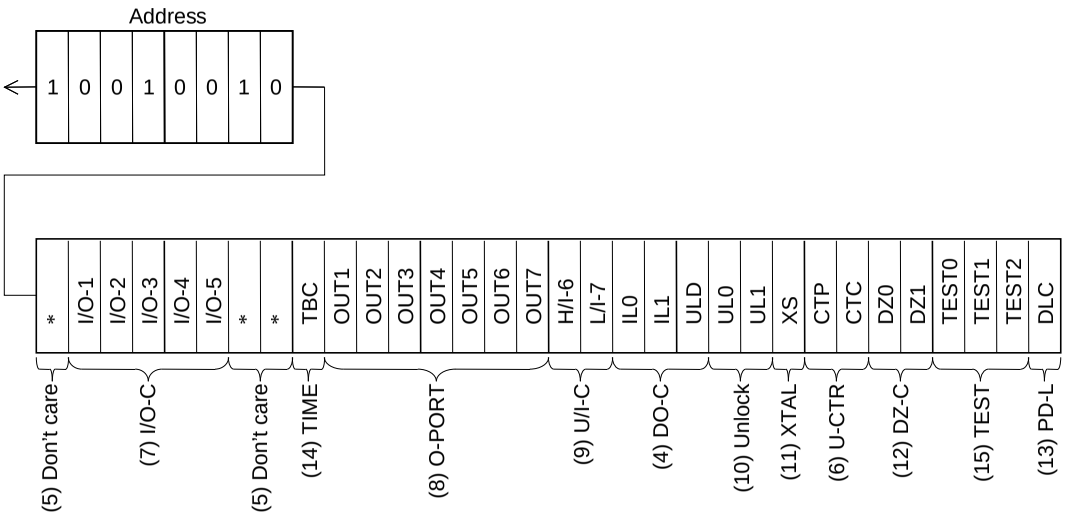


Structure of the DI control data (serial data input)

[1] IN1 mode



[2] IN2 mode



DI control data functions

<table>
<tr><th>Number</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15
DVS, SNS</td><td>
• This data sets the divisor provided by the programmable divider. This is a binary value with P15 the MSB. The LSB depends on the DVS and SNS settings.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Set divisor (N)</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td></tr>
</table>
*: When P4 is the LSB, P0 to P3 are ignored.

• DVS selects the input pin (FMIN or AMIN) whose signal is input to the programmable divider and SNS switches the input frequency range.
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input pin frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 180 MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td></tr>
</table>
*: See the “Structure of the Programmable Divider” item for details.
</td><td></td></tr>
<tr><td>(2)</td><td>Sub-charge pump control data
PDC0, PDC1</td><td>
• Sub-charge pump control data
<table>
<tr><th>PDC1</th><th>PDC0</th><th>Sub-charge pump state</th></tr>
<tr><td>0</td><td>*</td><td>High impedance</td></tr>
<tr><td>1</td><td>1</td><td>Charge pump operation (normal)</td></tr>
<tr><td>1</td><td>0</td><td>Charge pump operation (unlocked mode)</td></tr>
</table>
*: The sub-charge pump is connected to the gate of the low-pass filter amplifier transistor. A high-speed locking circuit can be formed by using this function in conjunction with PD0 and PD1 (main charge pump).
See the “Structure of the Charge Pump” item for details.
</td><td>UL0
UL1
DLC</td></tr>
<tr><td>(3)</td><td>Reference divider data
R0 to R3</td><td>
• Reference frequency selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>30</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL inhibit + X’tal OSC stop</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL inhibit</td></tr>
</table>
*: PLL INHIBIT
In this state, the programmable divider is stopped, the FMIN and AMIN pins are pulled down to ground, and the charge pump goes to the high-impedance state.
</td><td></td></tr>
</table>

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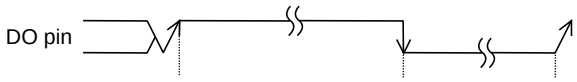
<table>
<tr><th>Number</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(4)</td><td>DO and I/O-5 pin control data
ULD
DT0, DT1
IL0, IL1</td><td>
• This data selects the output from the DO pin.
<table>
<tr><th>ULD</th><th>DT1</th><th>DT0</th><th>DO pin state</th><th>I/O-5 pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Low when the unlocked state is detected.</td><td rowspan="4"></td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC *1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>IN *2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td><td rowspan="4"></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Open</td><td rowspan="3">Low when the unlocked state is detected. *3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>end-UC *1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>IN *2</td></tr>
</table>
*1. end-UC is the general-purpose counter measurement complete check function.


(1) Counting starts (2) Counting completes (3) CE: HI
(1) When end-UC is set and the counter started (CTE = 0 → 1), the DO pin automatically goes to the open state.
(2) When the general-purpose counter measurement completes, the DO pin goes to the low level, and it becomes possible to check for the count complete state.
(3) The DO pin goes to the open state due to the I/O of serial data (when the CE pin is high).
*2
<table>
<tr><th>IL1</th><th>IL0</th><th>IN</th></tr>
<tr><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>I-1 (pin state)</td></tr>
<tr><td>1</td><td>0</td><td>I-2 (pin state)</td></tr>
<tr><td>1</td><td>1</td><td>DO goes low when I-1 changes state.</td></tr>
</table>
However, when the I/O-1 and I/O-2 pins are specified to be output ports, IN will go to the open state.
*3: This is invalid if the I/O-5 pin is specified to be an input port.
Note: The DO pin will be in the open state, regardless of the state of the DO pin control data, during the data input period (the period when CE is high in IN1 or IN2 mode).
Furthermore, the DO pin will output the content of the internal DO serial data in synchronization with CL, regardless of the state of the DO pin control data during the data output period (the period when CE is high in OUT mode).
DO cannot be used (it does not change state) in crystal oscillator stopped mode (R0=0, R1=R2=R3=1).
</td><td>CTE

OUT5
I/O-1
I/O-2
I/O-5</td></tr>
<tr><td>(5)</td><td>*</td><td>Don’t Care</td><td></td></tr>
</table>

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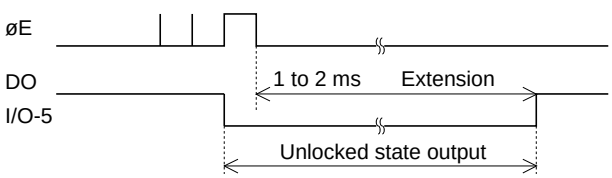
<table>
<tr><th>Number</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(6)</td><td>General-purpose counter control data
CTS0, CTS1
CTE
GT0, GT1

CTP
CTC</td><td>
• CTS1 and CTS0 select the input pin (HCTR or LCTR) for the general-purpose counter.
<table>
<tr><th>CTS1</th><th>CTS0</th><th>Input pin</th><th>Measurement mode</th></tr>
<tr><td>1</td><td>*</td><td>HCTR</td><td>Frequency</td></tr>
<tr><td>0</td><td>1</td><td>LCTR</td><td>Frequency</td></tr>
<tr><td>0</td><td>0</td><td>LCTR</td><td>Period</td></tr>
</table>
• CTE controls the general-purpose counter measurement operation.
CTE = 1: Starts the count
= 0: Resets the counter
• GT1 and GT0 determine the general-purpose counter measurement time (in frequency mode) and number of periods (in period mode)
<table>
<tr><th rowspan="2">GT1</th><th rowspan="2">GT0</th><th colspan="2">Frequency measurement</th><th rowspan="2">Period measurement</th></tr>
<tr><th>Measurement time</th><th>Wait time</th></tr>
<tr><td>0</td><td>0</td><td>4 ms</td><td>3 to 4 ms</td><td>1 period</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td><td>1 period</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td><td>2 periods</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td><td>2 periods</td></tr>
</table>
• When CTE is 0, pulling down the input is disabled by setting CTP to 1.
Note: The wait time will be 1 to 2 ms.
However, CTP must be set to 1 at least 4 ms before CTE is set to 1.
• The input sensitivity is reduced when CTC is set to 1. (Sensitivity: 10 to 30 mVrms)
* See the “Structure of the General-Purpose Counter” item for details.
</td><td>H/I-6
L/I-7</td></tr>
<tr><td>(7)</td><td>I/O port control data
I/O-1 to I/O-5</td><td>
• This data specifies the I/O direction of the shared-function I/O pins (I/O-1 to I/O-5).
Data = 0: Input port
= 1: Output port
</td><td>OUT1 to OUT5
ULD</td></tr>
<tr><td>(8)</td><td>Output port data
OUT1 to OUT7</td><td>
• This data determines the output from the output ports O-1 to O-7.
Data = 0: Low
= 1: Open or high
• This data is invalid if input port operation or unlocked state output is specified.
</td><td>I/O-1 to I/O-5
ULD</td></tr>
<tr><td>(9)</td><td>General-purpose counter input control data
H/I-6, L/I-7</td><td>
• Sets the general-purpose counter pins to function as input ports.
H/I-6 = 0: I-6 (input port)
= 1: HCTR (general-purpose counter)
L/I-3 = 0: I-7 (input port)
= 1: LCTR (general-purpose counter)
</td><td>CTS0
CTS1</td></tr>
<tr><td>(10)</td><td>Unlocked state detection data
UL0, UL1</td><td>
• UL0 and UL1 select the phase error (øE) detection width used for judging the PLL locked state. If a phase error in excess of the widths listed in the table below occurs, the PLL will be seen to be in the unlocked state. When unlocked, the detection pin goes low.
(* : don’t care)
<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detection output</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>øE is output directly.</td></tr>
<tr><td>1</td><td>0</td><td>±0.56 µs</td><td>øE is extended by 1 to 2 ms.</td></tr>
<tr><td>1</td><td>1</td><td>±1.11 µs</td><td>øE is extended by 1 to 2 ms.</td></tr>
</table>


</td><td>ULD
DT0, DT1</td></tr>
</table>

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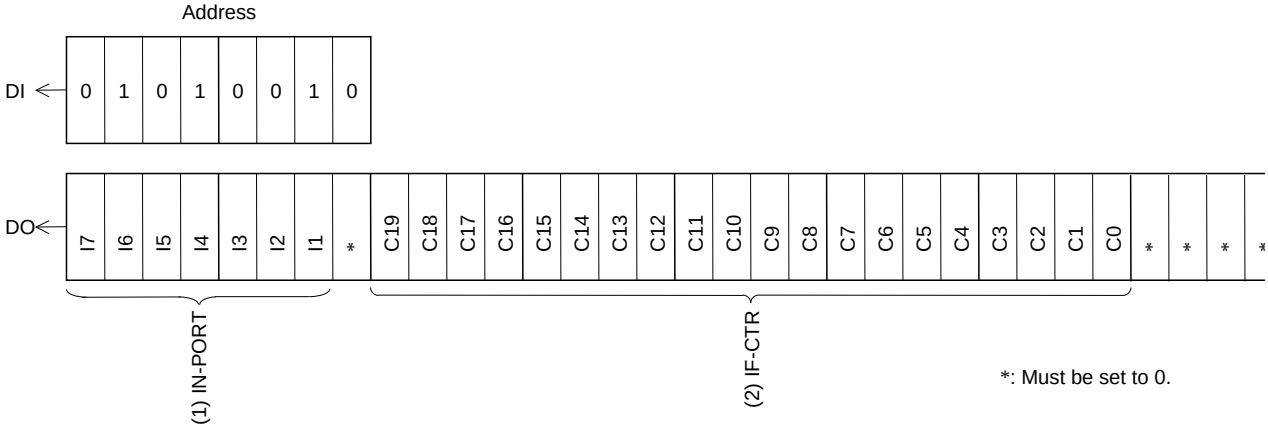
<table>
<tr><th>Number</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(11)</td><td>Crystal oscillator circuit
XS</td><td>• Selects the crystal oscillator.
XS = 1: 7.2 MHz
= 0: 4.5 MHz
* The 4.5 MHz setting is selected after the power-on reset.</td><td></td></tr>
<tr><td>(12)</td><td>Phase comparator control data
DZ0, DZ1</td><td>• Controls the phase comparator’s dead band.
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead band mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
The width of the dead band settings: DZA < DZB <DZC < DZD
* DZA is selected after the power-on reset. (We recommend using either DZD or DZC.) †</td><td></td></tr>
<tr><td>(13)</td><td>Charge pump control data</td><td>• This data forcibly sets the charge pump output to the low level (Vss).
DLC = 1: Low level
= 0: Normal operation
* When the circuit deadlocks due to the oscillator stopping when the PLL VCO control voltage (Vtune) goes to 0 V, this bit can be used to clear the deadlocked state.
(Deadlock clear circuit)
This setting is set to normal operation after the power-on reset. †</td><td></td></tr>
<tr><td>(14)</td><td>Clock time base
TBC</td><td>• Setting this bit to 1 causes a clock time base signal (8 Hz, 40% duty) to be output from the O-7 pin. (The OUT7 data is invalid in this mode.)
* TBC = 0 is selected after the power-on reset.</td><td>OUT7</td></tr>
<tr><td>(15)</td><td>IC test data
TEST0 to TEST2</td><td>• IC test data.
TEST0
TEST1 All these bits must be set to 0.
TEST2
All these bits are set to 0 after the power-on reset. †</td><td></td></tr>
</table>

†: Although these bits are initialized by the power-on reset circuit after power is applied, for safety, immediately after power is applied, always initialize this setting by sending the CCB data.

Structure of the DO output data (serial output data)

[3] OUT mode

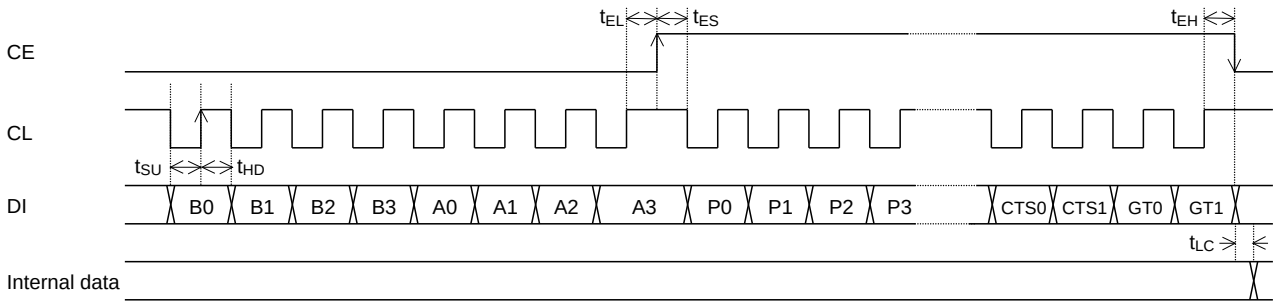


Description of the DO output data

Number	Control block/data	Description	Related data
(1)	I/O port data I7 to I1	• This data is latched from the states of I/O port pins I-1 to I-7. This data outputs (reports) the states of the pins regardless of the I/O direction specified for the I/O ports. Data is latched at the point data output mode (OUT mode) is entered. I1 to I5 ← The I/O-1 to I/O-5 pin states ⎫ Hi : "1" I6, I7 ← The HCTR/I-6 and LCTR/I-7 pin states ⎭ Low : "0" The following data is output if these pins are set to function as output ports or as general-purpose counter input pins. I1, I2, I3: Output pin states (open drain) I4, I5: Output pin state (CMOS) I6, I7: 0	I/O-1 to I/O-5 H/I-6, L/I-7 OUT1 to OUT5
(2)	IF counter binary data C19 to C0	• This data is latched from the contents of the IF counter (the 20-bit binary counter). C19 ← MSB of the binary counter C0 ← LSB of the binary counter	CTE CTS0 CTS1

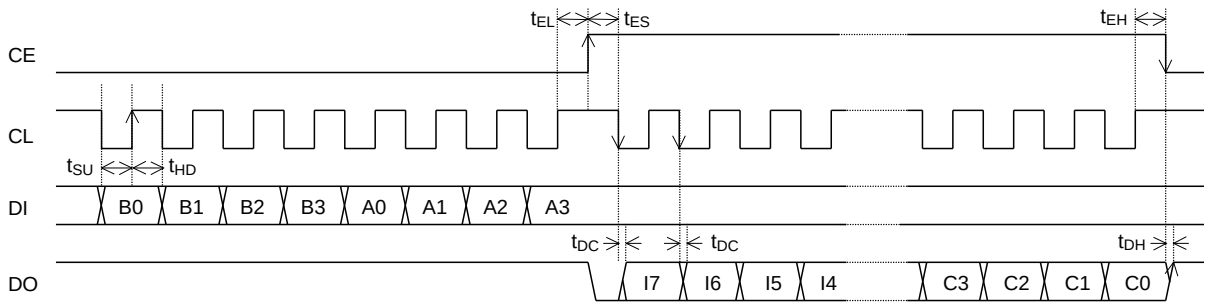
Serial data input (IN1/IN2)

t_{SU}, t_{HD}, t_{EL}, t_{ES}, $t_{EH} \geq 0.45$ µs $t_{LC} < 0.45$ µs



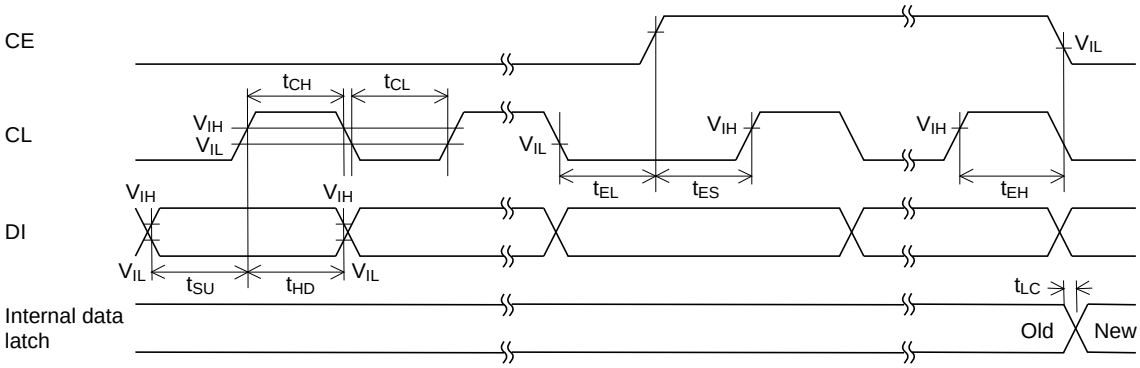
Serial data output (OUT)

t_{SU}, t_{HD}, t_{EL}, t_{ES}, $t_{EH} \geq 0.45$ µs t_{DC}, $t_{DH} < 0.2$ µs

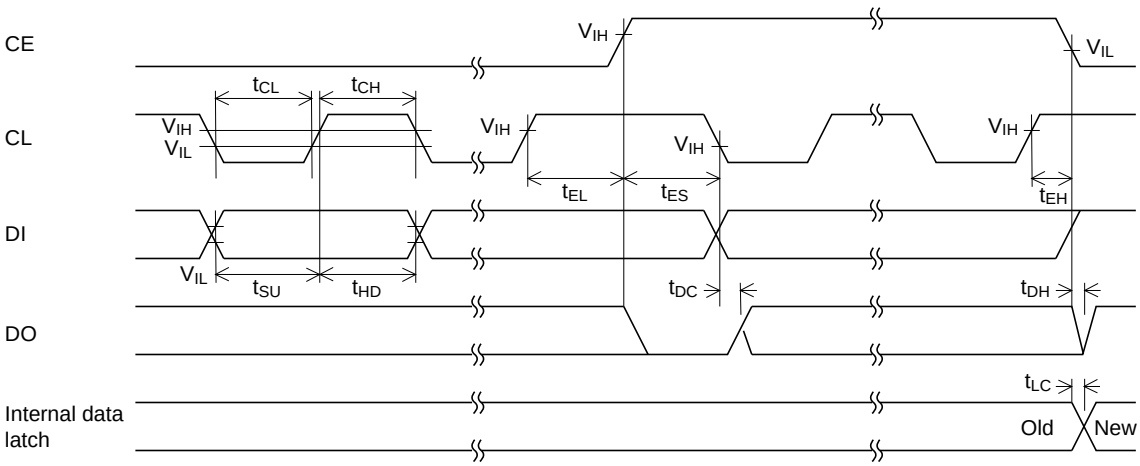


Note: Since the DO pin is an n-channel open-drain output, the data output times (t_{DC} and t_{DH}) depend on the value of the pull-up resistor used and the circuit board capacitance.

Serial data timing



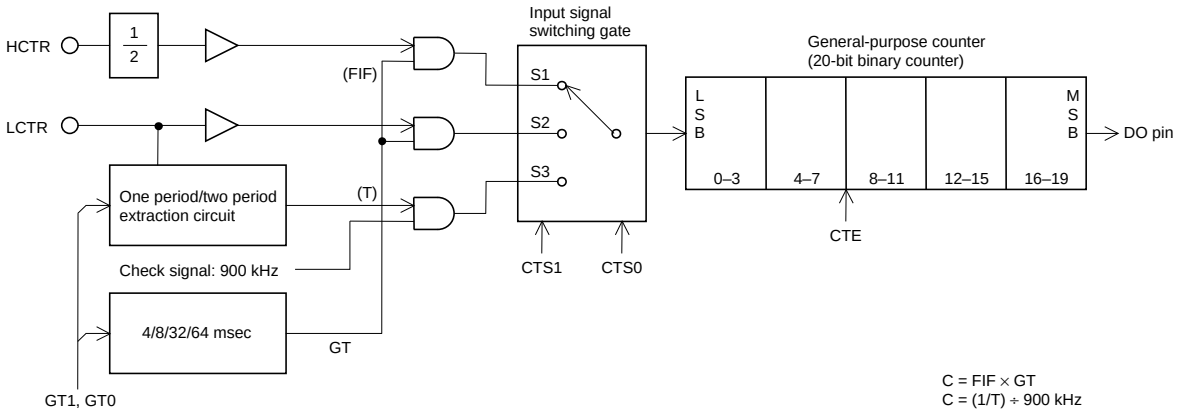
When stopped with CL at the low level



When stopped with CL at the high level

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Data setup time	t_{SU}	DI, CL	0.45			µs
Data hold time	t_{HD}	DI, CL	0.45			µs
Clock low-level time	t_{CL}	CL	0.45			µs
Clock high-level time	t_{CH}	CL	0.45			µs
CE wait time	t_{EL}	CE, CL	0.45			µs
CE setup time	t_{ES}	CE, CL	0.45			µs
CE hold time	t_{EH}	CE, CL	0.45			µs
Data latch change time	t_{LC}				0.45	µs
Data output time	t_{DC}	DO, CL, These times depend on the values of the pull-up resistors used and the circuit board capacitance.			0.2	µs
	t_{DH}	DO, CE, These times depend on the values of the pull-up resistors used and the circuit board capacitance.				

Structure of the General-Purpose Counter



	CTS1	CTS0	Input pin	Measurement mode	Frequency range	Input sensitivity
S1	1	*	HCTR	Frequency	0.4 to 25.0 MHz	40 mVrms *1
S2	0	1	LCTR	Frequency	10 to 500 kHz	40 mVrms *1
S3	0	0	LCTR	Period	1.0 to 20 × 10^3 Hz	(pulse)

*1 CTC = 0 : 40 mVrms
CTC = 1 : 70 mVrms

HCTR: Minimum input sensitivity rating f [MHz]			
CTC	0.4 ≤ f < 8	8 ≤ f < 12	12 ≤ f ≤ 25
0 (Normal mode)	40 mVrms	40 mVrms (0.1 to 5 mVrms)	40 mVrms
1 (Degraded mode)	—	70 mVrms (20 to 40 mVrms)	—

LCTR: Minimum input sensitivity rating f [kHz]		
CTC	10 ≤ f < 400	400 ≤ f ≤ 500
0 (Normal mode)	40 mVrms	20 mVrms (0.1 to 4 mVrms)
1 (Degraded mode)	—	70 mVrms (20 to 30 mVrms)

—: No rating (not guaranteed)
( ): Actual performance (provided for reference purposes)

GT1	GT0	Frequency measurement mode		Period measurement mode
		Measurement time	Wait time	
0	0	4 ms	3 to 4 ms	1 period
0	1	8		
1	0	32	7 to 8 ms	2 periods
1	1	64		

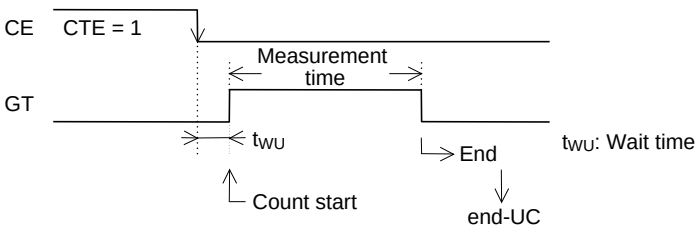
CTC is the input sensitivity switching data; when CTC is 1, the input sensitivity is degraded.
However, the actual performance will be:

HCTR → 20 to 40 mV rms (frequency: 10.7 MHz)
LCTR → 20 to 30 mV rms (frequency: 450 kHz)

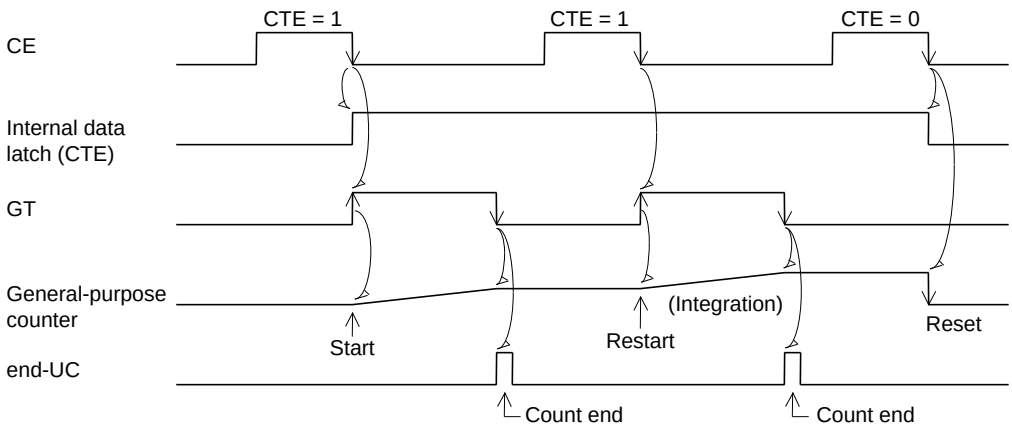
CTP: Pulling down the input is disabled (when CTE is 0) by setting CTP to 1.
CTP must be set to 1 at least 4 ms before CTE is set to 1. If the counter is not used, CTP must be left set to 0. The wait time is reduced 1 to 2 ms when CTP is set to 1.

The LC72148V general-purpose counter is a 20-bit binary counter. The results of count operations can be read out MSB first through the DO pin. When using the general-purpose counter for frequency measurement, one of four times, 4, 8, 32, or 64 ms, can be selected as the measurement time with GT0 and GT1. The frequency of the signal input to either the HCTR or LCTR pin can be measured by determining how many pulses were input to the general-purpose counter during this measurement time.

When using the general-purpose counter for frequency measurement, the period of the signal input to the LCTR pin can be measured by determining how many cycles of the check signal (900 kHz) were input to the general-purpose counter during 1 or 2 periods of the signal input to the LCTR pin.
The general-purpose counter counting is started by setting CTE in the serial data to 1. The serial data is confirmed internally to the LC72148V by dropping the CE signal from high to low. However, the signal input to the HCTR or LCTR pin must be provided within the wait time after CE is set low.
Next, the value of the general-purpose counter following completion of the measurement must be read out during the period while CTE is 1. (The general-purpose counter is reset when CTE is set to 0.)
One point that requires care here is that the general-purpose counter must be reset (cleared) by setting CTE to 0 before starting the general-purpose counter. Another is that although the signal input to the LCTR pin is transmitted directly to the general-purpose counter, the signal input to the HCTR pin is passed through a divide-by-two circuit before being transmitted to the general-purpose counter. Therefore, the result of the count by the general-purpose counter for the HCTR pin is 1/2 the value as compared to the actual frequency input to the HCTR pin.



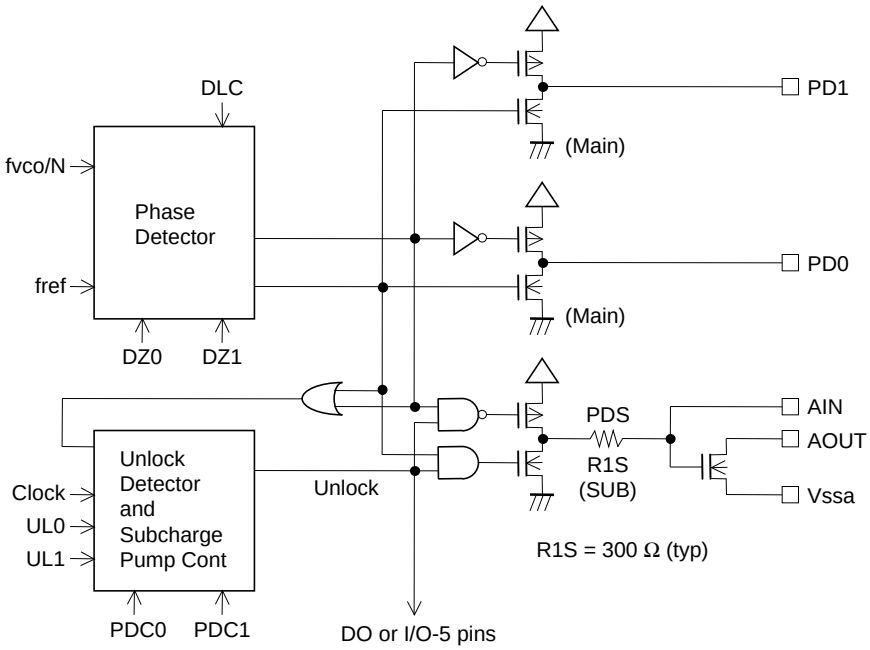
For an integrating count



*: CTE: 0 → • Resets the general-purpose counter
1 → • Starts the general-purpose counter
• Restarts when set to 1 again.

For an integrating count, the value counted is accumulated in the general-purpose counter.
Here, counter overflow may occur, and requires caution.
Count value: 0_H to $FFFFF_H$ (1,048,575)

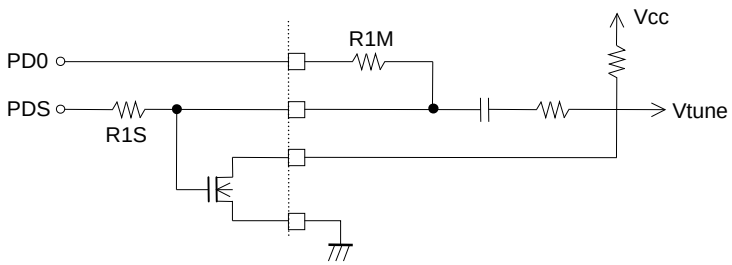
Structure of the Charge Pump



PDC1	PDC0	PDS (Sub-charge pump state)
0	*	High impedance
1	1	Charge pump operation (normal)
1	0	Charge pump operation (unlocked mode)

DLC	PD1, PD0, PDS
0	Normal operation
1	Forced low.

Note*: When the unlocked state is detected when changing stations, PDS (the sub-charge pump) operates, R1 becomes R1M/R1S, the low-pass filter time constant is made smaller, and frequency locking is accelerated.



Other Items

1. Notes on the phase comparator dead band

DZ1	DZ0	Dead band mode	Charge pumps	Dead band
0	0	DZA	ON/ON	- - 0 s
0	1	DZB	ON/ON	- 0 s
1	0	DZC	OFF/OFF	+0 s
1	1	DZD	OFF/OFF	++0 s

When the charge pumps are in one of the ON/ON states, correction pulses will be output from the charge pumps even if the PLL is locked, making it easier for the loop to become unstable. Thus particular care is required in the design stage for these settings.

The following problems may occur when the ON/ON states are used.
(1) Side bands may be created by reference frequency leakage.
(2) Side bands may be created by low-frequency leakage due to the envelope of the correction pulses.

When a dead band is present (the OFF/OFF settings), the loop will be stable. However, it will be difficult to achieve a high signal-to-noise ratio. Inversely, with no dead band, it is easy to achieve a high signal-to-noise ratio but hard to achieve high loop stability.
Therefore, the DZA and DZB settings, in which there is no dead band, can be effective for cases where an FM signal-to-noise ratio of 90 to 100 dB or greater is required, or when it is desirable to increase the AM stereo pilot margin.
However, if such a high signal-to-noise ratio is not required in FM reception, or an adequate AM stereo pilot margin can be achieved, or AM stereo is not used, DZC or DZD, which provide a dead band, should be selected.

Dead Zone (Dead Band) Definition

The phase comparator compares fp with the reference frequency (fr) as shown in figure 1. This circuit outputs a level (A) that is proportional to the phase difference ø as shown in figure 2. However, due to internal delays and other factors, the actual IC is unable to compare small phase differences, and thus a dead zone (B) appears in the output. To achieve a high signal-to-noise ratio in the end product, the dead zone should be as small as possible.

However, in popularly-priced models, there are cases where a somewhat wider dead zone may be easier to work with. This is because in some situations, such as when a powerful signal is applied to the RF input, in popularly-priced models there may be RF leakage from the mixer to the VCO. When the dead zone is narrow, outputs to correct this leakage are output, that output in turn modulates the VCO, and generates a beat signal with the RF.

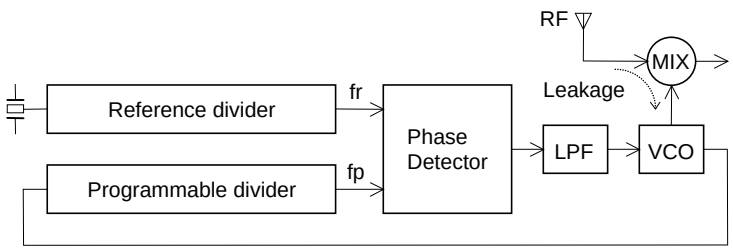


Figure 1

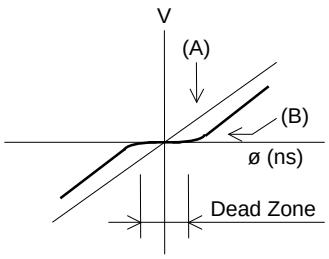


Figure 2

2. Notes on the FMIN, AMIN, HCTR/I-6, and LCTR/I-7 pins

The coupling capacitors must be located as close as possible to these pins. A capacitance of approximately 100 pF is desirable.
In particular, if the HCTR/I-6 and LCTR/I-7 pin capacitors are over about 1000 pF, the time required to reach the bias level may become excessive, and incorrect counting may occur due to the relationship with the wait time.

3. Notes on using IF counting with the HCTR/I-6 and LCTR/I-7 pins

If IF counting is used, the microcontroller must test the state of the IF IC SD (station detect) signal, and only if the SD signal is present, turn on the IF counter buffer output and perform an IF count operation. Methods in which auto-search operations are implemented only using the IF count may incorrectly stop at frequencies where no station is present due to leakage from the IF counter buffer.

4. Using the DO pin

At times other than data output mode, the DO pin can also be used to check for general-purpose counter count operation completion, to output the unlock state detection signal, and to check for changes in the input pins.

Note that the states of the input pins (I/O-1 and I/O-2) can be input to the system microcontroller through the DO pin.

5. Power supply pins

Capacitors must be inserted between the V_{DD} and V_{SSd} power supply pins to reduce noise. These capacitors must be located as close to the V_{DD} and V_{SSd} pins as possible.

6. Notes on VCO design

The VCO (local oscillator) must be designed so that the VCO oscillation does not stop if the control voltage (Vtune) becomes 0 V. If it is possible for this oscillator to stop, use the charge pump control data (DLC) to forcible set Vtune to V_{CC} temporarily to prevent the PLL circuit from deadlocking. (This function is called a deadlock clear circuit.)

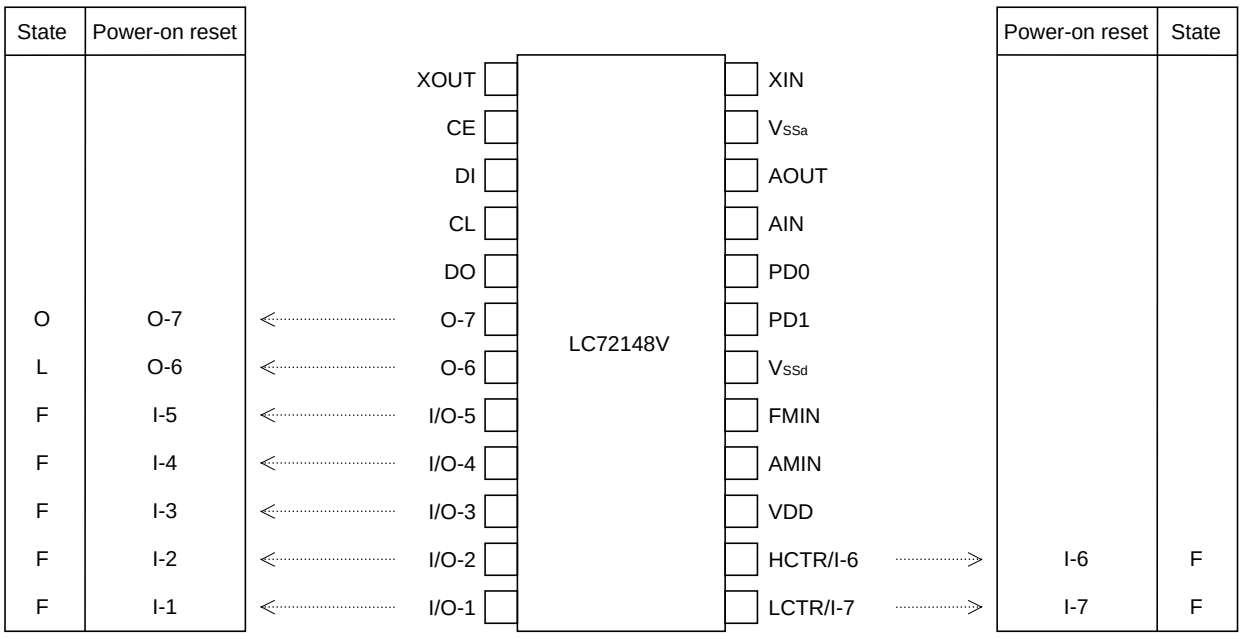
7. Notes on the PD pin

When switching from the LC72146 (5 V system) to this IC (3 V system), the charge pump output voltage will be reduced, thus reducing the loop gain. Thus various aspects of the circuit, such as the loop filter coefficients, and the locking time (the SD wait time) must be reviewed.

8. Microcontroller interface

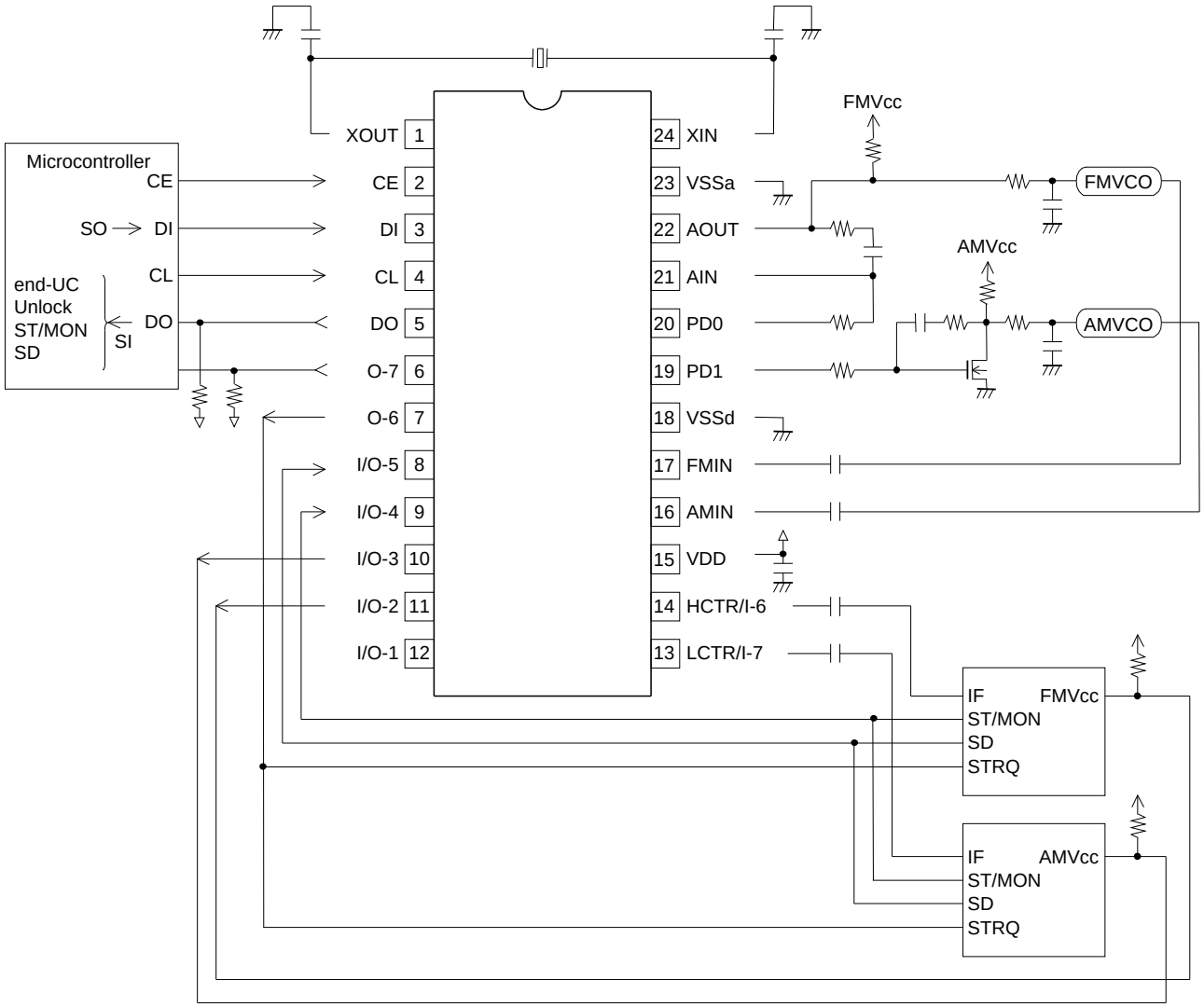
Although this IC is a 3 V system IC, it can accept 5 V system inputs over the microcontroller interface (the CE, DI, and CL pins).

Pin states after a power-on reset



O: Open, L: Low, F: Floating

Sample Application Circuit



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