Ordering number : EN*6008

CMOS IC

LC587208A, 587206A, 587204A, 587202A

4-Bit Single-Chip Microcontroller
LCD Driver ROM: 2, 4, 6, or 8 K × 16 bits, RAM: 512 × 4 bits

Preliminary

Overview

The LC587202A through LC587208A are 4-bit CMOS microcontrollers that integrate ROM, RAM, and an extensive set of peripheral functions around a CPU core that supports low-voltage operation. Memory capacities include 2, 4, 6, or 8 K of 16-bit ROM, 512 × 4 bits of RAM, and a special-purpose RAM for the 8-level stack. Peripheral functions include two 8-bit timers (one of which can be used as an event counter), an 8-bit synchronous serial interface, an alarm signal generator, a remote controller carrier signal generator, and an LCD controller/driver circuit. These microcontrollers provide a powerful set of standby functions for reduced power dissipation.

Applications

- Portable electronic equipment that uses an LCD display (These microcontrollers are particularly well-suited for portable equipment that requires low-power operation for extended battery life.)
- Control and LCD display in portable CD players, timers, and consumer health maintenance equipment
- Remote controls for CD players, VCRs, and tuners

Features

ROM

- LC587208A (8192 × 16 bits)
- LC587206A (6144 × 16 bits)
- LC587204A (4096 × 16 bits)
- LC587202A (2048 × 16 bits)

RAM

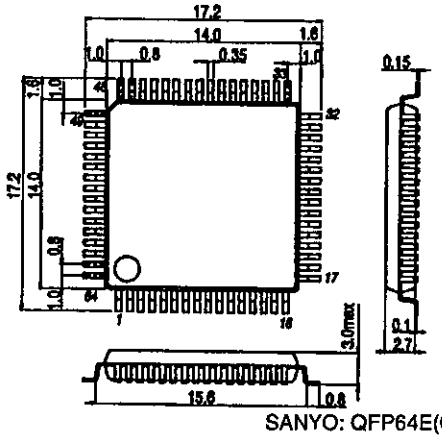
- LC587208A (512 × 4 bits)
- LC587206A (512 × 4 bits)
- LC587204A (512 × 4 bits)
- LC587202A (512 × 4 bits)

Package Dimensions

Unit: mm

3159-QFP64E

[LC587208A/06A/04A/02A]



SANYO: QFP64E(QIP64E)

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Instruction cycle times

Except for the table reference instruction, all instructions execute in a single cycle.

Cycle time	Supply voltage	System clock oscillator	Oscillator frequency
667 ns	4.5 to 6.0 V	CF (ceramic) oscillator	6 MHz
1 µs	2.8 to 6.0 V	CF (ceramic) oscillator	4 MHz
4 µs	2.5 to 6.0 V	CF (ceramic) oscillator	1 MHz
10 µs	2.2 to 6.0 V	CF (ceramic) oscillator	400 kHz
122 µs	2.0 to 6.0 V	Crystal oscillator	32.768 kHz

Ports

Input-only pins

- Port S (4 pins)
- The INT pin (1 pin)

I/O Pins

- Port K (4 pins)
  The output circuits are CMOS circuits, and cannot be modified.
- Port M (4 pins)
  The output circuits are either CMOS or p-channel circuits, and the type can be selected under program control in single-port units. (The M4 pin is set to its input pin function when timer 2 is used as an event counter.)
- Port SO (4 pins)
  The output circuits are either CMOS or n-channel circuits, and the type can be selected under program control in single-port units. The three pins SO1, SO2, and SO3 also function as the serial interface pins. (Two-pin serial interface operation is also supported.)
- Port P (4 pins)
  The output circuits are either CMOS or p-channel circuits, and the type can be selected under program control in single-port units.

Output-only pins

- Port N (4 pins)
  The N3 pin also functions as the remote controller carrier output pin, and the N4 pin also functions as the alarm output pin.

LCD drive pins

- Common pins (4 pins)
- Segment pins (23 pins)
  The segment pin circuits include built-in memory (called "segment memory") that holds the output data. These pins can also be switched in single-pin units in the mask options to function as general-purpose outputs (CMOS, p-channel, or n-channel).

Wide selection of LCD drive techniques

LCD drive technique	Number of segments that can be driven	Required common pins
1/3bias 1/4duty	92 segments	COM1 to COM4
1/3bias 1/3duty	69 segments	COM1 to COM3
1/2bias 1/4duty	92 segments	COM1 to COM4
1/2bias 1/3duty	69 segments	COM1 to COM3
Duplex	46 segments	COM1, COM2
Static	23 segments	COM1

LCD controller (Hardware functions that facilitate the development of display control software)

Segment PLA (option)

This technique allows the LCD drivers (common 1 through common 4) to be controlled according to user software design, i.e. the relationship between LCD segment control strobe signals and the data. This technique is more difficult for the chip manufacturer, but it allows software design and the LCD panel layout design to be completely independent. Thus it supports highly efficient product development and is a major plus for the user. Furthermore, there is no need for a routine that converts data held in RAM to LCD driver output data.

Segment decoder

These microcontrollers provide a decoder for 7-segment displays. This circuit also allows binary data to be output without modification for display control of flag areas that display various operating states.

Strobe decoder

This function groups segments for easier program development and display control.

Timers

Timer 1

- Six-bit prescaler + 8-bit programmable reload timer
  (The prescaler is shared by timer 1, timer 2, and the serial interface.)
- Supports the generation of remote control carrier signals under program control.

Timer 2

- Six-bit prescaler + 8-bit programmable timer
  (The prescaler is shared by timer 1, timer 2, and the serial interface.)
- Can also be used as an event counter.

Base timer (When the 32.768 kHz crystal oscillator option is selected)

- Two frequencies from a set of four base frequencies (either 125 ms and 500 ms, or 100 ms and 250 ms) can be selected as a combination of mask option and program selection to flexibly support end products.

Standby functions

Halt mode

- Instruction execution is stopped in this mode. The oscillator circuits, the timers, the LCD controller and driver circuits, and the serial interface continue to operate. This mode allows unnecessary loops to be avoided and therefore power dissipation can be reduced by the effective use of this mode.
- The halt mode clear (exit) conditions can be set by application programs. The following functions can be used to clear halt mode.
  — Transitions on the INT pin signal (1 factor)
  — Timer 1 (1 factor)
  — Timer 2 (1 factor)
  — Base timer (1 factor)
  — Transitions on either the serial interface pins or the SO4 pin (One or the other of these two factors)
  — Transitions on the S and K port signals as defined by the SSW instruction (8 factors)
  — The reset signal

Hold mode

- This is a full standby mode in which the oscillator circuits are stopped.
- The hold mode clear (exit) conditions can be set by application programs. The following functions can be used to clear hold mode.
  — Transitions on the INT pin signal (1 factor)
  — Timer 2 in event counter mode (1 factor)
  — Transitions on either the serial interface pins or the SO4 pin (One or the other of these two factors)
  — Transitions on the S and K port signals as defined by the SSW instruction (8 factors)
  — The reset signal

Interrupt function (5 factors with 4 vector addresses)

  — Transitions on the INT pin signal (1 factor)
  — Timer 1 (1 factor)
  — Timer 2 (1 factor)
  — Transitions on either the serial interface pins or the SO4 pin (One or the other of these two factors)

Watchdog timer

A 16-bit counter is used. This circuit supports reset based on a combination of two points the program passes through for flexible application support. This watchdog timer circuit supports the following operating times.

Crystal oscillator used (32.768 kHz, 1 or 2 cycles): Up to 2000 ms (max)
CF oscillator used (1 MHz, 1 cycle): Up to 65.536 ms (max)

Subroutine stack

These microcontrollers provide an 8-level stack in special-purpose RAM for subroutines and interrupt handling. Thus data RAM is not required for saving the program counter.

Instruction set

These microcontrollers provide 126 easy-to-use instructions, including accumulator manipulation, register to/from memory transfer, arithmetic, logical operation, flag manipulation, and I/O port control instructions, as well as a full set of conditional branch instructions.

Oscillator circuits (three types)

Single-oscillator specifications: One oscillator, either a CF, RC, or crystal oscillator.
Dual-oscillator specifications: Either a CF and a crystal oscillator, or an RC and a crystal oscillator.
CF (ceramic) oscillator circuit
- Used for the system clock in fast mode
- 400 kHz to 6 MHz

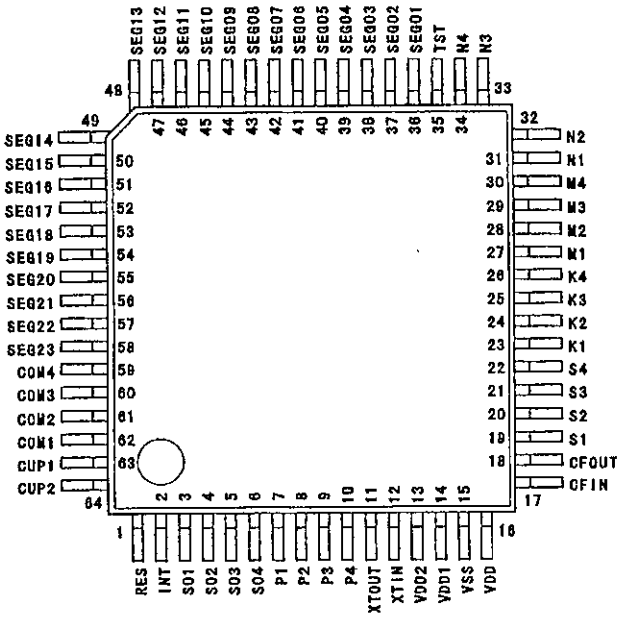
RC (resistor/capacitor) oscillator circuit
- Used for the system clock in fast mode
- 400 kHz to 800 kHz
- Two-terminal oscillator circuit

Crystal oscillator circuit
- Used for the system clock in slow mode
- 32.768, 38.2293, or 65.536 kHz

Package options

- QIP64E (flat package)
- Chip

Pin Assignment

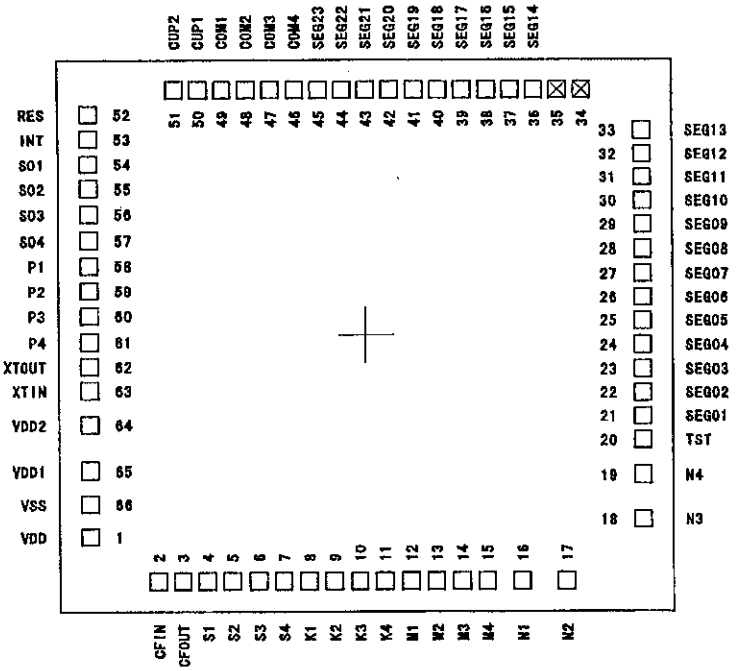


Top view

- Pin 35 (TST) must be connected to VSS during normal operation.
- Consult your Sanyo representative in advance before using solder bath or spray techniques for mounting.

Pad Arrangement

(Applies to the chip version of the product.)

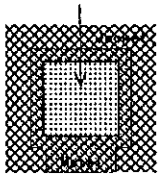


Chip size: 4.10 × 3.69 mm

Thickness: 480 µm

Jacket opening dimensions: 110 × 110 µm

Bonding must be performed within the jacket opening area.



Enlargement View of a Pad

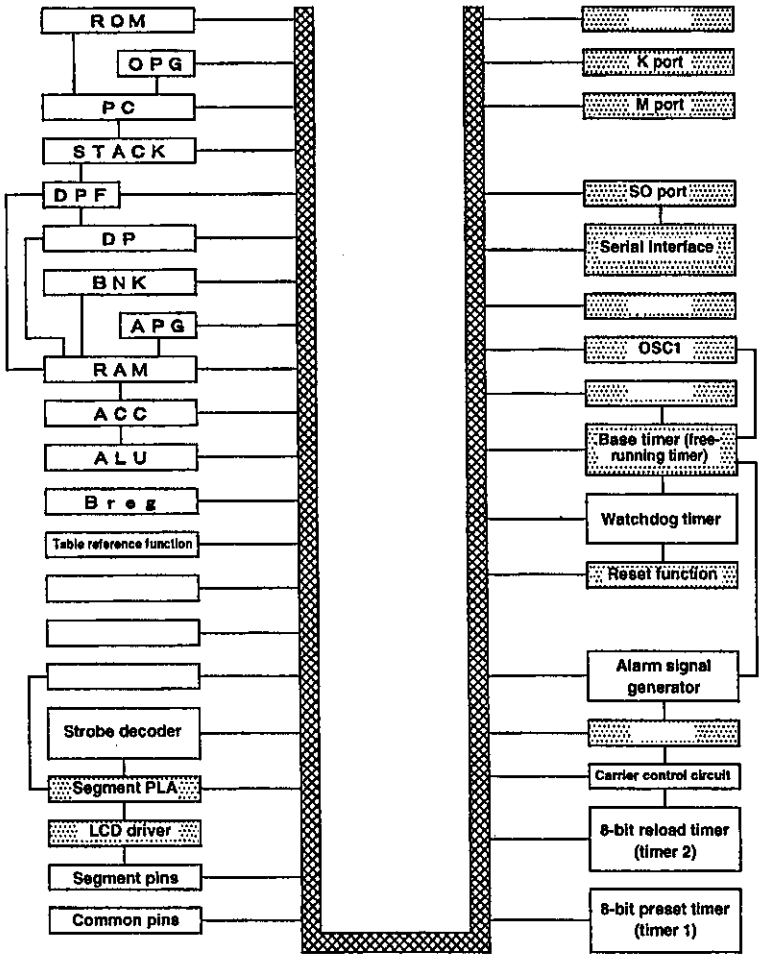
Pad Coordinates (unit: µm)

(Applies to the chip version of the product.)

No.	Pad	X	Y	No.	Pad	X	Y
1	VDD	−1854	−1345	34	——	1452	1650
2	CFIN	−1396	−1650	35	——	1292	1650
3	CFOUT	−1236	−1650	36	SEG14	1132	1650
4	S1	−1071	−1650	37	SEG15	972	1650
5	S2	−901	−1650	38	SEG16	812	1650
6	S3	−731	−1650	39	SEG17	652	1650
7	S4	−561	−1650	40	SEG18	492	1650
8	K1	−391	−1650	41	SEG19	332	1650
9	K2	−221	−1650	42	SEG20	172	1650
10	K3	−51	−1650	43	SEG21	12	1650
11	K4	119	−1650	44	SEG22	−148	1650
12	M1	289	−1650	45	SEG23	−308	1650
13	M2	459	−1650	46	COM4	−468	1650
14	M3	629	−1650	47	COM3	−628	1650
15	M4	799	−1650	48	COM2	−788	1650
16	N1	1034	−1650	49	COM1	−948	1650
17	N2	1333	−1650	50	CUP1	−1108	1650
18	N3	1854	−1234	51	CUP2	−1268	1650
19	N4	1854	−935	52	RES	−1854	1488
20	TST	1854	−705	53	INT	−1854	1323
21	SEG01	1854	−545	54	SO1	−1854	1153
22	SEG02	1854	−385	55	SO2	−1854	983
23	SEG03	1854	−225	56	SO3	−1854	813
24	SEG04	1854	−65	57	SO4	−1854	643
25	SEG05	1854	95	58	P1	−1854	473
26	SEG06	1854	255	59	P2	−1854	303
27	SEG07	1854	415	60	P3	−1854	133
28	SEG08	1854	575	61	P4	−1854	−37
29	SEG09	1854	735	62	XTOUT	−1854	−202
30	SEG10	1854	895	63	XTIN	−1854	−362
31	SEG11	1854	1055	64	VDD2	−1854	−594
32	SEG12	1854	1215	65	VDD1	−1854	−898
33	SEG13	1854	1375	66	VSS	−1854	−1122

- Pad 20 must be connected to V_{SS}.
- Pads 34 and 35 must be left open.

System Block Diagram



Note: Shaded blocks can be selected by the user as mask options.

Mask options overview

Mask options are provided to allow the microcontroller hardware functions to closely match the specifications of the end product. The user can select any combination of options desired. In addition, these microcontroller also provide, as a mask option, a segment PLA function that can set up a correspondence, in single-segment units, between the operation of independently developed software and the actual LCD segments.

Oscillator Circuit Options

- Oscillator selection: Selects oscillator specifications appropriate for the application.
  1: CF, 2: EXT, 3: RC, 4: Crystal, 5: CF & crystal, 6: EXT & crystal, 7 RC & crystal
- CF/EXT frequency: Selects the frequency of the CF (ceramic) or external oscillator.
  1: 400 kHz/10 µs, 2: 800 kHz/5 µs, 3: 2 MHz/2 µs, 4: 4 MHz/1 µs, 5: 6 MHz/0.7µs
- RC frequency: Selects the frequency of the RC (resistor/capacitor) oscillator.
  1: 400 kHz/10 µs, 2: 800 kHz/5 µs
- Xtal selection: Selects the frequency of the crystal oscillator.
  1: 32 kHz/122 µs, 2: 38 kHz/105 µs, 3: 65 kHz/61 µs
- Crystal oscillator specification: Selects the Rd and Cd used with the crystal oscillator.
  1: Internal Rd and Cd used, 2: Internal Rd and Cd unused

LCD Controller/Driver Options

- LCD driver: Selects the LCD driver/controller operating mode appropriate for the drive technique used by the LCD panel used.
  1: Static, 2: Duplex, 3: 1/2B-1/3D, 4: 1/2B-1/4D, 5: 1/3B-1/3D, 6: 1/3B-1/4D, 7 Unused
- LCD frequency: Selects the drive frequency (frame frequency) appropriate for the LCD panel used.
  1: Slow, 2: Typ, 3: Fast

Base Timer Options
- Base timer overflow signal: Selects the base timer basic frequency.
  1: DIVIN divided by 8192 or 32768, 2: DIVIN divided by 4096 or 16384

Serial Interface Options
- SIO counter internal clock speed: Selects the frequency of the internal clock used by the serial interface.
  1: 1 machine cycle, 2: 2 machine cycles, 3: 4 machine cycles

INT Pin Options
- INT pin resistor: Selects the type of INT pin input circuit appropriate for the application
  1: Pulled down, 2: Pulled up, 3: Open
- INT pin interrupt edge: Selects the input level at which the INT external interrupt pin operates.
  1: Falling edge (high to low), 2: Rising edge (low to high)
- INT pin hold transistor: Selects whether or not the level hold function built into the INT pin circuit is used.
  1: Low/high level hold transistor used, 2: Low/high level hold transistor unused

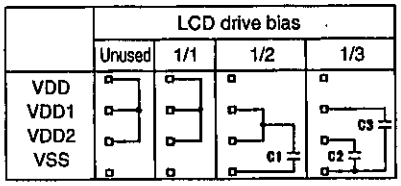
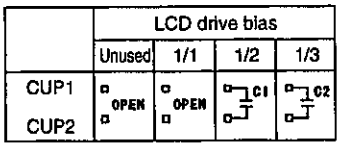
Reset Options
- RESET pin resistor: Selects the type of RES pin input circuit appropriate for the application
  1: Pulled down (high resistance), 2 Pulled up (low resistance), 3: Open (high resistance), 4: Open (low resistance)
- Internal reset: Selects whether or not the internal reset circuit should be used in conjunction with the external reset function.
  1: Used, 2: Unused

Port Internal Resistor Options
- Resistor connection selection: Selects the programmable resistors and the level hold functions that are built into the input ports.
  1. Pull-down resistor, 2: Pull-up resistor

Port Built-in Level Hold Function Options (Selected in 4-bit units): These depend on which of the above-described options were selected.
- Port S hold transistor: Selects whether or not the port S level hold function is used.
  1: Low/high level hold transistors used, 2: Low/high level hold transistors unused
- Port K hold transistors: Selects whether or not the port K level hold function is used.
  1: Low/high level hold transistors used, 2: Low/high level hold transistors unused
- Port M hold transistors: Selects whether or not the port M level hold function is used.
  1: Low/high level hold transistors used, 2: Low/high level hold transistors unused
- Port P hold transistors: Selects whether or not the port P level hold function is used.
  1: Low/high level hold transistors used, 2: Low/high level hold transistors unused
- Port SO hold transistors: Selects whether or not the port SO level hold function is used.
  1: Low/high level hold transistors used, 2: Low/high level hold transistors unused

Port N Options
- N1 pin output type: Selects the type of the port N1 output circuit.
  1: CMOS type, 2: N-channel type
- N2 pin output type: Selects the type of the port N2 output circuit.
  1: CMOS type, 2: N-channel type
- N3 pin output type: Selects the type of the port N3 output circuit.
  1: CMOS type, 2: N-channel type
- N4 pin output type: Selects the type of the port N4 output circuit.
  1: CMOS type, 2: N-channel type
- Port N initial output state: Selects the output levels for port N (N1 through N4) when the reset signal is applied.
  1: High level or off, 2: Low level

Pin Functions

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>State during a reset</th></tr>
<tr><td>VSS</td><td>—</td><td>Ground (–)</td><td></td></tr>
<tr><td>VDD</td><td>—</td><td>Power supply (+)</td><td></td></tr>
<tr><td>VDD1
VDD2</td><td>—
—</td><td>• LCD power supply connections
• The external handling of these pins differs depending on the LCD drive bias technique used.

C1, C2, C3 = 0.1 µF (typ)</td><td></td></tr>
<tr><td>CUP1
CUP2</td><td>—
—</td><td>• LCD drive pins
• The external handling of these pins differs depending on the LCD drive bias technique used.

C1, C2, C3 = 0.1 µF (typ)</td><td></td></tr>
<tr><td>CFIN
CFOUT</td><td>Input
Output</td><td>• OSC1 (fast mode) oscillator element connections
CF specifications: 400 kHz to 6 MHz
RC specifications: 400 kHz to 800 kHz
EXT specifications: 200 kHz to 4 MHz</td><td></td></tr>
<tr><td>XTIN
XTOUT</td><td>Input
Output</td><td>• OSC2 (slow mode) oscillator element connections
Xtal: 32, 38, or 65 kHz</td><td></td></tr>
<tr><td>INT</td><td>Input</td><td>• 1-bit input
• External interrupt input
• The input circuit type and the interrupt level are set in the mask options.
(Pulled up, pulled down, or open)
(Rising edge or falling edge)
• A level hold function, which is designed to prevent input floating states from occurring, is also available as an option.</td><td>• Interrupt reception: disabled
• Level hold function: operational</td></tr>
<tr><td>S1
S2
S3
S4</td><td>Input
Input
Input
Input</td><td>• 4-bit input port
• Pull-up and pull-down resistors, which can be enabled or disabled under program control in a single port unit, are built in.
• Input signal transition detection circuits and chattering exclusion circuits, which can be enabled or disabled under program control in 1-bit units, are built in.
• The chattering exclusion time differs depending on the oscillator specifications.
When a 32.768 kHz crystal oscillator is used the time will be 1.95 or 7.8 ms.
• A level hold function, which is designed to prevent input floating states from occurring on these pins, is also available as an option.</td><td>• Pull-down or pull-up resistors: enabled
(After the reset is cleared: disabled)
• Level hold function: operation disabled
(After the reset is cleared: operation starts)</td></tr>
<tr><td>K1
K2
K3
K4</td><td>I/O
I/O
I/O
I/O</td><td>• 4-bit I/O port
• Pull-up and pull-down resistors, which can be enabled or disabled under program control in a single port unit, are built in.
• Input signal transition detection circuits and chattering exclusion circuits, which can be enabled or disabled under program control in a single port unit, are built in.
• The chattering exclusion time differs depending on the oscillator specifications.
When a 32.768 kHz crystal oscillator is used the time will be 1.95 or 7.8 ms.
• Output circuit type: CMOS
• A level hold function, which is designed to prevent input floating states from occurring on these pins, is also available as an option.</td><td>• Input mode
• Pull-down or pull-up resistors: enabled
(After the reset is cleared: disabled)
• Level hold function: operation disabled
(After the reset is cleared: operation starts)
• Output latch data: high</td></tr>
</table>

Continued on next page.

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Pin	I/O	Function	State during a reset
SO1 SO2 SO3 SO4	I/O I/O I/O I/O	• 4-bit I/O port (also used for the serial interface) SO1: Serial interface input SO2: Serial interface output SO3: Serial interface clock • The serial interface can also be used as a 2-wire interface. • When the serial interface function is not used, the SO4 pin can be used to clear halt mode or as an interrupt pin. • Pull-up and pull-down resistors, which can be enabled or disabled under program control in a single port unit, are built in. • The output circuit type can be switched under program control in a single port unit. (CMOS/n-channel) • A level hold function, which is designed to prevent input floating states from occurring on these pins, is also available as an option.	• Input mode • Pull-down or pull-up resistors: enabled (After the reset is cleared: disabled) • Level hold function: operation disabled (After the reset is cleared: operation starts) • 4-bit parallel mode • Output latch data: high
M1 M2 M3 M4	I/O I/O I/O I/O	• 4-bit I/O port • Pull-up and pull-down resistors, which can be enabled or disabled under program control in a single port unit, are built in. • The output circuit type can be switched under program control in a single port unit. (CMOS/n-channel) • The M4 pin functions as a clock input when timer 2 is operated in event counter mode. • A level hold function, which is designed to prevent input floating states from occurring on these pins, is also available as an option.	• Input mode • Pull-down or pull-up resistors: enabled (After the reset is cleared: disabled) • Level hold function: operation disabled (After the reset is cleared: operation starts) • Output latch data: high
P1 P2 P3 P4	I/O I/O I/O I/O	• 4-bit I/O port • Pull-up and pull-down resistors, which can be enabled or disabled under program control in a single port unit, are built in. • The output circuit type can be switched under program control in a single port unit. (CMOS/n-channel) • A level hold function, which is designed to prevent input floating states from occurring on these pins, is also available as an option.	• Input mode • Pull-down or pull-up resistors: enabled (After the reset is cleared: disabled) • Level hold function: operation disabled (After the reset is cleared: operation starts) • Output latch data: high
N1 N2 N3 N4	Output Output Output Output	• 4-bit output port • The output circuit type can be switched under program control in 1-bit units. (CMOS/n-channel) • This port handles medium-level voltages when the n-channel open-drain output circuit type is selected. • N3 is the remote controller carrier signal output pin. • N4 is the alarm pulse signal output pin.	• The output levels are specified as mask options
SEG1 to SEG23	Output Output	• LCD panel segment drive pins • Six drive techniques are supported. • These pins can be used as general-purpose outputs (either CMOS, p-channel, or n-channel) by specifying mask options. • Any combination of LCD drive and general-purpose output pins can be set up.	• The LCD drive state is specified as a mask option. (Either all lit or all off.) • The LCD driver/controller either operates or stops depending on the oscillator specifications and other mask options. • The states of those pins set up as general-purpose outputs are determined by the mask options. If all segments lit is specified: High or off. If all segments off is specified: Low or off.
COM1 COM2 COM3 COM4	Output Output Output Output	• LCD panel common plate drive pins • One of four pins COM1 to COM4 is selected according to the LCD drive duty technique used. • The LCD drive frequency (frame frequency) is determined by the mask option.	• The LCD driver/controller either operates or stops depending on the oscillator specifications and other mask options
RES	Input	• Microcontroller reset input Applications must apply the reset signal level for at least 200 µs. • The input circuit and the reset level are specified as mask options.	
TST	Input	• Test input • This pin must be tied to the VSS level (the minus side of the power supply).	

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Maximum supply voltage	V_{DD}		−0.3		+7.0	V
	$V_{DD}1$		−0.3		V_{DD}	V
	$V_{DD}2$		−0.3		V_{DD}	V
Maximum input voltage	V_I1	Allowable levels in the specified circuit. XTIN, CFIN	Voltages up to the generated voltage are allowed.			
	V_I2	S1 to 4, K1 to 4, P1 to 4, SO1 to 4, RES, INT, TST (With the K, P, M, and SO ports in input mode)	−0.3		V_{DD} + 0.3	V
Maximum output voltage	V_O1	Allowable levels in the specified circuit. XTOUT, CFOUT	Voltages up to the generated voltage are allowed.			
	V_O2	K1 to 4, P1 to 4, SO1 to 4, N1 to 4, CUP1, CUP2, Seg1 to 23, COM1 to 4 (With the K, P, M, and SO ports in output mode)	−0.3		V_{DD} + 0.3	V
	V_O3	With the open-drain specifications N1 o 4 (Nch)	−0.3		+16	V
Pin output current	I_O1	Per pin. K1 to 4, P1 to 4, M1 to 4, SO1 to 4	0		+10	mA
	I_O2		−10		0	mA
	I_O3		0		5	mA
	I_O4		−5		0	mA
	ΣI_O1	Total current for all pins: K1 to 4, P1 to 4, M1 to 4, SO1 to 4 N1 to 4, Seg1 to 35			40	mA
	ΣI_O2		−40			mA
Allowable power dissipation	Pd max	QFP64E(QIP64E) flat package			300	mW
Operating temperature	Topr		−30		+70	°C
Storage temperature	Tstg		−55		+125	°C

Allowable Operating Ranges at Ta = −30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	LCD unused specifications: $V_{DD}1 = V_{DD}2 = V_{DD}$	2.0		6.0	V
		Static drive specifications: $V_{DD}1 = V_{DD}2 = V_{DD}$	2.0		6.0	V
		1/2 bias specifications: $V_{DD}1 = V_{DD}2 = 1/2V_{DD}$	2.8		6.0	V
		1/3 bias specifications: $V_{DD}1 = 2 \times 1/3V_{DD}$, $V_{DD}2 = 1/3V_{DD}$	2.8		6.0	V
Memory retention supply voltage	V_{HD}	Voltages at which the RAM and register contents are retained*	2.0		V_{DD}	V
High-level input voltage	$V_{IH}1$	S1 to 4, K1 to 4, P1 to 4, M1 to 4, SO1 to 4, INT (With the K, P, M, and SO ports in input mode)	0.7 V_{DD}		V_{DD}	V
Low-level input voltage	$V_{IL}1$	S1 to 4, K1 to 4, P1 to 4, M1 to 4, SO1 to 4, INT (With the K, P, M, and SO ports in input mode)	0		0.3 V_{DD}	V
High-level input voltage	$V_{IH}2$	RES	0.75 V_{DD}		V_{DD}	V
Low-level input voltage	$V_{IL}2$	RES	0		0.25 V_{DD}	V
High-level input voltage	$V_{IH}3$	CFIN	0.75 V_{DD}		V_{DD}	V
Low-level input voltage	$V_{IL}3$	CFIN	0		0.25 V_{DD}	V
Operating frequency 1	fopg1	V_{DD} = 2.0 V to 6.0 V, XTIN/XOUT, 32 kHz Crystal oscillator	32		33	kHz
Operating frequency 2	fopg2	V_{DD} = 2.2 V to 6.0 V, XTIN/XOUT, 38 kHz Crystal oscillator	37		39	kHz
Operating frequency 3	fopg3	V_{DD} = 2.2 V to 6.0 V, XTIN/XOUT, 65 kHz Crystal oscillator	60		70	kHz
Operating frequency 4	fopg4	V_{DD} = 2.2 V to 6.0 V CFIN, CFOUT CF specifications	390		810	kHz
Operating frequency 5	fopg5	V_{DD} = 2.5 V to 6.0 V CFIN, CFOUT CF specifications	390		1200	kHz
Operating frequency 6	fopg6	V_{DD} = 2.8 V to 6.0 V CFIN, CFOUT CF specifications	390		4200	kHz
Operating frequency 7	fopg7	V_{DD} = 4.5 V to 6.0 V CFIN, CFOUT CF specifications	390		6000	kHz
Operating frequency 8	fopg8	V_{DD} = 4.5 V to 6.0 V CFIN, CFOUT RC specifications	400		800	kHz
Operating frequency 9	fopg9	V_{DD} = 3.0 V to 6.0 V CFIN, CFOUT EXT specifications	190		4000	kHz
Operating frequency 10	fopg10	V_{DD} = 3.0 V to 6.0 V Pins SO1 and SO3 (in serial interface mode) Rising and falling edges on the input signal and clock waveform must be ≤ 10 µs	DC		200	kHz

Note * : The state where the CF/RC and crystal oscillators are completely stopped, and all internal circuits completely stopped.

Electrical Characteristics at Ta = –30 to +70°C, V_{DD} = 2.5 to 3.2 V, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Input resistance	$R_{IN}1$ A	V_{IN} = 0.2 V_{DD}, Low level hold transistor*	60	300	1200	kΩ
	$R_{IN}1$ B	Pull-down resistor*	30	150	500	kΩ
	$R_{IN}1$ C	V_{IN} = 0.8 V_{DD}, High level hold transistor*	60	300	1200	kΩ
	$R_{IN}1$ D	V_{IN} = V_{SS}, Pull-up resistor*	30	150	500	kΩ
	$R_{IN}2$ A	V_{IN} = 0.2 V_{DD}, INT pin low level hold transistor	60	300	1200	kΩ
	$R_{IN}2$ B	V_{IN} = V_{DD}, INT pin pull-down resistor	300	1500	5000	kΩ
	$R_{IN}2$ C	V_{IN} = 0.8 V_{DD}, INT pin high level hold transistor	60	300	1200	kΩ
	$R_{IN}2$ D	V_{IN} = V_{SS}, INT pin pull-up resistor	300	1500	5000	kΩ
	$R_{IN}3$	V_{IN} = V_{DD}, RES pin pull-down resistor	10	30	50	kΩ
	$R_{IN}4$	V_{IN} = V_{SS}, RES pin pull-up resistor	10	30	50	kΩ
	$R_{IN}5$	V_{IN} = V_{DD}, TST pin pull-down resistor	10	30	50	kΩ
High-level output voltage	$V_{OH}1$	I_{OH} = –500 µA, N1 to 4	V_{DD} – 0.5			V
Low-level output voltage	$V_{OL}1$	I_{OL} = 1.0 mA, N1 to 4			0.5	V
High-level output voltage	$V_{OH}2$	I_{OH} = –400 µA, K1 to 4, P1 to 4, M1 to 4, SO1 to 4 (With the K, P, M, and SO ports in output mode)	V_{DD} – 0.5			V
Low-level output voltage	$V_{OL}2$	I_{OL} = 400 µA, K1 to 4, P1 to 4, M1 to 4, SO1 to 4 (With the K, P, M, and SO ports in output mode)			0.5	V
Output off leakage current	$\|I_{OFF}\|$	V_{OH} = 10.5 V, N1 to 4 (Open specifications)			1.0	µA
Segment Port Output Impedances						
[CMOS output port mode]						
High-level output voltage	$V_{OH}3$	I_{OH} = –100 µA, Seg 1 to 23	V_{DD} – 0.5			V
Low-level output voltage	$V_{OL}3$	I_{OL} = 100 µA, Seg 1 to 23			0.5	V
[P-channel open-drain output port mode]						
High-level output voltage	$V_{OH}3$	I_{OH} = –100 µA, Seg 1 to 23	V_{DD} – 0.5			V
Output off leakage current	$\|I_{OFF}\|$	V_{OL} = V_{SS}, Seg 1 to 23			1.0	µA
[N-channel open-drain output port mode]						
Low-level output voltage	$V_{OL}3$	I_{OL} = 100 µA, Seg 1 to 23			0.5	V
Output off leakage current	$\|I_{OFF}\|$	V_{OH} = V_{DD}, Seg 1 to 23			1.0	µA
[Static drive]						
High-level output voltage	$V_{OH}4$	I_{OH} = –20 µA, Seg 1 to 23	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}4$	I_{OL} = 20 µA, Seg 1 to 23			0.2	V
High-level output voltage	$V_{OH}5$	I_{OH} = –100 µA, COM1	V_{DD} – 0.2			V
Low-level output voltage	$V_{OL}5$	I_{OL} = 100 µA, COM1			0.2	V

Note *: The 20 pins S1 to S4, K1 to K4, P1 to P4, M1 to M4, and SO1 to SO4.

Electrical Characteristics at Ta = –30 to +70°C, V_{DD} = 3.0 to 4.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions and applicable pins	Ratings			Unit
			min	typ	max	
Input resistance	R_{IN}1 A	V_{IN} = 0.2 V_{DD}, Low level hold transistor*	35	200	800	kΩ
	R_{IN}1 B	Pull-down resistor*	15	80	300	kΩ
	R_{IN}1 C	V_{IN} = 0.8 V_{DD}, High level hold transistor*	35	200	800	kΩ
	R_{IN}1 D	V_{IN} = V_{SS}, Pull-up resistor*	15	80	300	kΩ
	R_{IN}2 A	V_{IN} = 0.2 V_{DD}, INT pin low level hold transistor	35	200	800	kΩ
	R_{IN}2 B	V_{IN} = V_{DD}, INT pin pull-down resistor	150	800	3000	kΩ
	R_{IN}2 C	V_{IN} = 0.8 V_{DD}, INT pin high level hold transistor	35	200	800	kΩ
	R_{IN}2 D	V_{IN} = V_{SS}, INT pin pull-up resistor	150	800	3000	kΩ
	R_{IN}3	V_{IN} = V_{DD}, RES pin pull-down resistor	10	30	50	kΩ
	R_{IN}4	V_{IN} = V_{SS}, RES pin pull-up resistor	10	30	50	kΩ
	R_{IN}5	V_{IN} = V_{DD}, TST pin pull-down resistor	10	30	50	kΩ
High-level output voltage	V_{OH}1	I_{OH} = –1.0 mA, N1 to 4	V_{DD} – 0.5			V
Low-level output voltage	V_{OL}1	I_{OL} = 2.0 mA, N1 to 4			0.5	V
High-level output voltage	V_{OH}2	I_{OH} = –500 µA, K1 to 4, P1 to 4, M1 to 4, SO1 to 4 (With the K, P, M, and SO ports in output mode)	V_{DD} – 0.5			V
Low-level output voltage	V_{OL}2	I_{OL} = 500 µA, K1 to 4, P1 to 4, M1 to 4, SO1 to 4 (With the K, P, M, and SO ports in output mode)			0.5	V
Output off leakage current	| OFF |	V_{OH} = 10.5 V, N1 to 4 (Open specifications)			1.0	µA
Segment Port Output Impedances						
[CMOS output port mode]						
High-level output voltage	V_{OH}3	I_{OH} = –300 µA, Seg 1 to 23	V_{DD} – 0.5			V
Low-level output voltage	V_{OL}3	I_{OL} = 300 µA, Seg 1 to 23			0.5	V
[P-channel open-drain output port mode]						
High-level output voltage	V_{OH}3	I_{OH} = –300 µA, Seg 1 to 23	V_{DD} – 0.5			V
Output off leakage current	| OFF |	V_{OL} = V_{SS}, Seg 1 to 23			1.0	µA
[N-channel open-drain output port mode]						
Low-level output voltage	V_{OL}3	I_{OL} = 300 µA, Seg 1 to 23			0.5	V
Output off leakage current	| OFF |	V_{OH} = V_{DD}, Seg 1 to 23			1.0	µA
[Static drive]						
High-level output voltage	V_{OH}4	I_{OH} = –20 µA, Seg 1 to 23	V_{DD} – 0.2			V
Low-level output voltage	V_{OL}4	I_{OL} = 20 µA, Seg 1 to 23			0.2	V
High-level output voltage	V_{OH}5	I_{OH} = –100 µA, COM1	V_{DD} – 0.2			V
Low-level output voltage	V_{OL}5	I_{OL} = 100 µA, COM1			0.2	V
[1/2 bias drive]						
High-level output voltage	V_{OH}4	I_{OH} = –20 µA, Seg 1 to 23	V_{DD} – 0.2			V
Low-level output voltage	V_{OL}4	I_{OL} = 20 µA, Seg 1 to 23			0.2	V
High-level output voltage	V_{OH}5	I_{OH} = –100 µA, COM1 to 4	V_{DD} – 0.2			V
Output middle-level voltage	V_{OM}	I_{OH} = –100 µA, COM1 to 4	$V_{DD}/2$ – 0.2		$V_{DD}/2$ + 0.2	V
		I_{OL} = 100 µA, COM1 to 4	–0.2		+0.2	V
Low-level output voltage	V_{OL}5	I_{OL} = 100 µA, COM1 to 4			0.2	V
[1/3 bias drive]						
High-level output voltage	V_{OH}4	I_{OH} = –20 µA, Seg1 to 23	V_{DD} – 0.2			V
Output middle-level voltage	V_{OM}1-1	I_{OH} = –20 µA, Seg1 to 23	$2V_{DD}/3$ – 0.2		$2V_{DD}/3$ + 0.2	V
	V_{OM}1-2	I_{OL} = 20 µA, Seg1 to 23	$V_{DD}/3$ – 0.2		$V_{DD}/3$ + 0.2	V
Low-level output voltage	V_{OL}4	I_{OL} = 20 µA, Seg 1 to 23			0.2	V
High-level output voltage	V_{OH}6	I_{OH} = –100 µA, COM1 to 4	V_{DD} – 0.2			V
Output middle-level voltage	V_{OM}2-1	I_{OH} = –100 µA, COM1 to 4	$2V_{DD}/3$ – 0.2		$2V_{DD}/3$ + 0.2	V
	V_{OM}2-2	I_{OL} = 100 µA, COM1 to 4	$V_{DD}/3$ – 0.2		$V_{DD}/3$ + 0.2	V
Low-level output voltage	V_{OL}6	I_{OL} = 100 µA, COM1 to 4			0.2	V

Note *: The 20 pins S1 to S4, K1 to K4, P1 to P4, M1 to M4, and SO1 to SO4.

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Parameter	Symbol	Conditions and applicable pins			Ratings min	Ratings typ	Ratings max	Unit
Supply leakage current	ILEK1	V_{DD} = 3.0 V, Ta = 25°C				0.2	1.0	µA
	ILEK2	V_{DD} = 3.0 V, Ta = 50°C				1.0	5.0	µA
Input leakage current	I OFF	V_{IN} = V_{DD}	V_{DD} = 3.0 V, S1 to 4, K1 to 4, P1 to 4, M1 to 4, SO1 to 4, INT, RES (With the K, P, M, and SO ports in input mode and with the open specifications selected for the INT and RES pins.)				1.0	µA
		V_{IN} = V_{SS}			–1.0			µA
Output voltage 1	V_{DD}1-1	V_{DD} = 3.0 V, C1 = C2 = 0, 1 µF, V_{DD}1 = V_{DD}2, 1/2Bias, fopg = 32.768 kHz			1.3	1.5	1.7	V
Supply current 1	I_{DD}1-1	V_{DD} = 3.0 V, Ta = 25°C		Crystal oscillator specifications Crystal: 32 kHz (Cd and Rd built in) Cg = 11 pF, CI = 31 kΩ Halt mode, LCD = 1/3bias		7	15	µA
	I_{DD}1-2	V_{DD} = 3.0 V, Ta = 50°C					20	µA
Supply current 2	I_{DD}2-1	V_{DD} = 3.0 V, Ta = 25°C		CF oscillator specifications CF: 455 kHz Ccg = Ccd = 220 pF Halt mode, LCD = 1/3 bias		100	150	µA
	I_{DD}2-2	V_{DD} = 3.0 V, Ta = 50°C					200	µA
Supply current 3	I_{DD}3-1	V_{DD} = 3.0 V, Ta = 25°C		CF oscillator specifications CF: 1000 kHz Ccg = Ccd = 100 pF Halt mode, LCD = 1/3 bias		150	200	µA
	I_{DD}3-2	V_{DD} = 3.0 V, Ta = 50°C					300	µA
Supply current 4	I_{DD}4-1	V_{DD} = 3.0 V, Ta = 25°C		CF oscillator specifications CF: 4000 kHz Ccg = Ccd = 33 pF Halt mode, LCD = 1/3 bias		160	220	µA
	I_{DD}4-2	V_{DD} = 3.0 V, Ta = 50°C					330	µA
Oscillator startup voltage	$\|V_{STT}\|$	Tstt ≤ 5 s		Crystal oscillator specifications Crystal: 32 kHz (Cd and Rd built in) Cg = 11 pF, CI = 31 kΩ			2.2	V
Oscillator hold voltage	$\|V_{HOLD}\|$				2.0		6.0	V
Oscillator startup time	$\|T_{STT}\|$	V_{DD} = 2.2 V					5	s
Oscillator stability	Δf	V_{DD} = 2.95 to 3.05 V					3	ppm
Oscillator startup voltage	$\|V_{STT}\|$	Tstt ≤ 5 s		Crystal oscillator specifications Crystal: 38 or 65 kHz XCg = 12 pF, CI ≤ 31 kΩ			2.4	V
Oscillator hold voltage	$\|V_{HOLD}\|$				2.2		6.0	V
Oscillator startup time	$\|T_{STT}\|$	V_{DD} = 2.4 V					5	s
Oscillator startup voltage	$\|V_{STT}\|$	Tstt ≤ 30 ms		CF oscillator specifications With a 455-kHz CF element used Ccg = Ccd = 220 pF			2.2	V
Oscillator hold voltage	$\|V_{HOLD}\|$				2.1		6.0	V
Oscillator startup time	$\|T_{STT}\|$	V_{DD} = 2.2 V					30	ms
Oscillator startup voltage	$\|V_{STT}\|$	Tstt ≤ 30 ms		CF oscillator specifications With a 1-MHz CF element used Ccg = Ccd = 100 pF			2.5	V
Oscillator hold voltage	$\|V_{HOLD}\|$				2.4		6.0	V
Oscillator startup time	$\|T_{STT}\|$	V_{DD} = 2.5 V					30	ms
Oscillator startup voltage	$\|V_{STT}\|$	Tstt ≤ 30 ms		CF oscillator specifications With a 4-MHz CF element used Ccg = Ccd = 33 pF			2.8	V
Oscillator hold voltage	$\|V_{HOLD}\|$				2.7		6.0	V
Oscillator startup time	$\|T_{STT}\|$	V_{DD} = 2.8 V					30	ms
Oscillator correction capacitance	Cd	V_{DD} = 3.0 V, XTOUT (built in)				20		pF

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Parameter	Symbol	Conditions and applicable pins	Ratings min	Ratings typ	Ratings max	Unit
Input resistance	$R_{IN}1$ A	V_{IN} = 0.2 V_{DD}, Low level hold transistor*	30	120	500	kΩ
	$R_{IN}1$ B	V_{IN} = V_{DD}, Pull-down resistor*	10	50	200	kΩ
	$R_{IN}1$ C	V_{IN} = 0.8 V_{DD}, High level hold transistor*	30	120	500	kΩ
	$R_{IN}1$ D	V_{IN} = V_{SS}, Pull-up resistor*	10	50	200	kΩ
	$R_{IN}2$ A	V_{IN} = 0.2 V_{DD}, INT pin low level hold transistor	30	120	500	kΩ
	$R_{IN}2$ B	V_{IN} = V_{DD}, INT pin pull-down resistor	100	500	2000	kΩ
	$R_{IN}2$ C	V_{IN} = 0.8 V_{DD}, INT pin high level hold transistor	30	120	500	kΩ
	$R_{IN}2$ D	V_{IN} = V_{SS}, INT pin pull-up resistor	100	500	2000	kΩ
	$R_{IN}3$	V_{IN} = V_{DD}, RES pin pull-down resistor	10	30	50	kΩ
	$R_{IN}4$	V_{IN} = V_{SS}, RES pin pull-up resistor	10	30	50	kΩ
	$R_{IN}5$	V_{IN} = V_{DD}, TST pin pull-down resistor	10	30	50	kΩ
High-level output voltage	$V_{OH}1$	I_{OH} = −5.0 mA, N1 to 4	V_{DD} − 0.5			V
Low-level output voltage	$V_{OL}1$	I_{OL} = 5.0 mA, N1 to 4			0.5	V
High-level output voltage	$V_{OH}2$	I_{OH} = −1.0 mA, K1 to 4, P1 to 4, M1 to 4, SO1 to 4 (With the K, P, M, and SO ports in output mode)	V_{DD} − 0.5			V
Low-level output voltage	$V_{OL}2$	I_{OL} = 2.0 mA, K1 to 4, P1 to 4, M1 to 4, SO1 to 4 (With the K, P, M, and SO ports in output mode)			0.5	V
Output off leakage current	$\|I_{OFF}\|$	V_{OH} = 10.5 V, N1 to 4 (Open specifications)			1.0	μA
Segment Port Output Impedances						
[CMOS output port mode]						
High-level output voltage	$V_{OH}3$	I_{OH} = −500 μA, Seg 1 to 23	V_{DD} − 0.5			V
Low-level output voltage	$V_{OL}3$	I_{OL} = 500 μA, Seg 1 to 23			0.5	V
[P-channel open-drain output port mode]						
High-level output voltage	$V_{OH}3$	I_{OH} = −500 μA, Seg 1 to 23	V_{DD} − 0.5			V
Output off leakage current	$\|I_{OFF}\|$	V_{OL} = V_{SS}, Seg 1 to 23			1.0	μA
[N-channel open-drain output port mode]						
Low-level output voltage	$V_{OL}3$	I_{OL} = 500 μA, Seg 1 to 23			0.5	V
Output off leakage current	$\|I_{OFF}\|$	V_{OH} = V_{DD}, Seg 1 to 23			1.0	μA
[Static drive]						
High-level output voltage	$V_{OH}4$	I_{OH} = −40 μA, Seg 1 to 23	V_{DD} − 0.2			V
Low-level output voltage	$V_{OL}4$	I_{OL} = 40 μA, Seg 1 to 23			0.2	V
High-level output voltage	$V_{OH}5$	I_{OH} = −400 μA, COM1	V_{DD} − 0.2			V
Low-level output voltage	$V_{OL}5$	I_{OL} = 400 μA, COM1			0.2	V
[1/2 bias drive]						
High-level output voltage	$V_{OH}4$	I_{OH} = −40 μA, Seg 1 to 23	V_{DD} − 0.2			V
Low-level output voltage	$V_{OL}4$	I_{OL} = 40 μA, Seg 1 to 23			0.2	V
High-level output voltage	$V_{OH}5$	I_{OH} = −400 μA, COM1 to 4	V_{DD} − 0.2			V
Output middle-level voltage	V_{OM}	I_{OH} = −400 μA, COM1 to 4	$V_{DD}/2$ − 0.2		$V_{DD}/2$ + 0.2	V
		I_{OL} = 400 μA, COM1 to 4	$V_{DD}/2$ − 0.2		$V_{DD}/2$ + 0.2	V
Low-level output voltage	$V_{OL}5$	I_{OL} = 400 μA, COM1 to 4			0.2	V
[1/3 bias drive]						
High-level output voltage	$V_{OH}4$	I_{OH} = −40 μA, Seg1 to 23	V_{DD} − 0.2			V
Output middle-level voltage	$V_{OM}1$-1	I_{OH} = −40 μA, Seg1 to 23	$2V_{DD}/3$ − 0.2		$2V_{DD}/3$ + 0.2	V
	$V_{OM}1$-2	I_{OL} = 40 μA, Seg1 to 23	$2V_{DD}/3$ − 0.2		$2V_{DD}/3$ + 0.2	V
Low-level output voltage	$V_{OL}4$	I_{OL} = 40 μA, Seg 1 to 23			0.2	V
High-level output voltage	$V_{OH}6$	I_{OH} = −400 μA, COM1 to 4	V_{DD} − 0.2			V
Output middle-level voltage	$V_{OM}2$-1	I_{OH} = −400 μA, COM1 to 4	$2V_{DD}/3$ − 0.2		$2V_{DD}/3$ + 0.2	V
	$V_{OM}2$-2	I_{OL} = 400 μA, COM1 to 4	$V_{DD}/3$ − 0.2		$V_{DD}/3$ + 0.2	V
Low-level output voltage	$V_{OL}6$	I_{OL} = 400 μA, COM1 to 4			0.2	V

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Parameter	Symbol	Conditions and applicable pins			Ratings min	Ratings typ	Ratings max	Unit
Supply leakage current	ILEK1	V_{DD} = 6.0 V, Ta = 25°C				0.2	1.0	µA
	ILEK2	V_{DD} = 6.0 V, Ta = 50°C				1.0	5.0	µA
Input leakage current	I OFF	V_{IN} = V_{DD}	V_{DD} = 3.0 V, S1 to 4, K1 to 4, P1 to 4, M1 to 4, SO1 to 4, INT, RES (With the K, P, M, and SO ports in input mode and with the open specifications selected for the INT and RES pins.)				1.0	µA
		V_{IN} = V_{SS}			−1.0			µA
Output voltage 2	V_{DD}1-2	V_{DD} = 5.0 V, C1 = C2 = 0.1 µF, V_{DD}1 = V_{DD}2, 1/2Bias, fopg = 32.768 kHz			2.4	2.5	2.6	V
Output voltage 3	V_{DD}1-3	V_{DD} = 5.0 V, C1 = C2 = 0.1 µF			1.4	1.67	1.8	V
	V_{DD}2-3	1/3 bias, fopg = 32.768 kHz			3.1	3.33	3.5	V
Current drain 1	I_{DD}1-1	V_{DD} = 5.0 V, Ta = 25°C	Crystal oscillator specifications Crystal: 32 kHz (Cd and Rd built in) Cg = 11 pF, CI = 31 kΩ Halt mode, LCD = 1/3bias			45.0	60.0	µA
	I_{DD}1-2	V_{DD} = 5.0 V, Ta = 50°C					65	µA
Current drain 2	I_{DD}2-1	V_{DD} = 5.0 V, Ta = 25°C	CF oscillator specifications CF: 455 kHz Ccg = Ccd = 220 pF Halt mode, LCD = 1/3 bias			450	600	µA
	I_{DD}2-2	V_{DD} = 5.0 V, Ta = 50°C					650	µA
Current drain 3	I_{DD}3-1	V_{DD} = 5.0 V, Ta = 25°C	CF oscillator specifications CF: 4000 kHz Ccg = Ccd = 33 pF Halt mode, LCD = 1/3 bias			500	700	µA
	I_{DD}3-2	V_{DD} = 5.0 V, Ta = 50°C					800	µA
Current drain 4	I_{DD}4-1	V_{DD} = 5.0 V, Ta = 25°C	CF oscillator specifications CF: 6000 kHz Ccg =. Ccd = 33 pF Halt mode, LCD = 1/3 bias			800	1000	µA
	I_{DD}4-2	V_{DD} = 5.0 V, Ta = 50°C					1150	µA
Oscillator correction capacitance	Cd	V_{DD} = 5.0 V, XTOUT (built in)				20		pF

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