Ordering number: EN5233

Monolithic Digital IC

# LB8109M

## Actuator Driver for Portable CD Players

## Overview

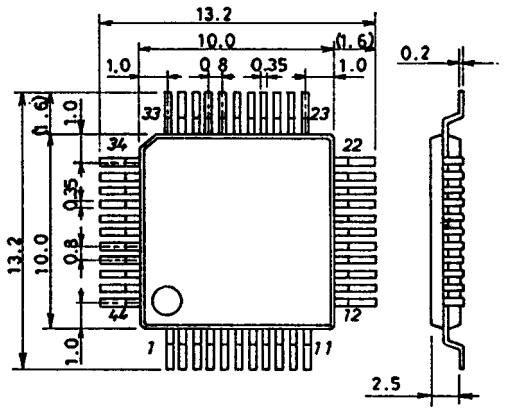
The LB8109M is an actuator driver IC designed for portable CD players that operate at 2.4 V (two Ni-Cd batteries) or 3.0 V (two dry cells).

## Package Dimensions

unit : mm

**3148-QIP44MA**

[LB8109M]




SANYO : QIP44MA

## Functions and Features

- H bridge drivers (output dynamic range maximum is about 2 V) on chip for four channels to drive each CD actuator (the focus coil, the tracking coil, the spindle motor, and the sled motor).
- Step-up circuit (voltage to be set by an external resistor) on chip that is used to apply voltage to the CD DSP, ASP and microcontroller. Center-tap coil for step-up circuit makes it possible to supply the driver control voltage. (However, the drive Tr, L, C, and Di are all external.)
- Oscillator circuits for each converter on chip. (C and R are external.)
- Four-channel driver control output is divided into two groups (the focus/tracking group and the spindle/sled group) for minimum loss at double-speed play.
  Higher operating voltage in each group is converted to power supply of each 2ch H bridge driver by PMW conversion.
  (However, the PWM PNP-Tr, NPN-Tr, L, C, and Di are all external.)
- Sled motor driving mode is switchable between step drive mode for lower power dissipation, and normal V-type drive mode.
  (The other three channels are fixed to V-type.)
- In the spindle motor drive circuit, the control gain can be doubled for double-speed play. (Switching port provided.)
- PWM step-down circuit for external power operates when external power (8 V or more) is supplied.
  In this function, external power is converted to $V_{CC}$ power supply, and two type voltage setting is possible.
  In play mode, step-up voltage for DSP has to be set lower than $V_{CC}$, but in charging the battery, it has to be set higher than $V_{CC}$.
  So step-down voltage ($V_{CC}$) setting of two types is possible with two pairs of external resistor. (Switching port is provided.)
  (However, the PWM PNP-Tr, NPN-Tr, L, C, and Di are all external.)
- Battery pulse charging function on chip. (However, the drive NPN-Tr, and the current feedback C and R are external.)
- Having one 358-type OP amplifier on chip, it is suitable for a variety of applications. (Power supply: $V_{CD}$)
- The system can be started up and stopped by outputs from the microcontroller.
- Actuator muting function on chip (for all four channels simultaneously).
- Thermal shutdown circuit on chip.

# Specifications

## Absolute Maximum Ratings at Ta = 25 °C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}$max | | 7 | V |
| $V_{CD}$ pin input voltage | $V_{CD}$max | | 10 | V |
| H bridge output current | $I_{OUT}$max | Maximum per channel is 400 mA. | 800 | mA |
| Allowable power dissipation | Pd max | Independant IC | 700 | mW |
| Operating temperature | Topr | | –20 to +75 | °C |
| Storage temperature | Tstg | | –55 to +150 | °C |

## Allowable Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 1.6 to 5.0 | V |
| $V_{CD}$ pin input voltage | $V_{CD}$ | | 3.6 to 9.0 | V |
| $V_{CC}$ drop setting voltage when external voltage input is applied | $V_{CC(EXT)}$ | | 3.0 to 5.0 | V |

## Electrical Characteristics at Ta = 25 °C, $V_{CC}$ = 3 V, $V_{CD}$ = 4 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| [Power Supply Block] | | | | | | |
| Standby current drain | $I_{CCO}$ | S/S = [H], the total of $V_{CC}$ and $V_{CD}$ | | | 20 | µA |
| $V_{CC}$ no-signal current drain | $I_{CC}$ | S/S = [L], $V_{CC}$ line only | | 7.0 | 10.0 | mA |
| $V_{CD}$ no-signal current drain | $I_{CD}$ | S/S = [L], with no driver input | | 5.0 | 8.0 | mA |
| [Externally set step-up circuit] | | | | | | |
| ASP drive output current | $I_{O\ ASPDRV}$ | $V_{ASP}$ = 1 V | 2.2 | 2.8 | 3.4 | mA |
| Reference voltage of step-up circuit | $V_{ref\ ASP}$ | Determined at ASP drive pin | 1.23 | 1.28 | 1.33 | V |
| $V_{ASP}$ pin input bias current | $I_{B\ V\ ASP}$ | $V_{ASP}$ = 1.5 V | | | 200 | nA |
| UPBASE pin saturation voltage | $V_{O\ UPBASE}$ | $I_O$ = 1 mA | | | 0.2 | V |
| Load regulation | $R_{LD\ ASP}$ | $V_{ASP}$ = 3.5 V, L = 30 µH, C = 220 µF | | | 1000 | mV/A |
| Line regulation | $R_{LN\ ASP}$ | $V_{ASP}$ = 3.5 V, L = 30 µH, C = 220 µF | | | 100 | mV/V |
| Minimum off duty | $D_{min\ ASP}$ | | | 20 | | % |
| [S/S Pin Function] | | | | | | |
| S/S start voltage | $V_{SS}$ON | | | | $V_{CC}$–1.0 | V |
| S/S off voltage | $V_{SS}$OFF | | $V_{CC}$–0.5 | | | V |
| [H Bridge Output Block, PWM Block] | | | | | | |
| Output saturation voltage | $V_{H\ sat}$ | $I_O$ = 200 mA, TOP + BOTTOM | | 0.30 | 0.45 | V |
| $V_{OUT}$ pin maximum output voltage | $V_{OUT}$ max | | | 2.25 | | V |
| PWM applied offset voltage | $V_{PWMOFF}$ | At mute state (each output = 0) | 0.23 | 0.26 | 0.29 | V |
| DNB – 1,2 pins output current | Io DNB1,2 | | | $V_{OUT}$/600 | | A |
| Load regulation | $R_{LD}V_{OUT}$ | $V_{OUT}$ = max, L = 30 µH | | | 1000 | mV/A |
| Line regulation | $R_{LN}V_{OUT}$ | $V_{OUT}$ = max, L = 30 µH | | | 100 | mV/V |
| [Drive Control Block] | | | | | | |
| CH1 to 4 input voltage range | $V_{IN1–4}$ | | 0.5 | | $V_{CD}$–0.5 | V |
| ASP REF input voltage range | $V_{ASPR}$ | | 1.2 | | $V_{CD}$–1.3 | V |
| Input bias current | $I_{B\ IN}$ | Each $V_{IN}$ = $V_{ASP\ REF}$ = 2 V | | | 2.0 | µA |
| Input offset voltage | $V_{off\ IN}$ | $V_{ASP\ REF}$ = 2 V | –30 | | +30 | mV |
| CH1,2,4 transfer gain | $G124_{IN}$ | $R_L$ = 10 Ω | 7.1 | 8.3 | 9.5 | dB |
| CH3 L side transfer gain | $G3L_{IN}$ | $R_L$ = 10 Ω | 7.1 | 8.3 | 9.5 | dB |
| CH3 H side transfer gain | $G3H_{IN}$ | $R_L$ = 10 Ω | 13.6 | 14.8 | 16.0 | dB |

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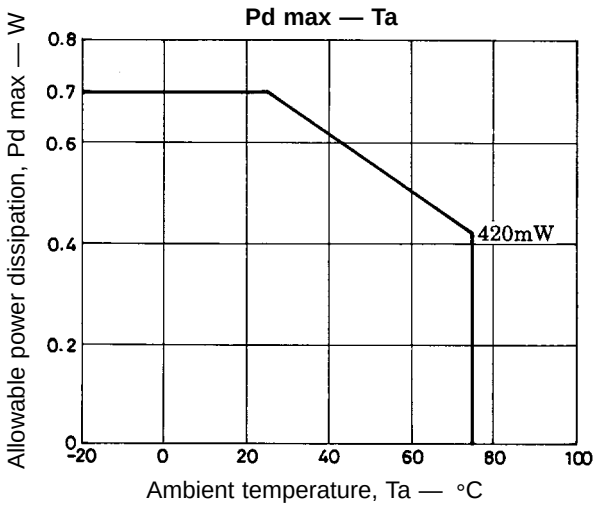
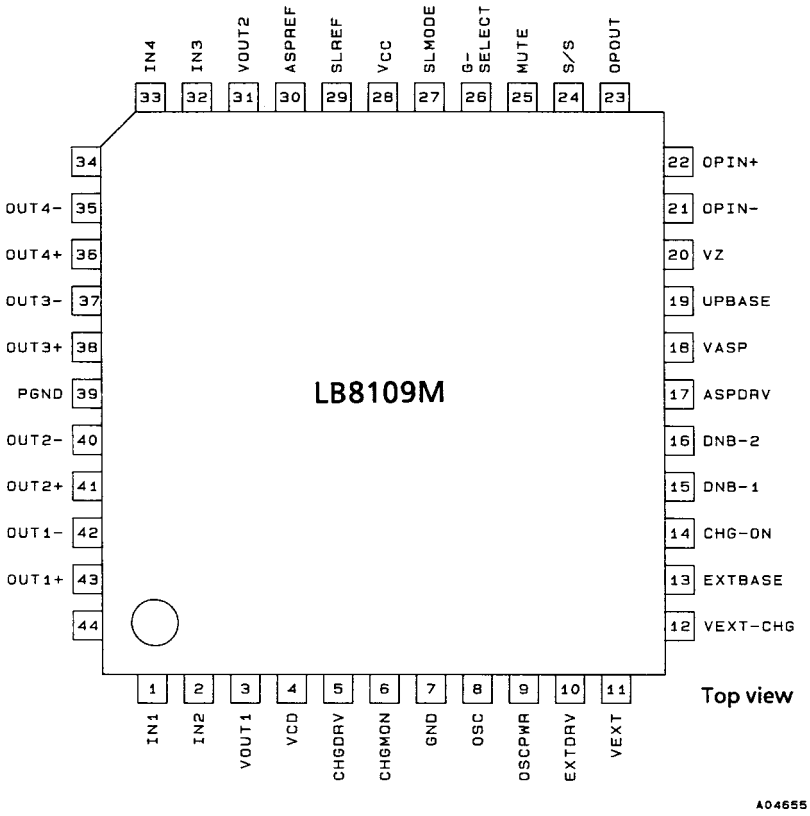
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Negative/positive transfer gain difference | $\Delta G_{IN}$ | $R_L$ = 10 Ω | –1.0 | 0 | +1.0 | dB |
| Input dead zone voltage range | $V_{DZ}$ | $R_L$ = 10 Ω, output voltage difference 5 mV or less | 0 | | 30 | mV |
| G-SELECT pin low-gain side selection voltage | $V_{GSELL-TH}$ | | 2.0 | | | V |
| G-SELECT pin high-gain side selection voltage | $V_{GSELH-TH}$ | | | | 1.0 | V |
| [SLED Drive Circuit] | | | | | | |
| SL REF pin input voltage range | $V_{SL\ REF}$ | | $V_{ASP\ REF}$+0.1 | | $V_{CD}$–1.0 | V |
| SL REF pin input bias current | $I_{B\ SL\ REF}$ | $V_{SL\ REF}$ = 2 V | | | 200 | nA |
| Positive side setting offset voltage between IN4 and SL REF | $V_{off\ SL\ REF}$ | $V_{SL\ REF}$ = 2.3 V, $V_{ASP\ REF}$ = 2 V | –20 | | +20 | mV |
| Dual side step width difference voltage | $V_{SL\ DIFF}$ | $V_{SL\ REF}$ = 2.3 V, $V_{ASP\ REF}$ = 2 V | –25 | | +25 | mV |
| SL MODE pin high voltage | $V_{H\ SL\ MODE}$ | | 2.0 | | | V |
| SL MODE pin low voltage | $V_{L\ SL\ MODE}$ | | | | 1.0 | V |
| [Muting Block] | | | | | | |
| Mute on voltage | $V_{ON\ MUTE}$ | | 2.0 | | | V |
| Mute off voltage | $V_{OFF\ MUTE}$ | | | | 1.0 | V |
| [OP Amplifier Block] | | | | | | |
| Input offset voltage | $V_{OFF\ OP}$ | | –5 | | +5 | mV |
| Input bias current for each input | $I_{B\ OP}$ | OPin(+) = OPin(–) = 2 V | | | 200 | nA |
| Common-mode input voltage range | $V_{CM\ OP}$ | | | | $V_{CD}$–1.5 | V |
| Open-loop voltage gain | $G_{V\ OP}$ | at f = 10 kHz | 31 | 34 | 37 | dB |
| [External Voltage Input Block] | | | | | | |
| Minimum operating input voltage when external voltage input is applied | $V_{I\ EXT}$ | $R_{IN}$ = 1 kΩ | 8.0 | | | V |
| EXTDRV pin output current | $I_{O\ EXT\ DRV}$ | $V_{EXT}$ = 1 V (CHG-ON [L]) | 170 | 210 | 250 | μA |
| VZ pin voltage | $V_Z$ | $V_{EXT}$ = 10 V, $R_{IN}$ = 1 kΩ | 6.4 | 6.9 | 7.4 | V |
| VZ pin inflow current | $I_{VZ}$ | | | | 20 | mA |
| $V_{EXT}$, $V_{EXT}$-CHG pin Input bias current | $I_{B\ EXTCHG}$ $I_{B\ EXT}$ | $V_{EXT}$ = 1.5 V $V_{EXT-CHG}$ = 1.5 V (CHG-ON [H]) | | | 200 | nA |
| $V_{EXT}$, $V_{EXT}$-CHG pin Step-up circuit reference voltage | $Vref_{E-CHG}$ $Vref_{EXT}$ | Both determined at EXTDRV pin EXT-CHG side: CHG-ON [H] | 1.23 | 1.28 | 1.33 | V |
| EXTBASE pin saturation voltage | $V_{EXTBASE}$ | $I_O$ = 1 mA | | | 0.2 | V |
| [OSC Block] | | | | | | |
| OSCPWR pin output voltage | $V_{OSCPWR}$ | | $V_{CC}$–0.15 | | | V |
| Maximum oscillation frequency | $F_{OSC\ max}$ | | | | 100 | kHz |
| Input bias current | $I_{B\ OSC}$ | $V_{OSC}$ = 0 V | –2.0 | | | μA |
| [Pulse Charging Function] | | | | | | |
| Internal reference voltage | $V_{CHG\ REF}$ | | 0.32 | 0.35 | 0.38 | V |
| CHG-ON pin ON voltage | $V_{CHG-ON}$ | | 2.0 | | | V |
| CHG-ON Pin OFF voltage | $V_{CHG-OFF}$ | | | | 1.0 | V |
| CHG-MON pin input bias current | $I_{B\ CHG\ MON}$ | $V_{CHG\ MON}$ = 0.3 V | | | 200 | nA |
| CHGDRV pin output current | $I_{O\ CHG\ DRV}$ | $V_{CHG\ MON}$ = 0 V | 2.4 | 3.0 | 3.6 | mA |
| [TSD Block] | | | | | | |
| Operating temperature | $T_{TSD}$ | Design target value, Note 1 | | 180 | | °C |
| Temperature hysteresis width | $\Delta T_{TSD}$ | Design target value, Note 1 | | 20 | | °C |

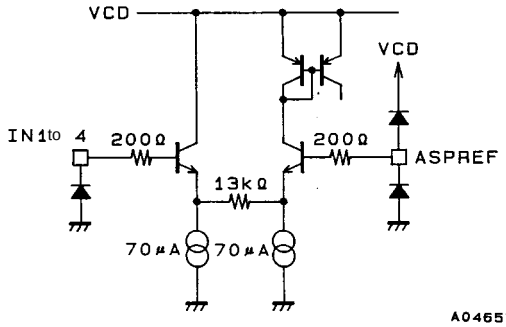
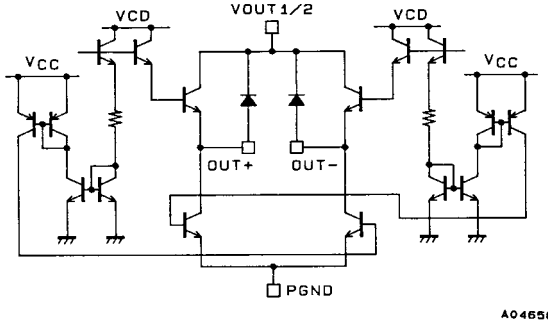
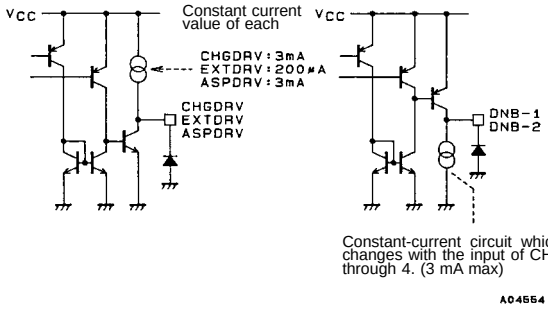
Note 1: For parameters which have an entry of ‘‘design target value’’ in the ‘‘Conditions’’ column, no measurements are made.




## Pin Assignment



## Pin Functions

| Pin No. | Symbol | Equivalent circuit | Function |
|---|---|---|---|
| 1, 2<br>32, 33 | IN1, IN2<br>IN3, IN4 |  | Actuator control signals for each driver:<br>IN1: Focus, IN2: Tracking,<br>IN3: Spindle, IN4: Sled.<br>These signals are input from the ASP (DSP). |
| 30 | $ASP_{REF}$ | | Control reference signal input pin for each driver. This signal is input from the ASP (DSP). |
| 43, 42<br>41, 40<br>38, 37<br>36, 35 | $OUT1^+$, $1^-$<br>$OUT2^+$, $2^-$<br>$OUT3^+$, $3^-$<br>$OUT4^+$, $4^-$ |  | Focus coil actuator drive output pins.<br>Tracking coil actuator drive output pins.<br>Spindle motor drive output pins.<br>Sled motor drive output pins.<br>(Each channel includes built-in spark killer diodes.) |
| 3<br>31 | $V_{OUT}1$<br>$V_{OUT}2$ | | Power supply pins for the H bridge driver. $V_{OUT}1$ is for the focus/tracking group and $V_{OUT}2$ is for the spindle/sled group. Maximum value + α (α : saturation voltage of upper/lower output Tr) of control output for each 2CH is set by external PWM step-down circuit. |
| 4 | $V_{CD}$ | | Power supply for the actuator driver controller, maximum value circuit for PWM, sled controller, and MUTE block. |
| 5 | CHGDRV |  | Base drive output pin for the external NPN-Tr for the battery pulse charging circuit. |
| 10 | EXTDRV | | Base drive output pin for the external step-down NPN-Tr used when external voltage input is applied. |
| 15 | DNB-1 | | Base drive output pin for the PNP-Tr for the step-down PWM that generates the power supply for the H bridge driver that drives the focus/tracking group actuators. |
| 16 | DNB-2 | | Base drive output pin for the PNP-Tr for the step-down PWM that generates the power supply for the H bridge driver that drives the spindle/sled group actuators. |
| 17 | ASPDRV | | Base drive output pin for the external NPN-Tr for the step-up circuit that sets the external voltage for the DSP. |

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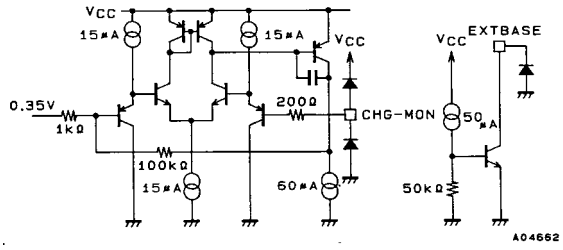
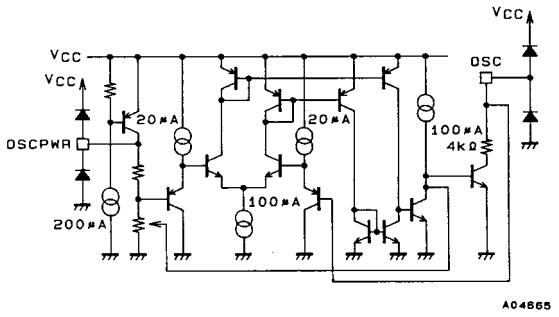
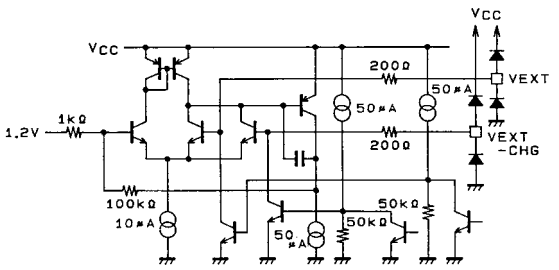
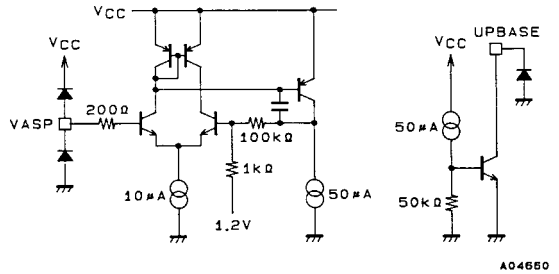
| Pin No. | Symbol | Equivalent circuit | Function |
|---|---|---|---|
| 6 | CHG MON |  | Constant-current feedback input pin for the charging circuit. The charging current is determined by comparing this input voltage and the internal reference voltage (0.35 V typ.). |
| 13 | EXTBASE | | Connection pin for the resistor that is used to set the voltage for the external step-down circuit. This prevents invalid current at no power supply. |
| 7 | GND | | GND pin for small-signal block. (GND except output power Tr) |
| 8 | OSC |  | Input pin for the free-running oscillation circuit that is used to operate the PWM step-down circuit and step-up circuit. The oscillating frequency is determined by external CR. |
| 9 | OSCPWR | | CR power supply pin that is used to prevent invalid current for the oscillation circuit in standby mode. |
| 11 | $V_{EXT}$ |  | Voltage feedback input pin for the external power supply step-down circuit. $V_{CC}$ for playback is set by comparing this pin voltage with the internal reference voltage (1.28 V typ.). |
| 12 | $V_{EXTCHG}$ | | Voltage feedback input pin for the external power supply step-down circuit. $V_{CC}$ for charging is set by comparing this pin voltage with the internal reference voltage (1.28 V typ.). |
| 18 | $V_{ASP}$ |  | Voltage feedback input pin for the step-up circuit. The step-up voltage is determined by comparing this pin voltage with the internal reference voltage (1.28 V typ.). |
| 19 | UPBASE | | Connection pin for the resistor that is used to set the voltage of the step-up circuit. This prevents invalid current in standby mode. |

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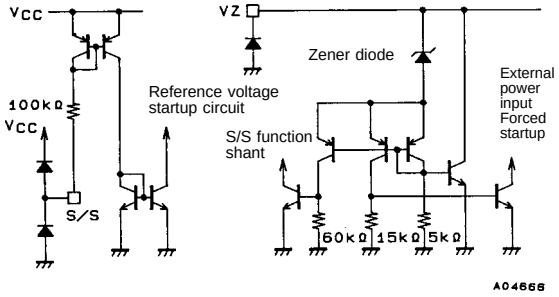
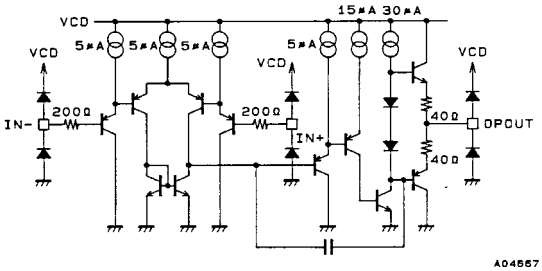
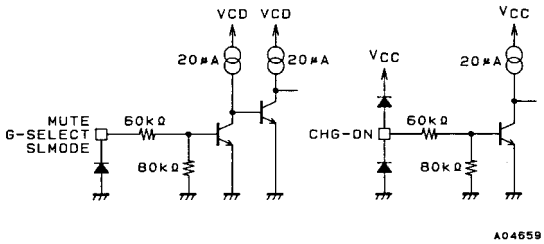
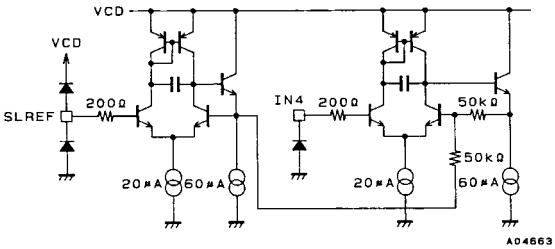
| Pin No. | Symbol | Equivalent circuit | Function |
|---|---|---|---|
| 20 | VZ |  | Input pin for start-up circuit when an external voltage input is applied. The external voltage input is applied through a resistor inserted in series. The voltage is basically determined by the Zener diode + $2V_{BE}$; this pin has a current draining capacity up to 20 mA. |
| 24 | S/S | | LB8109M start-up input. (Start on a low-level input.) |
| 21 | $OPIN^-$ |  | Inverting input pin for internal OP amplifier. |
| 22 | $OPIN^+$ | | Noninverting input pin for internal OP amplifier. |
| 23 | OPOUT | | Output pin for internal OP amplifier. The output circuit type is “push-pull.” |
| 14 | CHG-ON |  | Pin for selecting battery charging when external voltage input is applied. This pin determines the drop voltage for the external voltage input. When low, the drop voltage set by VEXT is selected; when high, the drop voltage set by VEXT-CHG is selected. |
| 25 | MUTE | | Input pin for simultaneously muting the drivers for the four channels. (High: mute) |
| 26 | G-SELECT | | Pin for switching the spindle driver transfer gain between 8.3 dB and 14.8 dB (typ. value each). (Low: high gain) |
| 27 | SLMODE | | Pin for switching the sled driver between V-type control and step control. (High: V-type control; low: step control) |
| 28 | $V_{CC}$ | | Power supply voltage pin. |
| 29<br>33 | SLREF<br>IN4 |  | Threshold input pin for driving the sled motor stepwise. Both the positive and negative step levels (with positive-negative symmetry) are determined by the voltage differential between the pin voltage and the ASPREF pin voltage. |
| 39 | PGND | | Output Tr. GND for the four-channel H bridge drivers. This pin is not internally connected to the small-signal system GND. |

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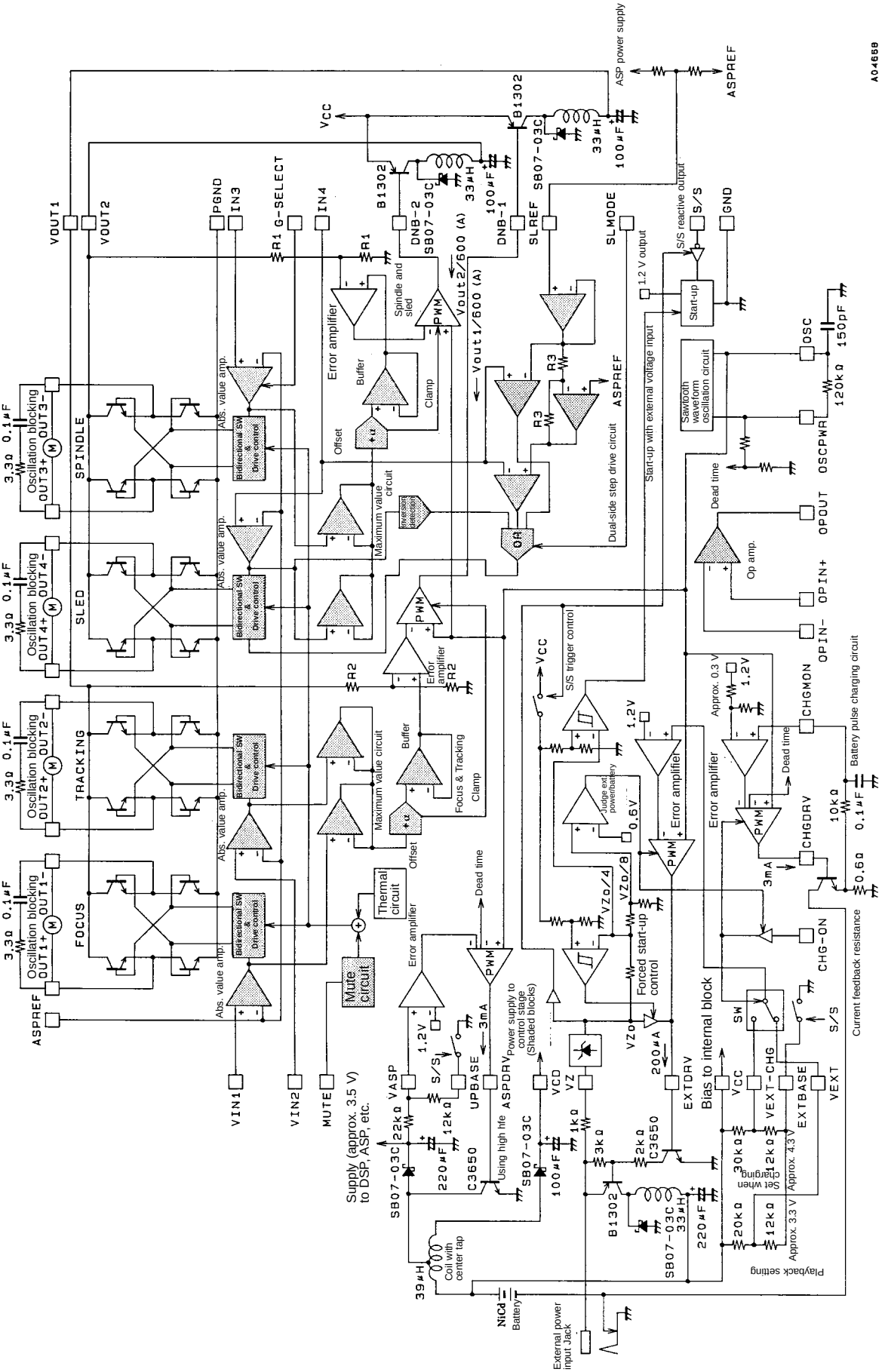
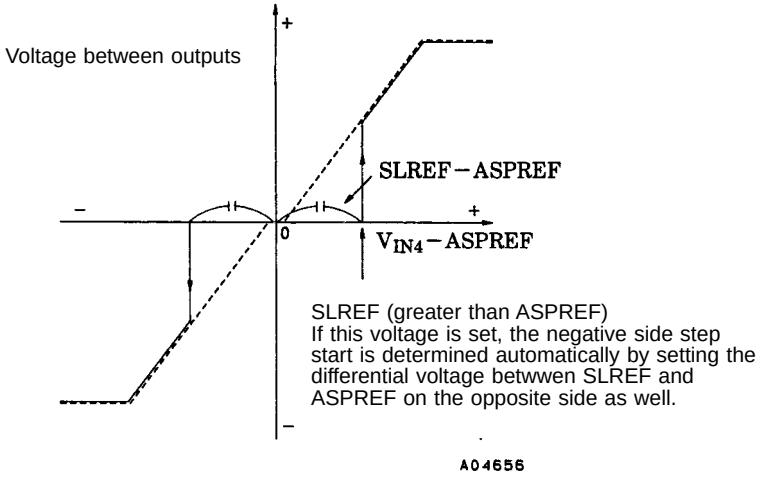
## Block Diagram and Sample Application Circuit




Note: It should be noted that Type Nos., contants specified herein are for example only, with no guarantee for characteristics implied.

### Supplementary Explanation

1. $V_{CD}$ supply
   The $V_{CD}$ line is the power supply for the driver control blocks of channels 1 to 4. The VCD line can be supplied from the DSP step-up circuit by using a coil with center tap (as shown in the Block Diagram).
   However, because the allowable operating range for $V_{CD}$ is 3.6 V to 9.0 V, it is recommended that in order to reduce power dissipation, the voltage should be set to the low end of this range. (Even if this power supply does not affect the control performance such as the transfer gain.)
2. Sled step drive
   Stepping control in this IC for the sled actuator is as described below. Normal V-type control is used if the SLMODE pin is set high, but by setting this pin low it is possible to use step drive mode, which has a marked effect in reducing power dissipation. (This only affects channel 4.)
   The step drive starting level is input from the SLREF pin (only a voltage higher than ASPREF will be accepted), and the positive side step start is determined by comparing the input voltage with IN4. For the negative side, the step start is determined automatically by setting the differential voltage between the SLREF and the ASPREF on the opposite side, and then comparing that voltage to IN4. In other words, the control characteristics become as defined by the solid line in the diagram below. (The rise on the positive and negative steps has no hysteresis.)

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