Ordering number : EN6197C

LB1927

Monolithic Digital IC

For Office Automation Equipment

3-phase Brushless Motor Driver

ON Semiconductor®

http://onsemi.com

Overview

The LB1927 is a 3-phase brushless motor driver well suited for drum and paper feed motors in laser printers, plain-paper copiers and other office automation equipment. Direct PWM drive allows control with low power losses. Peripheral circuitry including speed control circuit and FG amplifier is integrated, thus allows drive circuit to be constructed with a single chip.

Features

- 3-phase bipolar drive (30V, 2.5A)
- Direct PWM drive technique
- Built-in diode for absorbing output lower-side kickback
- Speed discriminator and PLL speed control
- Speed lock detection output
- Built-in forward/reverse switching circuit
- Built-in protection circuitry includes current limiter, overheat protection, motor restraint protection, etc.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		30	V
Maximum output current	I_O max	T ≤ 500ms	2.5	A
Allowable power dissipation 1	Pd max 1	Independent IC	3	W
Allowable power dissipation 2	Pd max 2	With an arbitrary large heat sink	20	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Semiconductor Components Industries, LLC, 2013

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage range 1	V_{CC}		9.5 to 28	V
Regulator voltage output current	I_{REG}		-30 to 0	mA
LD output current	I_{LD}		0 to 15	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = VM = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply current 1	$I_{CC}1$			23	30	mA
Power supply current 2	$I_{CC}2$	In STOP mode		3.5	5.0	mA
Output						
Output saturation voltage 1	$V_O$sat1	I_O = 1.0A, V_O (SINK) +V_O (SOURCE)		2.0	2.5	V
Output saturation voltage 2	$V_O$sat2	I_O = 2.0A, V_O (SINK) +V_O (SOURCE)		2.6	3.2	V
Output leak current	$I_O$leak				100	µA
Lower-side diode forward voltage 1	V_D1	ID = -1.0A		1.2	1.5	V
Lower-side diode forward voltage 2	V_D2	ID = -2.0A		1.5	2.0	V
5V regulator voltage output						
Output voltage	V_{REG}	I_O = -5mA	4.65	5.00	5.35	V
Voltage fluctuation	$\Delta V_{REG}1$	V_{CC} = 9.5 to 28V		30	100	mV
Load fluctuation	$\Delta V_{REG}2$	I_O = -5 to -20mA		20	100	mV
Hall amplifier						
Input bias current	I_{HB}		-2	-0.5		µA
Common mode input voltage range	VICM		1.5		V_{REG}-1.5	V
Hall input sensitivity			80			mVp-p
Hysteresis width	ΔV_{IN}		15	24	42	mV
Input voltage L→H	VSLH			12		mV
Input voltage H→L	VSHL			-12		mV
PWM oscillator						
Output High level voltage	V_{OH} (PWM)		2.5	2.8	3.1	V
Output Low level voltage	V_{OL} (PWM)		1.2	1.5	1.8	V
Oscillator frequency	F (PWM)	C = 3900pF		18		kHz
Amplitude	V (PWM)		1.05	1.30	1.55	Vp-p
CSD circuit						
Operating voltage	V_{OH} (CSD)		3.6	3.9	4.2	V
External capacitance charge current	ICHG		-17	-12	-9	µA
Operating time	T (CSD)	C = 10µF Design target value		3.3		s
Current limiter operation						
Limiter	VRF	V_{CC}-VM	0.45	0.5	0.55	V
Thermal shutdown operation						
Thermal shutdown operating temperature	TSD	Design target value (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target value (junction temperature)		50		°C
FG amplifier						
Input offset voltage	V_{IO} (FG)		-10		+10	mV
Input bias current	I_B (FG)		-1		+1	µA
Output High level voltage	V_{OH} (FG)	IFGO = -0.2mA	VREG-1.2	VREG-0.8		V
Output Low level voltage	V_{OL} (FG)	IFGO = 0.2mA		0.8	1.2	V
FG input sensitivity		GAIN 100 times	3			mV
Next-stage Schmitt comparator width		Design target value	100	180	250	mV
Operation frequency range					2	kHz
Open-loop gain		f (FG) = 2kHz	45	51		dB

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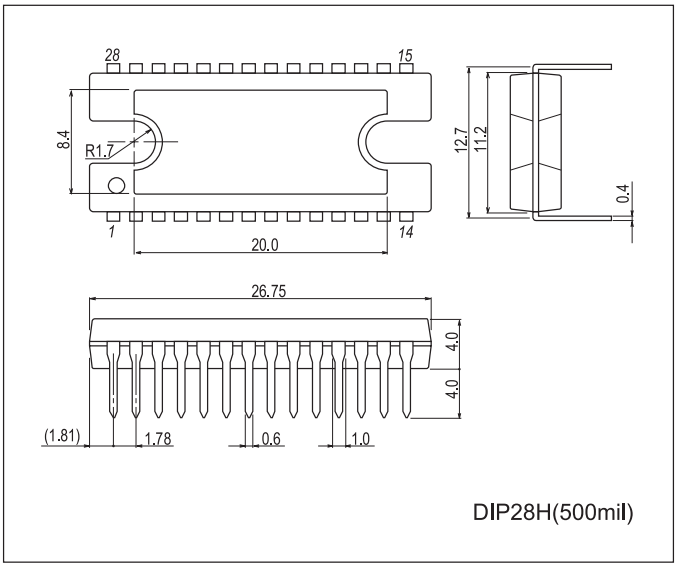
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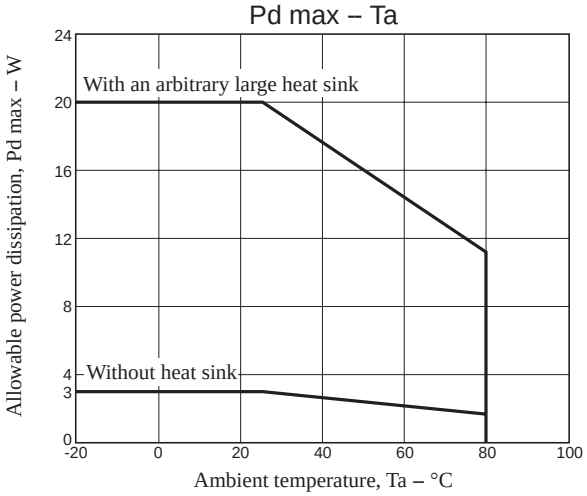
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Speed discriminator						
Output High level voltage	V_{OH} (D)	IDO = -0.1mA	VREG-1.0	VREG-0.7		V
Output Low level voltage	V_{OL} (D)	IDO = 0.1mA		0.8	1.1	V
Count number				512		
PLL output						
Output High level voltage	V_{OH} (P)	IPO = -0.1mA	VREG-1.8	VREG-1.5	VREG-1.2	V
Output Low level voltage	V_{OL} (P)	IPO = 0.1mA	1.2	1.5	1.8	V
Lock detection						
Output Low level voltage	V_{OL} (LD)	ILD = 10mA		0.15	0.5	V
Lock range				6.25		%
Integrator						
Input bias current	IB (INT)		-0.4		+0.4	µA
Output High level voltage	V_{OH} (INT)	I_{INTO} = -0.2mA	VREG-1.2	VREG-0.8		V
Output Low level voltage	V_{OL} (INT)	I_{INTO} = 0.2mA		0.8	1.2	V
Open-loop gain		f (INT) = 1kHZ	45	51		dB
Gain bandwidth product		Design target value		450		kHz
Reference voltage		Design target value	-5%	VREG/2	5%	V
Crystal oscillator						
Operating frequency range	f_{OSC}		3		10	MHz
Low level pin voltage	$V_{OSC}L$	I_{OSC} = -0.5mA		1.65		V
High level pin current	$I_{OSC}H$	$V_{OSC} = V_{OSC}L+0.3V$		0.4		mA
Start/stop pin						
High level input voltage range	V_{IH} (S/S)		3.5		VREG	V
Low level input voltage range	V_{IL} (S/S)		0		1.5	V
Input open voltage	V_{IO} (S/S)		VREG-0.5		VREG	V
Hysteresis width	ΔV_{IN}		0.35	0.50	0.65	V
High level input current	I_{IH} (S/S)	V (S/S) = VREG	-10	0	10	µA
Low level input current	I_{IL} (S/S)	V (S/S) = 0V	-280	-210		µA
Forward/reverse pin						
High level input voltage range	V_{IH} (F/R)		3.5		VREG	V
Low level input voltage range	V_{IL} (F/R)		0		1.5	V
Input open voltage	V_{IO} (F/R)		VREG-0.5		VREG	V
Hysteresis width	ΔV_{IN}		0.35	0.50	0.65	V
High level input current	I_{IH} (F/R)	V (F/R) = VREG	-10	0	+10	µA
Low level input current	I_{IL} (F/R)	V (F/R) = 0V	-280	-210		µA

Package Dimensions

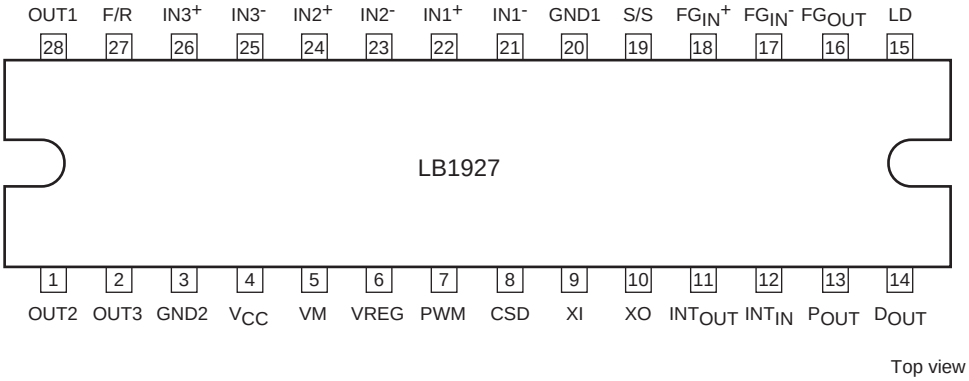
unit : mm (typ)

3147C





Pin Assignment



Top view

Relationship between crystal oscillator frequency f_{OSC} and FG frequency f_{FG} is as follows.

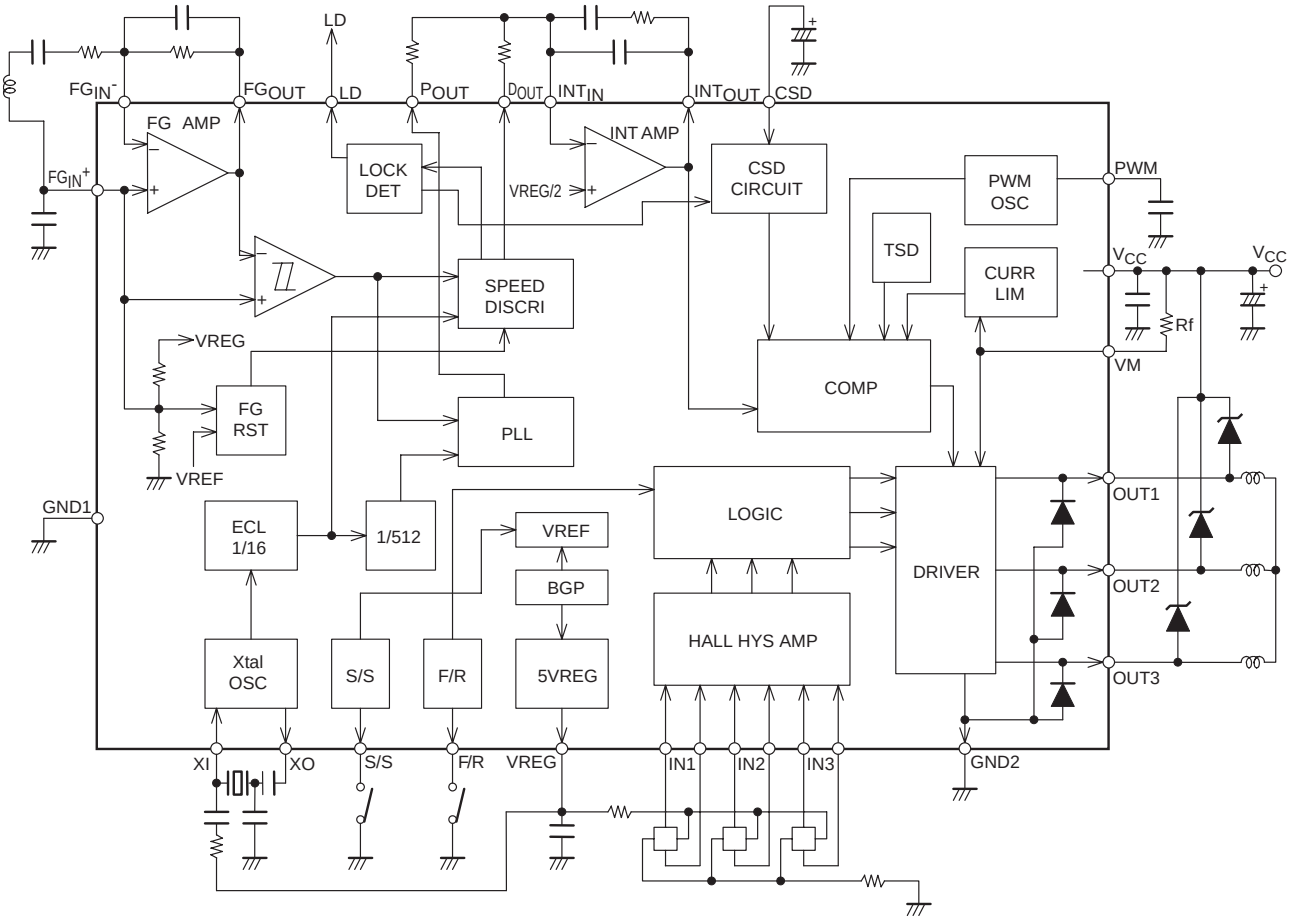
f_{FG} (servo) = f_{OSC}/ (ECL divide-by-16×count number)

= f_{OSC}/8192

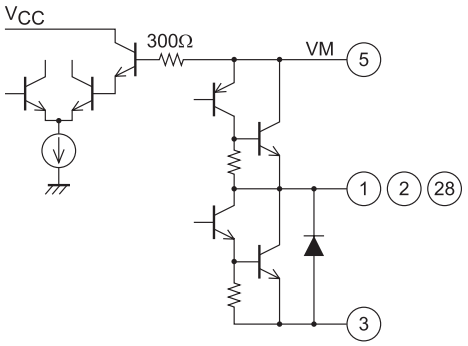
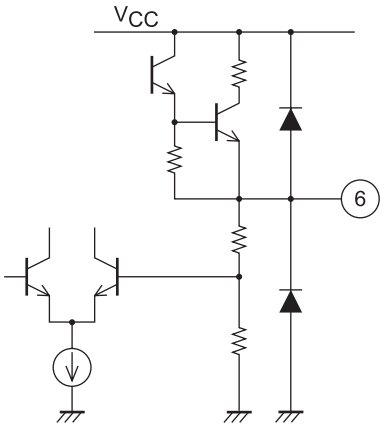
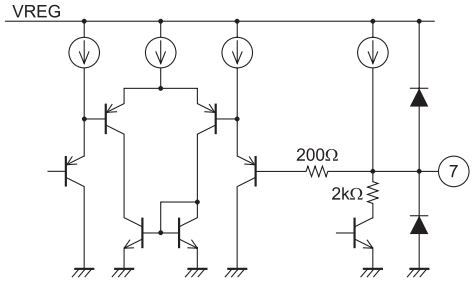
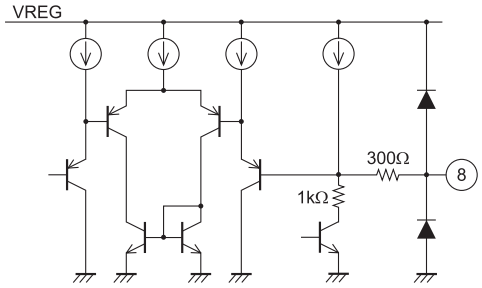
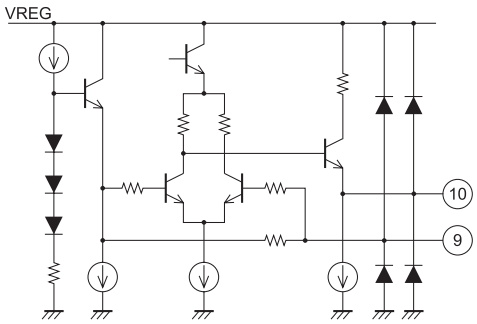
Truth Table

	Source / Sink	F/R = "L"			F/R = "H"		
		IN1	IN2	IN3	IN1	IN2	IN3
1	OUT2→OUT1	H	L	H	L	H	L
2	OUT3→OUT1	H	L	L	L	H	H
3	OUT3→OUT2	H	H	L	L	L	H
4	OUT1→OUT2	L	H	L	H	L	H
5	OUT1→OUT3	L	H	H	H	L	L
6	OUT2→OUT3	L	L	H	H	H	L

Block Diagram and Sample Application Circuit

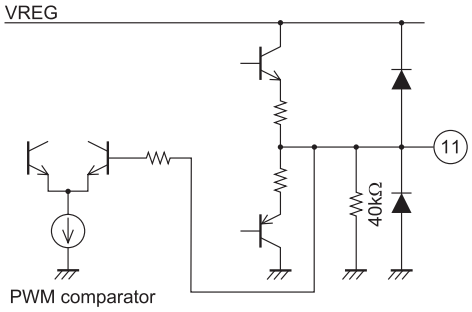
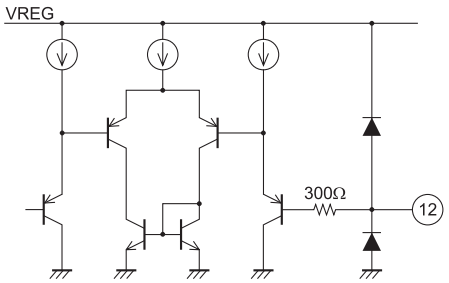
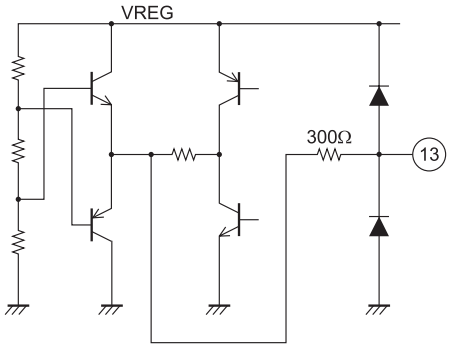
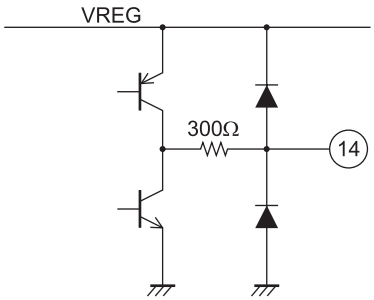
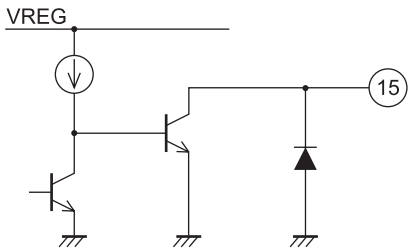


Pin Description

Pin No.	Pin name	Pin function	Equivalent circuit
28 1 2	OUT1 OUT2 OUT3	Motor drive output pins. Connect a Schottky diode between these outputs and V_{CC}.	
3	GND2	Output ground pin.	
5	VM	Output block power supply and output current detection pin. Connect a resistor (Rf) between this pin and V_{CC} to detect the output current as a voltage. The output current is limited according to the equation $I_{OUT} = V_{RF}/R_f$.	
4	V_{CC}	Power supply pin (except for output block).	
6	VREG	Regulated power supply output pin (5V output). Connect a capacitor (approx. 0.1μF) between this pin and ground to stabilize the output.	
7	PWM	PWM frequency setting pin. Connect a capacitor between this pin and ground. C = 3900pF results in a frequency of about 18kHz.	
8	CSD	Lock protection circuit operation time setting pin. Connecting a capacitor of about 10μF between this pin and ground results in a protection circuit operation time of about 3.3 seconds.	
9 10	XI XO	Crystal oscillator pins. Connect to quartz oscillator to generate the reference clock. When an external clock (of several MHz) is used, the clock signal should be input via a resistor of about 5.1kΩ connected in series with the XI pin. In this case, the XO pin must be left open.	

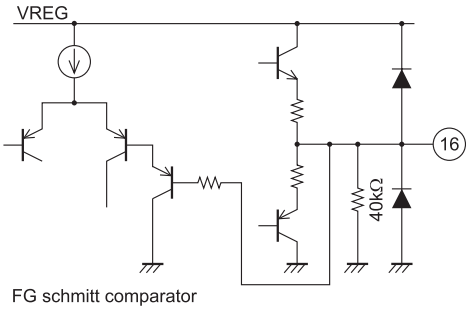
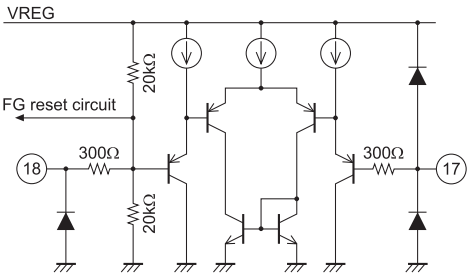
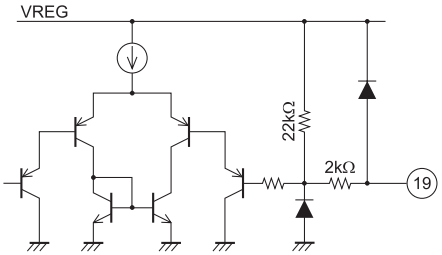
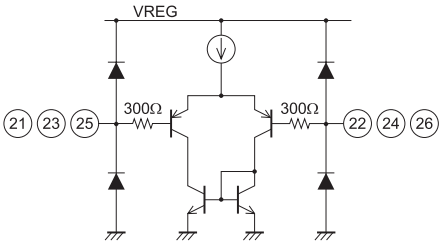
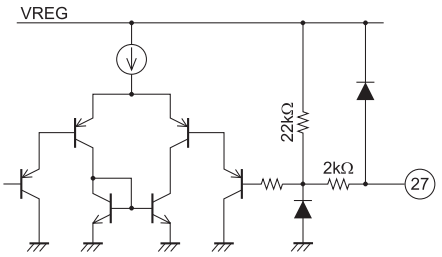
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Pin No.	Pin name	Pin function	Equivalent circuit
11	INT_{OUT}	Integrator output pin (speed control pin).	
12	INT_{IN}	Integrator input pin.	
13	P_{OUT}	PLL output pin.	
14	D_{OUT}	Speed discriminator output pin. Acceleration : High, Deceleration : Low	
15	LD	Speed lock detection pin. When motor rotation is within lock range (±6.25%) : Low Withstand voltage : 30V max.	

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Pin No.	Pin name	Pin function	Equivalent circuit
16	FG_{OUT}	FG amplifier output pin.	
17 18	FG_{IN}^- FG_{IN}^+	FG amplifier input pin. By connecting a capacitor (approx. 0.1μF) between FG_{IN}^+ and ground, the logic circuitry is reset.	
19	S/S	Start/stop control pin. Start (Low) : 0V to 1.5V Stop (High) : 3.5V to VREG High when open. Hysteresis width : approx. 0.5V.	
20	GND1	Ground pin (except for output block).	
22 21 24 23 26 25	$IN1^+$ $IN1^-$ $IN2^+$ $IN2^-$ $IN3^+$ $IN3^-$	Hall input pins. High when $IN^+ > IN^-$, Low when $IN^+ < IN^-$. Hall signal should have an amplitude of at least 100mVp-p (differential operation). When Hall signal noise is a problem, connect a capacitor between IN^+ and IN^-.	
27	F/R	Forward/reverse control pin. Forward (Low) : 0V to 1.5V Reverse (High) : 3.5V to VREG High when open. Hysteresis width : approx. 0.5V.	

Description of the LB1927

1. Speed control circuit

The IC performs speed control through combined use of a speed discrimination circuit and PLL circuit. The speed control circuit counts FG cycles and outputs a deviation signal every 2FG cycles. The PLL circuit outputs a phase deviation signal every FG cycle.

The FG servo frequency is determined by the following equation. The motor rotation speed is set by the number of FG pulses and the crystal oscillator frequency.

$$f_{FG}(servo) = f_{OSC}/8192$$

f_{OSC} : Crystal oscillator frequency

2. Output drive circuit

In order to reduce power loss at the output, the LB1927 uses the PWM drive technique. While ON, the output transistors are always saturated, and motor drive power is adjusted by varying the output ON duty ratio. Because output PWM switching is performed by the lower-side output transistor, a Schottky diode must be connected between OUT and V_{CC}. (If the reverse recovery time of the diode is too long, a feedthrough current will flow at the instant when the lower-side transistor goes ON.) An internal diode is provided between OUT and GND. If large output current causes a problem (waveform distortion during lower-side kickback, etc.), an external rectifying diode or Schottky diode should be connected.

The output diode is integrated only on the lower side.

3. Current limiting circuit

The current limiting circuit limits the peak current to the value I = VRF/Rf (VRF = 0.5V typ., Rf : current detector resistance). Current limiting is achieved by reducing the ON duty ratio of the output, which reduces the current.

4. Power save circuit

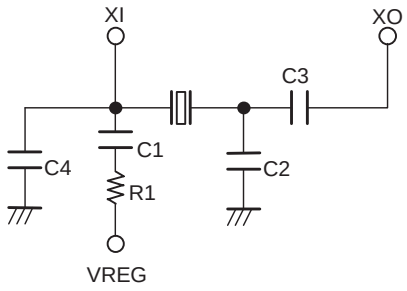
In order to reduce current drain in the STOP condition, the IC goes into power save mode. In this condition, bias current to most circuits is cut off, but the 5V regulator output remains active.

5. Reference clock

The reference clock for speed control can be input using one of the following two methods.

(1) Using a crystal oscillator

When a crystal is used for oscillation, connect the crystal, capacitors, and a resistor as shown in the figure below.



C1, R1 : For stable oscillation
C3 : For oscillator coupling
C2 : For stabilization and to prevent oscillation at upper harmonic frequencies
C4 : Prevents oscillation at upper harmonic frequencies

(Reference values)

Oscillator frequency (MHz)	C1 (μF)	C2 (pF)	C3 (pF)	C4 (pF)	R1 (Ω)
3 to 5	0.1	15	47	10	330k
5 to 8	0.1	10	47	None	330k
8 to 10	0.1	10	22	None	330k

The circuit configuration and values are for reference only. The crystal oscillator's characteristics as well as the possibility of floating capacitance and noise due to layout factors must be taken into consideration when designing an actual application.

[Precautions for wiring layout design]
Since the crystal oscillator circuit operates at high frequencies, it is susceptible to the influence of floating capacitance from the circuit board. Wiring should be kept as short as possible and traces should be kept narrow. When designing the external circuitry, pay special attention to the wiring layout between the oscillator and C3 (C2), to minimize the influence of floating capacitance. The capacitor C4 is quite effective at reducing the negative resistance (gain) at high frequencies. However, care is required to avoid excessive reduction in the negative resistance at the fundamental frequency.

(2) External clock input (equivalent to crystal oscillator, several MHz)
When using an external signal source instead of a crystal oscillator, the clock signal should be input from the XI pin through a resistor of about 5.1kΩ connected to the pin in series. The XO pin should be left open. Signal input level
Low : 0 to 0.8V
High : 2.5 to 5.0V

6. Speed lock range
The speed clock range is ±6.25% of the rated speed. When the motor rotation is within the lock range, the LD pin becomes Low (open collector output). When the motor rotation goes out of the lock range, the ON duty ratio of the motor drive output is varied according to the amount of deviation to bring the rotation back into the lock range.

7. PWM frequency
The PWM frequency is determined by the capacitance connected to the PWM pin.
$f_{PWM} \approx 1/ (14400 \times C)$
PWM frequency in the range 15 to 25kHz is desirable. The ground side of the connected capacitor must be connected to the GND1 pin with a lead that is as short as possible.

8. Hall input signal
The Hall input requires a signal with an amplitude of at least the hysteresis width (42mV max.). Taking possible noise influences into consideration, an amplitude of at least 100mV is desirable. If noise during output phase switching disrupts the output waveform, insert capacitors across the Hall signal inputs (between the + and - inputs), and position those capacitors as close as possible to the pins.

9. Forward/reverse switching
Forward/reverse switching of motor rotation is carried out with the F/R pin. If this is performed while the motor is running, the following points must be observed :
- Feedthrough current during switching is handled by proper circuit design. However, the V_{CC} voltage rise during switching (caused by momentary return of motor current to power supply) must not exceed the rated voltage (30V). If problems occur, the capacitance between V_{CC} and GND must be increased.
- If the motor current after switching exceeds the current limiter value, the lower-side transistors go OFF but the upper-side transistors go into the short brake state, which causes a current flow. The magnitude of the current is determined by the motor counterelectromotive voltage and the coil resistance. This current may not exceed the rated current (2.5A). (Forward/reverse switching at high speed therefore is not safe.)

10. Motor restraint protection circuit
To protect the IC and the motor itself when rotation is inhibited, a restraint protection circuit is provided. If the LD output is High (unlocked) for a certain interval in the start condition, the lower-side transistors are turned off. The length of the interval is determined by the capacitance at the CSD pin. A capacitance of 10μF results in a set interval of about 3.3 seconds. (Tolerance approx. ±30%)
Set interval (s) ≈ 0.33×C (μF)
If the capacitor arrangement is subject to leak current, possible adverse effects such as setting time tolerances must be taken into consideration.
When the restraint protection circuit has been activated, the condition can only be canceled by setting the system to the stop condition or by turning the power off and on again (in the stop condition). When wishing not to use the restraint protection circuit, connect the CSD pin to ground.
If the stop time when releasing the restraint protection is short, the capacitor charge will not be fully dissipated. This in turn will cause a shorter restraint protection activation time after the motor has been restarted. The stop time should therefore be designed to be sufficiently long, using the equation shown below (also when restarting in the motor start transient state).
Stop time (ms) ≥ 15×C (μF)

11. Power supply stabilization

Because this IC provides a high output current and uses a switching drive technique, power supply line fluctuations can occur easily. Therefore, a capacitor of sufficient capacitance (several ten μF or higher) must be connected between the V_{CC} pin and ground to assure stable operation. The ground connection of this capacitor must be connected to the GND2 pin, which is the power block ground, at a point as close as possible to the IC. If, due to problems associated with the heat sink, the (electrolytic) capacitor cannot be connected near the this pin, a ceramic capacitor of about 0.1μF must be connected near the pin.

Since the likelihood of power line fluctuation increases if diodes are inserted in the power supply lines to prevent destruction of the IC if power is connected with reverse polarity, a larger capacitance will be required.

12. VREG stabilization

A capacitor (about 0.1μF) must be connected to the VREG pin (the 5V regulator output), which functions as the control circuit power supply, for stabilization. The ground side of this capacitor must be connected to the GND1 pin with a lead that is as short as possible.

13. Integrating amplifier related component values

The external components used in the integrating amplifier must be located as close as possible to the IC to minimize the circuit's susceptibility to noise. These components must be located as far as possible from the motor.

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