Ordering number : EN6002

Monolithic Digital IC

LB1875

Polygon Mirror Motor Predriver IC

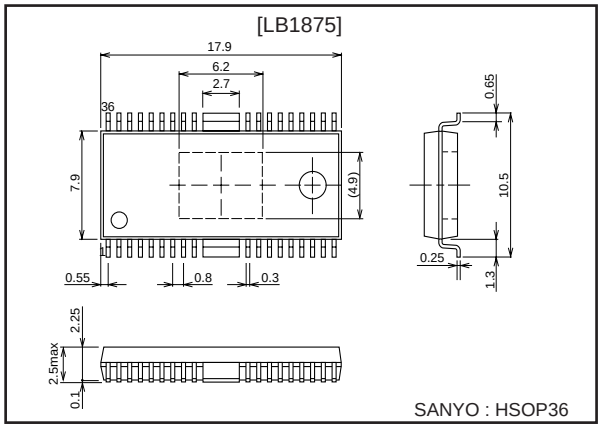
Overview

The LB1875 is a predriver IC for polygon mirror motors. By using a driver array or discrete transistors (FETs) at the output, motor drive with high rotation precision is possible. PAM drive or direct PWM drive can be selected for the output to realize high-efficiency control with minimum power loss.

Package Dimensions

unit: mm

3235-HSOP36



Features

- Three-phase bipolar drive
- Direct PWM drive (bottom side) or PAM drive selectable
- PLL speed control circuit
- PWM oscillator
- Quartz oscillator
- Frequency divider
- FG with Schmitt comparator
- FG input single edge, dual edge selector circuit
- Integrating amplifier
- Phase lock detector output
- Current limiter
- Motor lock protection
- Thermal protection
- Forward/reverse circuit
- 5V regulator output

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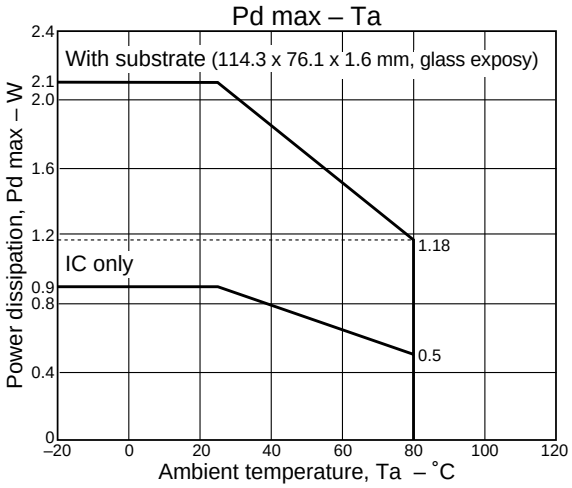
Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14.5	V
Output current	I_O max		30	mA
Allowable power dissipation	Pd max	IC only	0.9	W
		with substrate (114.3 x 76.1 x 1.6 mm^3, glass exposy)	2.1	W
Operating temperature	Topr		– 20 to +80	℃
Storage temperature	Tstg		– 55 to +150	℃

Operation Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}1		8 to 13.5	V
	V_{CC}2	When shorted between V_{CC} and V_{REG}	4.5 to 5.5	V
Output current	I_O		20	mA
5V regulated output current	I_{REG}		0 to –20	mA
Voltage applied at LD pin	V_{LD}		0 to 13.5	V
LD pin output current	I_{LD}		0 to 10	mA
Voltage applied at PWM pin	V_{PWM}		0 to 13.5	V
PWM pin output current	I_{PWM}		0 to 20	mA



Electrical Characteristics at Ta = 25°C, V_{CC} = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply current	I_{CC}			30	40	mA
[5V regulated output]						
Output fluctuation	V_{REG}		4.65	5.0	5.35	V
Voltage fluctuation	$\Delta V_{REG}1$	V_{CC}=8 to 13.5V		40	100	mV
Load fluctuation	$\Delta V_{REG}2$	I_O=0 to –15 mA		20	100	mV
Temperature coefficcient	$\Delta V_{REG}3$	Design target value		0		mV/°C
[Output Section]						
Output saturation voltage	V_O(sat)1-1	UH, VH, WH "L" level, I_O=50 µA		0.1	0.3	V
	Vo(sat)1-2	UH, VH, WH "L" level, I_O=10 mA		0.9	1.1	V
	V_O(sat)2	UH, VH, WH "L" level, I_O=20 mA		V_{CC}–0.9	V_{CC}–1.1	V
	V_O(sat)3	UL, VL, WL, I_O=20 mA		0.2	0.4	V
Output leak current	$I_O$leak	UL, VL, WL			10	µA
[Hall amplifier]						
Input bias current	I_{HB}(HA)		–4	–1		µA
Same-phase input voltage range	V_{ICM}		0		V_{CC}–2.0	V
Hall input sensitivity			30			mV_{P-P}
Hysteresis width	ΔV_{IN}(HA)		8	14	24	mV
Input voltage L->H	V_{SLH}			7		mV
Input voltage H->L	V_{SHL}			–7		mV
[FG/Schmitt comparator section]						
Input bias current	I_B(FGS)		–4	–1		µA
Same-phase input voltage range	V_{ICM}(FGS)		0		V_{CC}–2.0	V
Input sensitivity	V_{IN}(FGS)		30			mV_{P-P}
Hysteresis width	ΔV_{IN}(FGS)	Design target value	8	14	24	mV
Input voltage L->H	V_{SLH}(FGS)	Design target value		7		mV
Input voltage H->L	V_{SHL}(FGS)	Design target value		–7		mV
[PWM oscillator]						
Output High level voltage	V_{OH}(OSC)		2.7	3.0	3.3	V
Output Low level voltage	V_{OL}(OSC)		1.5	1.8	2.1	V
Oscillator frequency	f(OSC)	C=2200 pF		30		kHz
Amplitude	V(OSC)		1.0	1.2	1.4	V_{P-P}
[PWM output]						
Output saturation voltage	V_{OL}(PWM)	I_{PWM}=15 mA		0.9	2.0	V
Output leak current	I_L(PWM)	V_O=V_{CC}			10	µA
[CSD oscillator]						
Output High level voltage	V_{OH}(CSD)		2.5	2.8	3.1	V
Output Low level voltage	V_{OL}(CSD)		0.55	0.85	1.15	V
External C charge current	$I_{CHG}1$		–13	–10	–7	µA
External C discharge current	$I_{CHG}2$		7	10	13	µA
Oscillator frequency	f_{CSD}	C=0.068 µF		35		Hz
Amplitude	V_{CSD}		1.75	1.95	2.15	V_{P-P}
[Phase comparator output]						
Output High level voltage	V_{PDH}	I_{OH}=–100 µA	V_{REG}–0.2	V_{REG}–0.1		V
Output Low level voltage	V_{PDL}	I_{OH}=100 µA		0.1	0.2	V
Output source current	I_{PD}^+	V_{PD}=V_{REG}/2			–0.6	mA
Output sink current	I_{PD}^-	V_{PD}=V_{REG}/2	1.5			mA
[Phase lock detector output]						
Output saturation voltage	V_{OL}(LD)	I_{LD}=10 mA		0.1	0.4	V
Output leak current	I_L(LD)	V_O=V_{CC}			10	µA

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[ERR amplifier]						
Input offset voltage	V_{IO}(ER)	Design target value	–10		+10	mV
Input bias current	I_B(ER)		–1		+1	µA
Ouput High level voltage	V_{OH}(ER)	I_{OH} = –500 µA	V_{REG}–1.2	V_{REG}–0.9		V
Ouput Low level voltage	V_{OL}(ER)	I_{OL}=500 µA		0.9	1.2	V
DC bias level	V_B(ER)		–5%	V_{REG}/2	+ 5%	V
[Current limiter]						
Limiter voltage	V_{RF}		0.45	0.5	0.55	V
[Low-voltage protection circuit]						
Operation voltage	V_{SDL}		3.55	3.75	3.95	V
Release voltage	V_{SDH}		3.8	4.0	4.2	V
Hysteresis width	ΔVSD		0.15	0.25	0.35	℃
[Thermal shutdown operation]						
Termal shutdown temperature	TSD	Design target value (junction temperature)	150	180		℃
Hysteresis width	ΔTSD	Design target value (junction temperature)		30		℃
[SOFT pin]						
Stop voltage	V_{SFT}	In stop condition	3.0	3.3	3.6	V
External C discharge current	I_{DCHG}		4	6	8	µA
[Quartz oscillator]						
Quartz oscillator frequency	f_{OSC}		2		10	MHz
Low level pin voltage	V_{OSCL}	I_{OSC}=–0.5 mA		1.45		V
High level pin voltage	V_{OSCH}	V_{OSC}=V_{OSCL}+0.6V		0.5		mA
[CLK_{OUT} pin]						
Output saturation voltage	V_{OL}(CKOUT)	I_{CKOUT}=2 mA		0.1	0.4	V
Output leak current	I_L(CKOUT)	V_O=V_{CC}			10	µA
[CLK_{IN} pin]						
External input frequency	$f_{I(CKIN)}$		0.1		10	kHz
High level input voltage	$V_{IH(CKIN)}$		3.5		V_{REG}	V
Low level input voltage	$V_{IL(CKIN)}$		0		1.5	V
Input open voltage	$V_{IO(CKIN)}$		V_{REG}–0.5		V_{REG}	V
Hysteresis width	$V_{IS(CKIN)}$		0.3	0.4	0.5	V
High level input current	$I_{IH(CKIN)}$	V_{CKIN}=V_{REG}	–10	0	+10	µA
Low level input current	$I_{IL(CKIN)}$	V_{CKIN}=0V	–200	–140		µA
[S/S pin]						
High level input voltage	V_{IH}(SS)		3.5		V_{REG}	V
Low level input voltage	V_{IL}(SS)		0		1.5	V
Input open voltage	V_{IO}(SS)		V_{REG}–0.5		V_{REG}	V
Hysteresis width	V_{IS}(SS)		0.3	0.4	0.5	V
High level input current	I_{IH}(SS)	VS/S=V_{REG}	–10	0	+10	µA
Low level input current	I_{IL}(SS)	VS/S=0V	–200	–140		µA
[F/R pin]						
High level input voltage	V_{IH}(FR)		3.5		V_{REG}	V
Low level input voltage	V_{IL}(FR)		0		1.5	V
Input open voltage	V_{IO}(FR)		V_{REG}–0.5		V_{REG}	V
High level input current	I_{IH}(FR)	VF/R=V_{REG}	–10	0	+10	µA
Low level input current	I_{IL}(FR)	VF/R=0V	–200	–140		µA
[FG_{SEL} pin]						
High level input voltage	V_{IH}(FSEL)		3.5		V_{REG}	V
Low level input voltage	V_{IL}(FSEL)		0		1.5	V
Input open voltage	V_{IO}(FSEL)		V_{REG}–0.5		V_{REG}	V
High level input current	I_{IH}(FSEL)	V_{FSEL}=V_{REG}	–10	0	+10	µA
Low level input current	I_{IL}(FSEL)	V_{FSEL}=0V	–200	–140		µA

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[CLK_{SEL} pin]						
High level input voltage	V_{IH}(CSEL)		4.0		V_{REG}	V
Middle level input voltage	V_{IM}(CSEL)		2.0		3.0	V
Low level input voltage	V_{IL}(CSEL)		0		1.0	V
Input open voltage	V_{IO}(CSEL)		V_{REG}–0.5		V_{REG}	V
High level input current	I_{IH}(CSEL)	V_{CSEL}=V_{REG}	–10	0	+10	µA
Low level input current	I_{IL}(CSEL)	V_{CSEL}=0V	–200	–140		µA
[LIM pin]						
High level input voltage	V_{IH}(LIM)		3.5		V_{REG}	V
Low level input voltage	V_{IL}(LIM)		0		1.5	V
Input open voltage	V_{IO}(LIM)		V_{REG}–0.5		V_{REG}	V
High level input current	I_{IH}(LIM)	V_{LIM}=V_{REG}	–10	0	+10	µA
Low level input current	I_{IL}(LIM)	V_{LIM}=0V	–200	–140		µA

3-phase logic truth table (IN = “H” indicates the $IN^+ > IN^-$ condition)

	F/R= "L"			F/R= "H"			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	SOURCE	SYNC
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

S/S pin

Input state	Condition
High or open	Stop
L	Start

FGSEL pin

Input state	Edge detection
High or open	FG dual edge
L	FG single edge

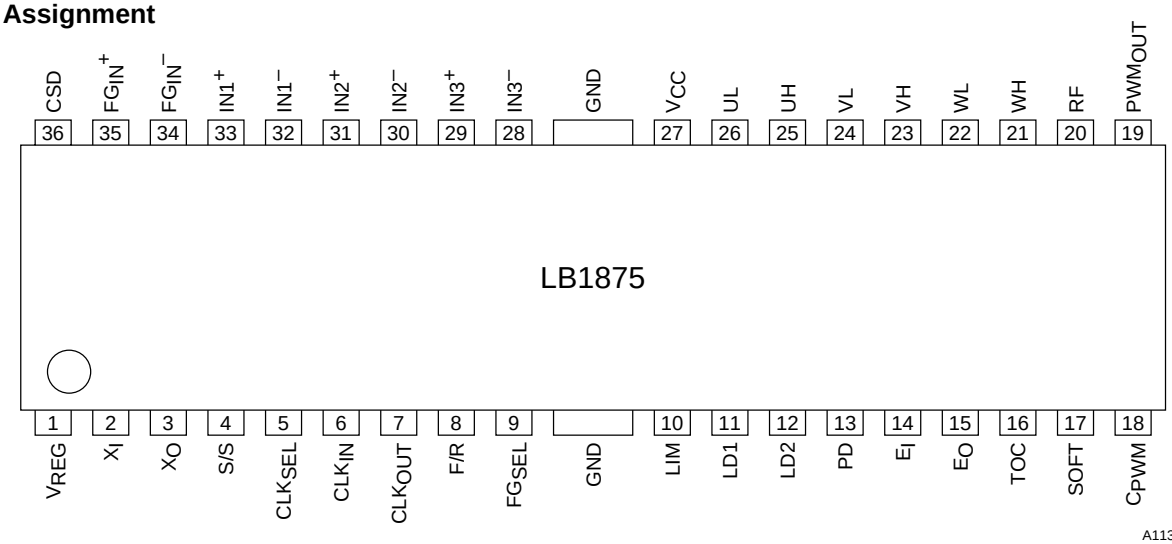
CLKSEL pin

Input state	Divisor
High or open	1024 x 4
M	1024
L	1024 x 3

LIM pin

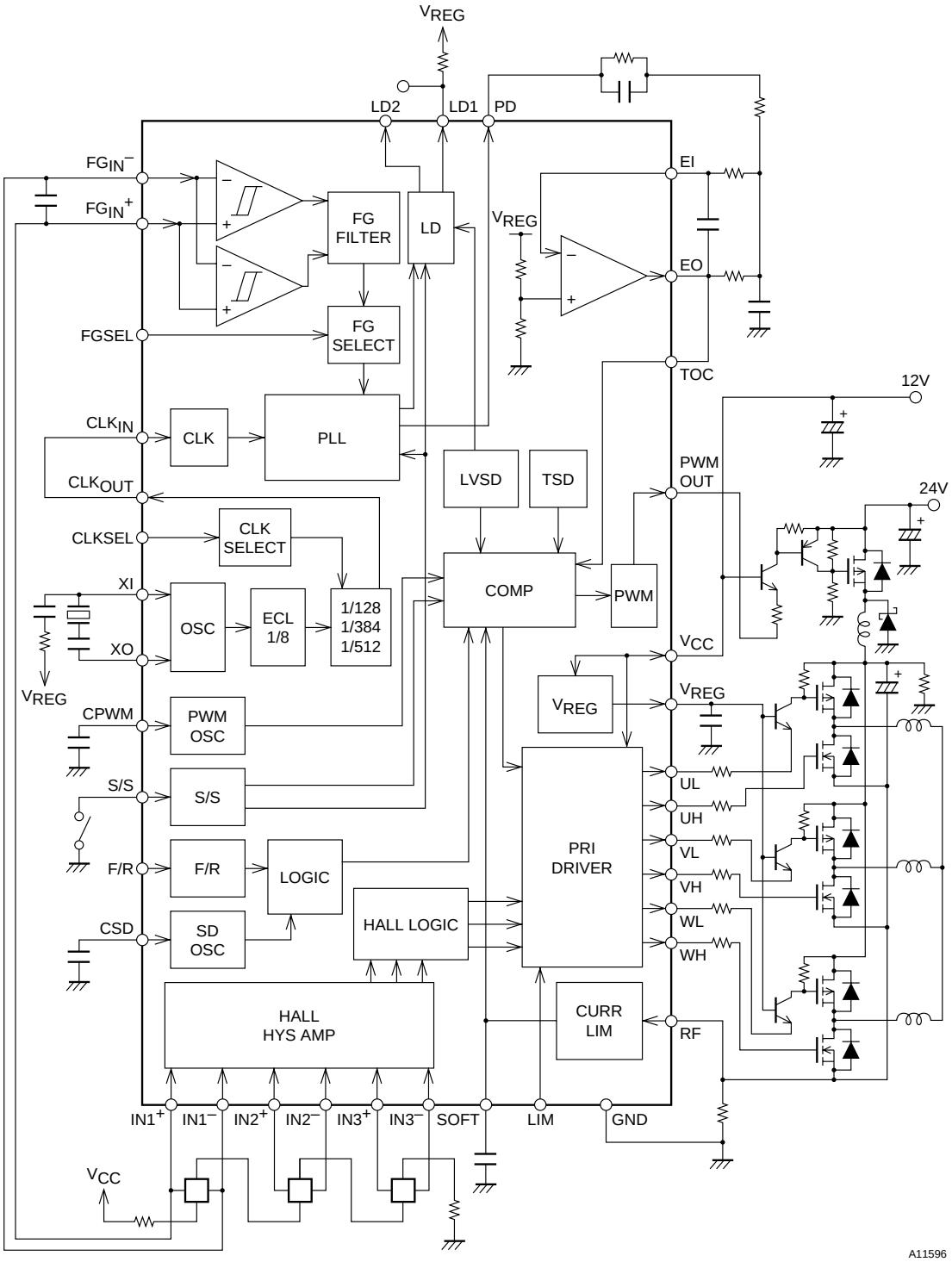
Input state	Output pin (UH, VH, WH)	PWMOUT pin
High or open	No PWM (PAM operation)	PWM output
L	PWM (direct PWN operation)	FG/Schmitt comparator output

Pin Assignment



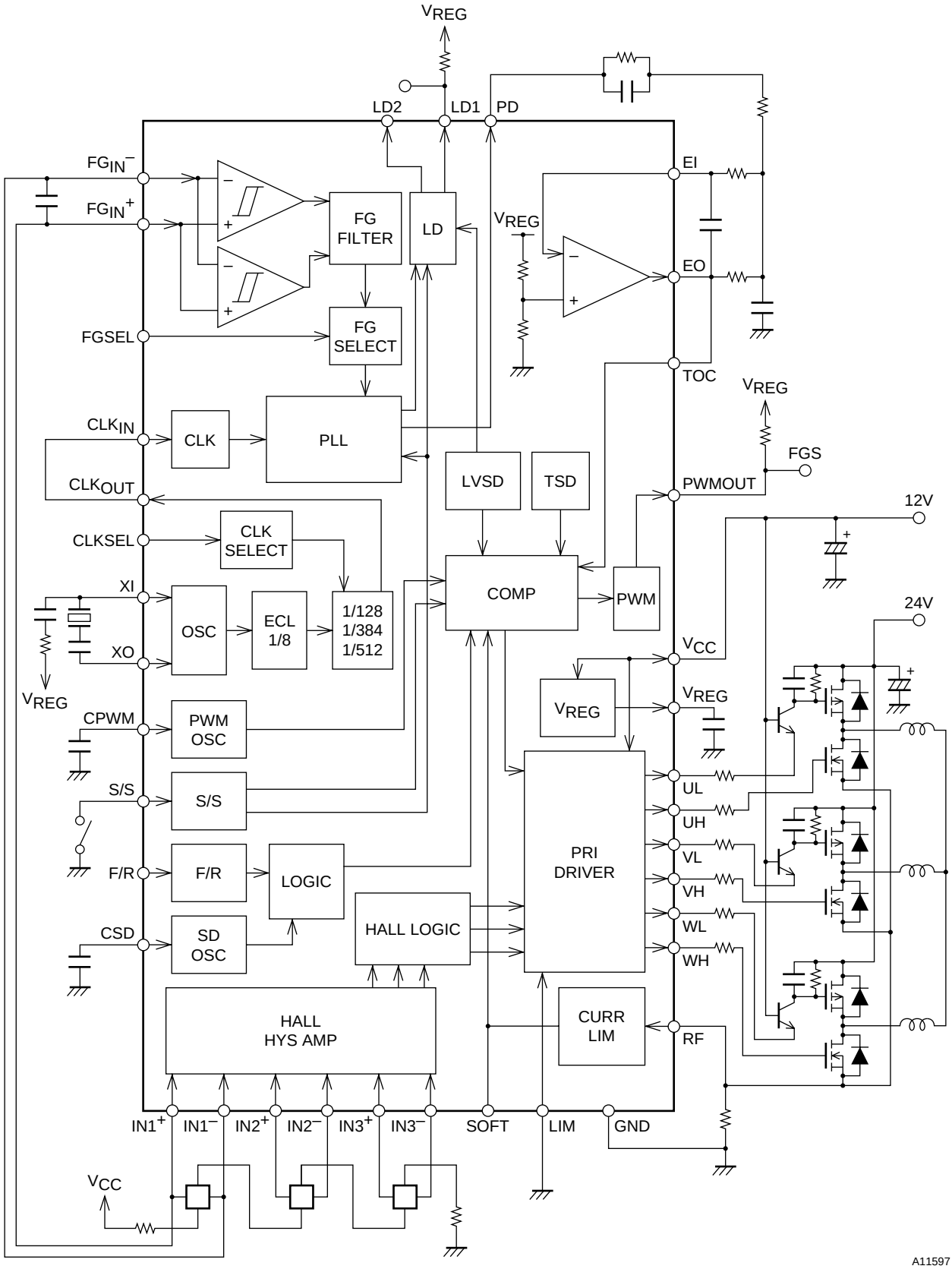
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Block Diagram and Sample Application Circuit (Sample application: PAM drive, FET output)

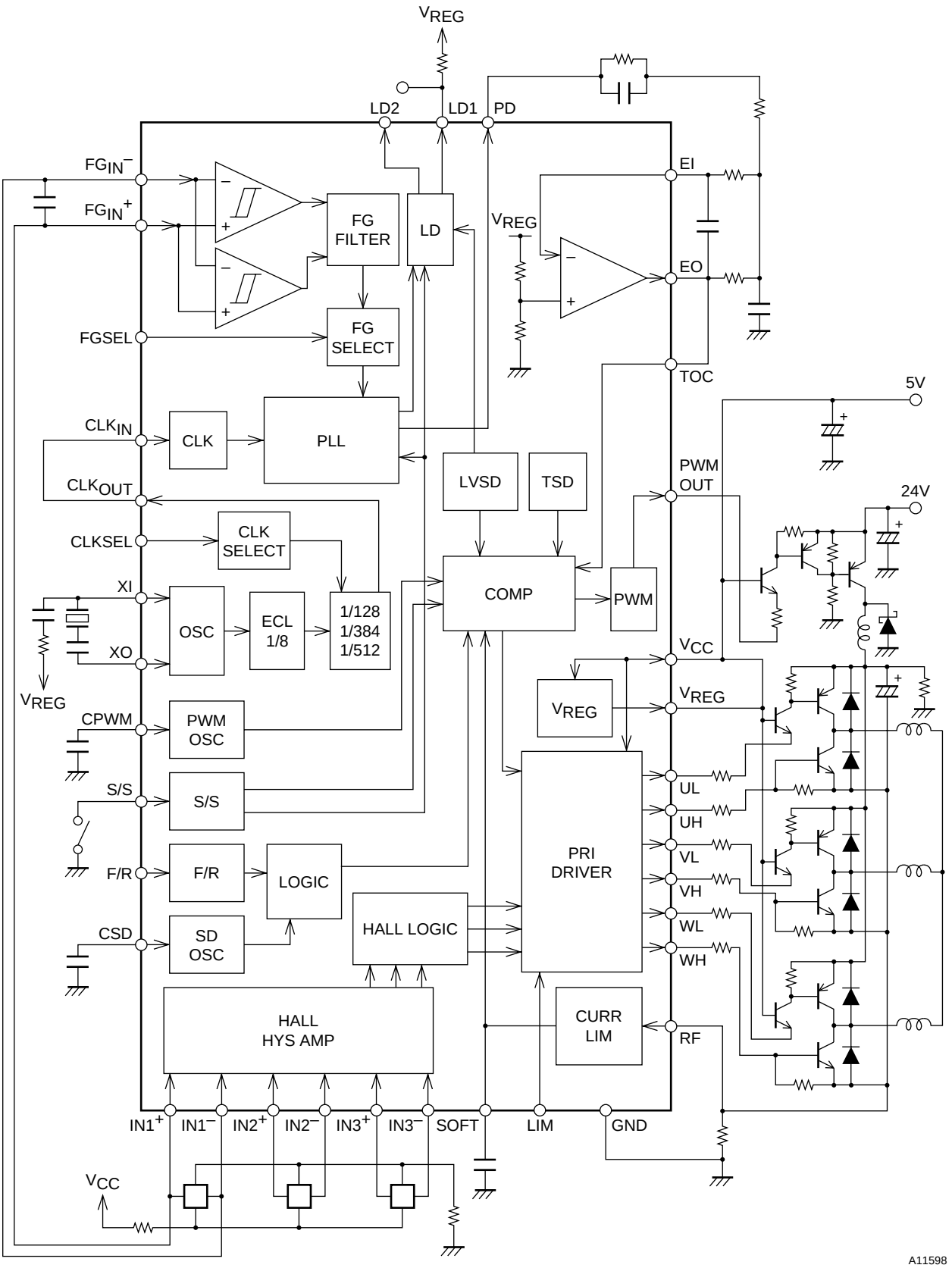


Note: For applications where the motor has variable speed and control at low motor voltages is required, the base voltage of the output interface transistor must be made low. In this case, a P-channel FET which can be used at low gate voltages must be selected.

(Sample application: direct PWM drive, FET output)



(Sample application: PAM drive, bipolar transistor output)



Description of the LB1875

1. Speed control circuit

This IC uses the PLL speed control technique which allows stable, high-precision motor rotation with low jitter. The PLL circuit performs phase comparison of the falling edge of the clock input (CLK_{IN}) with the edge of the FG input. Control is based on the differential output.

When the FG_{SEL} pin is Low, only the falling edge of the FG signal is valid. When the pin is High or open, both edges are valid. When both edges are used, the FG waveform precision becomes critical.

When using an external clock input (supplied from CLK_{IN} pin), the FG servo frequency is determined by the following equation.

f_{FG} (servo) = f_{CLK} (FG_{SEL} = Low)

f_{FG} (servo) = $f_{CLK}/2$ (FG_{SEL} = High or open)

When using the internal clock, the FG servo frequency is determined by the following equation. The number of FG pulses and the quartz oscillator frequency determine the motor rotation speed.

f_{FG} (servo) = f_{OSC}/N (FG_{SEL} = Low)

f_{FG} (servo) = $f_{OSC}/2N$ (FG_{SEL} = High or open)

f_{OSC}: Quartz oscillator frequency

N: Clock divisor (see table)

2. Output drive

This IC allows selection of PAM drive or direct PWM drive.

When the LIM pin is Low, the direct PWM mode is selected. The ON duty cycle of the UH, VH, and WH output (external bottom-side transistor drive output) changes, thereby controlling the motor speed. Current control is also realized by changing the ON duty cycle to limit the current. At this time, the Schmitt comparator output of the FG is supplied at the PWM_{OUT} pin. When bipolar transistors are used externally, the top-side transistors should not have an integrated diode, but Schottky barrier diodes should be used instead (to prevent feedthrough current caused by diode reverse recovery during PWM switching).

When the LIM pin is High or open, the PAM drive mode is selected. The PWM_{OUT} pin carries the PWM signal. This output can drive an external switching regulator circuit for varying the motor supply voltage and thereby controlling motor speed. Current control is also realized by changing the motor supply voltage. In this case, a delay in the switching regulator circuit will cause a delay in the current control action. During the delay, a higher current than the set current may flow, which must be taken into consideration when selecting output transistors. For applications where the motor has variable speed and control at low motor voltages is required, the lowest operation voltage is limited by the base voltage of the interface transistor for top-side output transistor drive. If this causes a problem, the base voltage must be made low (for example by dividing the V_{REG} voltage with resistors). When FETs are used as top-side output transistors, types which can be used at low gate voltages must be selected.

3. Current limiting circuit

The current limiting circuit limits the peak current to the value $I = V_{RF}/Rf$ (V_{RF} = 0.5V typ., Rf: current detector resistor). As mentioned above, in PAM drive mode, a current higher than the set current may flow during the delay interval. If the capacitor charge current of the switching regulator circuit is a problem, a smoothing capacitor may be inserted, with the negative side connected to the RF pin.

If PWM noise is a problem in the RF waveform, a filter should be provided at the input.

4. Reference clock

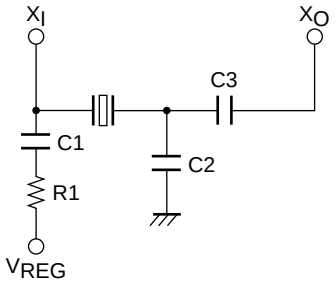
Since the clock input of the PLL circuit (CLK_{IN}) and the internal divisor output (CLK_{OUT}) are separate, various applications are possible.

(1) Using the internal divider circuit

Basically, CLK_{IN} and CLK_{OUT} are shorted. If a division ratio other than the built-in ratio is required, an external divider circuit can be inserted between these two pins.

[1] Using a quartz oscillator

An oscillator using a quartz crystal and C, R components can be configured as shown below.



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C1, R1 : For stable oscillation
C2 : For overtone oscillation prevention
C3 : For crystal coupling

(Reference values)

Oscillator frequency (MHz)	C1 (μF)	C2 (pF)	C3 (pF)	R1 (Ω)
2 to 3	0.1	10	100	330k
3 to 7	0.1	None	47	330k
7 to 9	0.1	None	22	330k
9 to 10	0.1	None	12	330k

The circuit configuration and values are for reference only. The quartz crystal characteristics as well as the possibility of floating capacitance and noise due to layout factors must be taken into consideration when designing an actual application.

[Precautions for wiring layout design]

Since the quartz oscillator circuit operates at high frequencies, it is susceptible to the influence of floating capacitance from the circuit board. Wiring should be kept as short as possible and traces should be kept narrow.

[2] External clock input (equivalent to quartz oscillator, several MHz)

When using an external signal source instead of a quartz oscillator, a resistor of about 13 kΩ should be inserted in series at the X_I input. The XO pin should be left open.

Signal input level

Low: 0 to 0.8 V

High: 2.5 to 5 V

(2) When not using the internal divider circuit

When using an external signal source to supply a signal equivalent to the FG frequency (several kHz), the signal is input via the CLK_{IN} pin. When not using a quartz oscillator, the X_I pin should be left open or connected to the V_{REG} pin (XO is open).

5. Hall input signal

The Hall input requires a signal with an amplitude of at least the hysteresis width (24 mV max.). Taking possible noise influences into consideration, an amplitude of at least 100 mV is desirable. If noise at the Hall input is a problem, a noise-canceling capacitor (about 0.001 to 0.1 μF) should be connected across the Hall input pins .

Since the same-phase input range is 0 to V_{CC}–2V, a Hall element can be connected in series if 12V is applied at the V_{CC} pin.

6. FG input signal

The FG input is designed mainly for input from a Hall element and has the same specifications as the Hall input. If the input is to be used for an FG pattern or other very low-level signal, an external amplifier must be used to amplify the signal first.

When there is noise at the FG input, locking may be impaired and jitter may increase. If PWM switching noise or other noise is found to be present, countermeasures such as making the Hall element power supply more stable or connecting a capacitor across the input will be necessary.

7. PWM frequency

The PWM frequency is determined by the capacitance connected to the C_{PWM} pin.

f PWM ≒ 1/(15000 x C)

The PWM frequency should be between 15 and 50 kHz. If the frequency is too low, noise and control performance may be a problem. If it is too high, switching losses will increase.

8. LD output

The LD1 output is ON when phase lock is achieved. Phase lock is evaluated only by the phase (through edge comparison), not by speed deviation. Therefore when LD1 is ON, speed deviation is affected by the FG signal acceleration for example when establishing the lock condition. (The lower the acceleration, the lower the speed deviation.) When it is necessary to limit speed deviation when LD1 is ON, the results of actual motor speed measurement must be applied.

9. Power supply

When using FETs as bottom-side output transistors, applying a voltage of 12V to the V_{CC} pin makes it possible to supply a gate voltage of about 10V. When using FETs or bipolar transistors that can handle a low gate voltage, the V_{CC} and V_{REG} pins can also be short- circuited to apply 5V. (In this case, do not apply voltage higher than 5.5V.)

Since this IC is designed for use in high-current motors, the power supply line may fluctuate easily. Therefore a capacitor of sufficient capacitance must be provided between the V_{CC} pin and ground, to assure stable operation. If a diode is used in the power line for reverse-connection protection, power line fluctuations may be further increased, which will require more capacitance.

10. Motor lock protection circuit

To protect the IC and the motor itself when rotation is inhibited, a motor lock protection circuit is provided. If the LD output is High (unlocked) for a certain interval in the start condition, the external bottom-side transistors are turned off. The length of the interval is determined by the capacitance at the CSD pin. A capacitance of 0.1 μF results in a trigger interval of about 10 seconds.

Trigger interval (S) ≒ 110 x C (μF)

The trigger interval should be set so as to leave sufficient leeway for motor startup. Speed reduction due to clock frequency switching does not trigger the protection circuit.

When the protection circuit has been triggered, the condition can only be canceled by setting the system to the stop condition or by turning the power off and on again. When wishing not to use the motor lock protection circuit, connect the CSD pin to ground.

11. Low voltage protection circuit

The low voltage protection circuit cuts off the bottom-side output transistors (external) when the voltage at the V_{REG} pin falls below 3.75V (typ.). The circuit action is released when the voltage rises above approx. 4.0V (typ.).

12. F/R switching

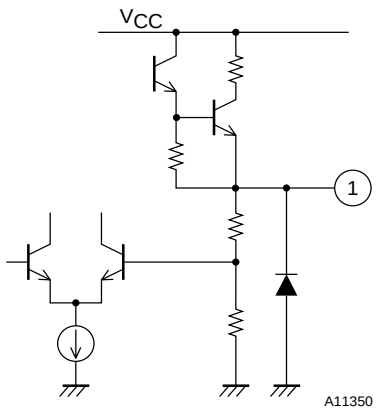
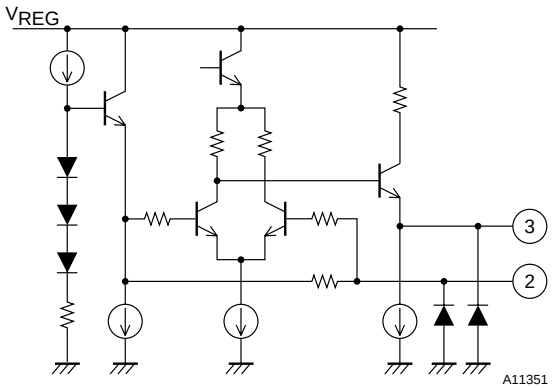
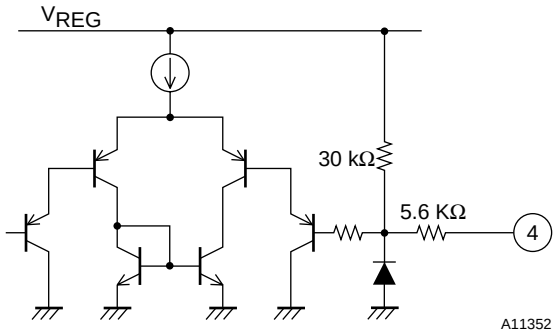
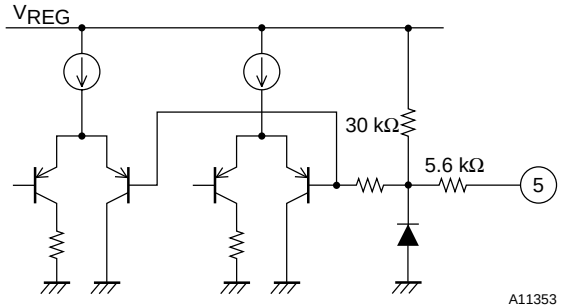
Forward/reverse switching in principle should be carried out while the motor is stopped. If switching is carried out while the motor is running, feedthrough current (due to output transistor delay) is prevented by the circuit design, but a high current will flow in the output transistors (due to counterelectromotive voltage and coil resistance). If such a condition is anticipated, the output transistors must be selected appropriately, to allow handling even higher current than in normal use.

13. Soft start

In PAM drive mode, connecting a capacitor (approx. 0.01 to 0.1 μF) between the SOFT pin and ground enables soft start (gradual increase in PWM ON duty cycle, causing a sloped rise in motor supply voltage). This prevents the current flow exceeding the set current due to switching regulator circuit delay at startup. The Soft start function is active only immediately after motor startup.

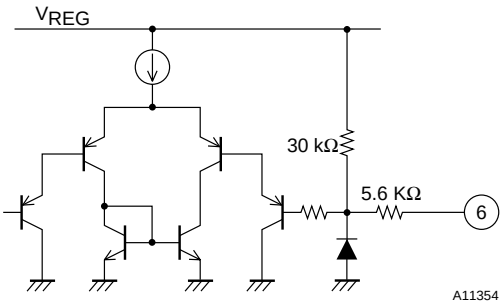
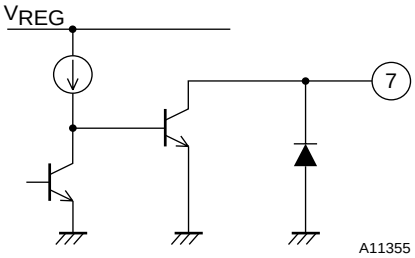
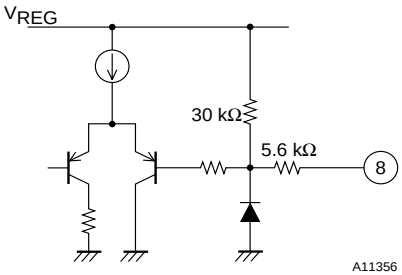
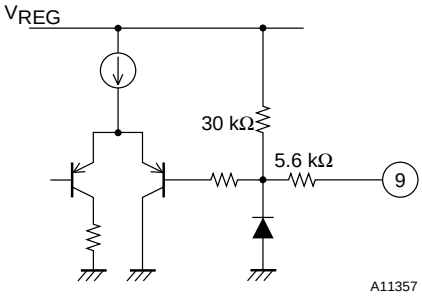
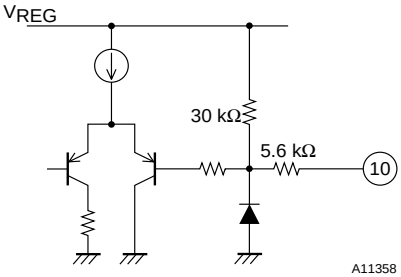
When the motor is stopped, the output transistors are turned off, therefore the charge accumulated in the switching regulator smoothing capacitors can only be discharged as leak current of the output transistors. When the motor is restarted before the supply voltage has dropped, the soft start function will not be active. Therefore it is necessary to discharge the capacitors via a resistor so that the soft start function operates properly.

Pin Descriptions

Pin number	Pin name	Equivalent circuit	Pin function
1	V_{REG}		5V regulator output (control circuit power supply) For stable operation, pin should be connected to ground via a capacitor (0.1 μF or more).
2 3	X_I X_O		Pin 2: Quartz oscillator input. Maximum oscillation frequency is 10 MHz Pin 3: Quartz oscillator output Generates reference clock. When an external clock (several MHz) is used, connect a resistor of about 13 kΩ in series to the X_I pin, so that the signal is input via the resistor. Leave the X_O pin open.
4	S/S		Start/stop pin Low: Start High: Stop High when open.
5	CLK_{SEL}		Divisor selector pin "L": (divisor 3072): 0 to 1.0V "M": (divisor 1024): 2.0 to 3.0V "H": (divisor 4093): 4.0V to V_{REG} High when open.

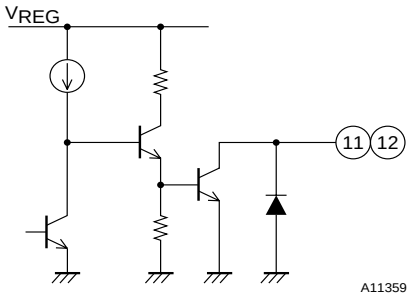
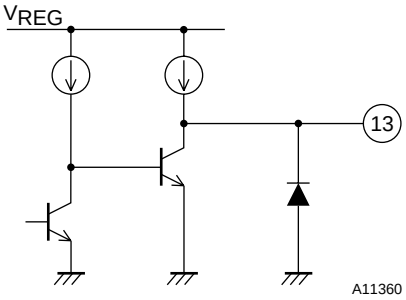
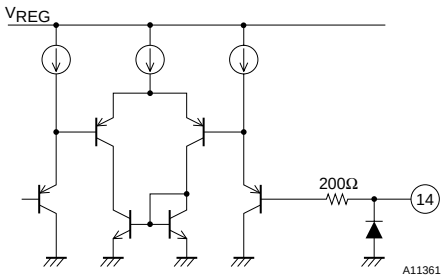
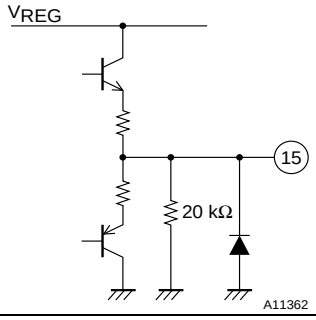
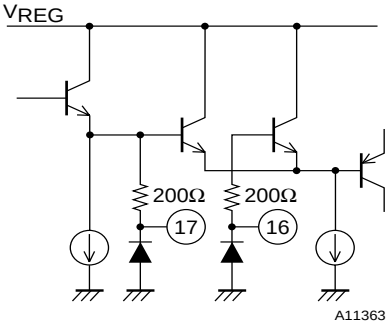
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Pin number	Pin name	Equivalent circuit	Pin function
6	CLK_{IN}		Clock input (max. 10 kHz) Low: 0 to 1.5V High: 3.5V to V_{REG} High when open.
7	CLK_{OUT}		Quartz oscillator divider output Ratio is selected with pin 5. Open collector output
8	F/R		Forward/reverse switching pin Low: 0 to 1.5V High: 3.5V to V_{REG} High when open.
9	FG_{SEL}		FG comparator selector pin Low: 0 to 1.5V –> Speed control on FG single edge High: 3.5V to V_{REG} –> Speed control on FG dual edge High when open.
10	LIM		Drive mode selector pin Low: 0 to 1.5V –> Direct PWM drive mode High: 3.5 V to V_{REG} –> PAM drive mode High when open.

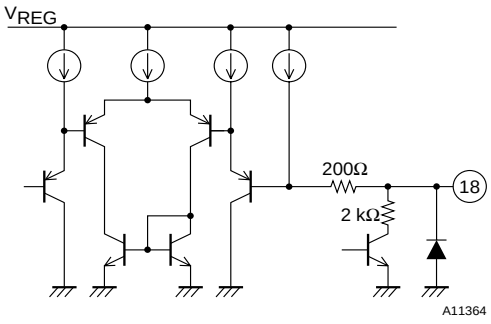
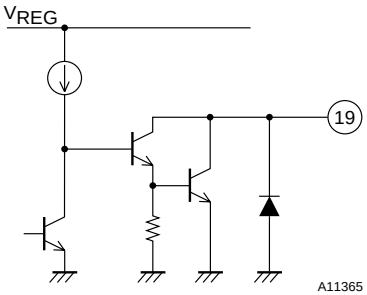
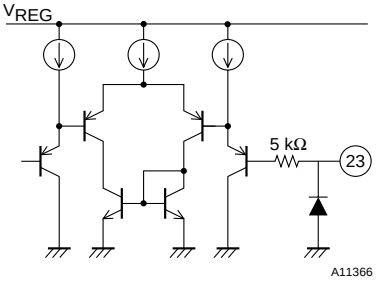
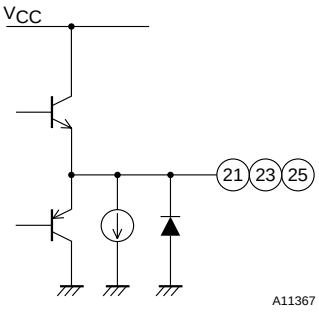
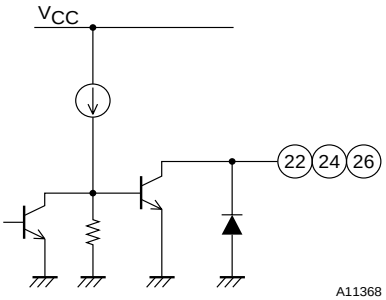
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Pin number	Pin name	Equivalent circuit	Pin function
11	LD1		Phase lock detector output On when PLL phase lock is achieved. Open collector output
12	LD2		Phase lock detector output (LD1 inverted output) On when PLL phase lock is achieved. Open collector output
13	PD		Phase comparator output (PLL output) Outputs the phase difference as a signal with changing pulse duty cycle. The higher the duty cycle, the higher the output current.
14	E_I		Differential amplifier input
15	E_O		Differential amplifier output Output current increases at Low.
16	TOC		Torque control input Normally connected to EO pin. When TOC pin goes Low, duty cycle of UH, VH, WH (direct PWM mode) or PWM output (PAM mode) changes, resulting in increased torque.
17	SOFT		Soft start control pin Connect to ground via a capacitor. Leave open when soft start is not to be used.

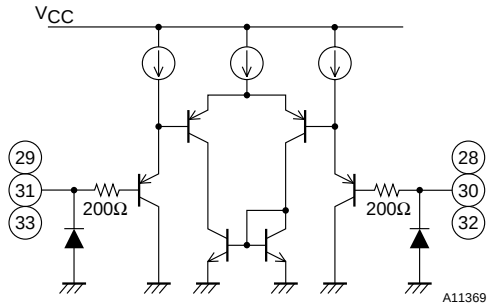
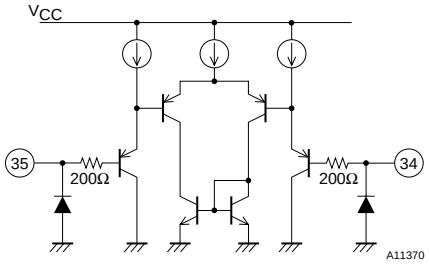
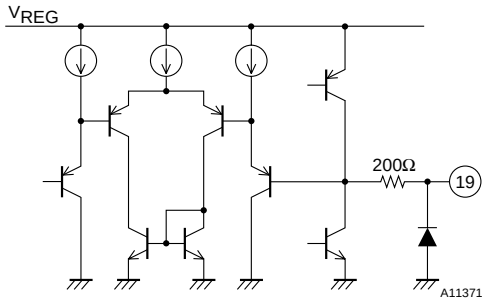
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Pin number	Pin name	Equivalent circuit	Pin function
18	PWM		PWM oscillator pin Connect to ground with a capacitor to set oscillation frequency.
19	PWM_{OUT}		PWM output Open collector output (Darlington connection). In direct PWM mode (LIM pin Low) the output is an FG Schmitt output.
20	RF		Output current detector pin Connect to ground via a lower resistor. Sets maximum output current I_{OUT} = 0.5/Rf.
21 23 25	WH VH UH		Output pin (for external bottom-side transistor drive) Performs duty cycle control in direct PWM mode (LIM pin Low).
22 24 26	WL VL UL		Output pin (for external bottom-side transistor drive) . Open collector output.

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Pin number	Pin name	Equivalent circuit	Pin function
27	V_{CC}		Power supply pin (output and regulator circuit power supply). Connect to ground via capacitor to prevent noise. When using the IC with a single 5V source, short this pin to the V_{REG} pin.
33 32 31 30 29 28	$IN1^+$ $IN1^-$ $IN2^+$ $IN2^-$ $IN3^+$ $IN3^-$		Hall inputs for various phases Logic "High" indicates $V_{IN^+}>V_{IN^-}$.
35 34	FG_{IN}^+ FG_{IN}^-		FG comparator input Pin 35: Non-inverted input Pin 36: Inverted input
36	CSD		Reference signal oscillator for motor lock protection circuit, clock interruption error protection circuit etc. Connect to ground via capacitor. Connect directly to ground if protection circuit is not to be used.
FRAME	GND		Ground

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