Ordering number : EN8317

LB11876

Monolithic Digital IC

For Polygonal Mirror Motors
Three-Phase Brushless Motor Driver

ON Semiconductor®

http://onsemi.com

Overview

The LB11876 is a 3-phase brushless motor driver developed for driving the polygonal mirror motor in plain-paper copiers and similar products. It can support any motor voltage and motor current required by the use of appropriate external components.

The LB11876 adopts direct PWM drive to achieve drive with minimal power loss.

Functions

- This is a version of the LB11875 with a modified constraint protection function.
- Three-phase bipolar drive (direct PWM)
- PLL speed control circuit
- Dedicated external clock
- Clock divider switching function
- Hall sensor FG support
- Short-circuit braking function
- Built-in current limiter, thermal protection, constraint protection, and undervoltage protection circuits

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		18	V
Input current	I13 max	V13 pin	5	mA
Output current	I_O max	UL pin, VL pin, WL pin, UH pin, VH pin, and WH pin	30	mA
LVSD pin apply voltage	LVSD max		18	V
Allowable power dissipation 1	Pd max1	Independent IC	0.62	W
Allowable power dissipation 2	Pd max2	When mounted on a circuit board *1	1.36	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

*1 Specified circuit board : 114.3 × 76.1 × 1.6mm^3, glass epoxy.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Semiconductor Components Industries, LLC, 2013

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	$V_{CC}1$		8 to 17	V
Supply voltage range 2	$V_{CC}2$	With V_{CC} shorted to VREG	4.5 to 5.5	V
Input current range	I13	V13 pin	0.5 to 4	mA
Output current	I_O	UL pin, VL pin, WL pin, UH pin, VH pin, and WH pin	20	mA
5V constant voltage output	IREG		0 to -30	mA
LD pin apply voltage	VLD		0 to 17	V
LD pin output current	ILD		0 to 15	mA
FGS pin apply voltage	VFGS		0 to 17	V
FGS pin output current	IFGS		0 to 10	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$			15	25	mA
Supply current 2	$I_{CC}2$	Stop mode		3	5	mA
5V constant voltage output (VREG pin)						
Output voltage	VREG		4.65	5.0	5.35	V
Line regulation	ΔVREG1	V_{CC} = 8 to 13.5V		40	100	mV
Load regulation	ΔVREG2	I_O = 0 to -15mA		20	100	mV
Temperature coefficient	ΔVREG3	Design target		0		mV/°C
13V constant voltage output (V13 pin)						
Output voltage	V13	I_O = 2mA	12.5	13.5	14.5	V
Output Block						
Output saturation voltage 1-1	V_O sat1-1	Low level, I_O = 400μA		0.2	0.5	V
Output saturation voltage 1-2	V_O sat1-2	Low level, I_O = 10mA		0.9	1.2	V
Output saturation voltage 2	V_O sat2	High level, I_O = -20mA	V_{CC} – 1.2	V_{CC} – 0.9		V
Output leakage current	I_O leak				10	μA
Hall Sensor Amplifier Block						
Input bias current	IHB (HA)		-2	-0.5		μA
Common-mode input voltage range1	VICM1 (HA)	When a Hall sensor is used	0.5		V_{CC} – 2.0	V
Common-mode input voltage range2	VICM2 (HA)	When a single-sided input bias is used (using a Hall sensor IC)	0		V_{CC}	V
Input sensitivity		Sine wave	80			mVp-p
Hysteresis	ΔVIN (HA)		15	24	42	mV
Input current low → high	VSLH (HA)			12		mV
Input current high → low	VSHL (HA)			-12		mV
FG Schmitt Trigger Block						
Input bias current	IB (FGS)		-2	-0.5		μA
Common-mode input voltage range1	VICM1 (FGS)	When a Hall sensor is used	0.5		V_{CC} – 2.0	V
Common-mode input voltage range2	VICM2 (FGS)	When a single-sided input bias is used (using a Hall sensor IC)	0		V_{CC}	V
Input sensitivity	V_{IN} (FGS)	Sine wave	80			mVp-p
Hysteresis	$ΔV_{IN}$ (FGS)	Design target	15	24	42	mV
Input current low → high	VSLH (FGS)	Design target		12		mV
Input current high → low	VSHL (FGS)	Design target		-12		mV

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FGS Output						
Output saturation voltage	V_{OL} (FGS)	I_{LD} = 7mA		0.15	0.5	V
Output leakage current	I_L (FGS)	$V_O = V_{CC}$			10	µA
PWM Oscillator						
High-level output voltage	V_{OH} (PWM)		2.6	2.9	3.2	V
Low-level output voltage	V_{OL} (PWM)		1.4	1.7	2.0	V
External capacitor charge current	ICHG	VPWM = 2.0V	-65	-50	-35	µA
Oscillator frequency	f (PWM)	C = 620pF		50		kHz
Amplitude	V (PWM)		1.0	1.2	1.4	Vp-p
CSD Oscillator Circuit						
High-level output voltage	V_{OH} (CSD)		3.2	3.5	3.8	V
Low-level output voltage	V_{OL} (CSD)		0.9	1.1	1.3	V
External capacitor charge current	ICHG1		-13	-10	-7	µA
External capacitor discharge current	ICHG2		7	10	13	µA
Oscillator frequency	f (CSD)	C = 0.068µF		30		Hz
Amplitude	V (CSD)		2.2	2.4	2.6	Vp-p
Phase Comparator Output						
High-level input voltage	VPDH	I_{OH} = -100µA	VREG - 0.2	VREG - 0.1		V
Low-level input voltage	VPDL	I_{OH} = 100µA		0.2	0.3	V
Input source current	IPD+	VPD = VREG/2			-0.6	mA
Input sink current	IPD-	VPD = VREG/2	1.5			mA
Phase Lock Detection Output						
Output saturation voltage	V_{OL}(LD)	I_{LD} = 10mA		0.15	0.4	V
Output leakage current	I_L (LD)	$V_O = V_{CC}$			10	µA
Error Amplifier Block						
Input offset voltage	V_{IO} (ER)	Design target value	-10		10	mV
Input bias current	IB (ER)		-0.4		0.4	µA
High-level output voltage	V_{OH} (ER)	IEI = -0.1mA, no load		3.7		V
Low-level output voltage	V_{OL} (ER)	IEI = 0.1mA, no load		1.3		V
DC bias level	VB (ER)	Design target value	-5%	VREG/2	5%	V
Current Llimiter Circuit						
Llimiter voltage	VRF		0.225	0.25	0.275	V
Low Voltage Protection Circuit						
Operating voltage	VSDL		3.5	3.7	3.9	V
Release voltage	VSDH		4.0	4.2	4.4	V
Hysteresis	ΔVSD		0.35	0.5	0.65	V
Thermal shutdown circuit						
Thermal shutdown operating temperature	TSD	Design target value (junction temperature)	150	180		°C
Thermal shutdown temperature hysteresis	ΔTSD	Design target value (junction temperature)		30		°C
CLD Circuit						
External capacitor discharge current	ICLD		-5	-4	-3	µA
Operating voltage	V_H (CLD)		3.25	3.5	3.75	V

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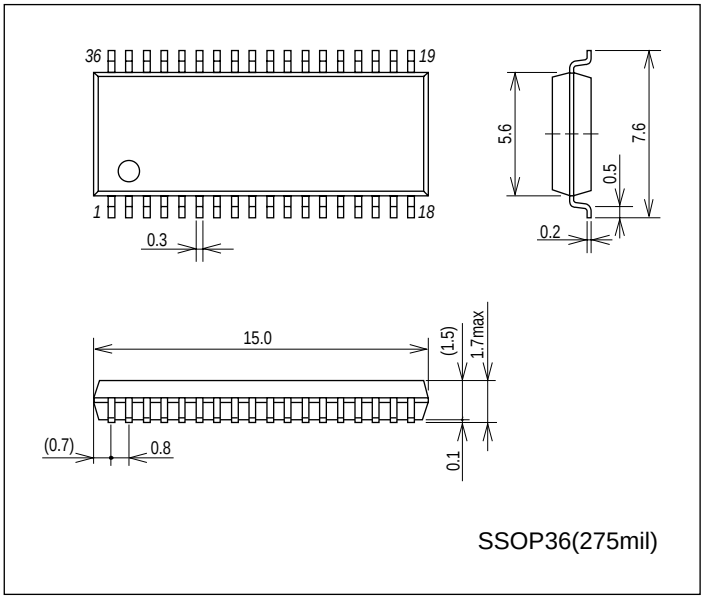
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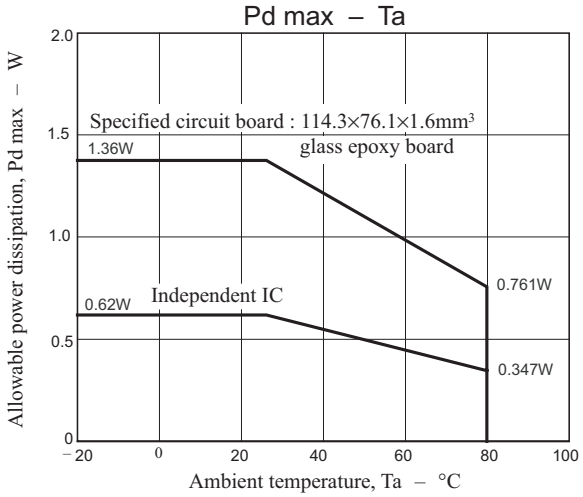
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CLKIN pin						
External input frequency	fI (CKIN)		0.1		10	kHz
High-level input voltage	V_{IH} (CKIN)		2.0		VREG	V
Low-level input voltage	V_{IL} (CKIN)		0		1.0	V
Input open voltage	V_{IO} (CKIN)		VREG – 0.5		VREG	V
Hysteresis	V_{IS} (CKIN)		0.13	0.21	0.29	V
High-level input current	I_{IH} (CKIN)	VCKIN = VREG	-10	0	10	µA
Low-level input current	I_{IL} (CKIN)	VCKIN = 0V	-130	-90		µA
S/S pin						
High-level input voltage	V_{IH} (SS)		2.0		VREG	V
Low-level input voltage	V_{IL} (SS)		0		1.0	V
Input open voltage	V_{IO} (SS)		VREG – 0.5		VREG	V
Hysteresis	V_{IS} (SS)		0.13	0.21	0.29	V
High-level input current	I_{IH} (SS)	VS/S = VREG	-10	0	10	µA
Low-level input current	I_{IL} (SS)	VS/S = 0V	-130	-90		µA
F/R pin						
High-level input voltage	V_{IH} (FR)		2.0		VREG	V
Low-level input voltage	V_{IL} (FR)		0		1.0	V
Input open voltage	V_{IO} (FR)		VREG – 0.5		VREG	V
Hysteresis	V_{IS} (FR)		0.13	0.21	0.29	V
High-level input current	I_{IH} (FR)	VF/R = VREG	-10	0	10	µA
Low-level input current	I_{IL} (FR)	VF/R = 0V	-130	-90		µA
BRSEL pin						
High-level input voltage	V_{IH} (BSEL)		2.0		VREG	V
Low-level input voltage	V_{IL} (BSEL)		0		1.0	V
Input open voltage	V_{IO} (BSEL)		VREG – 0.5		VREG	V
Hysteresis	V_{IS} (BSEL)		0.13	0.21	0.29	V
High-level input current	I_{IH} (BSEL)	VBSEL = VREG	-10	0	10	µA
Low-level input current	I_{IL} (BSEL)	VBSEL = 0V	-130	-90		µA
CLKSEL pin						
High-level input voltage	V_{IH} (CSEL)		2.0		VREG	V
Low-level input voltage	V_{IL} (CSEL)		0		1.0	V
Input open voltage	V_{IO} (CSEL)		VREG – 0.5		VREG	V
Hysteresis	V_{IS} (CSEL)		0.13	0.21	0.29	V
High-level input current	I_{IH} (CSEL)	VCSEL = VREG	-10	0	10	µA
Low-level input current	I_{IL} (CSEL)	VCSEL = 0V	-130	-90		µA

Package Dimensions

unit : mm (typ)

3247A





Three-Phase Logic Truth Table (The input "H" state is the state where IN+ > IN-)

	F/R= "L"			F/R ="H"			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	Source	Sink
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

S/S pin

Input state	State
High or open	Stop
Low	Start

BRSEL pin

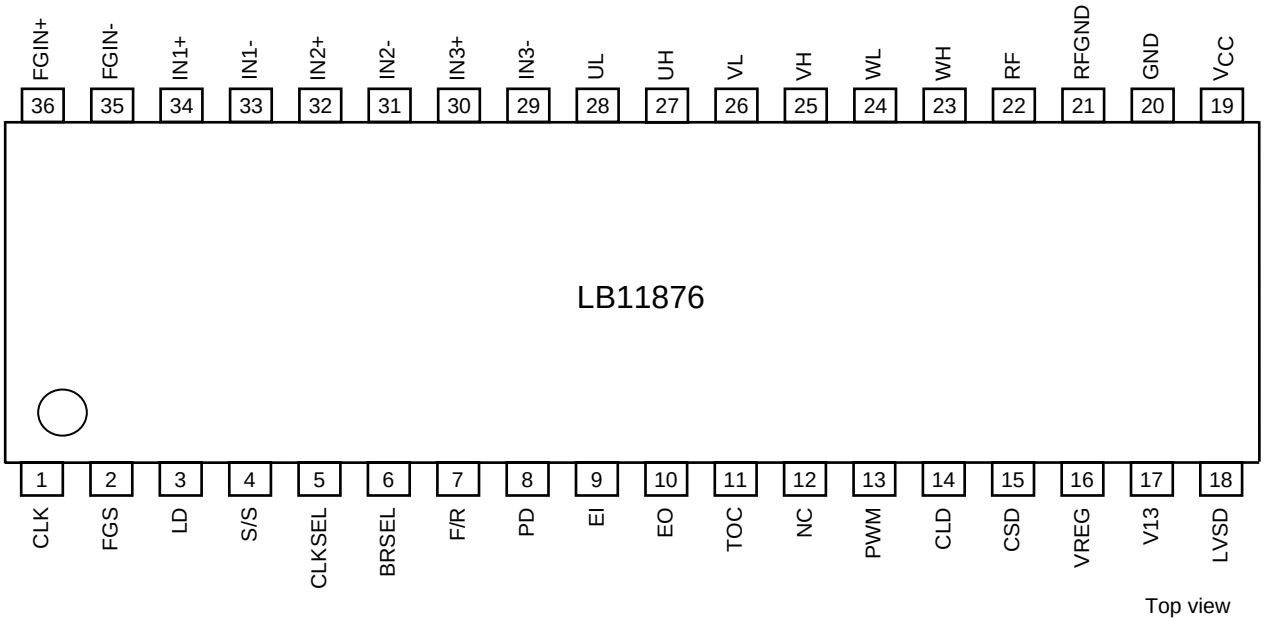
Input state	During deceleration
High or open	Free running
Low	Short-circuit braking

CLKSEL pin

Input state	Clock divisor
High or open	1
Low	2

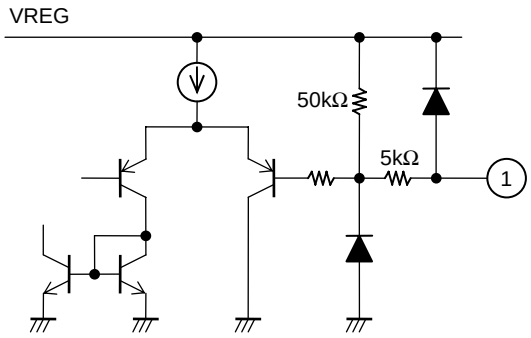
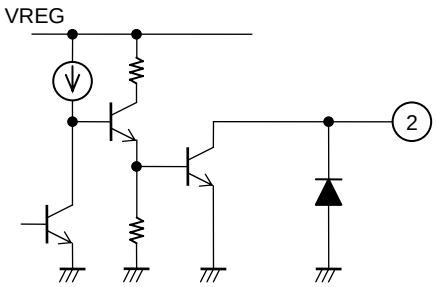
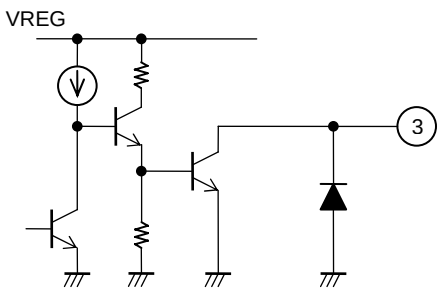
$f_{FG} = f_{CLK} \div \text{divisor}$

Pin Assignment



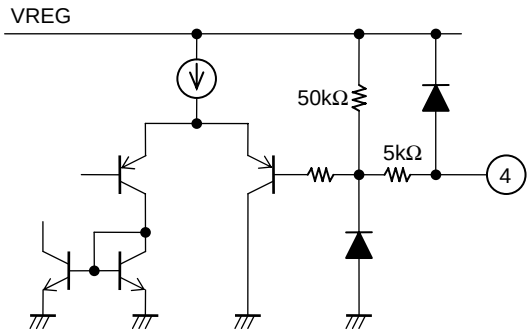
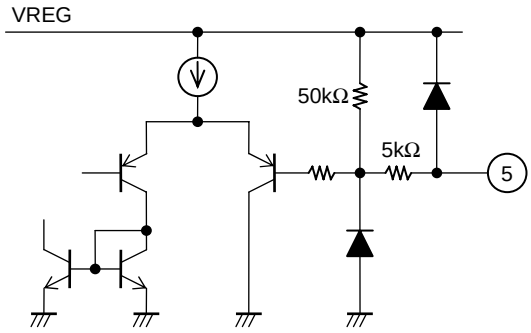
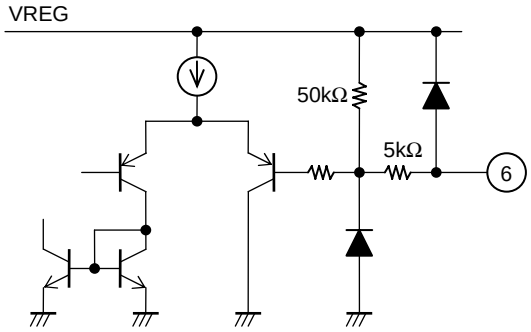
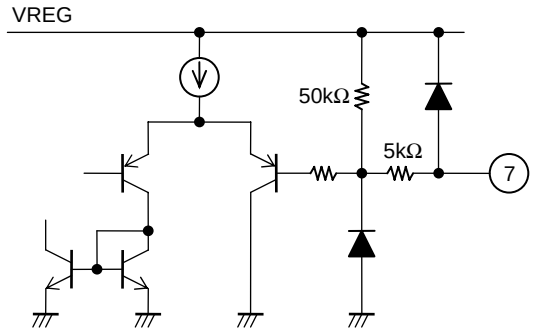
Top view

Pin Functions

Pin No.	Pin	Description	Equivalent Circuit
1	CLK	External clock signal input Low : 0V to 1.0V High : 2.0V to VREG This pin goes to the high level when open. Hysteresis : about 0.21V f = 10kHz (maximum)	
2	FGS	FG Schmitt trigger output This is an open-collector output.	
3	LD	Phase lock detection output This output goes to the on state (low-level output) in the phase locked state. This is an open-collector output.	

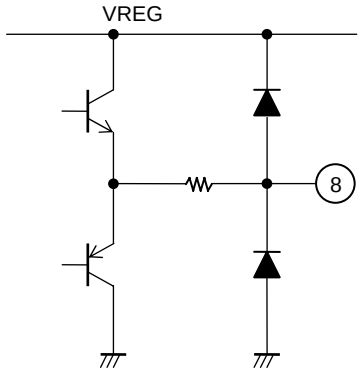
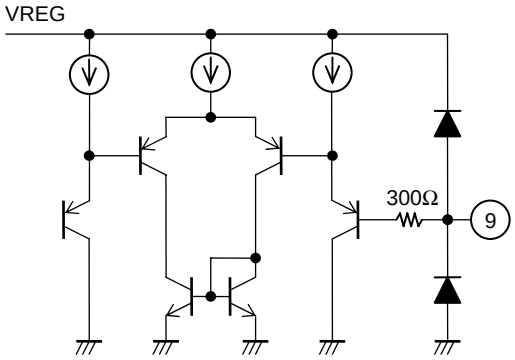
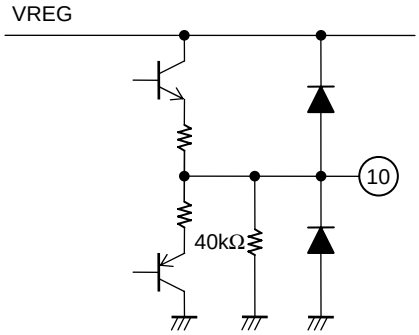
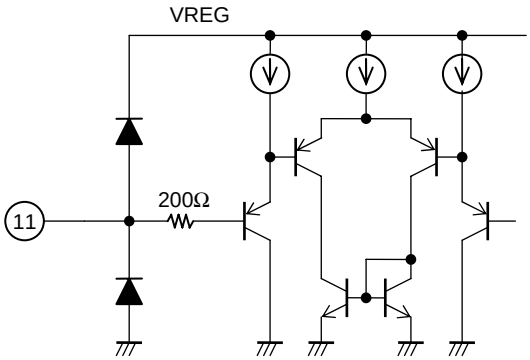
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Pin No.	Pin	Description	Equivalent Circuit
4	S/S	Start/stop control Low : 0V to 1.0V High : 2.0V to VREG This pin goes to the high level when open. A low level specifies the start state. Hysteresis : about 0.21V	
5	CLK SEL	Clock divisor selection Low : 0V to 1.0V High : 2.0V to VREG This pin goes to the high level when open. A low level specifies a divisor of two, and a high level specifies a divisor of 1. Hysteresis : about 0.21V	
6	BR SEL	Deceleration (braking) control selection Low : 0V to 1.0V High : 2.0V to VREG This pin goes to the high level when open. A low level specifies short-circuit braking, and a high level or open specifies free running operation. Hysteresis : about 0.21V	
7	F/R	Forward/reverse selection Low : 0V to 1.0V High : 2.0V to VREG This pin goes to the high level when open. A low level specifies forward operation. Hysteresis : about 0.21V	

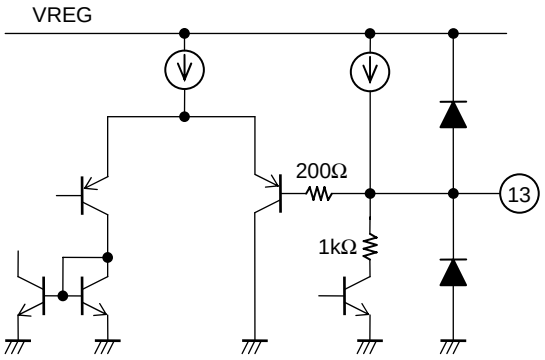
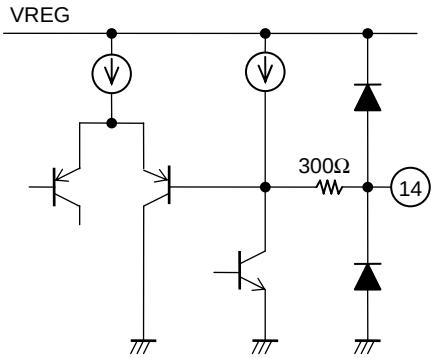
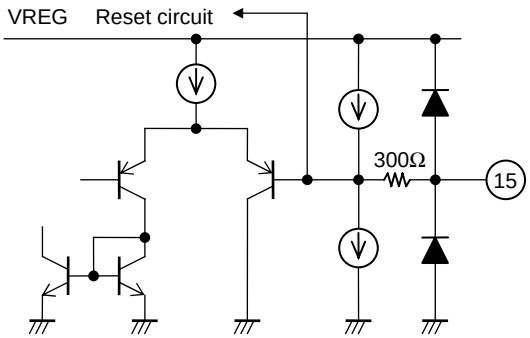
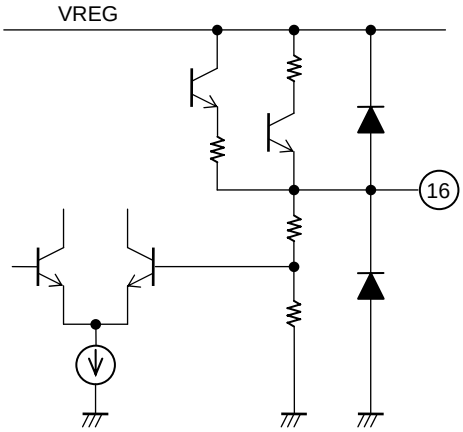
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Pin No.	Pin	Description	Equivalent Circuit
8	PD	Phase comparator output The phase error is converted to a pulse duty and output from this pin.	
9	EI	Error amplifier input	
10	EO	Error amplifier output	
11	TOC	Torque command input This pin is normally connected to the EO pin. When the TOC voltage falls, the UH, VH, and WH on duty is increased.	
12	NC	Since this pin is not connected to any internal circuits, it may be used as a connection point.	

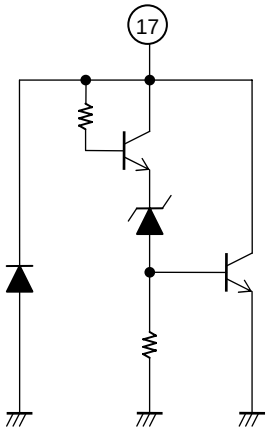
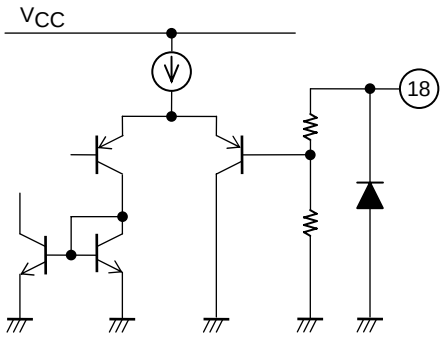
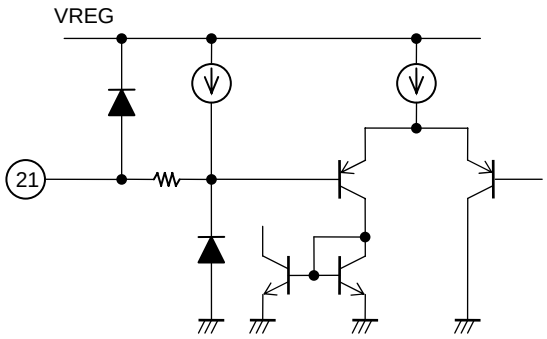
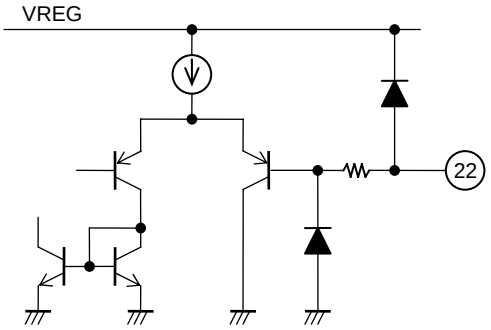
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Pin No.	Pin	Description	Equivalent Circuit
13	PWM	Sets the PWM oscillator frequency. Connect a capacitor between this pin and ground. A 620pF capacitor sets the oscillator frequency to be about 50kHz.	
14	CLD	Phase lock signal mask time setting A mask time of about 90ms can be set up by connected a capacitor (about 0.1μF) between this pin and ground.Leave this pin open if there is no need to mask the phase lock signal.	
15	CSD	Constraint protection circuit operating time setting and initialization pulse setting A protection circuit operating time of about 1 seconds can be set up by connecting a capacitor (about 0.068μF) between this pin and ground. Connect both a capacitor and a resistor (about 220kΩ and 4700pF) in parallel between this pin and ground if this protection circuit is not used.	
16	VREG	Stabilized power supply output (5V output) Connect a capacitor between this pin and ground for power supply stabilization. (About 0.1μF)	

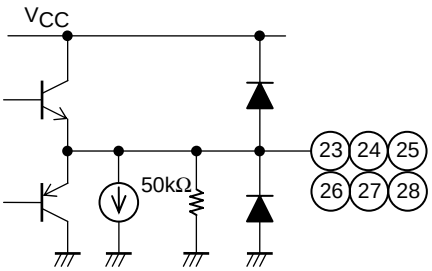
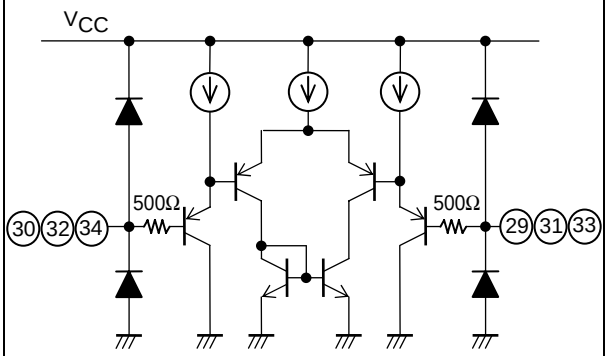
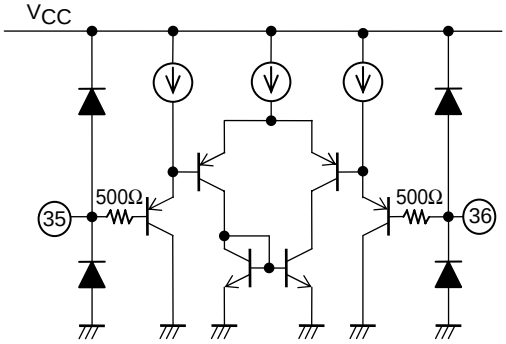
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Pin No.	Pin	Description	Equivalent Circuit
17	V13	13V shunt regulator output	
18	LVSD	Undervoltage protection detection If a power supply voltage of 5V or over is to be detected, connect a Zener diode in series to set the detection voltage.	
19	V_{CC}	Power supply. Connect a capacitor between this pin and ground for power supply stabilization.	
20	GND	Ground	
21	RF GND	Output current detection reference The external resistor Rf is connected to ground.	
22	RF	Output current detection A resistor is connected between RF and ground. The maximum output current I_{OUT} is determined by the equation I_{OUT} = 0.25/Rf.	

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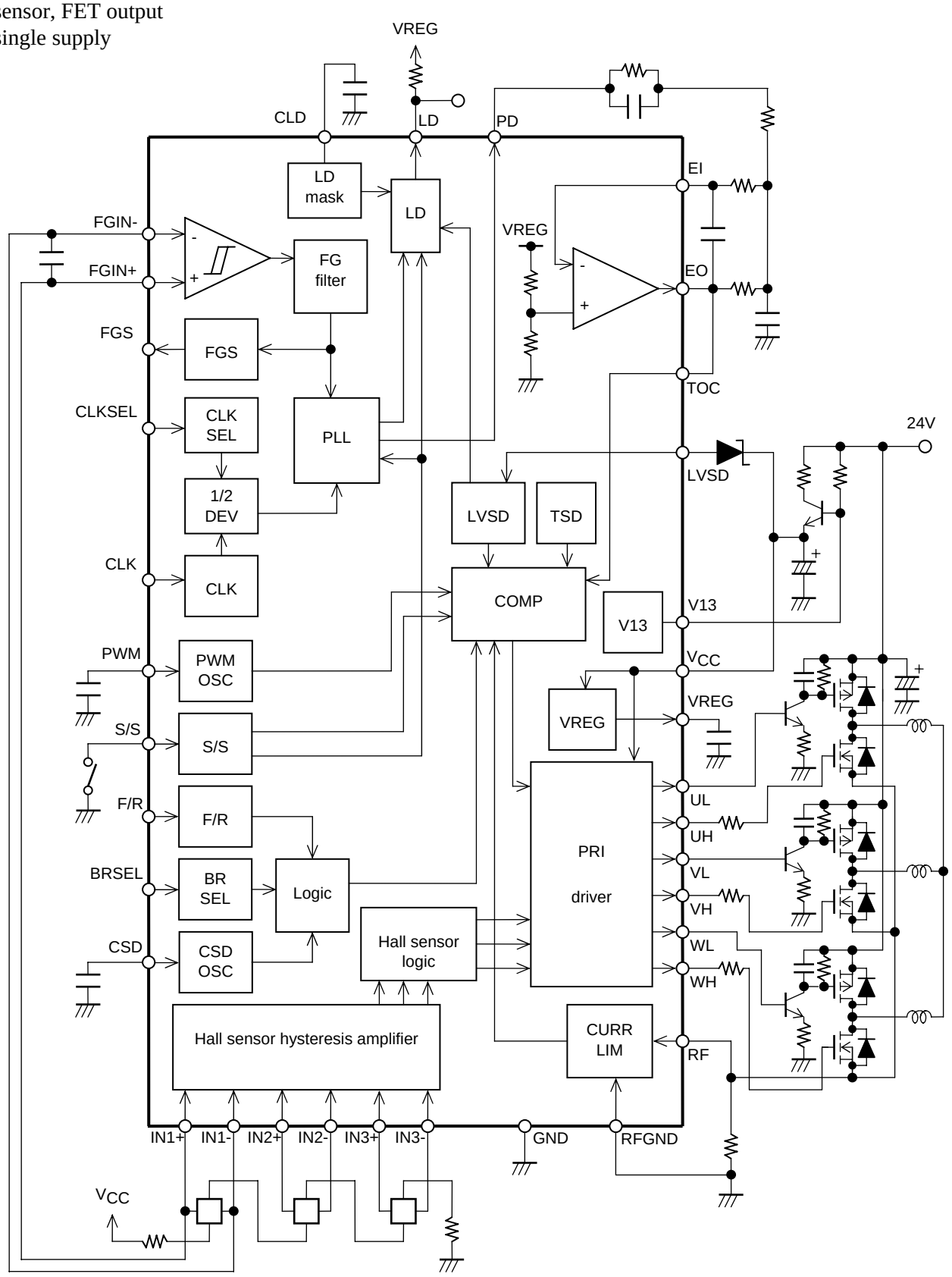
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Pin No.	Pin	Description	Equivalent Circuit
23 24 25 26 27 28	WH WL VH VL UH UL	Outputs (that drive external transistors) Duty control is applied to the UH, VH, and WH outputs.	
29 30 31 32 33 34	IN3- IN3+ IN2- IN2+ IN1- IN1+	Hall sensor inputs "H" is the state where IN+ > IN-, and "L" is the reverse state. If noise on the Hall sensor signals is a problem, connect capacitors between the IN+ and IN- inputs.	
35 36	FGIN- FGIN+	FG input If noise on the FG signal is a problem, the input signal can be filtered with a capacitor or a capacitor plus resistor.	

Internal Equivalent Circuit Block Diagram and External Reference Circuit

(Application example)

Hall sensor, FET output
24V single supply



LB11876 Overview

1. Speed control circuit

Since the LB11876 adopts PLL speed control, it provides precise, low-jitter, and stable motor operation. This PLL circuit compares the falling edge of the CLK signal with the FG signal (the falling edges of the FGIN+ or FGS output) and controls motor operation based on the difference.

The FG servo frequency during this control operation is controlled by the frequency given by the following formula which is based on the divisor selected by the clock input frequency (f_{CLK}) and the CLKSEL pin.

f_{FG} (servo) = f_{CLK} ÷ <divisor>

2. Output drive circuit

To minimize the power loss in the output, the LB11876 adopts direct PWM drive. The output transistors, which are external, are always saturated when on and the motor drive power is adjusted by changing the duty with which the output is on.

The PWM switching is performed with the UH, VH, and WH outputs. Either high side or low side switching can be selected by the way the output transistors are connected.

3. Current limiter circuit

The current limiter circuit limits the drive current to a current determined by the equation I = VRF/RF, where VRF = 0.25V (typical) and Rf is the current detection resistor. The limiting operation works by reducing other output on duty to suppress the drive current.

Detection with excellent precision can be acquired by connecting the RF and RFGND pin lines to points as close as possible to the ends of the current detection resistor (Rf).

4. Reference clock

Care must be taken to assure that no noise due to chattering or other problems appears on the externally input clock signal. While the input circuit is designed with hysteresis, noise must be rejected by, for example, inserting capacitors in the clock line if noise problems occur.

If the application is to be started in the state where there is no reference clock input signal, the motor will turn somewhat and then drive will be turned off.

5. PWM frequency

The PWM frequency is determined by the capacitance of the capacitor (C) connected to the PWM pin.

$f_{PWM} \approx 1/(30000 \times C)$

If a 620pF capacitor is used, the circuit will oscillate at about 50kHz. If the PWM frequency is too low the motor will emit switching noise, and if it is too high the power loss in the output will increase. A frequency in the range 30kHz to 100kHz is desirable. This capacitor must be connected between this pin and the GND pin by lines that are as short as possible to make this circuit immune to noise.

6. Hall sensor input signals

To prevent noise problems, the Hall sensor input signals should have an amplitude of at least 100mV. If the output waveforms (during phase switching) are disrupted by noise, this must be prevented by connecting capacitors across the inputs.

If the outputs from a Hall sensor IC are input, holding one side of the inputs (either the + or - side) at a voltage within the common-mode input range for direct Hall sensor signal input will allow the other side to be used as 0V to V_{CC} input.

7. FG input signal

Normally, one of the Hall sensor signals is used as the FG input signal. if noise is a problem, the input signal must be filtered with a capacitor or a capacitor plus resistor.

8. Constraint protection circuit

The LB11876 includes a built-in constraint protection circuit to protect the IC and the motor if the motor is physically constrained from turning. If one Hall sensor input signals do not switch states for a period in excess of a certain fixed time in the start state, the PWM drive side output is turned off. The time is set by the capacitor connected to the CSD pin.

Set time (seconds) ≈ 15.4 × C (μF)

If a 0.068μF capacitor is used, the protection time will be about 1.05 seconds. (If one Hall sensor input signal period becomes longer than this time, the PWM drive side output is turned off.) This set time must have a certain amount of margin with respect to the motor startup time. This protection circuit will not operate during deceleration due to switching the clock frequency. The constraint protection state can be cleared by either switching to the stop state or turning the power off and then on again.

Since the CSD pin also functions as the initial reset pulse generation pin, connecting this pin to ground will reset the logic circuits and make speed control operation impossible. Therefore, if the constraint protection circuit is not used, this pin must be connected to ground by a resistor of about 220kΩ and a capacitor of about 4700pF connected in parallel.

9. Undervoltage protection circuit

The LB11876 includes a undervoltage protection circuit to prevent incorrect operation when power is first applied or when the power supply voltage falls. The LVSD pin turns the PWM drive side output off at voltages under about 3.7V (typical), and clears the protection state when the voltage rises above about 4.2V (typical). An arbitrary operating voltage can be set by adding an external Zener diode.

Note that the maximum applied voltage for the LVSD pin is 18V.

10. Phase lock signal

(1) Phase lock range : Since this IC does not have a speed system counter, the speed error range in the phase locked state cannot be determined by the IC characteristics alone. (This is because the range is affected by the acceleration with changes in the FG frequency.) If it is necessary to stipulate this in conjunction with a motor, it will be necessary to measure the range with the actual motor state. Since speed errors occur easily in states where the FG acceleration is large, it is thought that the lock pull-in time at startup and the unlock time due to clock switching will be the cases where the speed error is the largest.

(2) Phase lock signal mask function : It is possible to assure that the lock signal is output in stable states by masking the short-term low levels due to hunting during lock pull-in. Note, however, that the lock signal output will be delayed by the amount of the mask time. The mask time is set by the capacitor connected between the CLD pin and ground.

Mask time (seconds) ≈ 0.9 × C (μF)

When a 0.1μF capacitor is used, the mask time will be about 90ms. If full masking is required, the mask time must be set with an adequate margin. Leave the CLD pin open if masking is not required.

11. Power supply stabilization

(1) V_{CC} : Since this IC is used in switching drive applications with large output currents, the power supply line is easily disrupted.

Therefore it is necessary to connect an adequately large capacitor between the V_{CC} pin and ground. The capacitor ground side should be located as close to the IC GND pin as possible.

Since the power supply line is most easily disrupted during lock pull-in at high speeds, designers must analyze this case carefully and select an adequately large capacitor.

Since the power supply line is particularly susceptible to disruption if a diode is inserted in the power supply line to prevent destruction of the IC by reverse connection, an even larger capacitor must be selected in this case.

(2) 13V regulator : When implementing a motor driver circuit with single-voltage power supply specifications and a voltage that is outside the power supply voltage range of this IC, the supply voltage required by this IC (approx. 13V) can be created using the V13 pin. The V13 pin circuit is a shunt regulator and can generate a 13V level by supplying current through an external resistor. A stabilized voltage is generating by setting the current to a level in the range 0.5mA to 4mA. An external transistor with a current capacity of over 80mA (I_{CC} + Hall sensor bias current + output source current) and a voltage handling capacity higher than the motor supply voltage must be selected. Since heat generation in the transistor may become a problem, heat dissipation must be provided by the package.

(3) 5V regulator : Connect a capacitor with a value over 0.1μF to stabilize the VREG voltage, which is the IC's control circuit power supply. That capacitor's ground side must be connected as close as possible to the IC ground.

12. Power saving circuit

This IC goes into a power saving state in which current drain is reduced when set to the stop state. This power saving state is implemented by cutting the bias current to most of the circuits in the IC. The 5V regulator output, however, is still output when the IC is in the power saving state.

13. Error amplifier system components

The external components for the error amplifier block must be located as close as possible to the IC to minimize the influence of noise. These components must also be located as far from the motor as possible.

14. Forward/reverse switching

In principle, forward/reverse switching must be performed with the motor in the stopped state.
This IC does provide circuit workarounds for handling the through currents that occur during switching if the direction is switched while the motor is turning. However, care is required with respect to lifting of the motor supply voltage during this switching, since the motor current will return to the power supply during brief instants. If this becomes a problem, the size of the capacitor connected between the power supply line and ground must be increased.
If the motor current after switching exceeds the current limit value, the PWM drive side output will be turned off. However, the opposite side output will go to the short-circuit braking state and a current determined by the motor induced voltage and the coil resistance. This current must be held under the current rating of the output transistors used. (This aspect requires more care the faster the motor speed at which forward/reverse switching occurs.)

15. Brake switching

Either free running or short-circuit braking can be selected with the BRSEL pin.
The short-circuit braking mode adopts a form in which all phases of the PWM drive side output transistors are turned on (all phases of the reverse side transistors are turned off). Care is required, since the current limiter function does not operate during braking. During braking, the output circuits go to a shorted state with 100% duty. The current that flows in the output transistors during braking is determined by the motor induced voltage and the coil resistance. This current must be held under the current rating of the output transistors used. (This aspect requires more care the faster the motor speed at which braking occurs.)

16. NC pins

Since the NC pins are electrically open, they can be used for intermediate wiring connections without problem.

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