Ordering number : ENA0081B

SANYO Semiconductors
DATA SHEET

Monolithic Digital IC

LB11873 — For Polygonal Mirror Motors Three-Phase Brushless Motor Driver

Overview

The LB11873 is a 3-phase brushless motor driver developed for driving the polygonal mirror motor used in plain-paper copiers and similar products. This IC can implement the circuits required for polygonal mirror motor drive (speed control and driver circuits) in a single chip.

The LB11873 implements low-noise/low-vibration PWM drive by changing the current at phase switching gradually to reduce motor noise.

Functions

- Three-phase bipolar drive (quiet direct PWM)
- PLL speed control circuit
- Hall sensor FG support
- Dedicated external clock
- Brake mode switching circuit (free running and reverse braking)
- Phase lock detection output (with masking function)
- Built-in current limiter, constraint protection, undervoltage protection, thermal protection, and CLK line disconnection protection circuits
- Input pins support 3V system microcontrollers

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		30	V
Output current	I_O max	T ≤ 500ms	1.8	A
Allowable power dissipation 1	Pd max1	Independent IC	0.9	W
Allowable power dissipation 2	Pd max2	When mounted on a circuit board *1	2.1	W

*1 Specified circuit board : 114.3 × 76.1 × 1.6mm^3, glass epoxy.

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Parameter	Symbol	Conditions	Ratings	Unit
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		9.5 to 28	V
5V constant voltage output	IREG		0 to -30	mA
LD pin apply voltage	VLD		0 to 28	V
LD pin output current	ILD		0 to 15	mA
FGS pin apply voltage	VFGS		0 to 28	V
FGS pin output current	IFGS		0 to 10	mA
HB pin apply voltage	VHBS		0 to 28	V
HB pin output current	IHBS		0 to 30	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = V_M = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$			22	28	mA
Supply current 2	$I_{CC}2$	Stop mode		4.0	6.0	mA
5V constant voltage output (VREG pin)						
Output voltage	VREG		4.65	5.0	5.35	V
Line regulation	ΔVREG1	V_{CC} = 9.5 to 28V		80	130	mV
Load regulation	ΔVREG2	I_O = -5 to -20mA		10	60	mV
Temperature coefficient	ΔVREG3	Design target*		0		mV/°C
Output Block						
Output saturation voltage 1	$V_O$sat1	I_O = 0.5A, V_O (sink) + V_O (source)		1.4	1.9	V
Output saturation voltage 2	$V_O$sat2	I_O = 1.2A, V_O (sink) + V_O (source)		2.0	2.6	V
Output leakage current	$I_O$leak				100	μA
High side diode forward voltage 1	VD2-1	ID = 0.5A		1.0	1.5	V
High side diode forward voltage 2	VD2-2	ID = 1.2A		1.5	2.0	V
Hall Sensor Amplifier Block						
Input bias current	IHB			2	10	μA
Differential input range	VIHIN	Sine wave input	50		350	
Common-mode input voltage range	VICM		1.5		VREG – 1.0	V
Input offset voltage	VIOH	Design target value*	-20		20	mV
Hall Sensor Bias						
Output saturation voltage	V_{OL} (HB)	IHB = 10mA	1.5		2.0	V
Output leakage current	I_L (HB)	V_O = V_{CC}, stop mode			10	μA
FG Schmitt Trigger Block (IN1)						
Input amplifier gain	GFG	Design target value*		5		Times
Input hysteresis (high → low)	VSHL	Design target value*		0		mV
Input hysteresis (low → high)	VSLH	Design target value*		-10		mV
Hysteresis	VFGL	Input conversion, design target value *	4	7	12	mV
PWM Oscillator						
High-level output voltage	V_{OH} (PWM)		2.65	2.95	3.25	V
Low-level output voltage	V_{OL} (PWM)		0.9	1.2	1.5	V
External capacitor charge current	ICHG	VPWM = 2V	-60	-45	-30	μA
Oscillator frequency	f (PWM)	C = 680pF		34		kHz
Amplitude	V (PWM)		1.45	1.75	2.05	Vp-p

* The design specification items are design guarantees and are not measured.

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FGS Pin						
Output saturation voltage	V_{OL} (FGS)	IFGS = 7mA		0.15	0.5	V
Output leakage current	I_L (FGS)	$V_O = V_{CC}$			10	µA
CSD Oscillator Circuit						
Oscillator frequency	f (CSD)	C = 0.033µF		31		Hz
High-level output voltage	V_{OH} (CSD)		3.50	3.75	4.00	V
Low-level output voltage	V_{OL} (CSD)		1.00	1.30	1.60	V
Amplitude	V (CSD)		2.20	2.45	2.80	Vp-p
External capacitor charge current	ICHG1	VCSD = 2V	-7	-5	-3	µA
External capacitor discharge current	ICHG2	VCSD = 2V	3	5	7	µA
Lock detection delay counts	CSDCT1			7		
Clock disconnected protection counts	CSDCT2			2		
Constraint protection operation counts	CSDCT3			31		
Initial reset voltage	VRES			0.6	0.8	V
Phase Comparator Output						
High-level input voltage	VPDH	I_{OH} = -100µA	VREG - 0.2	VREG - 0.1		V
Low-level input voltage	VPDL	I_{OL} = 100µA		0.2	0.3	V
Input source current	IPD+	VPD = VREG/2			-0.5	mA
Input sink current	IPD-	VPD = VREG/2	1.5			mA
Phase Lock Detection Output						
Output saturation voltage	V_{OL} (LD)	I_{LD} = 10mA		0.15	0.5	V
Output leakage current	I_L (LD)	$V_O = V_{CC}$			10	µA
Error Amplifier Block						
Input offset voltage	V_{IO} (ER)	Design target value*	-10		10	mV
Input bias current	IB (ER)		-1		1	µA
High-level output voltage	V_{OH} (ER)	IEI = -0.1mA, no load	3.7	4.0	4.3	V
Low-level output voltage	V_{OL} (ER)	IEI = 0.1mA, no load	0.7	1.0	1.3	V
DC bias level	VB (ER)		-5%	VREG/2	5%	V
Current Llimiter Circuit						
Drive gain 1	GDF1	In the phase locked state	0.4	0.5	0.6	Times
Drive gain 2	GDF2	In the unlocked state	0.8	1.0	1.2	Times
Llimiter voltage 1	VRF1	V_{CC} - VM, forward mode	0.45	0.5	0.55	V
Llimiter voltage 2	VRF2	V_{CC} - VM, reverse mode	0.225	0.25	0.275	V
Thermal shutdown circuit						
Thermal shutdown operating temperature	TSD	Design target value* (junction temperature)	150	170		°C
Thermal shutdown temperature hysteresis	ΔTSD	Design target value* (junction temperature)		40		°C
Low Voltage Protection Circuit						
Operating voltage	VSDL		8.1	8.45	8.9	V
Hysteresis	ΔVSD		0.2	0.35	0.5	V
CLK pin						
External input frequency	fI (CLK)		0.1		10	kHz
High-level input voltage	V_{IH} (CLK)		2.0		VREG	V
Low-level input voltage	V_{IL} (CLK)		0		1.0	V
Input open voltage	VIO (CLK)			3.0		V
Hysteresis	VIS (CLK)			0.25		V
High-level input current	I_{IH} (CLK)	VCKIN = VREG		115	150	µA
Low-level input current	I_{IL} (CLK)	VCKIN = 0V	-220	-175		µA

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Note : * The design specification items are design guarantees and are not measured.

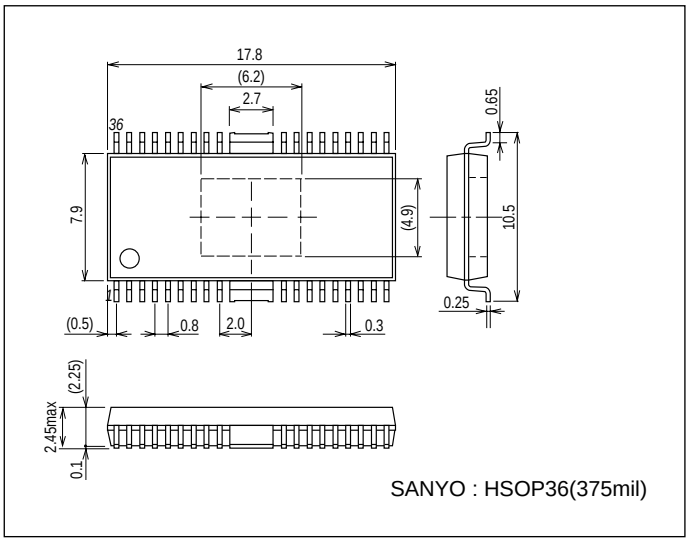
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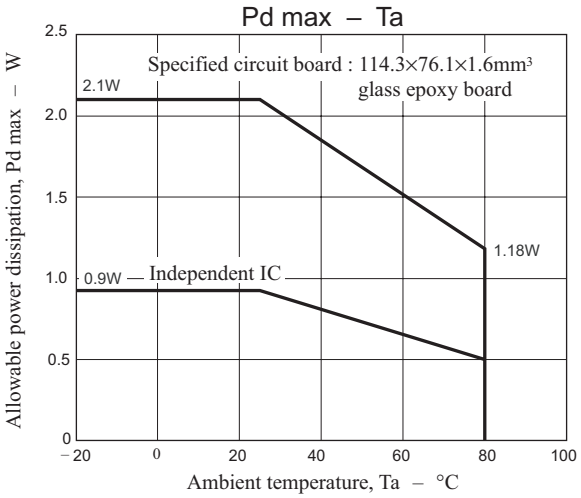
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
S/S pin						
High-level input voltage	V_{IH} (SS)		2.0		VREG	V
Low-level input voltage	V_{IL} (SS)		0		1.0	V
Input open voltage	VIO (SS)			3.0		V
Hysteresis	VIS (SS)		0.21	0.25	0.29	V
High-level input current	I_{IH} (SS)	VS/S = VREG		115	150	μA
Low-level input current	I_{IL} (SS)	VS/S = 0V	-220	-175		μA
BRSEL pin						
High-level input voltage	V_{IH} (BRSEL)		2.0		VREG	V
Low-level input voltage	V_{IL} (BRSEL)		0		1.0	V
Input open voltage	VIO (BRSEL)			3.0		V
Hysteresis	VIS (BRSEL)		0.21	0.25	0.29	V
High-level input current	I_{IH} (BRSEL)	VBRSEL = VREG		115	150	μA
Low-level input current	I_{IL} (BRSEL)	VBRSEL = 0V	-220	-175		μA

Package Dimensions

unit : mm (typ)

3235A





Three-Phase Logic Truth Table (The input "H" state is the state where IN+ > IN-)

IN1	IN2	IN3	OUT1	OUT2	OUT3
H	L	H	L	H	M
H	L	L	L	M	H
H	H	L	M	L	H
L	H	L	H	L	M
L	H	H	H	M	L
L	L	H	M	H	L

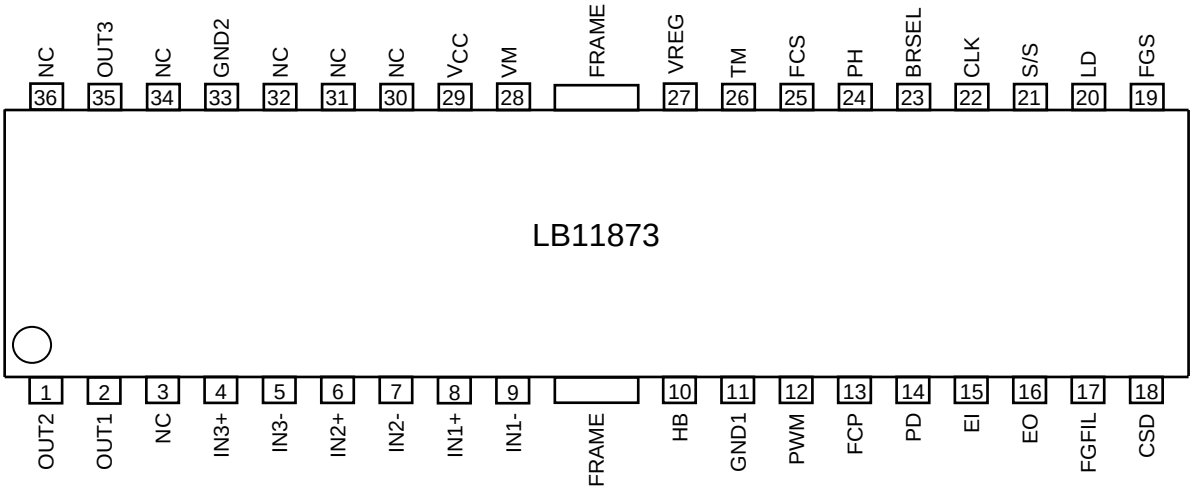
S/S pin

Input state	State
High or open	Stop
Low	Start

BRESEL pin

Input state	During deceleration
High or open	Free running
Low	Reverse braking

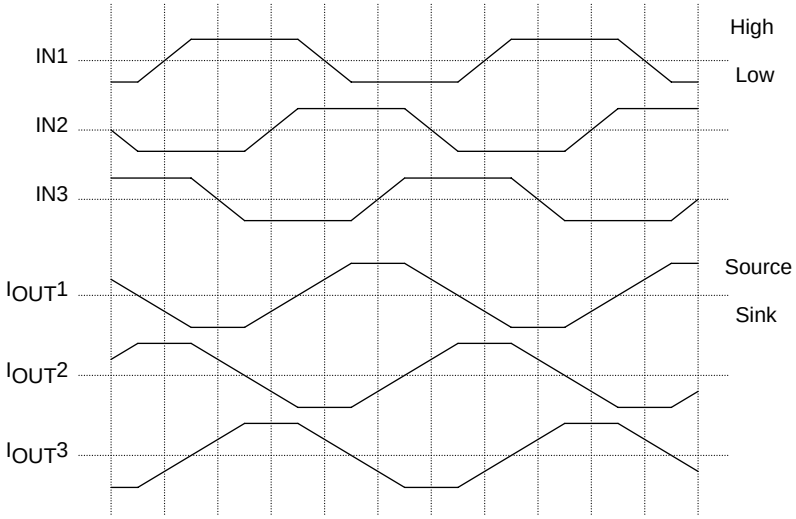
Pin Assignment



Top view

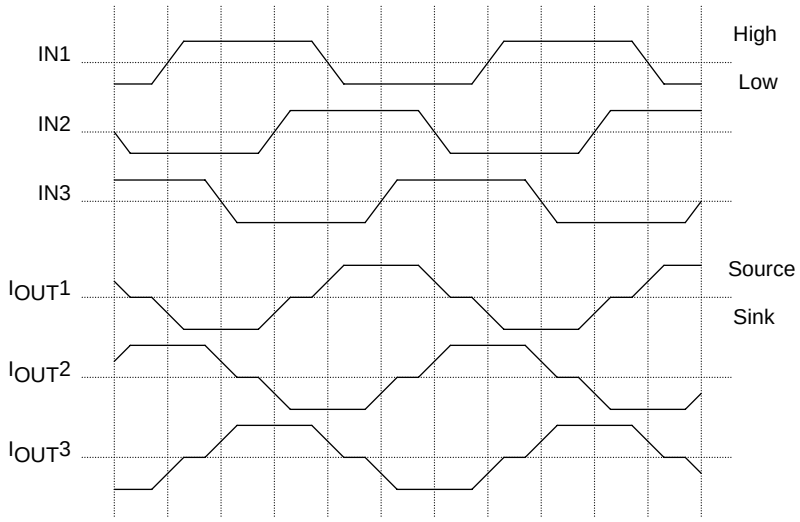
Hall sensor input waveforms and output current waveform

(1) When the Hall sensor input amplitude is small or when the input waveform slope is low



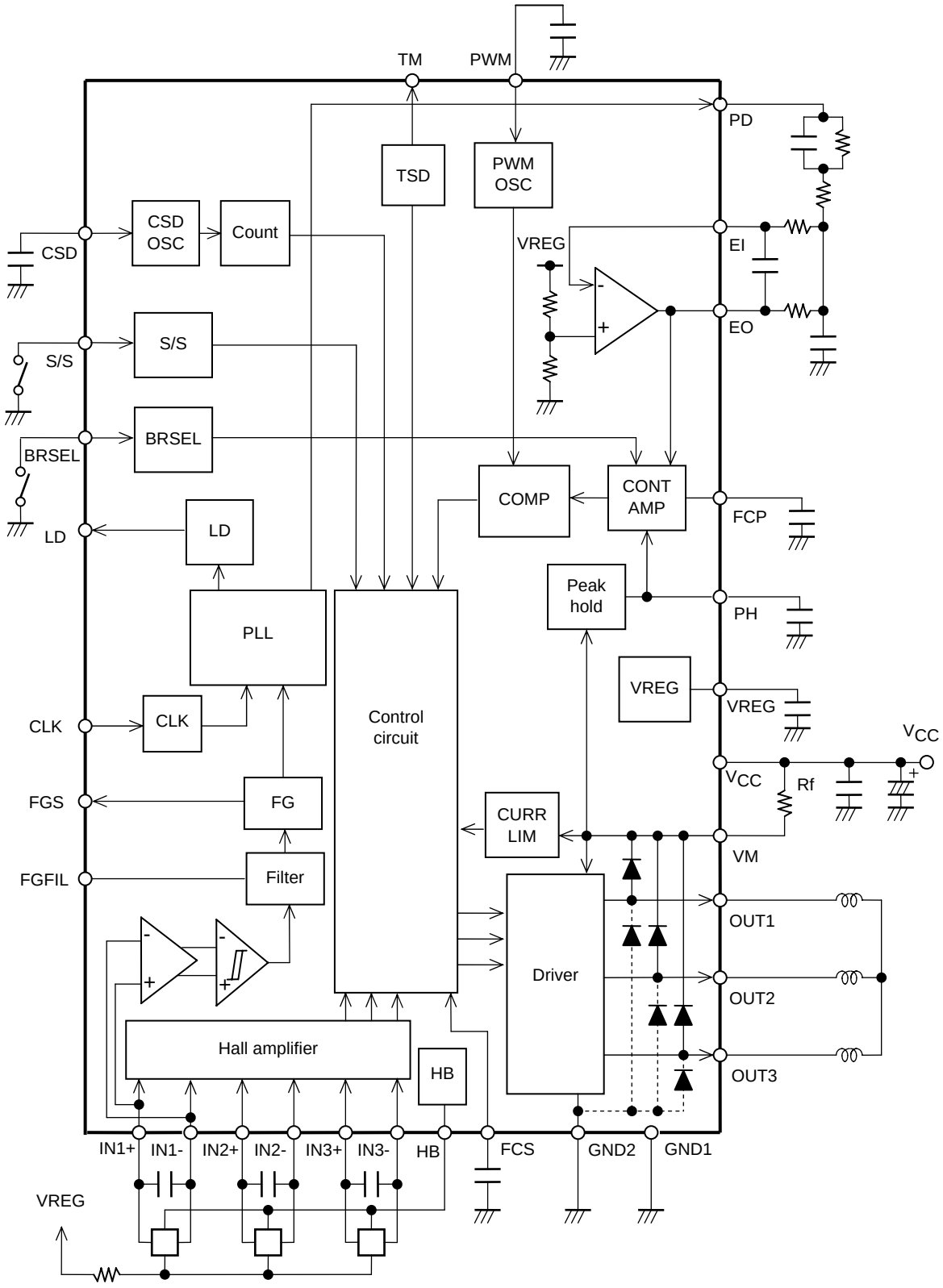
180° drive: Current flows during all periods; there are on off periods (180° drive)

(2) When the Hall sensor input amplitude is larger or when the input waveform slope is steep

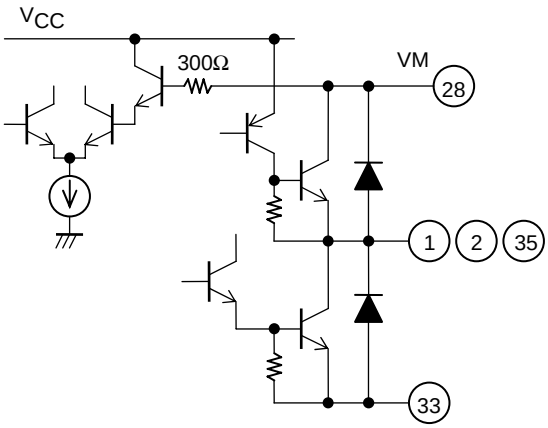
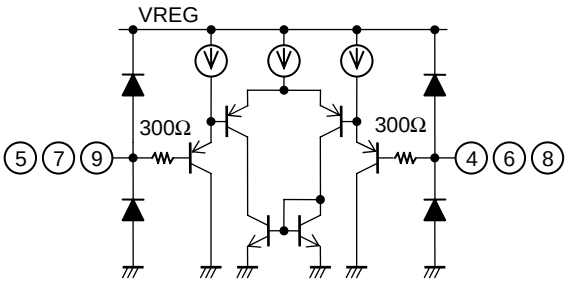
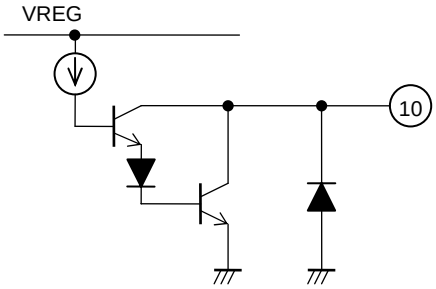
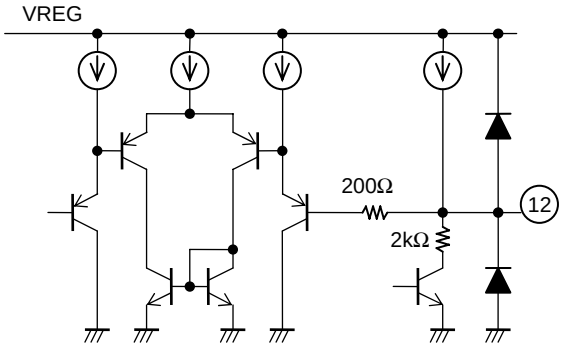


In this case, periods in which drive is off will occur (the off periods vary depending on the Hall sensor inputs).

Internal Equivalent Circuit Block Diagram and External Reference Circuit

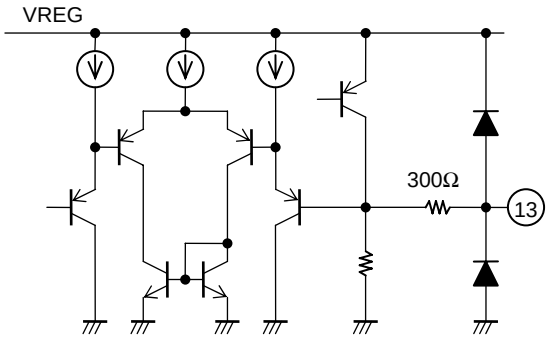
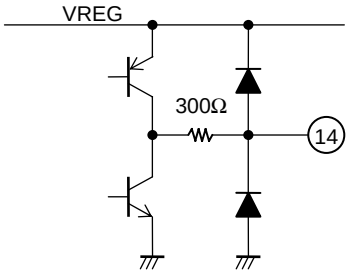
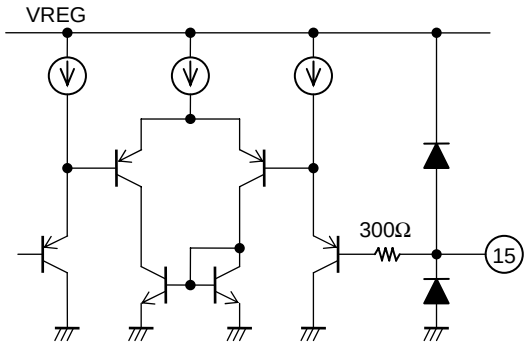
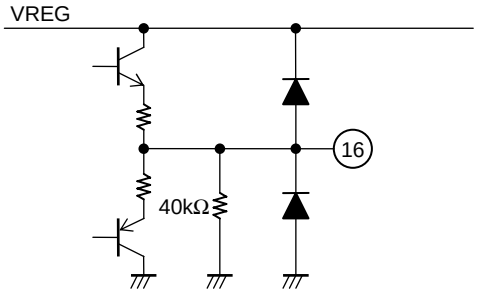
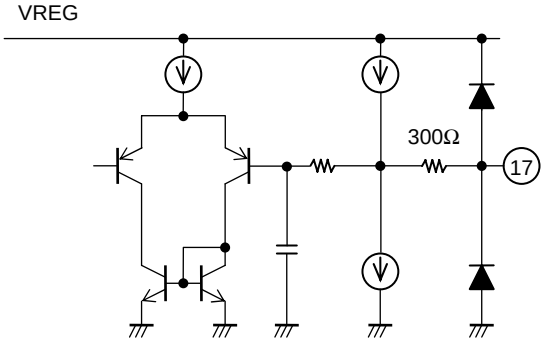


Pin Functions

Pin No.	Pin	Description	Equivalent Circuit
2 1 35	OUT1 OUT2 OUT3	Motor drive outputs	
33	GND2	Output block ground	
28	VM	Motor drive output power supply and output current detection Connect a resistor (Rf) between this pin and V_{CC}. The output current will be limited to the value I_{OUT} = VRF/Rf.	
8 9 6 7 4 5	IN1+ IN1- IN2+ IN2- IN3+ IN3-	Hall sensor inputs "H" is the state where IN+ > IN-, and "L" is the reverse state. It is desirable that the Hall sensor signals have an amplitude greater than 50 mVpp If noise on the Hall sensor signals is a problem, connect capacitors between the IN+ and IN- inputs.	
10	HB	Hall sensor element bias current This circuit is turned off in stop mode.	
11	GND1	Control circuit block ground	
12	PWM	Sets the PWM oscillator frequency. Connect a capacitor between this pin and ground. A 680pF capacitor sets the oscillator frequency to be about 34kHz.	

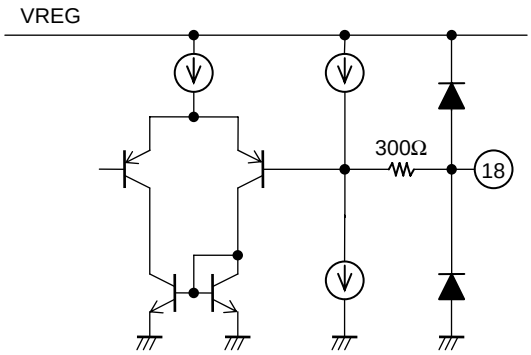
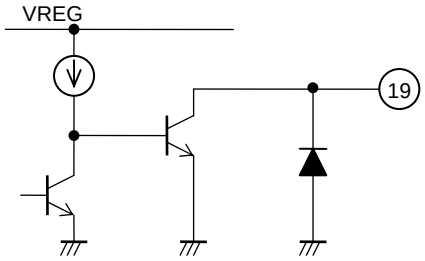
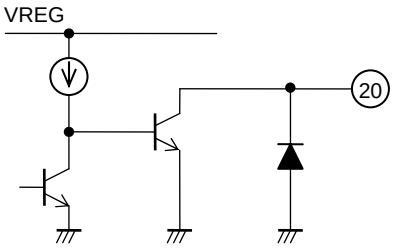
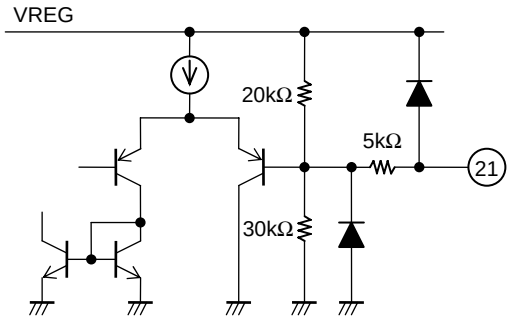
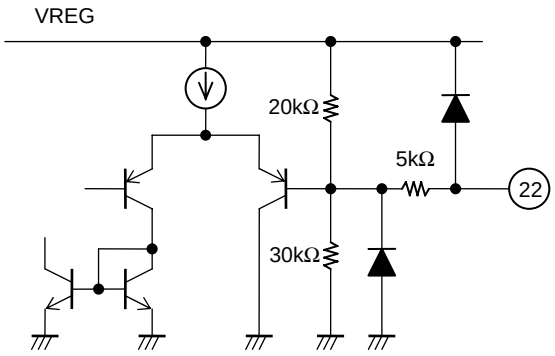
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Pin No.	Pin	Description	Equivalent Circuit
13	FCP	Current limiter circuit frequency characteristics correction Connect a capacitor (about 0.01µF to 0.1µF) between this pin and ground. The output duty is determined by comparing the voltage at this pin with the PWM oscillator waveform.	
14	PD	Phase comparator output The phase error is converted to a pulse duty and output from this pin.	
15	EI	Error amplifier input	
16	EO	Error amplifier output	
17	FGFIL	FG filter This pin is normally left open. If noise on the FG signal is a problem, connect a capacitor (about 20pF or smaller) between this pin and ground.	

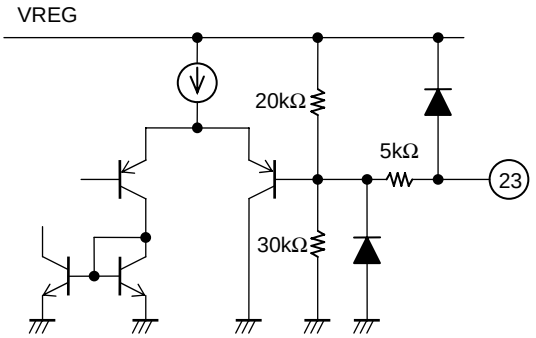
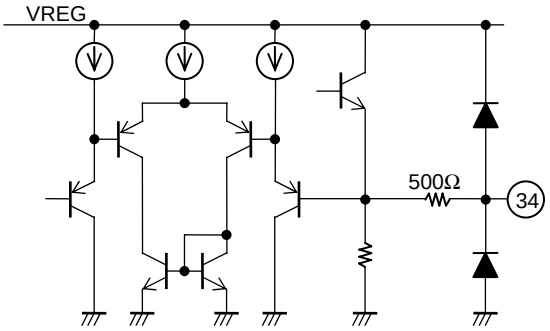
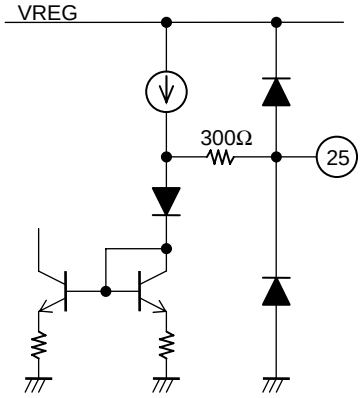
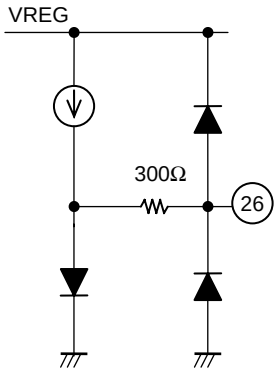
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Pin No.	Pin	Description	Equivalent Circuit
18	CSD	Initial reset pulse generation and protection circuit reference oscillator Connect a capacitor between this pin and ground.	
19	FGS	FG Schmitt trigger output	
20	LD	Phase lock detection output This output goes to the on state (low-level output) in the phase locked state.	
21	S/S	Start/stop control Low : 0V to 1.0V High : 2.0V to VREG Hysteresis : about 0.25V This pin goes to the high level when open. A low level specifies the start state.	
22	CLK	Clock input Low : 0V to 1.0V High : 2.0V to VREG Hysteresis : about 0.25V f_{CLK} = 10kHz max. If there is noise on this signal, insert a noise rejection capacitor at this input.	

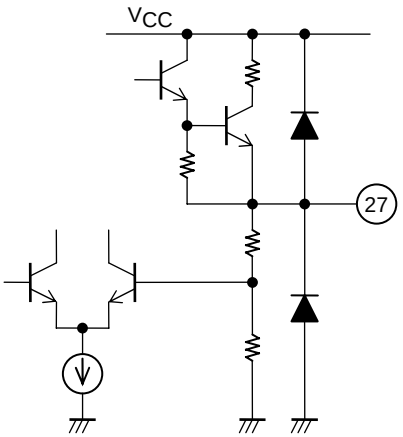
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Pin No.	Pin	Description	Equivalent Circuit
23	BRSEL	Deceleration (braking) control selection Low : 0V to 1.0V High : 2.0V to VREG This pin goes to the high level when open. A low level selects reverse torque control and a high level selects free running braking. If reverse torque control is used, an external Schottky barrier diode will be required on the low side of the output.	
24	PH	RF waveform smooth Connect a capacitor between this pin and ground.	
25	FCS	Control loop frequency characteristics correction Connect a capacitor between this pin and ground.	
26	TM	Monitor output This pin is normally left open.	

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Pin No.	Pin	Description	Equivalent Circuit
27	VREG	Stabilized power supply output (5V output) Connect a capacitor between this pin and ground for power supply stabilization. (About 0.1μF)	
29	V_{CC}	Power supply. Connect a capacitor (a few tens of μF or larger) between this pin and ground so that noise does not enter the IC.	
3, 30 31, 32 34, 36	NC	Since this pin is not connected internally to the chip, it can be used for wiring connections.	
	FRAME	Connect this pin to ground.	

LB11873 Overview

1. Speed control circuit

Since the LB11873 adopts PLL speed control, it provides precise, low-jitter, and stable motor operation. This PLL circuit compares the falling edge of the CLK signal with the FG signal (edges on which the IN1 input changes from low to high and FGS output rising edges) and controls motor operation based on the difference.

During control operation, the FG servo frequency is the same as the CLK signal frequency.

$$f_{FG}\ (\text{servo}) = f_{CLK}$$

2. Output drive circuit

This IC minimizes motor vibration and noise by changing the output current smoothly during phase switching. Since the change (slope) imposed on the output current during phase switching uses the slope of the Hall sensor input waveform, the changes in the output waveforms at phase switching will become too steep if the Hall sensor input waveform slope is steep. This will reduce the noise and vibration reducing effect of this technique. Thus care is required concerning the slope of the Hall sensor input waveform.

Low side output transistor PWM switching is used for motor speed control and the drive output is adjusted by changing the duty. The diode between OUT and VM used for the regenerative current when the PWM is off is built into this IC. Due to the parasitic diode between OUT and ground, if reverse control mode (torque braking) is selected for braking, an external Schottky barrier diode must be used. Also, if there are problems when the output current is large (for example, incorrect operation or waveform disruption during low side kickback) a Schottky barrier diode must be connected between OUT and ground.

Note that if it is necessary to reduce IC thermal dissipation during constant-speed operation, it may be effective to insert a Schottky barrier diode between OUT and VM. This effect occurs because the regenerative current during PWM switching will be dissipated in the external diode instead of the IC's internal diode.

3. Current limiter circuit

The current limiter circuit limits the drive current to a current determined by the equation I = VRF/RF, where VRF = 0.5V (typical) and Rf is the current detection resistor. The limiting operation works by reducing other output on duty to suppress the drive current.

The current limiter circuit detects the reverse recovery current due to PWM operation and, to assure that the current limiting operation is not performed incorrectly, provides a delay of about 2μs before it operates. Since the changes in the current levels at startup (the state where there is no counterelectromotive force from the motor) will be rapid if either the motor coil resistance is low or if the inductance is low, there are cases where current limiter will operates at a current level above that set due to this delay. In these cases, it will be necessary to take the amount of current increase due to the delay into account when setting the current limit value.

4. Power saving circuit

This IC goes into a power saving state in which current drain is reduced when set to the stop state. This power saving state is implemented by cutting the bias current to most of the circuits in the IC. The 5V regulator output, however, is still output when the IC is in the power saving state.

5. Reference clock

Care must be taken to assure that no noise due to chattering or other problems appears on the externally input clock signal. While the input circuit is designed with hysteresis, noise must be rejected by, for example, inserting capacitors in the clock line if noise problems occur.

The LB11873 provides a built-in clock disconnection protection circuit. At clock frequencies lower than the frequency determined by the following equation, the LB11873 will not perform its normal control operation, but rather will operate in an intermittent mode.

$f\ (Hz) \approx 1.02 \div CCSD$ CCSD (μF) : the capacitor connected between the CSD pin and ground.

If a 0.033μF capacitor is used, the frequency will be about 31Hz.

If the IC is set to the start state with absolutely no clock signal provided, the motor will first start to turn somewhat and then the drive will be turned off.

If motor rotation stops, a time in excess of the constraint protection operating time elapses, and then the clock signal is applied again, drive operation will not be restarted. However, if the clock signal is reapplied before the constraint protection circuit operates, drive operation will restart.

6. PWM frequency

The PWM frequency is determined by the capacitance of the capacitor (C) connected to the PWM pin.

$f_{PWM} \approx 1/(43000 \times C)$

If a 680pF capacitor is used, the circuit will oscillate at about 34kHz. If the PWM frequency is too low the motor will emit switching noise, and if it is too high the power loss in the output will increase. A frequency in the range 15kHz to 50kHz is desirable. This capacitor must be connected between this pin and the GND pin by lines that are as short as possible to make this circuit immune to noise.

The capacitor ground side must be connected as close as possible to the IC control block ground (the GND1 pin), to minimize the influence of the output.

7. Hall sensor input signals

The Hall sensor input signals must have an amplitude (differential) of over 50mVpp. If disruption of the output waveforms occurs due to noise on these signals, capacitors must be connected between the Hall sensor inputs (between the + and - sides).

8. FCS pin

The capacitor (about 0.1μF) connected to the FC pin is required for correction of the control loop frequency characteristics.

9. Constraint protection circuit

The LB11873 includes a built-in constraint protection circuit to protect the IC and the motor if the motor is physically constrained from turning.

If FG signal (one side edge of IN1) does not switch states for a period in excess of a certain fixed time in the start state, the PWM drive side output is turned off.

The time is set by the capacitor connected to the CSD pin.

Set time (seconds) $\approx 30.5 \times 0.98 \times$ CCSD (μF)

If a 0.033μF capacitor is used, the protection operation time will be about 0.99 seconds.

The constraint protection state can be cleared by either switching to the stop state (and remaining for over 100μs) or turning the power off and then on again. Note that the constraint protection circuit may not operate correctly if there is noise on the FG signal when the motor is physically constrained.

10. Phase lock signal

(1) Phase lock range

Since this IC does not have a speed system counter, the speed error range in the phase locked state cannot be determined by the IC characteristics alone. (This is because the range is affected by the acceleration with changes in the FG frequency.) If it is necessary to stipulate this in conjunction with a motor, it will be necessary to measure the range with the actual motor state. Since speed errors occur easily in states where the FG acceleration is large, it is thought that the lock pull-in time at startup and the unlock time due to clock switching will be the cases where the speed error is the largest.

(2) Phase lock signal mask function

It is possible to assure that the lock signal is output in stable states by masking the short-term low levels due to hunting during lock pull-in. Note, however, that the lock signal output will be delayed by the amount of the mask time.

The mask time is set by the capacitor connected between the CLD pin and ground.

$$\text{Mask time (s)} \approx 6.5 \times 0.98 \times \text{CCSD } (\mu\text{F})$$

When a 0.033μF capacitor is used, the mask time will be about 210ms. If full masking is required, the mask time must be set with an adequate margin.

11. Initial reset

To apply an initial reset to the logic circuit, the IC goes to the reset state until the CSD pin voltage changes from 0V to about 0.63V. After the reset is cleared, drive will start. The reset time can be calculated quite closely with the following equation.

$$\text{Reset time (s)} \approx 0.13 \times \text{CCSD } (\mu\text{F})$$

A reset time of over 100μs is required.

12. Power supply stabilization

Since this IC is used in switching drive applications with large output currents, the power supply line is easily disrupted.

Therefore it is necessary to connect an adequately large capacitor between the V_{CC} pin and ground.

The capacitor ground side is connected to the GND2 pin, which is the power system ground, and must be connected as close as possible to the pin.

If the capacitor (an electrolytic capacitor) cannot be connected close to the pin, a ceramic capacitor of about 0.1μF must be connected close to the pin.

If reverse control mode (torque braking) is selected for braking, since there will be states where the current returns to the power supply, the power supply line level will be especially subject to disruption. Since the power supply line is most easily disrupted during lock pull-in at high speeds, designers must analyze this case carefully and select an adequately large capacitor.

Since the power supply line is particularly susceptible to disruption if a diode is inserted in the power supply line to prevent destruction of the IC by reverse connection, an even larger capacitor must be selected in this case.

13. VREG stabilization

Connect a capacitor with a value over 0.1μF to stabilize the VREG voltage, which is the IC's control circuit power supply. This capacitor's ground side must be connected as close as possible to the IC's control block ground (the GND1 pin).

14. Error amplifier system components

The external components for the error amplifier block must be located as close as possible to the IC to minimize the influence of noise. These components must also be located as far from the motor as possible.

15. FRAME pin

An electrolytic capacitor must be connected between the FRAME pin and GND2 with the capacitor's ground side is connected to GND2.

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