LB11696V

Direct PWM Drive Brushless Motor Predriver IC

Monolithic Linear IC

Overview

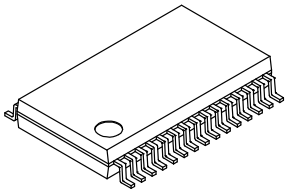
The LB11696V is a direct PWM drive predriver IC designed for three-phase power brushless motors. A motor driver circuit with the desired output power (voltage and current) can be implemented by adding discrete transistors in the output circuits. Furthermore, the LB11696V provides a full complement of protection circuits allowing it to easily implement high-reliability drive circuits. This device is optimal for driving all types of large-scale motors such as those used in air conditioners and on-demand water heaters.

Features

- Single-phase Full-wave Linear Drive with BTL Output (Gain Resistance 1 kΩ−360 kΩ): Most Appropriate for Consumer Appliances Power Supply, Namely Equipment that Requires Silence because this has No Switching Noise
- Three-phase Bipolar Drive
- Direct PWM Drive (Controlled either by Control Voltage or PWM Variable Duty Pulse Input)
- Built−in Forward/Reverse Switching Circuit
- Start/Stop Mode Switching Circuit (Stop Mode Power Saving Function)
- Built-in Input Amplifier
- 5 V Regulator Output (VREG Pin)
- Current Limiter Circuit (Supports 0.25 V (Typical) Reference Voltage Sensing Based High-precision Detection)
- Undervoltage Protection Circuit (The Operating Voltage can be Set with a Zener Diode)
- Automatic Recovery Type Constraint Protection Circuit with Protection Operating State Discrimination Output (RD Pin)
- Four Types of Hall Signal Pulse Outputs
- Supports Thermistor Based Thermal Protection of the Output Transistors

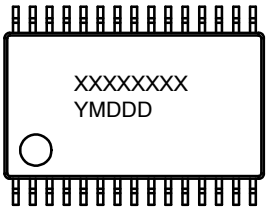
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SSOP30
CASE 565AT

MARKING DIAGRAM



XXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC} max	Supply Voltage 1	V_{CC} pin	18	V
I_O max	Output Current	UL, VL, WL, UH, VH, and WH pins	30	mA
LVS max	LVS Pin Applied Voltage	LVS pin	18	V
P_d max 1	Allowable Power Dissipation 1	Independent IC	0.45	W
P_d max 2	Allowable Power Dissipation 2	When mounted on a 114.3 × 76.1 × 1.6 mm glass epoxy board	1.05	W
T_{opr}	Operating Temperature		–20 to +100	°C
T_{stg}	Storage Temperature		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ALLOWABLE OPERATING RANGES (T_A = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}1–1	Supply Voltage Range 1–1	V_{CC} pin	8 to 17	V
V_{CC}1–2	Supply Voltage Range 1–2	V_{CC} pin, when V_{CC} is shorted to VREG	4.5 to 5.5	V
I_O	Output Current	UL, VL, WL, UH, VH, and WH pins	25	mA
IREG	5 V Constant Voltage Output Current		–30	mA
VHP	HP Pin Applied Voltage		0 to 17	V
IHP	HP Pin Output Current		0 to 15	mA
VRD	RD Pin Applied Voltage		0 to 17	V
IRD	RD Pin Output Current		0 to 15	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}1	Current Drain 1		–	12	16	mA
I_{CC}2	Current Drain 2	Stop mode	–	2.5	4	mA
5 V CONSTANT VOLTAGE OUTPUT (VREG PIN)						
VREG	Output Voltage		4.7	5.0	5.3	V
ΔVREG1	Line Regulation	V_{CC} = 8 to 17 V	–	40	100	mV
ΔVREG2	Load Regulation	I_O = –5 to –20 mA	–	10	30	mV
ΔVREG3	Temperature Coefficient	Design target value	–	0	–	mV/°C
OUTPUT BLOCK						
V_{OUT}1–1	Output Voltage 1–1	Low level, I_O = 400 μA	–	0.2	0.5	V
V_{OUT}1–2	Output Voltage 1–2	Low level, I_O = 10 mA	–	0.9	1.2	V
V_{OUT}2	Output Voltage 2	High level, I_O = –20 mA	V_{CC} – 1.1	V_{CC} – 0.9	–	V
I_O Leak	Output Leak Current		–	–	10	μA
HALL AMPLIFIER BLOCK						
IHB (HA)	Input Bias Current		–2	–0.5	–	μA
VICM1	Common-mode Input Voltage Range 1	When a Hall element is used	0.5	–	V_{CC} – 2.0	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HALL AMPLIFIER BLOCK						
VICM2	Common-mode Input Voltage Range 2	Single-sided input bias mode (when a Hall IC is used)	0	–	V_{CC}	V
	Hall Input Sensitivity		80	–	–	mVp-p
ΔVIN (HA)	Hysteresis		15	24	40	mV
VSLH (HA)	Input Voltage Low → High		5	12	20	mV
VSHL (HA)	Input Voltage High → Low		–20	–12	–5	mV
CTL AMPLIFIER						
V_{IO} (CTL)	Input Offset Voltage		–10	–	10	mV
I_B (CTL)	Input Bias Current		–1	–	1	μA
VICM	Common-mode Input Voltage Range		0	–	VREG – 1.7	V
V_{OH} (CTL)	High-level Output Voltage	ITOC = –0.2 mA	VREG – 1.2	VREG – 0.8	–	V
V_{OL} (CTL)	Low-level Output Voltage	ITOC = 0.2 mA	–	0.8	1.05	V
G (CTL)	Open-loop Gain	f (CTL) = 1 kHz	45	51	–	dB
PWM OSCILLATOR (PWM PIN)						
V_{OH} (PWM)	High-level Output Voltage		2.75	3.0	3.25	V
V_{OL} (PWM)	Low-level Output Voltage		1.2	1.35	1.5	V
ICHG	External Capacitor Charge Current	VPWM = 2.1 V	–120	–90	–65	μA
f (PWM)	Oscillator Frequency	C = 2000 pF	–	22	–	kHz
V (PWM)	Amplitude		1.4	1.6	1.9	Vp-p
TOC PIN						
VTOC1	Input Voltage 1	Output duty: 100%	2.68	3.0	3.34	V
VTOC2	Input Voltage 2	Output duty: 0%	1.2	1.35	1.5	V
VTOC1L	Input Voltage 1 Low	Design target value, when VREG = 4.7 V, 100%	2.68	2.82	2.96	V
VTOC2L	Input Voltage 2 Low	Design target value, when VREG = 4.7 V, 0%	1.23	1.29	1.34	V
VTOC1H	Input Voltage 1 High	Design target value, when VREG = 5.3 V, 100%	3.02	3.18	3.34	V
VTOC2H	Input Voltage 2 High	Design target value, when VREG = 5.3 V, 0%	1.37	1.44	1.50	V
HP PIN						
VHPL	Output Saturation Voltage	I_O = 10 mA	–	0.2	0.5	V
IHPleak	Output Leakage Current	V_O = 18 V	–	–	10	μA
CSD OSCILLATOR (CSD PIN)						
V_{OH} (CSD)	High-level Output Voltage		2.7	3.0	3.3	V
V_{OL} (CSD)	Low-level Output Voltage		0.7	1.0	1.3	V
ICHG1	External Capacitor Charge Current	VCSD = 2 V	–3.15	–2.5	–1.85	μA
ICHG2	External Capacitor Discharge Current	VCSD = 2 V	0.1	0.14	0.18	μA
RCSD	Charge/Discharge Current Ratio	(Change current) / (Discharge current)	15	18	21	times

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RD PIN						
VRDL	Low-level Output Voltage	I_O = 10 mA	–	0.2	0.5	V
I_L (RD)	Output Leakage Current	V_O = 18 V	–	–	10	μA
CURRENT LIMITER CIRCUIT (RF PIN)						
VRF	Limiter Voltage	RF−RFGND	0.225	0.25	0.275	V
UNDERVOLTAGE PROTECTION CIRCUIT (LVS PIN)						
VSDL	Operating Voltage		3.5	3.7	3.9	V
VSDH	Release Voltage		3.95	4.15	4.35	V
ΔVSD	Hysteresis		0.3	0.45	0.6	V
PWMIN PIN						
f (PI)	Input Frequency		–	–	50	kHz
V_{IH} (PI)	High-level Input Voltage		2.0	–	VREG	V
V_{IL} (PI)	Low-level Input Voltage		0	–	1.0	V
V_{IO} (PI)	Input Open Voltage		VREG – 0.5	–	VREG	V
V_{IS} (PI)	Hysteresis		0.2	0.25	0.4	V
I_{IH} (PI)	High-level Input Current	VPWMIN = VREG	−10	0	+10	μA
I_{IL} (PI)	Low-level Input Current	VPWMIN = 0 V	−130	−90	–	μA
S/S PIN						
V_{IH} (SS)	High-level Input Voltage		2.0	–	VREG	V
V_{IL} (SS)	Low-level Input Voltage		0	–	1.0	V
V_{IS} (SS)	Hysteresis		0.2	0.25	0.4	V
I_{IH} (SS)	High-level Input Current	VS/S = VREG	−10	0	+10	μA
I_{IL} (SS)	Low-level Input Current	VS/S = 0 V	−10	−1	–	μA
F/R PIN						
V_{IH} (FR)	High-level Input Voltage		2.0	–	VREG	V
V_{IL} (FR)	Low-level Input Voltage		0	–	1.0	V
V_{IO} (FR)	Input Open Voltage		VREG – 0.5	–	VREG	V
V_{IS} (FR)	Hysteresis		0.2	0.25	0.4	V
I_{IH} (FR)	High-level Input Current	VF/R = VREG	−10	0	+10	μA
I_{IL} (FR)	Low-level Input Current	VF/R = 0 V	−130	−90	–	μA
N1 PIN						
V_{IH} (N1)	High-level Input Voltage		2.0	–	VREG	V
V_{IL} (N1)	Low-level Input Voltage		0	–	1.0	V
V_{IO} (N1)	Input Open Voltage		VREG −0.5	–	VREG	V
I_{IH} (N1)	High-level Input Current	VN1 = VREG	−10	0	+10	μA
I_{IL} (N1)	Low-level Input Current	VN1 = 0 V	−130	−100	–	μA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N2 PIN						
V_{IH} (N2)	High-level Input Voltage		2.0	–	VREG	V
V_{IL} (N2)	Low-level Input Voltage		0	–	1.0	V
V_{IO} (N2)	Input Open Voltage		VREG – 0.5	–	VREG	V
I_{IH} (N2)	High-level Input Current	VN2 = VREG	–10	0	+10	μA
I_{IL} (N2)	Low-level Input Current	VN2 = 0 V	–130	–100	–	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THREE-PHASE LOGIC TRUTH TABLE ("IN = 'H'" INDICATES THE STATE WHERE IN+ > IN–)

	F/R = L			F/R = H			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	–
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

S/S PIN

Input State	State
H	Stop
L	Start

PWMIN PIN

Input State	State
High or Open	Output Off
L	Output On

N1 AND N2 PINS

Input State		HP Output
N1 Pin	N2 Pin	
L	L	Single Hall sensor period divided by 2
L	High or Open	Single Hall sensor period
High or Open	L	Three Hall sensor synthesized period divided by 2
High or Open	High or Open	Three Hall sensor synthesized period

Since the S/S pin does not have at internal pull-up resistor, an external pull-up resistor or equivalent is required to set the IC to the stop state. If either the S/S or PWMIN pins are not used, th unused pin input must be set to the low-level voltage.

The HP output can be selected (by the N1 an N2 settings) to be one of the following four functions: the IN1 Hall input converted to a pulsed output (one-Hall output), the one-Hall output divided by two, the three-phase output synthesized from the Hall inputs (three-Hall synthesized output) or the three-Hall synthesized output divided by two.

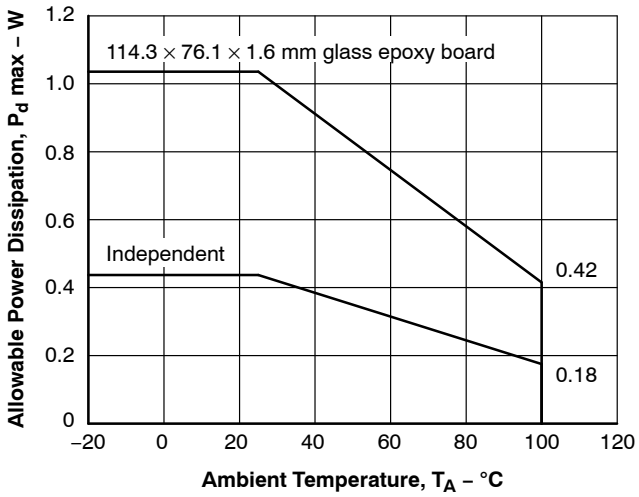


Figure 1. P_d max – T_A

PIN ASSIGNMENT

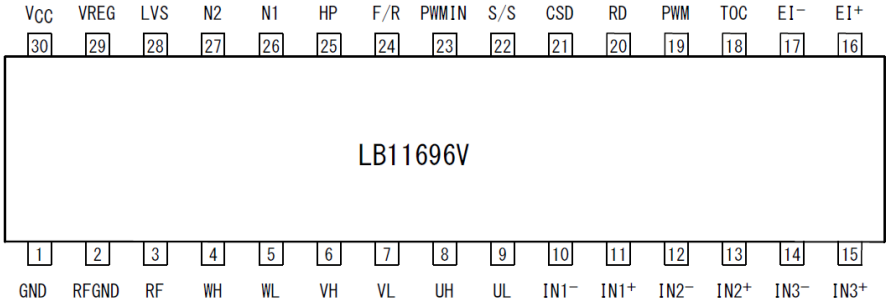
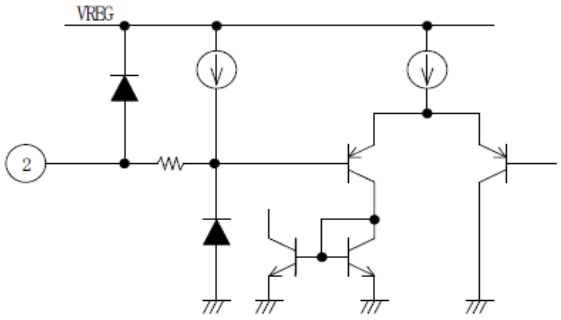
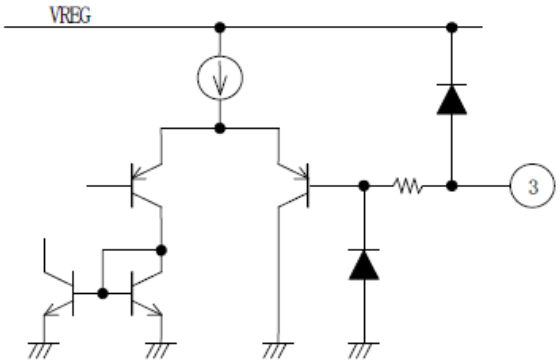
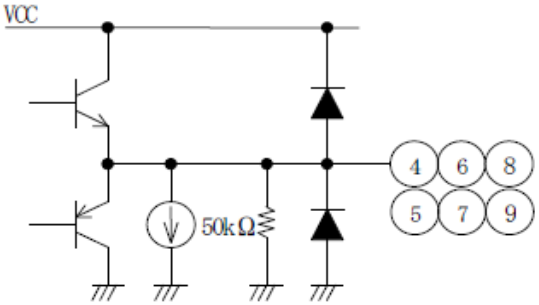
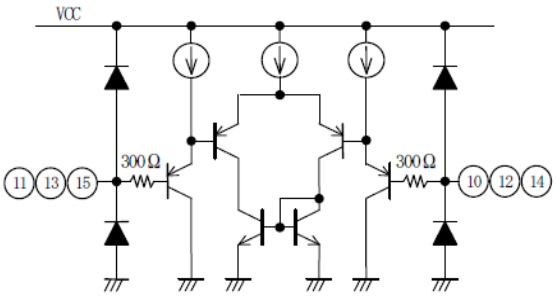
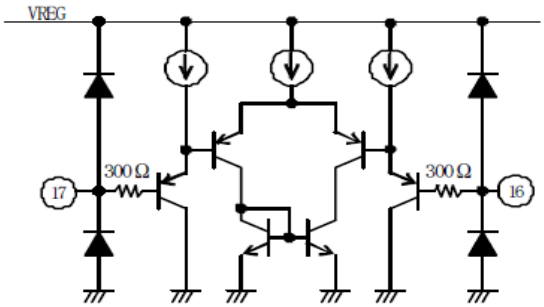


Figure 2. Pin Assignment

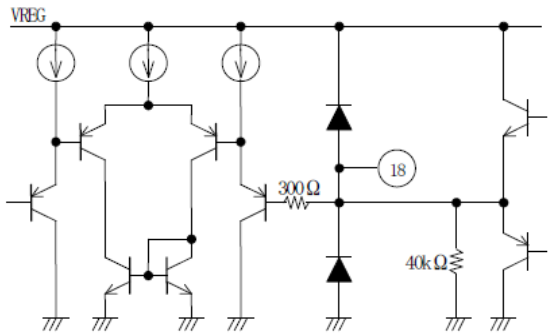
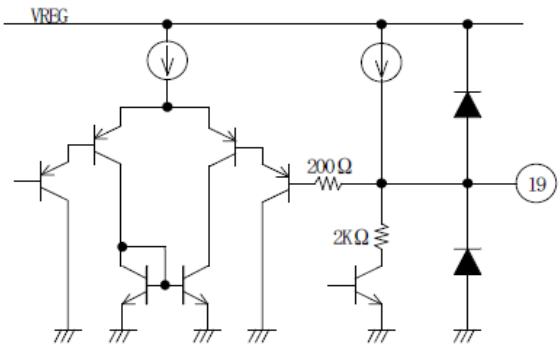
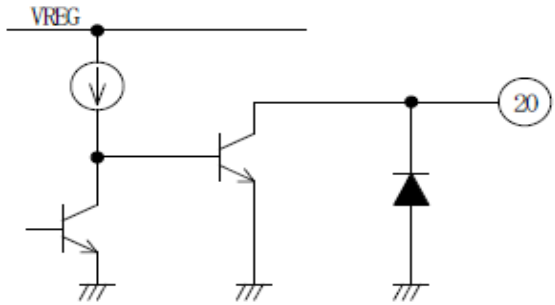
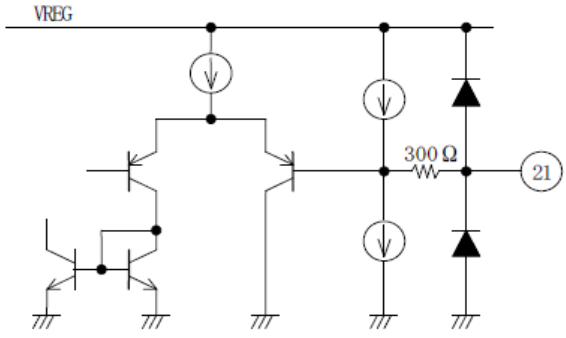
PIN FUNCTIONS

Pin No.	Pin Name	Equivalent Circuit	Description
1	GND		Ground pin.
2	RF GND		GND of output current detection, RF pin. Connect to GND of external RF resistor.

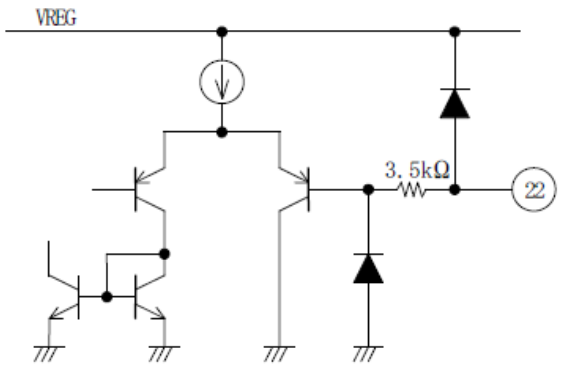
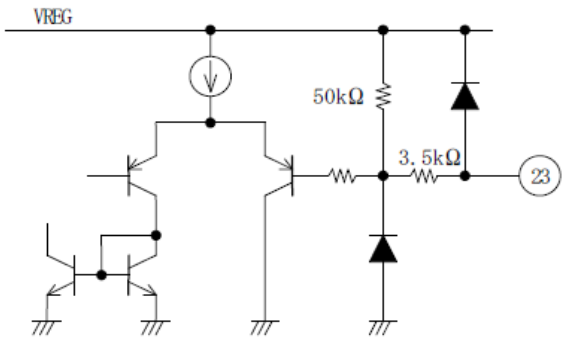
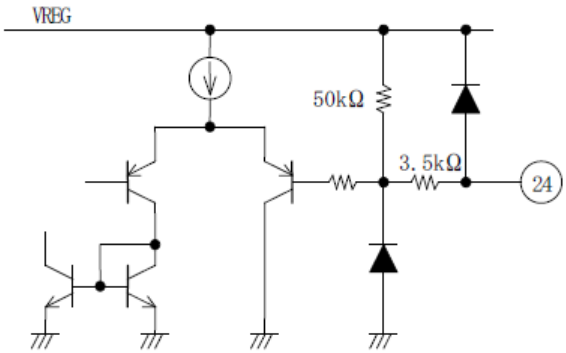
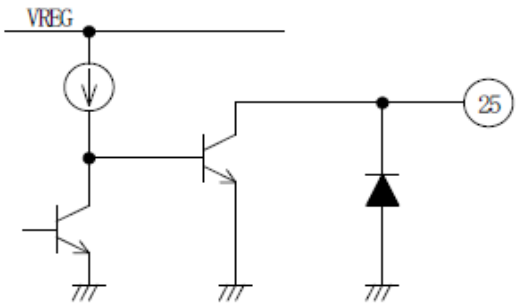
PIN FUNCTIONS (continued)

Pin No.	Pin Name	Equivalent Circuit	Description
3	RF		Output current detection. Implement small resistor between RF pin and RFGND. Set I_{OUT} = 0.25/Rf as a maximum current.
4 6 8 5 7 9	WH VH UH WL VL UL		Outputs (active by external Tr). UH, VH, WH control the duty.
10 11 12 13 14 15	IN1− NI1+ IN2− IN2+ IN3− IN3+		Hall signal input pin. The state is “High” in IN+ > IN− and the state is “Low” in opposite mode. If the Hall signal noise is problem, put the capacitor between IN+ and IN−.
16 17	EI+ EI−		CTL amplifier. The PWMIN pin must be held at the “Low” to use this input for motor control.

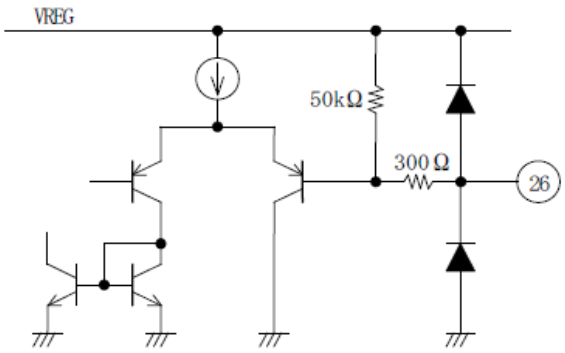
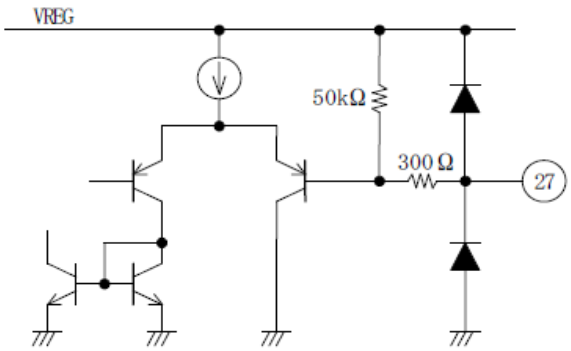
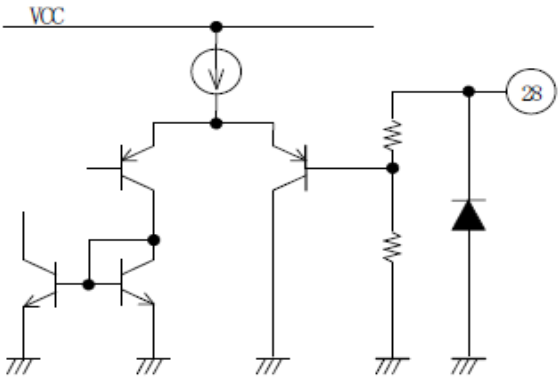
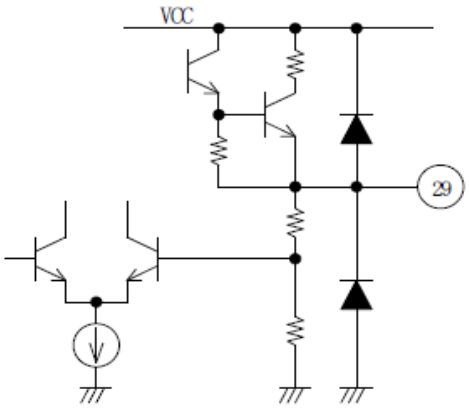
PIN FUNCTIONS (continued)

Pin No.	Pin Name	Equivalent Circuit	Description
18	TOC		CTL amplifier output. When TOC voltage rises up, the PWM duty of UH, VH, WH is changed and the torque force rises up.
19	PWM		The PWM oscillator frequency setting and the initial reset pulse setting pin. Connect a capacitor between this pin and GND. If C = 2000 pF, PWM set to about 22 kHz.
20	RD		Lock (motor constrained) detection state output. This output is turned on when the motor is turning and off when the lock protection function detects the motor stop.
21	CSD		Sets the operating time for the lock protection circuit. Connect a capacitor between this pin and GND. Connect this pin to GND if the lock protection function is not used.

PIN FUNCTIONS (continued)

Pin No.	Pin Name	Equivalent Circuit	Description
22	S/S		Start/Stop input pin. “L” = start, “H” = stop.
23	PWM IN		PWM pulse input pin. This pin is “Low”, the output goes to the drive state, and this pin is “High” or “OPEN”, the output is off state. To use this pin for the control, it is required that the CTL amplifier inputs to make the TOC pin voltage 100% duty state.
24	F/R		Forward/reverse control input.
25	HP		Hall signal output (HP output). Open collector type. This provides 4 output mode by the N1 and N2 settings.

PIN FUNCTIONS (continued)

Pin No.	Pin Name	Equivalent Circuit	Description
26	N1		Hall signal output (HP output) selection pin.
27	N2		Hall signal output (HP output) selection pin.
28	LVS		Low voltage protection detection. If the detection voltage is over 5 V, connect the Zener diode to VCC in series and adjust the detection voltage properly.
29	VREG		5 V regulator output used as the control circuit power supply. Connect a capacitor between this pin and GND for 5 V output stabilization (about 0.1 μF).
30	VCC		Power supply. Connect a capacitor between this pin and GND for VCC stabilization.

Hall Sensor Signal Input/Output Timing Chart

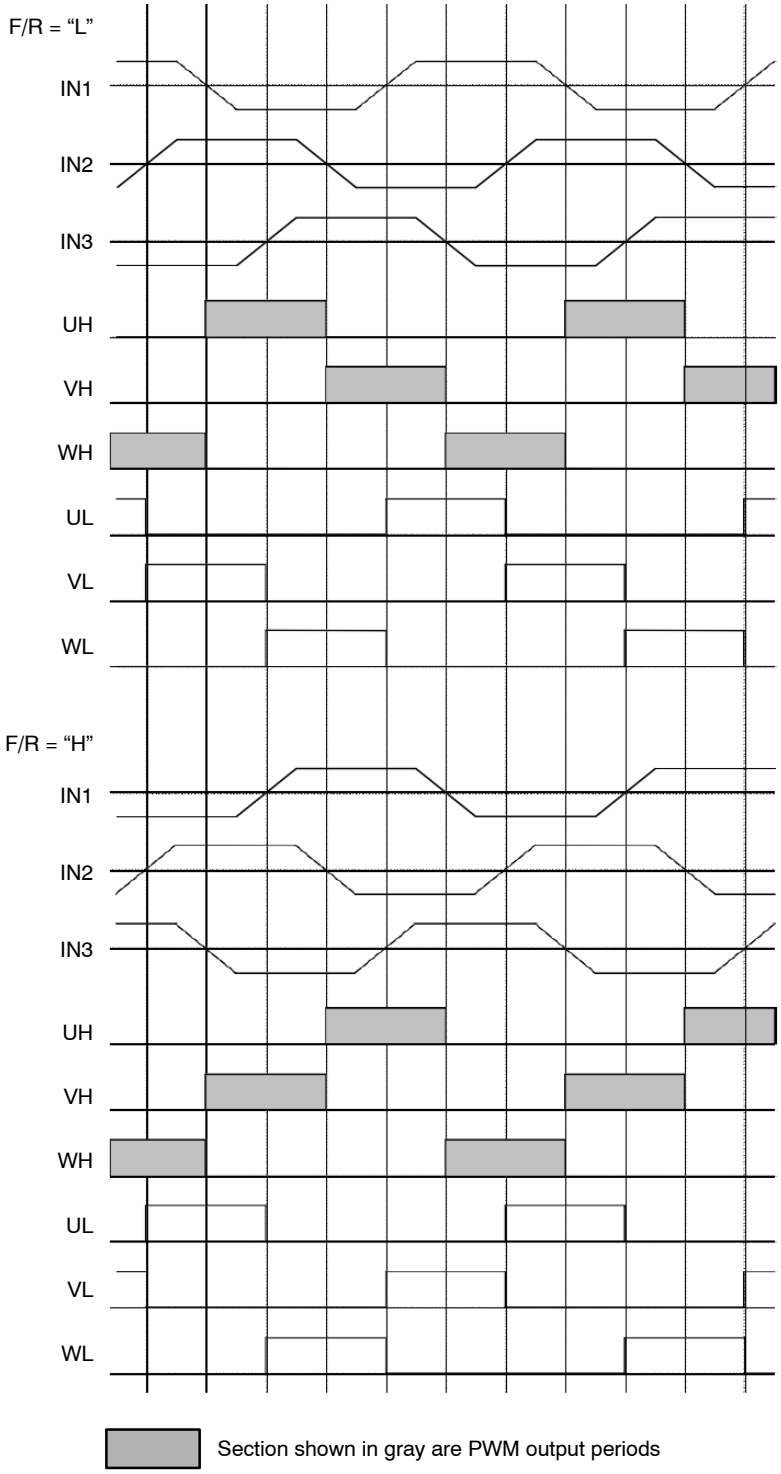


Figure 3. Hall Sensor Signal Input/Output Timing Chart

BLOCK DIAGRAM AND APPLICATION EXAMPLE 1

Bipolar transistor drive (high side PWM) using a 5 V power supply.

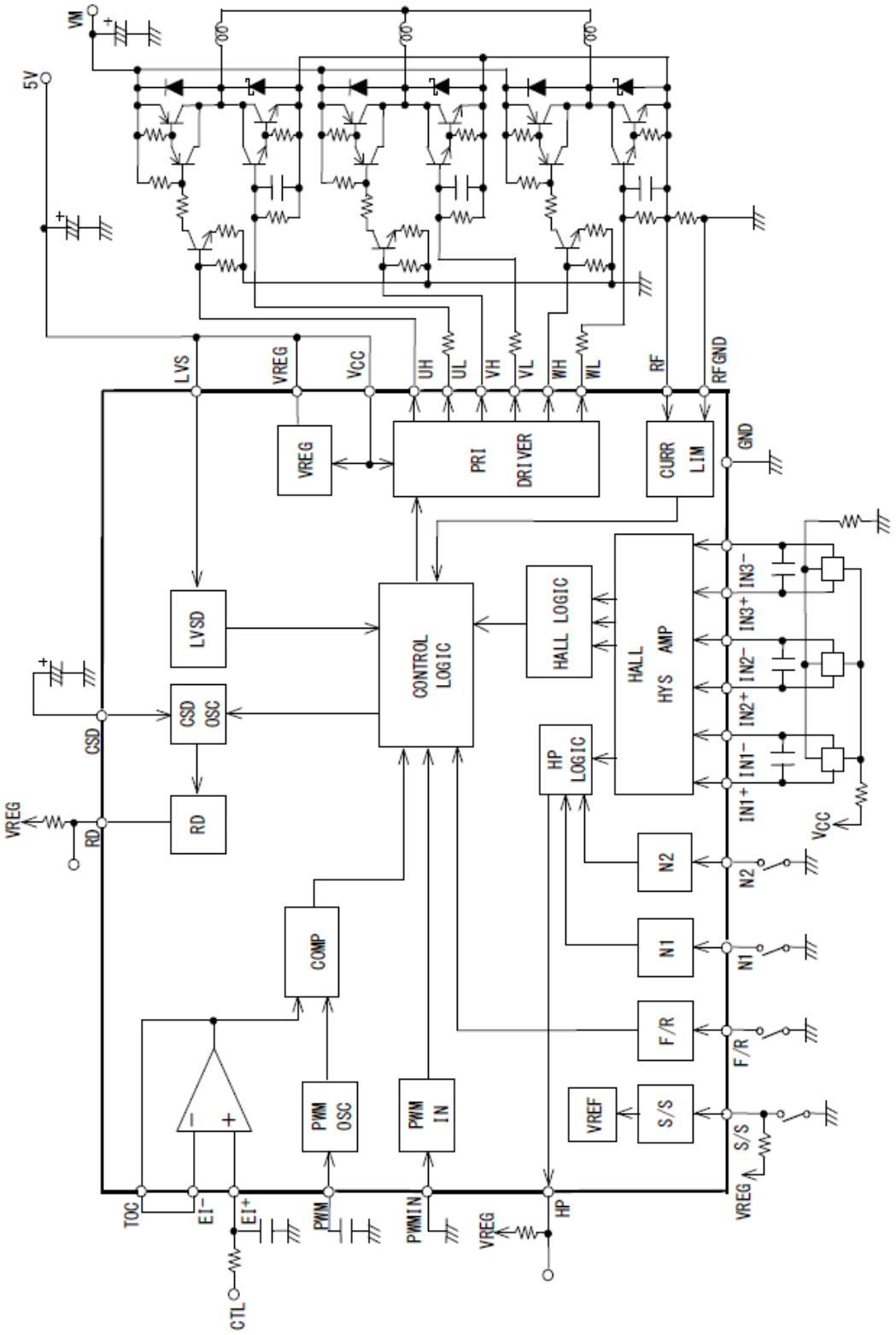


Figure 4. Application Example 1

APPLICATION EXAMPLE 2

MOS transistor drive (low side PWM) using a 12 V single-voltage power supply.

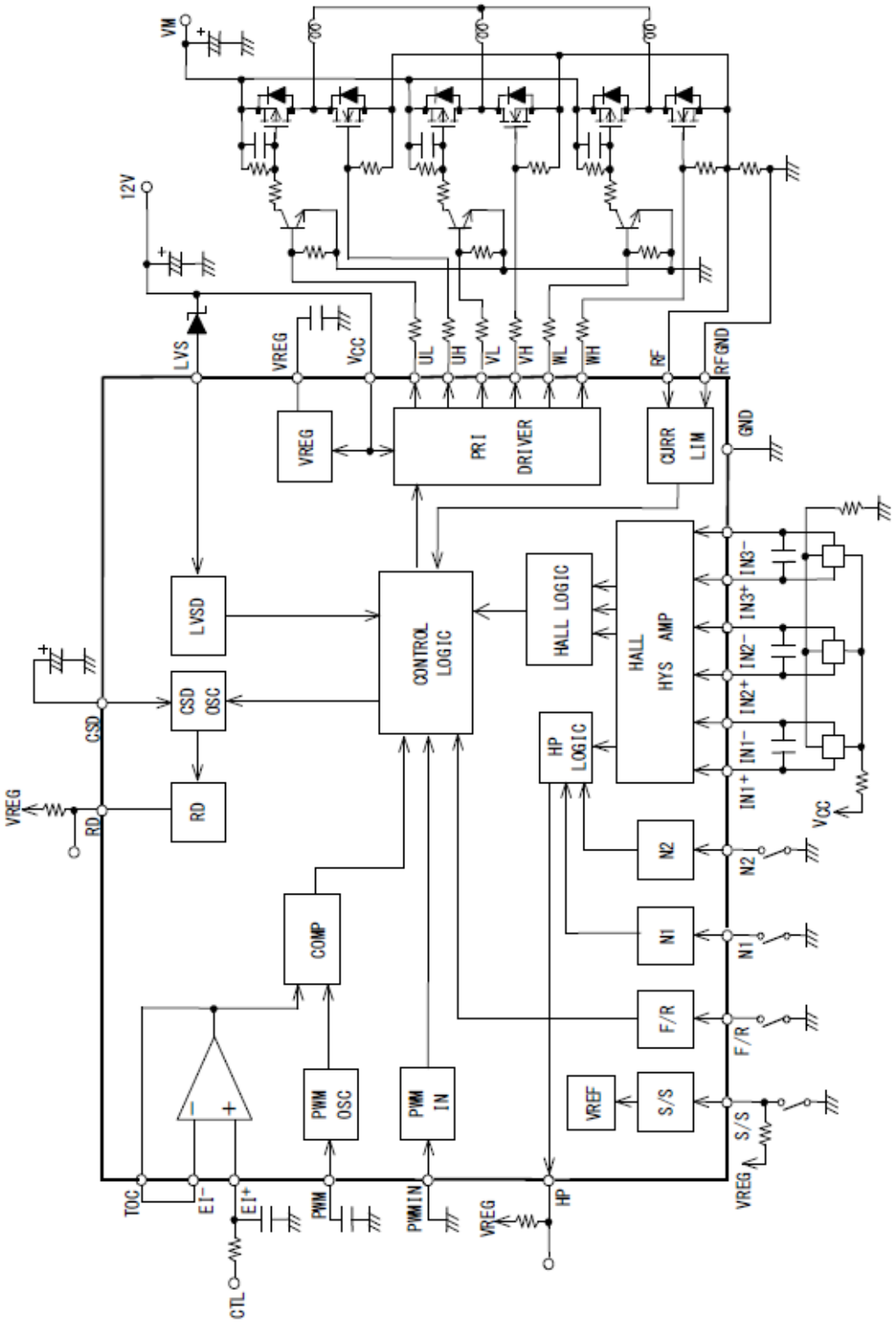


Figure 5. Application Example 2

APPLICATION EXAMPLE 3

N MOS transistor drive (low side PWM) using a V_{CC} = 12 V and Thermistor.

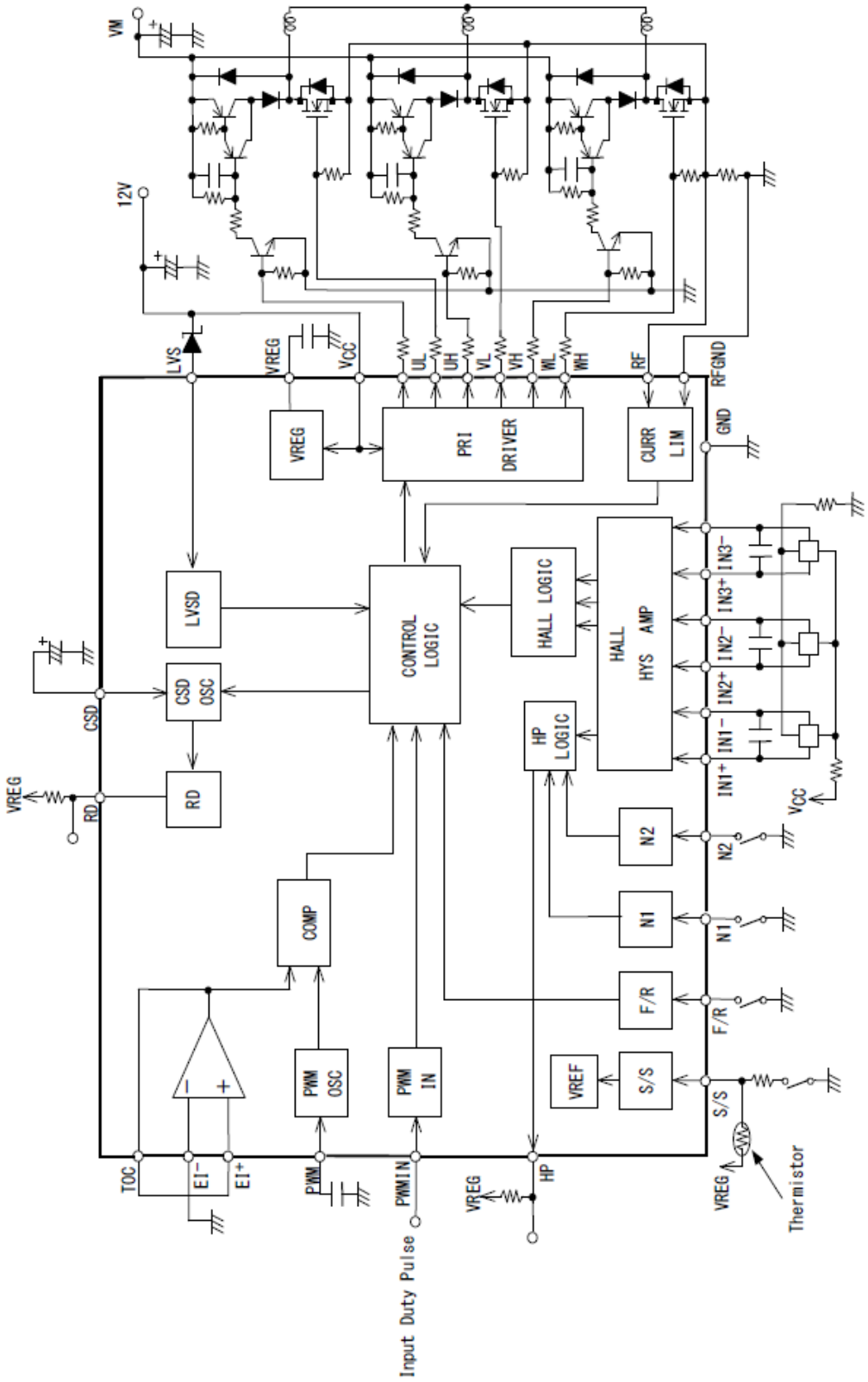
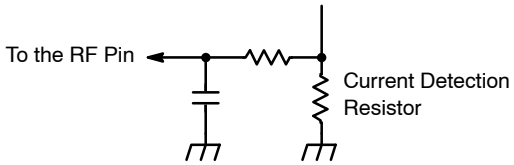


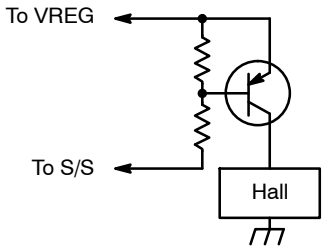
Figure 6. Application Example 3

LB11696V FUNCTIONAL DESCRIPTION

1. Output Drive Circuit:
   The LB11696V adopts direct PWM drive to minimize power loss in the outputs. The output transistors are always saturated when on, and the motor drive power is adjusted by changing the on duty of the output. The output PWM switching is performed on the UH, VH, and WH outputs. Since the UL to WL and UH to WH outputs have the same output form, applications can select either low side PWM or high side PWM drive by changing the way the external output transistors are connected. Since the reverse recovery time of the diodes connected to the non-PWM side of the outputs is a problem, these devices must be selected with care. (This is because through currents will flow at the instant the PWM side transistors turn on if diodes with a short reverse recovery time are not used.)
2. Current Limiter Circuit:
   The current limiter circuit limits the output current peak value to a level determined by the equation $I = V_{FR}/Rf$ (V_{RF} = 0.25 V typical, Rf: current detection resistor). This circuit suppresses the output current by reducing the output on duty.
   To get shorter the distance between Rf and RF pin and RF GND, to get the measurement more precisely.
   The current limiter circuit includes an internal filter circuit to prevent incorrect current limiter circuit operation due to detecting the output diode reverse recovery current due to PWM operation. Although there should be no problems with the internal filter circuit in normal applications, applications should add an external filter circuit (such as an RC low-pass filter) if incorrect operation occurs (if the diode reverse recovery current flows for longer than 1 μs).



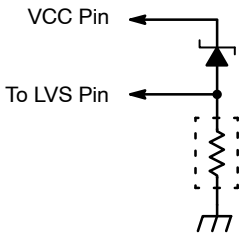
3. Power Save Circuit:
   For this IC, the state of motor stop is power save mode to decrease the power consumption. In this mode, almost all of the circuit are off, though VREG (5 V) output is active. If the bias current of Hall element should be off, connect Hall element and 5 V through PNP Tr.



4. Notes on the PWM Frequency:
   The PWM frequency is determined by the capacitor C (F) connected to the PWM pin.
   $$f_{PWM} \approx 1 / (22500 \times C)$$
   If a 2000 pF capacitor is used, the circuit will oscillate at about 22 kHz. If the PWM frequency is too low, switching noise will be audible from the motor, and if it is too high, the output power loss will increase. Thus a frequency in the range 15 kHz to 50 kHz must be used. The capacitor's ground terminal must be placed as close as possible to the IC's ground pin to minimize the influence of output noise and other noise sources.
5. Control Methods:
   The output duty can be controlled by either of the following methods:
   - Compare TOC Voltage and PWM Waveform:
     The low side output transistor duty is determined by the result of comparing the TOC pin voltage to the PWM oscillator waveform. When the TOC voltage is 1.35 V or lower, the duty is set to 0% and when the TOC voltage is 3.0 V or higher, it is set to 100%. Because the TOC pin is the output of the CTL amplifier, it is not able to input the control voltage into it. Hence, CTL amplifier is used as an all feedback amplifier (connect the EI^- and the TOC pin) and DC voltage should be input through the EI+ pin (the EI+ pin = the TOC pin voltage). The increase of EI+ voltage increases the output duty and when EI+ is open, the motor is in rotation. To stop the motor rotation, the pull-down register should be connected to EI+ pin.
     When the TOC pin voltage control is used, a low-level input must be applied to the PWMIN pin or that pin connected to GND.
   - Pulse Control Using the PWMIN Pin:
     A pulse signal can be input to the PWMIN pin, and the output can be controlled by the duty of that signal.
     The output is on when a low level is input to

the PWMIN pin, and off when a high level is input. When the PWMIN pin is open, the pin goes to the high level and the output is turned off. If inverted input logic is required, an external transistor (NPN) can allow it.
When controlling motor operation from the PWMIN pin, the EI^- pin must be connected to the GND and the EI+ pin must be connected to the TOC pin.
Note that since the PWM oscillator is also used as the clock for internal circuits, a capacitor (about 2000 pF) must be connected to the PWM pin even if the PWMIN pin is used for motor control.

6. Hall Input Signals:
A signal input with an amplitude in excess of the hysteresis (80 mV maximum) is required for the Hall inputs.
Considering the possibility of noise and phase displacement, an even larger amplitude is desirable.
If disruptions to the output waveforms (during phase switching) or to the HP output (Hall signal output) occur due to noise, this must be prevented by inserting capacitors across the inputs.
The constraint protection circuit uses the Hall inputs to discriminate the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required when using the constraint protection circuit.
If all three phases of the Hall input signal system go to the same input state, the outputs are all set to the off state (the UL, VL, WL, UH, VH, and WH outputs all go to the low level).
If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or – side) at a voltage within the common-mode input voltage range allows the other input side to be used as an input over the 0 V to V_{CC} range.
7. Under-voltage Protection Circuit:
The under-voltage protection monitors the LVS pin voltage and the circuit turns off the outputs (UH, VH, and WH) when the voltage falls below the minimum operation voltage (see the Electrical Characteristics). To prevent the reputation of the output on and off close to the protection threshold voltage, it has hysteresis which is 0.45 V (typical). Hence to release the protection mode, plus 0.45 V (typ.) to the operation voltage is needed.



The detection level of the protection voltage is 5 V system. If it is needed to go up the detection level, connect the Zenner diode to LVS pin in series to shift the detection voltage level. The LVS input current for the detection is about 75 μA. To increase the current of the Zenner diode to stabilize the rising voltage of it, insert the resistor between LVS pin and GND.
When the LVS pin is open, it becomes GND level and the output is off because of pull-down resistor inside the circuit. Hence, when it turns off, the voltage higher than 4.35 V should be input to LVS pin as a release voltage. The maximum ratings of LVS pin is 18 V.

8. Constraint Protection Circuit:
When the motor is physically constrained (held stopped), the CSD pin external capacitor is charged (to about 3.0 V) by a constant current of about 2.5 μA and is then discharged (to about 1.0 V) by a constant current of about 0.14 μA. This process is repeated, generating a saw-tooth waveform. The constraint protection circuit turns motor drive on and off repeatedly based on this saw-tooth waveform. (The UH, VH, and WH side outputs are turned on and off.) Motor drive is on during the period the CSD pin external capacitor is being charged from about 1.0 V to about 3.0 V, and motor drive is off during the period the CSD pin external capacitor is being discharged from about 3.0 V to about 1.0 V.
The IC and the motor are protected by this repeated drive on/off operation when the motor is physically constrained.
The motor drive on and off times are determined by the value of the connected capacitor C (in μF).
TCSD1 (drive on period) ≈ 0.8 × C (seconds)
TCSD2 (drive off period) ≈ 14.3 × C (seconds)
When a 0.47 μF capacitor is connected externally to the CSD pin, this iterated operation will have a drive on period of about 0.38 seconds and a drive

off period of about 6.7 seconds.
While the motor is turning, the discharge pulse signal (generated once for each Hall input period) that is created by combining the Hall inputs internally in the IC discharges the CSD pin external capacitor. Since the CSD pin voltage does not rise, the constraint protection circuit does not operate.
When the motor is physically constrained, the Hall inputs do not change and the discharge pulses are not generated.
As a result, the CSD pin external capacitor is charged by a constant current of 2.5 μA to about 3.0 V, at which point the constraint protection circuit operates. When the constraint on the motor is released, the constraint protection function is released.
Connect the CSD pin to ground if the constraint protection circuit is not used.

9. Forward/Reverse Direction Switching:
This IC is designed so that through currents (due to the output transistor off delay time when switching) do not flow in the output when switching directions when the motor is turning. However, if the direction is switched when the motor is turning, current levels in excess of the current limiter value may flow in the output transistors due to the motor coil resistance and the motor back EMF state when switching. Therefore, designers must consider selecting external output transistors that are not destroyed by those current levels or only switching directions after the speed has fallen below a certain speed.
10. Handling Different Power Supply Types:
When this IC is operated from an externally supplied 5 V power supply (4.5 to 5.5 V), short the V_{CC} pin to the VREG pin and connect them to the external power supply.
When this IC is operated from an externally supplied 12 V power supply (8 to 17 V), connect the V_{CC} pin to the power supply. (The VREG pin will generate a 5 V level to function as the control circuit power supply.)
11. Power Supply Stabilization:
Since this IC uses a switching drive technique, the power supply line level can be disturbed easily. Therefore capacitors with adequate capacitance to stabilize the power supply line must be inserted between V_{CC} and ground.
If diodes are inserted in the power supply lines to prevent destruction if the power supply is connected with reverse polarity, the power supply lines are even more easily disrupted, and even larger capacitors are required.
If the power supply is turned on and off by a switch, and if there is a significant distance between that switch and the stabilization capacitor, the supply voltage can be disrupted significantly by the line inductance and surge current into the capacitor. As a result, the withstand voltage of the device may be exceeded. In application such as this, the surge current must be suppressed and the voltage rise prevented by not using ceramic capacitors with a low series impedance, and by using electrolytic capacitors instead.
12. VREG Stabilization:
To stabilize the VREG voltage, which is the control circuit power supply, a 0.1 μF or larger capacitor must be inserted between the VREG pin and ground. The ground side of this capacitor must connected to the IC ground pin with a line that is as short as possible.

ORDERING INFORMATION

Device	Package	Wire Bond	Shipping† (Qty / Packing)†
LB11696V−MPB−E	SSOP30 (275mil) (Pb−Free)	Au wire	48 / Fan-Fold
LB11696V−TLM−E	SSOP30 (275mil) (Pb−Free)	Au wire	1,000 / Tape & Reel
LB11696V−TRM−E	SSOP30 (275mil) (Pb−Free)	Au wire	1,000 / Tape & Reel
LB11696V−TLM−H	SSOP30 (275mil) (Pb−Free / Halogen Free)	Au wire	1,000 / Tape & Reel
LB11696V−W−AH	SSOP30 (275mil) (Pb−Free / Halogen Free)	Cu wire	1,000 / Tape & Reel

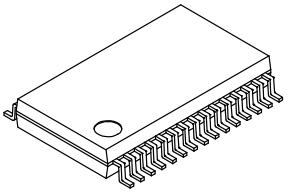
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

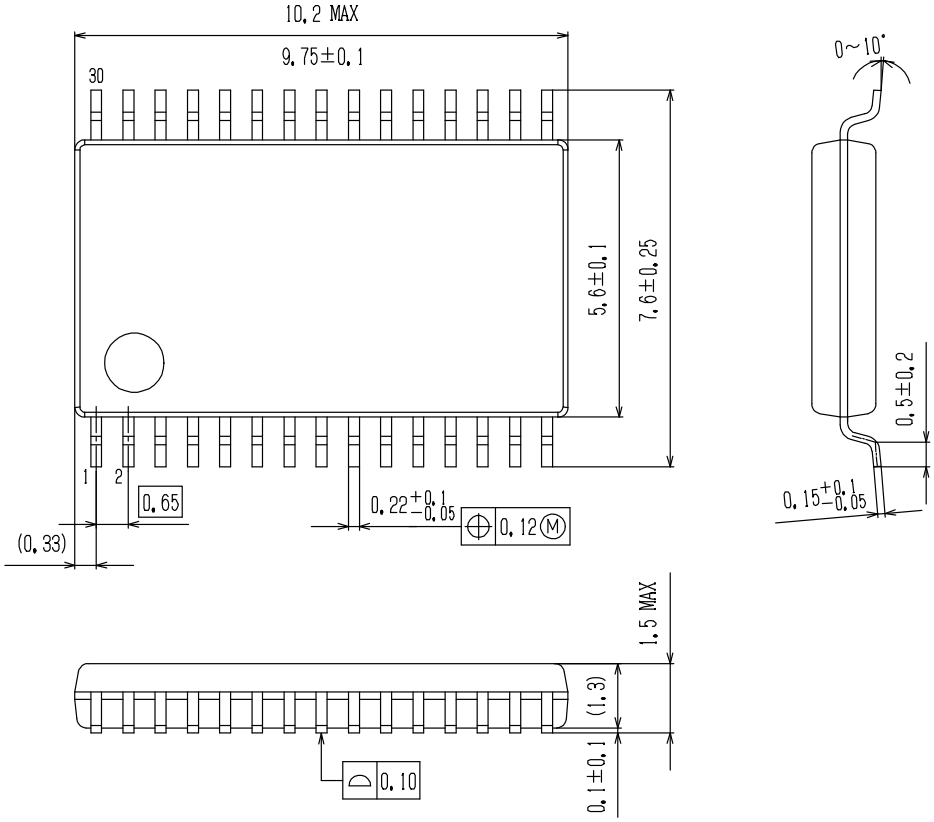
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PACKAGE DIMENSIONS

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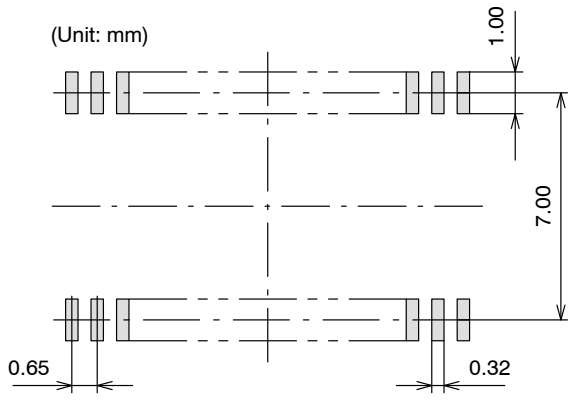
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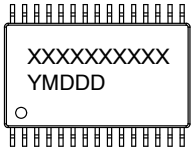




SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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