LAN91C110 REV. B

FEAST Fast Ethernet Controller for PCMCIA and Generic 16-Bit Applications

PRODUCT FEATURES

Data Brief

- Dual Speed CSMA/CD Engine (10 Mbps and 100 Mbps)
- Compliant with IEEE 802.3 100BASE-T Specification
- Supports 100BASE-TX, 100BASE-T4
- 16 Bit Wide Data Path (into Packet Buffer Memory)
- Generic 16-bit System Level Interface Easily Adaptable to ISA, PCMCIA (16-bit CardBus), and Various CPU System Interfaces
- Support for 16 and 8 Bit CPU Accesses
- Asynchronous Bus Interface
- 128 Kbyte External Memory
- Built-in Transparent Arbitration for Slave Sequential Access Architecture
- Flat MMU Architecture with Symmetric Transmit and Receive Structures and Queues
- EEE-802.3 MII (Media Independent Interface) Compliant MAC-PHY Interface Running at Nibble Rate
- MII Management Serial Interface
- EEE-802.3u Full Duplex Capability
- 144 Pin TQFP lead-free RoHS Compliant package (1.0 Millimeter Height)

ORDER NUMBER(S):

LAN91C110-PU for 144 pin, TQFP Lead-Free RoHS Compliant Package

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General Description

The LAN91C110 is designed to facilitate the implementation of second generation Fast Ethernet PC Card adapters and other non-PCI connectivity products. The LAN91C110 is a digital device that implements the Media Access Control (MAC) portion of the CSMA/CD protocol at 10 and 100 Mbps, and couples it with a lean and fast data and control path system architecture to ensure that the CPU to packet RAM data movement does not cause a bottleneck at 100 Mbps.

The LAN91C110 implements a generic 16-bit host interface which is adaptable to a wide range of system buses and CPUs. This makes the LAN91C110 ideal for 10/100 Fast Ethernet implementations in systems based on system buses other than PCI.

Total memory size is 128 Kbytes, equivalent to a total chip storage (transmit plus receive) of 64 outstanding packets. The LAN91C110 is software compatible with the LAN9000 family of products in the default mode and can use existing LAN9000 drivers (ODI, IPX, and NDIS) with minor modifications in 16 and 32 bit Intel X86 based environments.

Memory management is handled using a unique patented MMU (Memory Management Unit) architecture and an internal 32-bit wide data path. This I/O mapped architecture can sustain back-to-back frame transmission and reception for superior data throughput and optimal performance. It also dynamically allocates buffer memory in an efficient buffer utilization scheme, reducing software tasks and relieving the host CPU from performing these housekeeping functions. The total memory size is 128 Kbytes (external), equivalent to a total chip storage (transmit and receive) of 64 outstanding packets.

FEAST provides a flexible slave interface for easy connectivity with industry-standard buses. The host interface is “ISA-like” and is easily adapted to a wide range of system and CPU buses such as ISA, PCMCIA, etc.

An IEEE-802.3 compliant Media Independent Interface (MII) provided on the network side of the LAN91C110. The MII interface allows the use of a wide range of MII compliant Physical Layer (PHY) devices to be used with the LAN91C110. The LAN91C110 also provides an interface to the two-line MII serial management protocol.

Block Diagrams

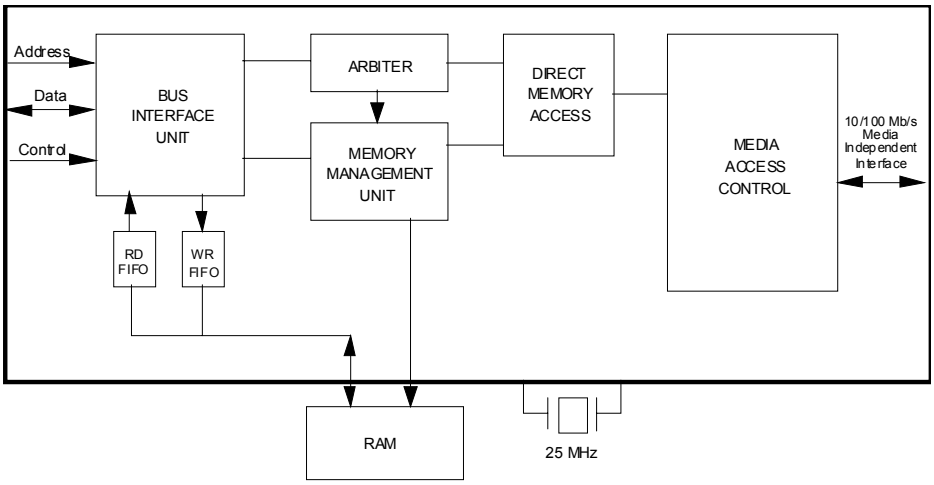


Figure 1 LAN91C110 Block Diagram

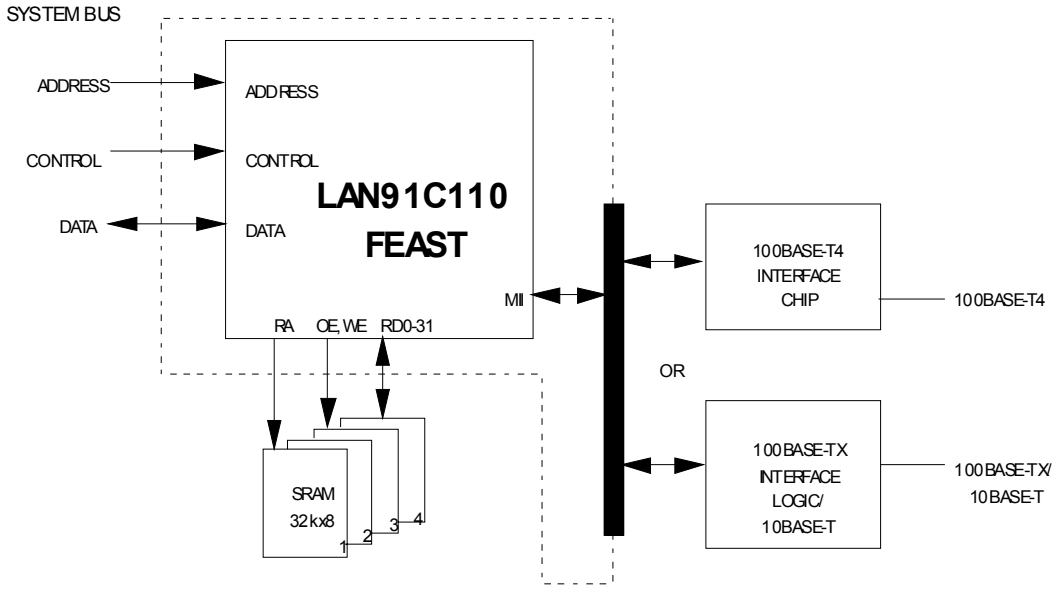


Figure 2 LAN91C110 System Diagram

PRODUCT PREVIEW

Package Outline

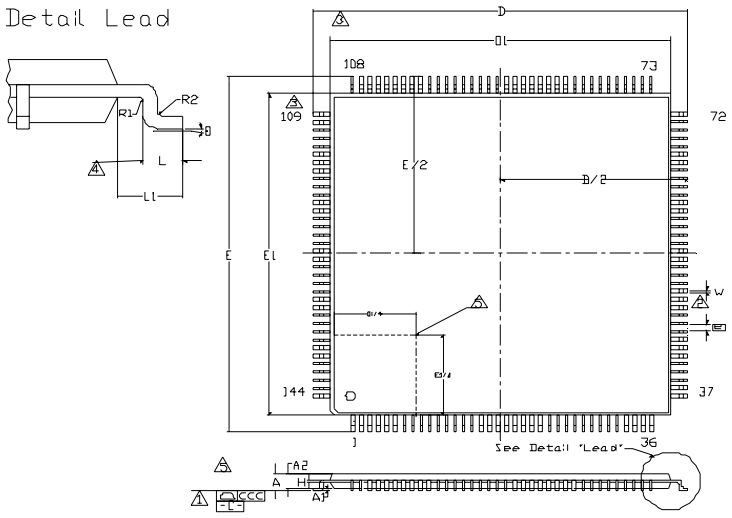


Figure 3 144 Pin TQFP Package Parameters

Table 1 144 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	1.0	1.20	Overall Package Height
A1	0.05	0.10	0.15	Standoff
A2	0.95	1.00	1.05	Body Thickness
D	21.80	22.00	22.20	X Span
D/2	10.90	11.00	11.10	$^1/_2$ X Span Measure from Centerline
D1	19.80	20.00	20.20	X body Size
E	21.80	22.00	22.20	Y Span
E/2	10.90	11.00	11.10	$^1/_2$ Y Span Measure from Centerline
E1	19.80	20.00	20.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e		0.50 Basic		Lead Pitch
?	0^o	3.5^o	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.0762	Max Coplanarity *(Assemblers)*
ccc	~	~	0.08	Max Coplanarity *(Test House)*

Note 1 Controlling Unit: millimeter

Note 2 Tolerance on the position of the leads is ± 0.04 mm maximum.

Note 3 Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion Is 0.25 mm.

Note 4 Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane is 0.78-1.08 mm.

Note 5 Details of pin 1 identifier are optional but must be located within the zone indicated.