LAN8700/LAN8700i

±15kV ESD Protected MII/RMII 10/100 Ethernet Transceiver with HP Auto-MDIX Support and flexPWR® Technology in a Small Footprint

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- ESD Protection levels of ±8kV HBM without external protection devices
- ESD protection levels of EN/IEC61000-4-2, ±8kV contact mode, and ±15kV for air discharge mode per independent test facility
- Comprehensive flexPWR® Technology
  - Flexible Power Management Architecture
- LVCMOS Variable I/O voltage range: +1.6V to +3.6V
- Integrated 3.3V to 1.8V regulator for optional single supply operation.
  - Regulator can be disabled if 1.8V system supply is available.
- Performs HP Auto-MDIX in accordance with IEEE 802.3ab specification
- Cable length greater than 150 meters
- Automatic Polarity Correction
- Latch-Up Performance Exceeds 150mA per EIA/JESD 78, Class II
- Energy Detect power-down mode
- Low Current consumption power down mode
- Low operating current consumption:
  - 39mA typical in 10BASE-T and
  - 79mA typical in 100BASE-TX mode
- Supports Auto-negotiation and Parallel Detection
- Supports the Media Independent Interface (MII) and Reduced Media Independent Interface (RMII)
- Compliant with IEEE 802.3-2005 standards
  - MII Pins tolerant to 3.6V
- IEEE 802.3-2005 compliant register functions
- Integrated DSP with Adaptive Equalizer
- Baseline Wander (BLW) Correction
- Vendor Specific register functions
- Low profile 36-pin QFN RoHS compliant package (6 x 6 x 0.9mm height)
- 4 LED status indicators
- Commercial Operating Temperature 0° C to 70° C
- Industrial Operating Temperature -40° C to 85° C version available (LAN8700i)

Applications

- Set Top Boxes
- Network Printers and Servers
- LAN on Motherboard
- 10/100 PCMCIA/CardBus Applications
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- Personal Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adaptors/Servers
- POS Terminals
- Automotive Networking
- Gaming Consoles
- Security Systems
- POE Applications
- Access Control

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1.0 GENERAL DESCRIPTION

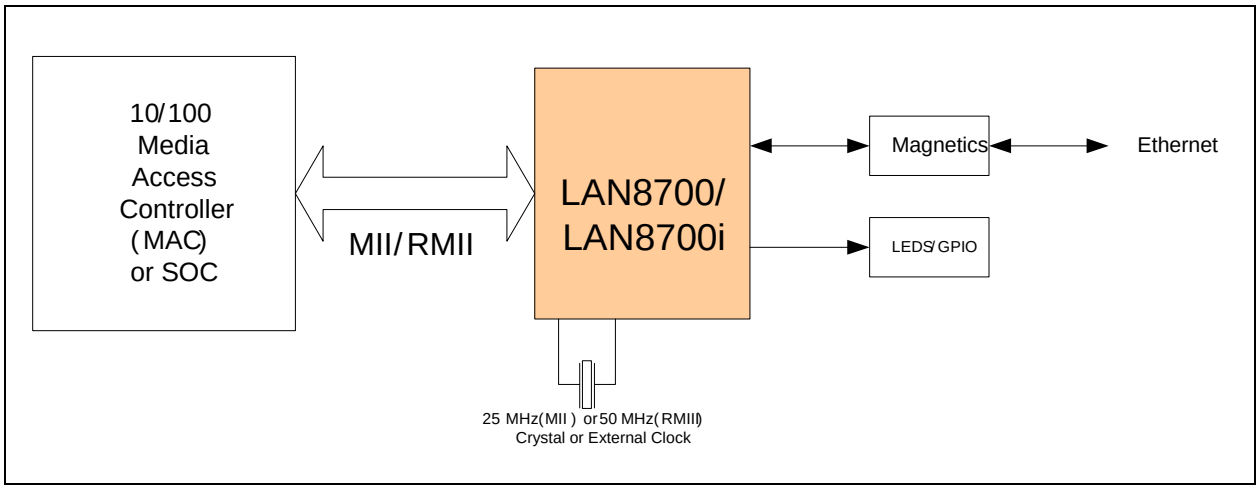
The Microchip LAN8700/LAN8700i is a low-power, industrial temperature (LAN8700i), variable I/O voltage, analog interface IC with HP Auto-MDIX support for high-performance embedded Ethernet applications. The LAN8700/LAN8700i can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.8V linear regulator. An option is available to disable the linear regulator to optimize system designs that have a 1.8V power plane available.

1.1 Architectural Overview

The LAN8700/LAN8700i consists of an encoder/decoder, scrambler/descrambler, wave-shaping transmitter, output driver, twisted-pair receiver with adaptive equalizer and baseline wander (BLW) correction, and clock and data recovery functions. The LAN8700/LAN8700i can be configured to support either the Media Independent Interface (MII) or the Reduced Media Independent Interface (RMII).

The LAN8700/LAN8700i is compliant with IEEE 802.3-2005 standards (MII Pins tolerant to 3.6V) and supports both IEEE 802.3-2005 compliant and vendor-specific register functions. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10-Mbps (10BASE-T) operation on Category 3 and Category 5 unshielded twisted-pair cable, and 100-Mbps (100BASE-TX) operation on Category 5 unshielded twisted-pair cable.

FIGURE 1-1: LAN8700/LAN8700I SYSTEM BLOCK DIAGRAM



Hubs and switches with multiple integrated MACs and external PHYs can have a large pin count due to the high number of pins needed for each MII interface. An increasing pin count causes increasing cost.

The RMII interface is intended for use on Switch based ASICs or other embedded solutions requiring minimal pincount for ethernet connectivity. RMII requires only 6 pins for each MAC to PHY interface plus one common reference clock. The MII requires 16 pins for each MAC to PHY interface.

The Microchip LAN8700/LAN8700i is capable of running in RMII mode. Please contact your Microchip sales representative for the latest RMII specification.

The LAN8700/LAN8700i referenced throughout this document applies to both the commercial temperature and industrial temperature components. The LAN8700i refers to only the industrial temperature component.

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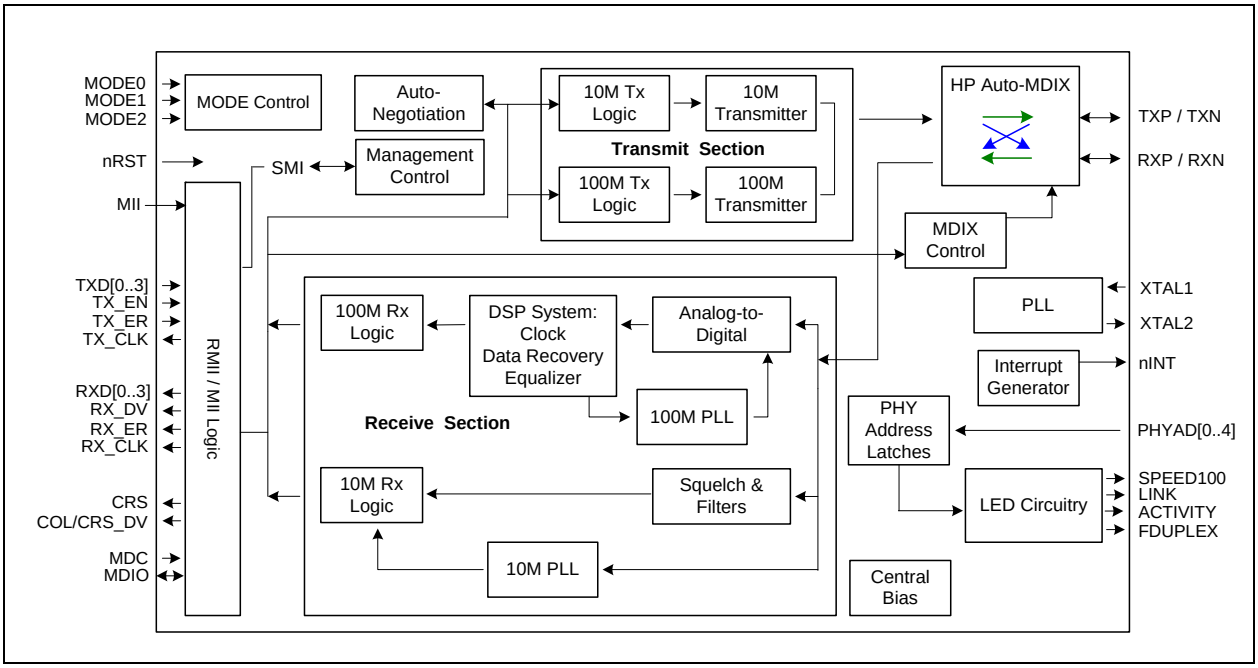
FIGURE 1-2: LAN8700/LAN8700I ARCHITECTURAL OVERVIEW



2.0 PIN CONFIGURATION

2.1 Package Pin-out Diagram and Signal Table

FIGURE 2-1: PACKAGE PINOUT (TOP VIEW)

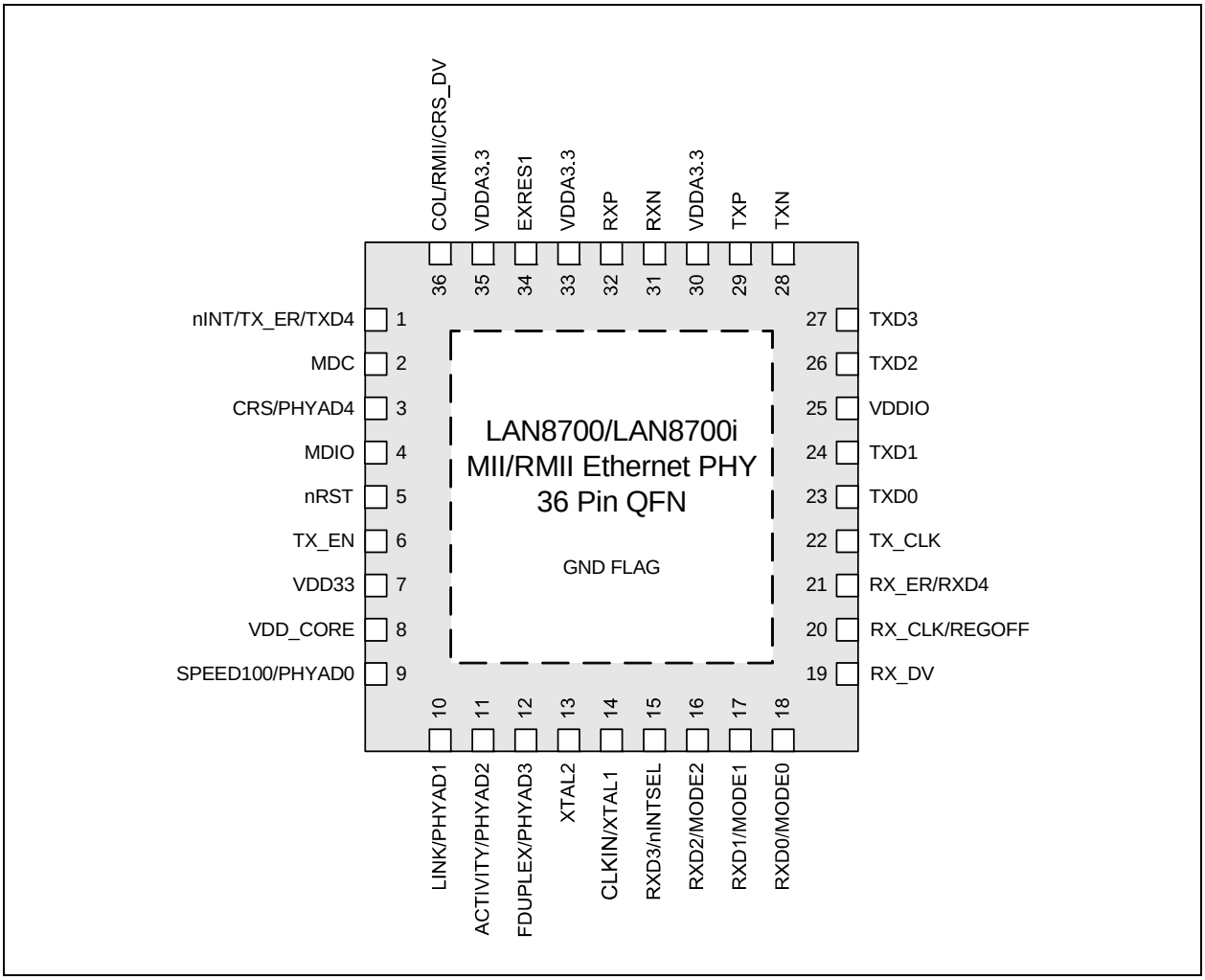


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TABLE 2-1: LAN8700/LAN8700I 36-PIN QFN PINOUT

Pin No.	Pin Name	Pin No.	Pin Name
1	nINT/TX_ER/TXD4	19	RX_DV
2	MDC	20	RX_CLK/REGOFF
3	CRS/PHYAD4	21	RX_ER/RXD4
4	MDIO	22	TXCLK
5	nRST	23	TXD0
6	TX_EN	24	TXD1
7	VDD33	25	VDDIO
8	VDD_CORE	26	TXD2
9	SPEED100/PHYAD0	27	TXD3
10	LINK/PHYAD1	28	TXN
11	ACTIVITY/PHYAD2	29	TXP
12	FDUPLEX/PHYAD3	30	VDDA3.3
13	XTAL2	31	RXN
14	CLKIN/XTAL1	32	RXP
15	RXD3/nINTSEL	33	VDDA3.3
16	RXD2/MODE2	34	EXRES1
17	RXD1/MODE1	35	VDDA3.3
18	RXD0/MODE0	36	COL/RMII/CRS_DV

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3.0 PIN DESCRIPTION

This chapter describes the signals on each pin. When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

3.1 I/O Signals

The following buffer types are shown in the TYPE column of the tables in this chapter.

- I Input. Digital LVCMOS levels.
- IPD Input with internal pull-down. Digital LVCMOS levels.
- O Output. Digital LVCMOS levels.
- OPD Output with internal pull-down. Digital LVCMOS levels.
- I/O Input or Output. Digital LVCMOS levels.
- IOPD Input or Output with internal pull-down. Digital LVCMOS levels.
- IOPU Input or Output with internal pull-up. Digital LVCMOS levels.

Note:	The digital signals are not 5V tolerant.They are variable voltage from +1.6V to +3.6V.

- AI Input. Analog levels.
- AO Output. Analog levels.

TABLE 3-1: MII SIGNALS

Signal Name	Type	Description
TXD0	I	**Transmit Data 0**: Bit 0 of the 4 data bits that are accepted by the PHY for transmission.
TXD1	I	**Transmit Data 1**: Bit 1 of the 4 data bits that are accepted by the PHY for transmission.
TXD2	I	**Transmit Data 2**: Bit 2 of the 4 data bits that are accepted by the PHY for transmission Note: This signal should be grounded in RMII Mode.
TXD3	I	**Transmit Data 3**: Bit 3 of the 4 data bits that are accepted by the PHY for transmission. Note: This signal should be grounded in RMII Mode
nINT/ TX_ER/ TXD4	IOPU	**MII Transmit Error**: When driven high, the 4B/5B encode process substitutes the Transmit Error code-group (/H/) for the encoded data word. This input is ignored in 10Base-T operation. **MII Transmit Data 4:** In Symbol Interface (5B Decoding) mode, this signal becomes the MII Transmit Data 4 line, the MSB of the 5-bit symbol code-group. • This signal is not used in RMII Mode. • This signal is mux’d with nINT • See Section 4.10, "nINT/TX_ER/TXD4 Strapping," on page 24 for additional information on configuration/strapping options.
TX_EN	IPD	**Transmit Enable**: Indicates that valid data is presented on the TXD[3:0] signals, for transmission. In RMII Mode, only TXD[1:0] have valid data.
TX_CLK	O	**Transmit Clock**: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode. • This signal is not used in RMII Mode. • For proper TXCLK operation, RX_ER and RX_DV must NOT be driven high externally on a hardware reset or on a LAN8700 power up.

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TABLE 3-1: MII SIGNALS (CONTINUED)

Signal Name	Type	Description
RXD0/ MODE0	IOPU	**Receive Data 0**: Bit 0 of the 4 data bits that are sent by the PHY in the receive path. **PHY Operating Mode Bit 0:** set the default MODE of the PHY. Note: See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options
RXD1/ MODE1	IOPU	**Receive Data 1**: Bit 1 of the 4 data bits that are sent by the PHY in the receive path. **PHY Operating Mode Bit 1:** set the default MODE of the PHY. Note: See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options.
RXD2/ MODE2	IOPU	**Receive Data 2**: Bit 2 of the 4 data bits that are sent by the PHY in the receive path. **PHY Operating Mode Bit 2:** set the default MODE of the PHY. • RXD2 is not used in RMII Mode. • See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options.
RXD3/ nINTSEL	IOPU	**Receive Data 3**: Bit 3 of the 4 data bits that are sent by the PHY in the receive path. **nINTSEL**: On power-up or external reset, the mode of the nINT/TXER/TXD4 pin is selected. • When RXD3/nINTSEL is floated or pulled to VDDIO, nINT is selected for operation on pin nINT/TXER/TXD4 (default). • When RXD3/nINTSEL is pulled low to VSS through a resistor, (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25), TXER/TXD4 is selected for operation on pin nINT/TXER/TXD4. • RXD3 is not used in RMII Mode • If the nINT/TXER/TXD4 pin is configured for nINT mode, then a pull-up resistor is needed to VDDIO on the nINT/TXER/TXD4 pin. see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25. • See Section 4.10, "nINT/TX_ER/TXD4 Strapping," on page 24 for additional information on configuration/strapping options.
RX_ER/ RXD4/	OPD	**Receive Error**: Asserted to indicate that an error was detected somewhere in the frame presently being transferred from the PHY. **MII Receive Data 4**: In Symbol Interface (5B Decoding) mode, this signal is the MII Receive Data 4 signal, the MSB of the received 5-bit symbol code-group. Unless configured in this mode, the pin functions as RX_ER. Note: This pin has an internal pull-down resistor, and must not be high during reset. The RX_ER signal is optional in RMII Mode.
RX_DV	O	**Receive Data Valid**: Indicates that recovered and decoded data nibbles are being presented on RXD[3:0]. Note: This pin has an internal pull-down resistor, and must not be high during reset. This signal is not used in RMII Mode.

TABLE 3-1: MII SIGNALS (CONTINUED)

Signal Name	Type	Description
RX_CLK/ REGOFF	IOPD	**Receive Clock**: In MII mode, this pin is the receive clock output. 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode. Note: This signal is not used in RMII Mode. **Regulator Off**: This pin pulled up to configure the internal 1.8V regulator off. As described in Section 4.9, this pin is sampled during the power-on sequence to determine if the internal regulator should turn on. When the regulator is disabled, external 1.8V must be supplied to VDD_CORE, and the voltage at VDD33 must be at least 2.64V before voltage is applied to VDD_CORE.
COL/ RMII/ CRS_DV	IOPD	**MII Mode Collision Detect**: Asserted to indicate detection of collision condition. **RMII –** MII/RMII mode selection is latched on the rising edge of the internal reset (nreset) based on the following strapping: • Float this pin for MII mode or pull-high with an external resistor to VDDIO (see Table 4-3, "Boot Strapping Configuration Resistors," on page 25) to set the device in RMII mode. • See Section 4.6.3, "MII vs. RMII Configuration," on page 21 for more details. **RMII Mode CRS_DV (Carrier Sense/Receive Data Valid)** Asserted to indicate when the receive medium is non-idle. When a 10BT packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received. In 10BT, half-duplex mode, transmitted data is not looped back onto the receive data pins, per the RMII standard.
CRS/ PHYAD4	IOPU	**Carrier Sense**: Indicates detection of carrier. Note: This signal is mux'd with PHYAD4

TABLE 3-2: LED SIGNALS

Signal Name	Type	Description
SPEED100/ PHYAD0	IOPU	**LED1 –** SPEED100 indication. Active indicates that the selected speed is 100Mbps. Inactive indicates that the selected speed is 10Mbps. Note: This signal is mux'd with PHYAD0
LINK/ PHYAD1	IOPU	**LED2 –** LINK ON indication. Active indicates that the Link (100Base-TX or 10Base-T) is on. Note: This signal is mux'd with PHYAD1
ACTIVITY/ PHYAD2	IOPU	**LED3 –** ACTIVITY indication. Active indicates that there is Carrier sense (CRS) from the active PMD. Note: This signal is mux'd with PHYAD2
FDUPLEX/ PHYAD3	IOPU	**LED4 –** DUPLEX indication. Active indicates that the PHY is in full-duplex mode. Note: This signal is mux'd with PHYAD3

TABLE 3-3: MANAGEMENT SIGNALS

Signal Name	Type	Description
MDIO	IOPD	**Management Data Input/OUTPUT**: Serial management data input/output.
MDC	IPD	**Management Clock**: Serial management clock.

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TABLE 3-4: BOOT STRAP CONFIGURATION INPUTS (Note 3-1)

Signal Name	Type	Description
CRS/ PHYAD4	IOPU	**PHY Address Bit 4:** set the default address of the PHY. This signal is mux'd with CRS Note: This signal is mux'd with CRS
FDUPLEX/ PHYAD3	IOPU	**PHY Address Bit 3:** set the default address of the PHY. Note: This signal is mux'd with FDUPLEX
ACTIVITY/ PHYAD2	IOPU	**PHY Address Bit 2:** set the default address of the PHY. Note: This signal is mux'd with ACTIVITY
LINK/ PHYAD1	IOPU	**PHY Address Bit 1:** set the default address of the PHY. Note: This signal is mux'd with LINK
SPEED100/ PHYAD0	IOPU	**PHY Address Bit 0:** set the default address of the PHY. Note: This signal is mux'd with SPEED100
RXD2/ MODE2	IOPU	**PHY Operating Mode Bit 2:** set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options. Note: This signal is mux'd with RXD2
RXD1/ MODE1	IOPU	**PHY Operating Mode Bit 1:** set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options. Note: This signal is mux'd with RXD1
RXD0/ MODE0	IOPU	**PHY Operating Mode Bit 0:** set the default MODE of the PHY. See Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46, for the MODE options. Note: This signal is mux'd with RXD0
COL/ RMII/ CRS_DV	IOPD	**Digital Communication Mode:** set the digital communications mode of the PHY to RMII or MII. This signal is muxed with the Collision signal (MII mode) and Carrier Sense/ receive Data Valid (RMII mode) • Float for MII mode. • Pull up with a resistor to VDDIO for RMII mode (see Table 4-3, "Boot Strapping Configuration Resistors," on page 25)
RXD3/ nINTSEL	IOPU	**nINT pin mode select:** set the mode of pin 1. • Default, left floating pin 1 is nINT, active low interrupt output. • For nINT mode, tie nINT/TXD4/TXER to VDDIO with a resistor (see Table 4-3, "Boot Strapping Configuration Resistors," on page 25). • Pulled to VSS by a resistor, (see Table 4-3, "Boot Strapping Configuration Resistors," on page 25) pin 1 is TX_ER/TXD4, Transmit Error or Transmit data 4 (5B mode). • For TXD4/TXER mode, do not tie nINT/TXD4/TXER to VDDIO or Ground.

Note 3-1 On nRST transition high, the PHY latches the state of the configuration pins in this table.

TABLE 3-5: GENERAL SIGNALS

Signal Name	Type	Description
nINT/ TX_ER/ TXD4	IOPU	**LAN Interrupt** – Active Low output. Place an external resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) pull-up to VCC 3.3V. • This signal is mux’d with TXER/TXD4 • See Section 4.10, "nINT/TX_ER/TXD4 Strapping," on page 24 for additional details on Strapping options.
nRST	I	**External Reset** – input of the system reset. This signal is active LOW. When this pin is deasserted, the mode register bits are loaded from the mode pins as described in Section 5.4.9.2.
CLKIN/ XTAL1	I/O	**Clock Input** – 25 Mhz or 50 MHz external clock or crystal input. • In MII mode, this signal is the 25 MHz reference input clock • In RMII mode, this signal is the 50 MHz reference input clock which is typically also driven to the RMII compliant Ethernet MAC clock input. Note: See Section 4.10, "nINT/TX_ER/TXD4 Strapping," on page 24 for additional details on Strapping options.
XTAL2	O	**Clock Output** – 25 MHz crystal output. Note: Float this pin if using an external clock being driven through CLKIN/XTAL1

TABLE 3-6: 10/100 LINE INTERFACE

Signal Name	Type	Description
TXP	AO	**Transmit Data Positive**: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
TXN	AO	**Transmit Data Negative**: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
RXP	AI	**Receive Data Positive**: 100Base-TX or 10Base-T differential receive inputs from magnetics.
RXN	AI	**Receive Data Negative**: 100Base-TX or 10Base-T differential receive inputs from magnetics.

TABLE 3-7: ANALOG REFERENCES

Signal Name	Type	Description
EXRES1	AI	Connects to reference resistor of value 12.4K-Ohm, 1% connected as described in the Analog Layout Guidelines. The nominal voltage is 1.2V and therefore the resistor will dissipate approximately 1mW of power.

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TABLE 3-8: POWER SIGNALS

Signal Name	Type	Description
VDDIO	POWER	+1.6V to +3.6V Variable I/O Pad Power
VDD33	POWER	+3.3V Core Regulator Input.
VDDA3.3	POWER	+3.3V Analog Power
VDD_CORE	POWER	+1.8V (Core voltage) - 1.8V for digital circuitry on chip. Supplied by the on-chip regulator unless configured for regulator off mode using the RX_CLK/REGOFF pin. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. When using the on-chip regulator, place a 4.7uF ±20% capacitor with ESR < 1ohm near this pin and connect the capacitor from this pin to ground. X5R or X7R ceramic capacitors are recommended since they exhibit an ESR lower than 0.1ohm at frequencies greater than 10kHz.
VSS	POWER	Exposed Ground Flag. The flag must be connected to the ground plane with an array of vias as described in the Analog Layout Guidelines

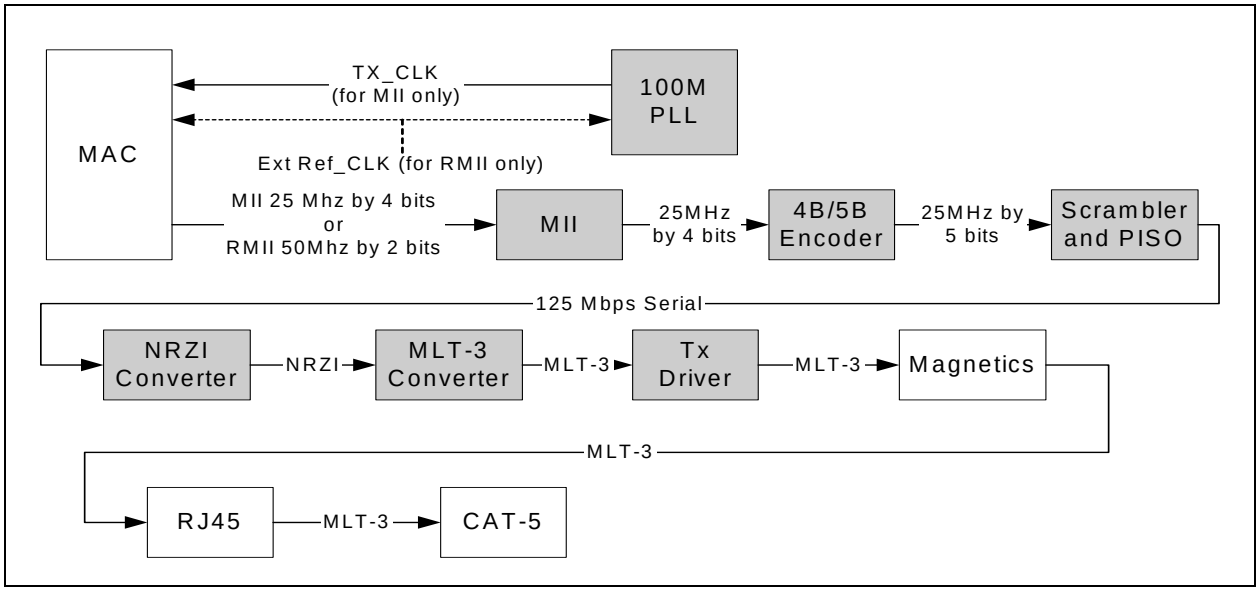
4.0 ARCHITECTURE DETAILS

4.1 Top Level Functional Architecture

Functionally, the PHY can be divided into the following sections:

- 100Base-TX transmit and receive
- 10Base-T transmit and receive
- MII or RMII interface to the controller
- Auto-negotiation to automatically determine the best speed and duplex possible
- Management Control to read status registers and write control registers

FIGURE 4-1: 100BASE-TX DATA PATH



4.2 100Base-TX Transmit

The data path of the 100Base-TX is shown in Figure 4-1. Each major block is explained below.

4.2.1 100M TRANSMIT DATA ACROSS THE MII/RMII INTERFACE

For MII, the MAC controller drives the transmit data onto the TXD bus and asserts TX_EN to indicate valid data. The data is latched by the PHY's MII block on the rising edge of TX_CLK. The data is in the form of 4-bit wide 25MHz data.

The MAC controller drives the transmit data onto the TXD bus and asserts TX_EN to indicate valid data. The data is latched by the PHY's MII block on the rising edge of REF_CLK. The data is in the form of 2-bit wide 50MHz data.

4.2.2 4B/5B ENCODING

The transmit data passes from the MII block to the 4B/5B encoder. This block encodes the data from 4-bit nibbles to 5-bit symbols (known as "code-groups") according to Table 4-1. Each 4-bit data-nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or are not valid.

The first 16 code-groups are referred to by the hexadecimal values of their corresponding data nibbles, 0 through F. The remaining code-groups are given letter designations with slashes on either side. For example, an IDLE code-group is /I/, a transmit error code-group is /H/, etc.

The encoding process may be bypassed by clearing bit 6 of register 31. When the encoding is bypassed the 5th transmit data bit is equivalent to TX_ER.

Note that encoding can be bypassed only when the MAC interface is configured to operate in MII mode.

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TABLE 4-1: 4B/5B CODE TABLE

Code Group	SYM	Receiver Interpretation			Transmitter Interpretation		
11110	0	0	0000	DATA	0	0000	DATA
01001	1	1	0001		1	0001	
10100	2	2	0010		2	0010	
10101	3	3	0011		3	0011	
01010	4	4	0100		4	0100	
01011	5	5	0101		5	0101	
01110	6	6	0110		6	0110	
01111	7	7	0111		7	0111	
10010	8	8	1000		8	1000	
10011	9	9	1001		9	1001	
10110	A	A	1010		A	1010	
10111	B	B	1011		B	1011	
11010	C	C	1100		C	1100	
11011	D	D	1101		D	1101	
11100	E	E	1110		E	1110	
11101	F	F	1111		F	1111	
11111	I	IDLE			Sent after /T/R until TX_EN		
11000	J	First nibble of SSD, translated to “0101” following IDLE, else RX_ER			Sent for rising TX_EN		
10001	K	Second nibble of SSD, translated to “0101” following J, else RX_ER			Sent for rising TX_EN		
01101	T	First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of RX_ER			Sent for falling TX_EN		
00111	R	Second nibble of ESD, causes deassertion of CRS if following /T/, else assertion of RX_ER			Sent for falling TX_EN		
00100	H	Transmit Error Symbol			Sent for rising TX_ER		
00110	V	INVALID, RX_ER if during RX_DV			INVALID		
11001	V	INVALID, RX_ER if during RX_DV			INVALID		
00000	V	INVALID, RX_ER if during RX_DV			INVALID		
00001	V	INVALID, RX_ER if during RX_DV			INVALID		
00010	V	INVALID, RX_ER if during RX_DV			INVALID		
00011	V	INVALID, RX_ER if during RX_DV			INVALID		
00101	V	INVALID, RX_ER if during RX_DV			INVALID		
01000	V	INVALID, RX_ER if during RX_DV			INVALID		
01100	V	INVALID, RX_ER if during RX_DV			INVALID		
10000	V	INVALID, RX_ER if during RX_DV			INVALID		

4.2.3 SCRAMBLING

Repeated data patterns (especially the IDLE code-group) can have power spectral densities with large narrow-band peaks. Scrambling the data helps eliminate these peaks and spread the signal power more uniformly over the entire channel bandwidth. This uniform spectral density is required by FCC regulations to prevent excessive EMI from being radiated by the physical wiring.

The seed for the scrambler is generated from the PHY address, PHYAD[4:0], ensuring that in multiple-PHY applications, such as repeaters or switches, each PHY will have its own scrambler sequence.

The scrambler also performs the Parallel In Serial Out conversion (PISO) of the data.

4.2.4 NRZI AND MLT3 ENCODING

The scrambler block passes the 5-bit wide parallel data to the NRZI converter where it becomes a serial 125MHz NRZI data stream. The NRZI is encoded to MLT-3. MLT3 is a tri-level code where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.

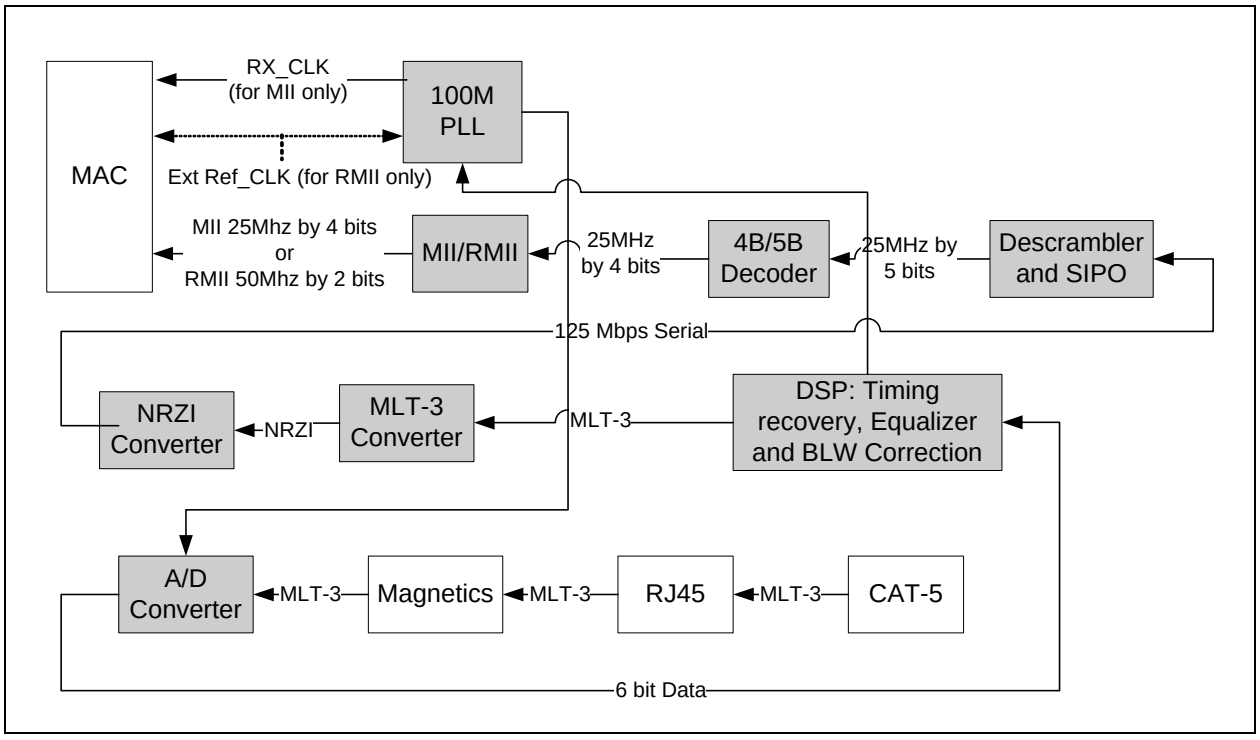
4.2.5 100M TRANSMIT DRIVER

The MLT3 data is then passed to the analog transmitter, which drives the differential MLT-3 signal, on outputs TXP and TXN, to the twisted pair media across a 1:1 ratio isolation transformer. The 10Base-T and 100Base-TX signals pass through the same transformer so that common “magnetics” can be used for both. The transmitter drives into the 100Ω impedance of the CAT-5 cable. Cable termination and impedance matching require external components.

4.2.6 100M PHASE LOCK LOOP (PLL)

The 100M PLL locks onto reference clock and generates the 125MHz clock used to drive the 125 MHz logic and the 100Base-Tx Transmitter.

FIGURE 4-2: RECEIVE DATA PATH



4.3 100Base-TX Receive

The receive data path is shown in Figure 4-2. Detailed descriptions are given below.

4.3.1 100M RECEIVE INPUT

The MLT-3 from the cable is fed into the PHY (on inputs RXP and RXN) via a 1:1 ratio transformer. The ADC samples the incoming differential signal at a rate of 125M samples per second. Using a 64-level quanitizer it generates 6 digital bits to represent each sample. The DSP adjusts the gain of the ADC according to the observed signal levels such that the full dynamic range of the ADC can be used.

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4.3.2 EQUALIZER, BASELINE WANDER CORRECTION AND CLOCK AND DATA RECOVERY

The 6 bits from the ADC are fed into the DSP block. The equalizer in the DSP section compensates for phase and amplitude distortion caused by the physical channel consisting of magnetics, connectors, and CAT- 5 cable. The equalizer can restore the signal for any good-quality CAT-5 cable between 1m and 150m.

If the DC content of the signal is such that the low-frequency components fall below the low frequency pole of the isolation transformer, then the droop characteristics of the transformer will become significant and Baseline Wander (BLW) on the received signal will result. To prevent corruption of the received data, the PHY corrects for BLW and can receive the ANSI X3.263-1995 FDDI TP-PMD defined “killer packet” with no bit errors.

The 100M PLL generates multiple phases of the 125MHz clock. A multiplexer, controlled by the timing unit of the DSP, selects the optimum phase for sampling the data. This is used as the received recovered clock. This clock is used to extract the serial data from the received signal.

4.3.3 NRZI AND MLT-3 DECODING

The DSP generates the MLT-3 recovered levels that are fed to the MLT-3 converter. The MLT-3 is then converted to an NRZI data stream.

4.3.4 DESCRAMBLING

The descrambler performs an inverse function to the scrambler in the transmitter and also performs the Serial In Parallel Out (SIPO) conversion of the data.

During reception of IDLE (/I/) symbols. the descrambler synchronizes its descrambler key to the incoming stream. Once synchronization is achieved, the descrambler locks on this key and is able to descramble incoming data.

Special logic in the descrambler ensures synchronization with the remote PHY by searching for IDLE symbols within a window of 4000 bytes (40us). This window ensures that a maximum packet size of 1514 bytes, allowed by the IEEE 802.3 standard, can be received with no interference. If no IDLE-symbols are detected within this time-period, receive operation is aborted and the descrambler re-starts the synchronization process.

The descrambler can be bypassed by setting bit 0 of register 31.

4.3.5 ALIGNMENT

The de-scrambled signal is then aligned into 5-bit code-groups by recognizing the /J/K/ Start-of-Stream Delimiter (SSD) pair at the start of a packet. Once the code-word alignment is determined, it is stored and utilized until the next start of frame.

4.3.6 5B/4B DECODING

The 5-bit code-groups are translated into 4-bit data nibbles according to the 4B/5B table. The translated data is presented on the RXD[3:0] signal lines. The SSD, /J/K/, is translated to “0101 0101” as the first 2 nibbles of the MAC preamble. Reception of the SSD causes the PHY to assert the RX_DV signal, indicating that valid data is available on the RXD bus. Successive valid code-groups are translated to data nibbles. Reception of either the End of Stream Delimiter (ESD) consisting of the /T/R/ symbols, or at least two /I/ symbols causes the PHY to de-assert carrier sense and RX_DV.

These symbols are not translated into data.

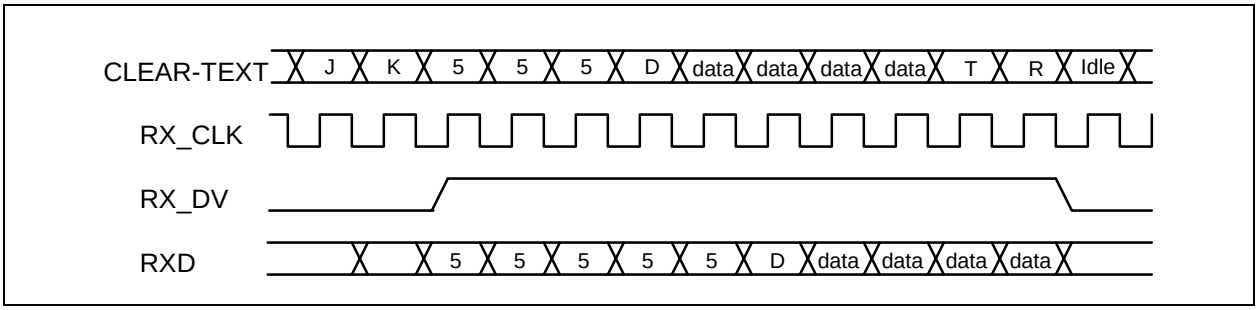
The decoding process may be bypassed by clearing bit 6 of register 31. When the decoding is bypassed the 5^{th} receive data bit is driven out on RX_ER/RXD4. Decoding may be bypassed only when the MAC interface is in MII mode.

4.3.7 RECEIVE DATA VALID SIGNAL

The Receive Data Valid signal (RX_DV) indicates that recovered and decoded nibbles are being presented on the RXD[3:0] outputs synchronous to RX_CLK. RX_DV becomes active after the /J/K/ delimiter has been recognized and RXD is aligned to nibble boundaries. It remains active until either the /T/R/ delimiter is recognized or link test indicates failure or SIGDET becomes false.

RX_DV is asserted when the first nibble of translated /J/K/ is ready for transfer over the Media Independent Interface (MII mode).

FIGURE 4-3: RELATIONSHIP BETWEEN RECEIVED DATA AND SPECIFIC MII SIGNALS



4.3.8 RECEIVER ERRORS

During a frame, unexpected code-groups are considered receive errors. Expected code groups are the DATA set (0 through F), and the /T/R/ (ESD) symbol pair. When a receive error occurs, the RX_ER signal is asserted and arbitrary data is driven onto the RXD[3:0] lines. Should an error be detected during the time that the /J/K/ delimiter is being decoded (bad SSD error), RX_ER is asserted true and the value ‘1110’ is driven onto the RXD[3:0] lines. Note that the Valid Data signal is not yet asserted when the bad SSD error occurs.

4.3.9 100M RECEIVE DATA ACROSS THE MII/RMII INTERFACE

In MII mode, the 4-bit data nibbles are sent to the MII block. These data nibbles are clocked to the controller at a rate of 25MHz. The controller samples the data on the rising edge of RX_CLK. To ensure that the setup and hold requirements are met, the nibbles are clocked out of the PHY on the falling edge of RX_CLK. RX_CLK is the 25MHz output clock for the MII bus. It is recovered from the received data to clock the RXD bus. If there is no received signal, it is derived from the system reference clock (CLKIN).

When tracking the received data, RX_CLK has a maximum jitter of 0.8ns (provided that the jitter of the input clock, CLKIN, is below 100ps).

In RMII mode, the 2-bit data nibbles are sent to the RMII block. These data nibbles are clocked to the controller at a rate of 50MHz. The controller samples the data on the rising edge of CLKIN/XTAL1 (REF_CLK). To ensure that the setup and hold requirements are met, the nibbles are clocked out of the PHY on the falling edge of CLKIN/XTAL1 (REF_CLK).

4.4 10Base-T Transmit

Data to be transmitted comes from the MAC layer controller. The 10Base-T transmitter receives 4-bit nibbles from the MII at a rate of 2.5MHz and converts them to a 10Mbps serial data stream. The data stream is then Manchester-encoded and sent to the analog transmitter, which drives a signal onto the twisted pair via the external magnetics.

The 10M transmitter uses the following blocks:

- MII (digital)
- TX 10M (digital)
- 10M Transmitter (analog)
- 10M PLL (analog)

4.4.1 10M TRANSMIT DATA ACROSS THE MII/RMII INTERFACE

The MAC controller drives the transmit data onto the TXD BUS. For MII, when the controller has driven TX_EN high to indicate valid data, the data is latched by the MII block on the rising edge of TX_CLK. The data is in the form of 4-bit wide 2.5MHz data.

In order to comply with legacy 10Base-T MAC/Controllers, in Half-duplex mode the PHY loops back the transmitted data, on the receive path. This does not confuse the MAC/Controller since the COL signal is not asserted during this time. The PHY also supports the SQE (Heartbeat) signal. See Section 5.4.2, "Collision Detect," on page 42, for more details.

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For RMII, TXD[1:0] shall transition synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the LAN8700/LAN8700i. TXD[1:0] shall be “00” to indicate idle when TX_EN is deasserted. Values of TXD[1:0] other than “00” when TX_EN is deasserted are reserved for out-of-band signalling (to be defined). Values other than “00” on TXD[1:0] while TX_EN is deasserted shall be ignored by the LAN8700/LAN8700i.TXD[1:0] shall provide valid data for each REF_CLK period while TX_EN is asserted.

4.4.2 MANCHESTER ENCODING

The 4-bit wide data is sent to the TX10M block. The nibbles are converted to a 10Mbps serial NRZI data stream. The 10M PLL locks onto the external clock or internal oscillator and produces a 20MHz clock. This is used to Manchester encode the NRZ data stream. When no data is being transmitted (TX_EN is low), the TX10M block outputs Normal Link Pulses (NLPs) to maintain communications with the remote link partner.

4.4.3 10M TRANSMIT DRIVERS

The Manchester encoded data is sent to the analog transmitter where it is shaped and filtered before being driven out as a differential signal across the TXP and TXN outputs.

4.5 10Base-T Receive

The 10Base-T receiver gets the Manchester- encoded analog signal from the cable via the magnetics. It recovers the receive clock from the signal and uses this clock to recover the NRZI data stream. This 10M serial data is converted to 4-bit data nibbles which are passed to the controller across the MII at a rate of 2.5MHz.

This 10M receiver uses the following blocks:

- Filter and SQUELCH (analog)
- 10M PLL (analog)
- RX 10M (digital)
- MII (digital)

4.5.1 10M RECEIVE INPUT AND SQUELCH

The Manchester signal from the cable is fed into the PHY (on inputs RXP and RXN) via 1:1 ratio magnetics. It is first filtered to reduce any out-of-band noise. It then passes through a SQUELCH circuit. The SQUELCH is a set of amplitude and timing comparators that normally reject differential voltage levels below 300mV and detect and recognize differential voltages above 585mV.

4.5.2 MANCHESTER DECODING

The output of the SQUELCH goes to the RX10M block where it is validated as Manchester encoded data. The polarity of the signal is also checked. If the polarity is reversed (local RXP is connected to RXN of the remote partner and vice versa), then this is identified and corrected. The reversed condition is indicated by the flag “XPOL“, bit 4 in register 27. The 10M PLL is locked onto the received Manchester signal and from this, generates the received 20MHz clock. Using this clock, the Manchester encoded data is extracted and converted to a 10MHz NRZI data stream. It is then converted from serial to 4-bit wide parallel data.

The RX10M block also detects valid 10Base-T IDLE signals - Normal Link Pulses (NLPs) - to maintain the link.

4.5.3 10M RECEIVE DATA ACROSS THE MII/RMII INTERFACE

For MII, the 4 bit data nibbles are sent to the MII block. In MII mode, these data nibbles are valid on the rising edge of the 2.5 MHz RX_CLK.

For RMII, the 2bit data nibbles are sent to the RMII block. In RMII mode, these data nibbles are valid on the rising edge of the RMII REF_CLK.

4.5.4 JABBER DETECTION

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition, that results in holding the TX_EN input for a long period. Special logic is used to detect the jabber state and abort the transmission to the line, within 45ms. Once TX_EN is deasserted, the logic resets the jabber condition.

As shown in Table 5-31, bit 1.1 indicates that a jabber condition was detected.

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4.6 MAC Interface

The MII/RMII block is responsible for the communication with the controller. Special sets of hand-shake signals are used to indicate that valid received/transmitted data is present on the 4 bit receive/transmit bus.

The device must be configured in MII or RMII mode. See Section 4.6.3, "MII vs. RMII Configuration," on page 21.

4.6.1 MII

The MII includes 16 interface signals:

- transmit data - TXD[3:0]
- transmit strobe - TX_EN
- transmit clock - TX_CLK
- transmit error - TX_ER/TXD4
- receive data - RXD[3:0]
- receive strobe - RX_DV
- receive clock - RX_CLK
- receive error - RX_ER/RXD4
- collision indication - COL
- carrier sense - CRS

In MII mode, on the transmit path, the PHY drives the transmit clock, TX_CLK, to the controller. The controller synchronizes the transmit data to the rising edge of TX_CLK. The controller drives TX_EN high to indicate valid transmit data. The controller drives TX_ER high when a transmit error is detected.

On the receive path, the PHY drives both the receive data, RXD[3:0], and the RX_CLK signal. The controller clocks in the receive data on the rising edge of RX_CLK when the PHY drives RX_DV high. The PHY drives RX_ER high when a receive error is detected.

4.6.2 RMII

The Microchip LAN8700/LAN8700i supports the low pin count Reduced Media Independent Interface (RMII) intended for use between Ethernet PHYs and Switch ASICs. Under IEEE 802.3, an MII comprised of 16 pins for data and control is defined. In devices incorporating many MACs or PHY interfaces such as switches, the number of pins can add significant cost as the port counts increase. The management interface (MDIO/MDC) is identical to MII. The RMII interface has the following characteristics:

- It is capable of supporting 10Mb/s and 100Mb/s data rates
- A single clock reference is sourced from the MAC to PHY (or from an external source)
- It provides independent 2 bit wide (di-bit) transmit and receive data paths
- It uses LVCMOS signal levels, compatible with common digital CMOS ASIC processes

The RMII includes 6 interface signals with one of the signals being optional:

- transmit data - TXD[1:0]
- transmit strobe - TX_EN
- receive data - RXD[1:0]
- receive error - RX_ER (Optional)
- carrier sense - CRS_DV
- Reference Clock - CLKIN/XTAL1 (RMII references usually define this signal as REF_CLK)

4.6.2.1 Reference Clock

The Reference Clock - CLKIN, is a continuous clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. The Reference Clock is sourced by the MAC or an external source. Switch implementations may choose to provide REF_CLK as an input or an output depending on whether they provide a REF_CLK output or rely on an external clock distribution device.

The “Reference Clock” frequency must be 50 MHz ± 50 ppm with a duty cycle between 40% and 60% inclusive. The Microchip LAN8700/LAN8700i uses the “Reference Clock” as the network clock such that no buffering is required on the transmit data path. The Microchip LAN8700/LAN8700i will recover the clock from the incoming data stream, the receiver will account for differences between the local REF_CLK and the recovered clock through use of sufficient elas-

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ticity buffering. The elasticity buffer does not affect the Inter-Packet Gap (IPG) for received IPGs of 36 bits or greater. To tolerate the clock variations specified here for Ethernet MTUs, the elasticity buffer shall tolerate a minimum of ±10 bits.

4.6.2.2 CRS_DV - Carrier Sense/Receive Data Valid

The CRS_DV is asserted by the LAN8700/LAN8700i when the receive medium is non-idle. CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when 2 non-contiguous zeroes in 10 bits are detected, carrier is said to be detected.

Loss of carrier shall result in the deassertion of CRS_DV synchronous to the cycle of REF_CLK which presents the first di-bit of a nibble onto RXD[1:0] (i.e. CRS_DV is deasserted only on nibble boundaries). If the LAN8700/LAN8700i has additional bits to be presented on RXD[1:0] following the initial deassertion of CRS_DV, then the LAN8700/LAN8700i shall assert CRS_DV on cycles of REF_CLK which present the second di-bit of each nibble and de-assert CRS_DV on cycles of REF_CLK which present the first di-bit of a nibble. The result is: Starting on nibble boundaries CRS_DV toggles at 25 MHz in 100Mb/s mode and 2.5 MHz in 10Mb/s mode when CRS ends before RX_DV (i.e. the FIFO still has bits to transfer when the carrier event ends.) Therefore, the MAC can accurately recover RX_DV and CRS.

During a false carrier event, CRS_DV shall remain asserted for the duration of carrier activity. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] shall be “00” until proper receive signal decoding takes place.

4.6.3 MII VS. RMII CONFIGURATION

The LAN8700/LAN8700i must be configured to support the MII or RMII bus for connectivity to the MAC. This configuration is done through the COL/RMII/CRS_DV pin. To select MII mode, float the COL/RMII/CRS_DV pin. To select RMII mode, pull the pin high with an external resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) to VDDIO. On the rising edge of the internal reset (nreset), the register bit 18.14 (MIIMODE) is loaded based on the strapping of the COL/RMII/CRS_DV pin.

Most of the MII and RMII pins are multiplexed. Table 4-2, "MII/RMII Signal Mapping", shown below, describes the relationship of the related device pins to what pins are used in MII and RMII mode.

TABLE 4-2: MII/RMII SIGNAL MAPPING

Signal Name	MII Mode	RMII Mode
TXD0	TXD0	TXD0
TXD1	TXD1	TXD1
TX_EN	TX_EN	TX_EN
RX_ER/ RXD4	RX_ER/ RXD4/	RX_ER Note 4-2
COL/RMII/ CRS_DV	COL	CRS_DV
RXD0	RXD0	RXD0
RXD1	RXD1	RXD1
TXD2	TXD2	Note 4-1
TXD3	TXD3	Note 4-1
TX_ER/ TXD4	TX_ER/ TXD4	
CRS	CRS	
RX_DV	RX_DV	
RXD2	RXD2	
RXD3/ nINTSEL	RXD3	
TX_CLK	TX_CLK	
RX_CLK	RX_CLK	
CLKIN/ XTAL1	CLKIN/ XTAL1	REF_CLK

Note 4-1 In RMII mode, this pin needs to tied to VSS.

Note 4-2 The RX_ER signal is optional on the RMII bus. This signal is required by the PHY, but it is optional for the MAC. The MAC can choose to ignore or not use this signal.

4.7 Auto-negotiation

The purpose of the Auto-negotiation function is to automatically configure the PHY to the optimum link parameters based on the capabilities of its link partner. Auto-negotiation is a mechanism for exchanging configuration information between two link-partners and automatically selecting the highest performance mode of operation supported by both sides. Auto-negotiation is fully defined in clause 28 of the IEEE 802.3 specification.

Once auto-negotiation has completed, information about the resolved link can be passed back to the controller via the Serial Management Interface (SMI). The results of the negotiation process are reflected in the Speed Indication bits in register 31, as well as the Link Partner Ability Register (Register 5).

The auto-negotiation protocol is a purely physical layer activity and proceeds independently of the MAC controller.

The advertised capabilities of the PHY are stored in register 4 of the SMI registers. The default advertised by the PHY is determined by user-defined on-chip signal options.

The following blocks are activated during an Auto-negotiation session:

- Auto-negotiation (digital)
- 100M ADC (analog)
- 100M PLL (analog)
- 100M equalizer/BLW/clock recovery (DSP)
- 10M SQUELCH (analog)
- 10M PLL (analog)
- 10M Transmitter (analog)

When enabled, auto-negotiation is started by the occurrence of one of the following events:

- Hardware reset
- Software reset
- Power-down reset
- Link status down
- Setting register 0, bit 9 high (auto-negotiation restart)

On detection of one of these events, the PHY begins auto-negotiation by transmitting bursts of Fast Link Pulses (FLP). These are bursts of link pulses from the 10M transmitter. They are shaped as Normal Link Pulses and can pass uncorrupted down CAT-3 or CAT-5 cable. A Fast Link Pulse Burst consists of up to 33 pulses. The 17 odd-numbered pulses, which are always present, frame the FLP burst. The 16 even-numbered pulses, which may be present or absent, contain the data word being transmitted. Presence of a data pulse represents a “1”, while absence represents a “0”.

The data transmitted by an FLP burst is known as a “Link Code Word.” These are defined fully in IEEE 802.3 clause 28. In summary, the PHY advertises 802.3 compliance in its selector field (the first 5 bits of the Link Code Word). It advertises its technology ability according to the bits set in register 4 of the SMI registers.

There are 4 possible matches of the technology abilities. In the order of priority these are:

- 100M Full Duplex (Highest priority)
- 100M Half Duplex
- 10M Full Duplex
- 10M Half Duplex

If the full capabilities of the PHY are advertised (100M, Full Duplex), and if the link partner is capable of 10M and 100M, then auto-negotiation selects 100M as the highest performance mode. If the link partner is capable of Half and Full duplex modes, then auto-negotiation selects Full Duplex as the highest performance operation.

Once a capability match has been determined, the link code words are repeated with the acknowledge bit set. Any difference in the main content of the link code words at this time will cause auto-negotiation to re-start. Auto-negotiation will also re-start if not all of the required FLP bursts are received.

The capabilities advertised during auto-negotiation by the PHY are initially determined by the logic levels latched on the MODE[2:0] bus after reset completes. This bus can also be used to disable auto-negotiation on power-up.

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Writing register 4 bits [8:5] allows software control of the capabilities advertised by the PHY. Writing register 4 does not automatically re-start auto-negotiation. Register 0, bit 9 must be set before the new abilities will be advertised. Auto-negotiation can also be disabled via software by clearing register 0, bit 12.

The LAN8700/LAN8700i does not support “Next Page” capability.

4.7.1 PARALLEL DETECTION

If the LAN8700/LAN8700i is connected to a device lacking the ability to auto-negotiate (i.e. no FLPs are detected), it is able to determine the speed of the link based on either 100M MLT-3 symbols or 10M Normal Link Pulses. In this case the link is presumed to be Half Duplex per the IEEE standard. This ability is known as “Parallel Detection.” This feature ensures interoperability with legacy link partners. If a link is formed via parallel detection, then bit 0 in register 6 is cleared to indicate that the Link Partner is not capable of auto-negotiation. The controller has access to this information via the management interface. If a fault occurs during parallel detection, bit 4 of register 6 is set.

Register 5 is used to store the Link Partner Ability information, which is coded in the received FLPs. If the Link Partner is not auto-negotiation capable, then register 5 is updated after completion of parallel detection to reflect the speed capability of the Link Partner.

4.7.2 RE-STARTING AUTO-NEGOTIATION

Auto-negotiation can be re-started at any time by setting register 0, bit 9. Auto-negotiation will also re-start if the link is broken at any time. A broken link is caused by signal loss. This may occur because of a cable break, or because of an interruption in the signal transmitted by the Link Partner. Auto-negotiation resumes in an attempt to determine the new link configuration.

If the management entity re-starts Auto-negotiation by writing to bit 9 of the control register, the LAN8700/LAN8700i will respond by stopping all transmission/receiving operations. Once the break_link_timer is done, in the Auto-negotiation state-machine (approximately 1200ms) the auto-negotiation will re-start. The Link Partner will have also dropped the link due to lack of a received signal, so it too will resume auto-negotiation.

4.7.3 DISABLING AUTO-NEGOTIATION

Auto-negotiation can be disabled by setting register 0, bit 12 to zero. The device will then force its speed of operation to reflect the information in register 0, bit 13 (speed) and register 0, bit 8 (duplex). The speed and duplex bits in register 0 should be ignored when auto-negotiation is enabled.

4.7.4 HALF VS. FULL DUPLEX

Half Duplex operation relies on the CSMA/CD (Carrier Sense Multiple Access / Collision Detect) protocol to handle network traffic and collisions. In this mode, the carrier sense signal, CRS, responds to both transmit and receive activity. In this mode, If data is received while the PHY is transmitting, a collision results.

In Full Duplex mode, the PHY is able to transmit and receive data simultaneously. In this mode, CRS responds only to receive activity. The CSMA/CD protocol does not apply and collision detection is disabled.

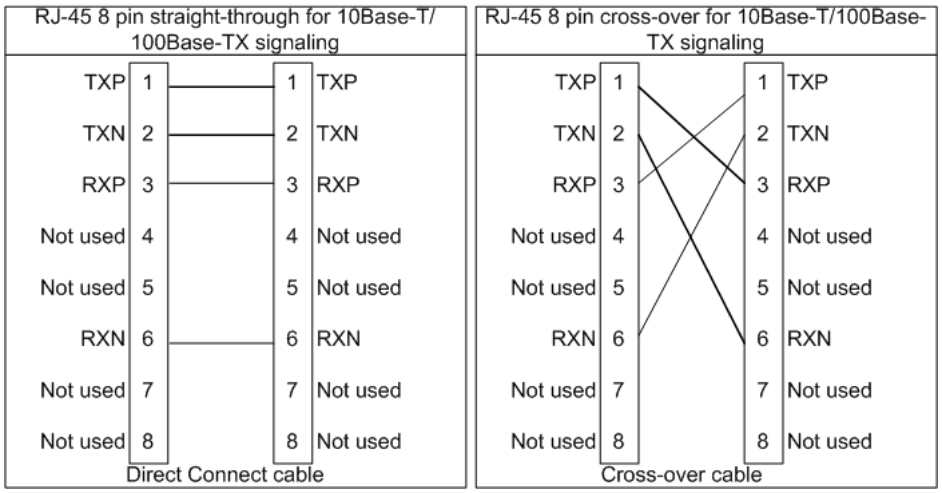
4.8 HP Auto-MDIX

HP Auto-MDIX facilitates the use of CAT-3 (10 Base-T) or CAT-5 (100 Base-T) media UTP interconnect cable without consideration of interface wiring scheme. If a user plugs in either a direct connect LAN cable, or a cross-over patch cable, as shown in FIGURE 4-4: on page 24, the Microchip LAN8700/LAN8700i Auto-MDIX PHY is capable of configuring the TXP/TXN and RXP/RXN pins for correct transceiver operation.

The internal logic of the device detects the TX and RX pins of the connecting device. Since the RX and TX line pairs are interchangeable, special PCB design considerations are needed to accommodate the symmetrical magnetics and termination of an Auto-MDIX design.

The Auto-MDIX function can be disabled through an internal register.

FIGURE 4-4: DIRECT CABLE CONNECTION VS. CROSS-OVER CABLE CONNECTION



4.9 Internal +1.8V Regulator Disable

One feature of the flexPWR technology is the ability to configure the internal 1.8V regulator off. When the regulator is disabled, external 1.8V must be supplied to VDD_CORE. This makes it possible to reduce total system power, since an external switching regulator with greater efficiency than the internal linear regulator may be used to provide the +1.8V to the PHY circuitry.

4.9.1 DISABLE THE INTERNAL +1.8V REGULATOR

To disable the +1.8V internal regulator, a pullup strapping resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) is connected from RXCLK/REGOFF to VDDIO. At power-on, after both VDDIO and VDDA are within specification, the PHY will sample the RXCLK/REGOFF pin to determine if the internal regulator should turn on. If the pin is sampled at a voltage greater than V_{IH}, then the internal regulator is disabled, and the system must supply +1.8V to the VDD_CORE pin. The voltage at VDD33 must be at least 2.64V (0.8 * 3.3V) before voltage is applied to VDD_CORE. As described in Section 4.9.2, when the RXCLK/REGOFF pin is left floating or connected to VSS, then the internal regulator is enabled and the system does not supply +1.8V to the VDD_CORE pin.

When the +1.8V internal regulator is disabled, a 0.1uF capacitor must be added at the VDD_CORE pin and placed close to the PHY to decouple the external power supply.

4.9.2 ENABLE THE INTERNAL +1.8V REGULATOR

The 1.8V for VDD_CORE is supplied by the on-chip regulator unless the PHY is configured for regulator off mode using the RX_CLK/REGOFF pin as described in Section 4.9.1. By default, the internal +1.8V regulator is enabled when the RXCLK/REGOFF pin is floating. As shown in Table 7-11, an internal pull-down resistor straps the regulator on if the RXCLK/REGOFF pin is floating.

During VDDIO and VDDA power-on, if the RXCLK/REGOFF pin is sampled below V_{IL}, then the internal +1.8V regulator will turn on and operate with power from the VDD33 pin.

When using the internal linear regulator, a 4.7uF bypass capacitor with ESR < 1ohm and a 0.1uF capacitor must always be added to VDD_CORE and placed close to the PHY to ensure stability of the internal regulator.

4.10 nINT/TX_ER/TXD4 Strapping

The nINT, TX_ER, and TXD4 functions share a common pin. There are two functional modes for this pin, the TX_ER/TXD4 mode and nINT (interrupt) mode. The RXD3/nINTSEL pin is used to select one of these two functional modes.

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The RXD3/nINTSEL pin is latched on the rising edge of the nRST. The system designer must float the nINTSEL pin to put the nINT/TX_ER/TXD4 pin into nINT mode or pull-low to VSS with an external resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) to set the device in TX_ER/TXD4 mode. The default setting is to float the pin high for nINT mode.

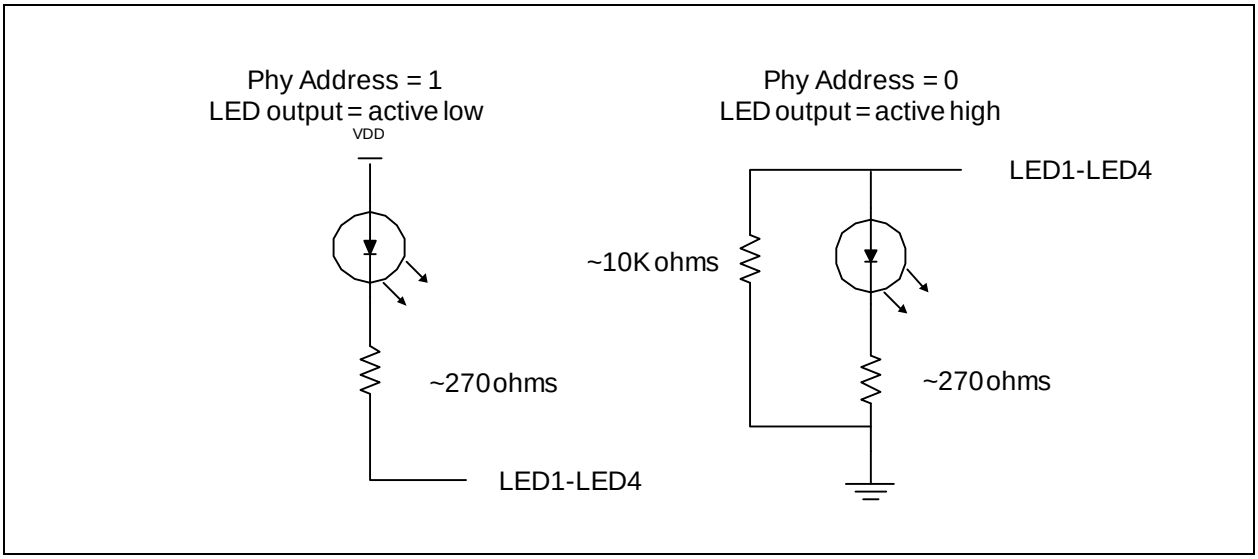
4.11 PHY Address Strapping and LED Output Polarity Selection

The PHY ADDRESS bits are latched on the rising edge of the internal reset (nRESET). The 5-bit address word[0:4] is input on the PHYAD[0:4] pins. The default setting is all high 5'b1_1111.

The address lines are strapped as defined in the diagram below. The LED outputs will automatically change polarity based on the presence of an external pull-down resistor. If the LED pin is pulled high (by an internal 100K pull-up resistor) to select a logical high PHY address, then the LED output will be active low. If the LED pin is pulled low (by an external pull-down resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) to select a logical low PHY address, the LED output will then be an active high output.

To set the PHY address on the LED pins without LEDs or on the CRS pin, float the pin to set the address high or pull-down the pin with an external resistor (see Table 4-3, “Boot Strapping Configuration Resistors,” on page 25) to GND to set the address low. See Figure 4-5, "PHY Address Strapping on LEDs":

FIGURE 4-5: PHY ADDRESS STRAPPING ON LEDS



4.12 Variable Voltage I/O

The Digital I/O pins on the LAN8700/LAN8700i are variable voltage to take advantage of low power savings from shrinking technologies. These pins can operate from a low I/O voltage of +1.8V-10% up to +3.3V+10%. Due to this low voltage feature addition, the system designer needs to take consideration as for two aspects of their design. Boot strapping configuration and I/O voltage stability.

4.12.1 BOOT STRAPPING CONFIGURATION

Due to a lower I/O voltage, a lower strapping resistor needs to be used to ensure the strapped configuration is latched into the PHY device at power-on reset.

TABLE 4-3: BOOT STRAPPING CONFIGURATION RESISTORS

I/O Voltage	Pull-up/Pull-down Resistor
3.0 to 3.6	10k ohm resistor
2.0 to 3.0	7.5k ohm resistor
1.6 to 2.0	5k ohm resistor

4.12.2 I/O VOLTAGE STABILITY

The I/O voltage the System Designer applies on VDDIO needs to maintain its value with a tolerance of ± 10%. Varying the voltage up or down, after the PHY has completed power-on reset can cause errors in the PHY operation.

4.13 PHY Management Control

The Management Control module includes 3 blocks:

- Serial Management Interface (SMI)
- Management Registers Set
- Interrupt

4.13.1 SERIAL MANAGEMENT INTERFACE (SMI)

The Serial Management Interface is used to control the LAN8700/LAN8700i and obtain its status. This interface supports registers 0 through 6 as required by Clause 22 of the 802.3 standard, as well as “vendor-specific” registers 16 to 31 allowed by the specification. Non-supported registers (7 to 15) will be read as hexadecimal “FFFF”.

At the system level there are 2 signals, MDIO and MDC where MDIO is bi-directional open-drain and MDC is the clock.

A special feature (enabled by register 17 bit 3) forces the PHY to disregard the PHY-Address in the SMI packet causing the PHY to respond to any address. This feature is useful in multi-PHY applications and in production testing, where the same register can be written in all the PHYs using a single write transaction.

The MDC signal is an aperiodic clock provided by the station management controller (SMC). The MDIO signal receives serial data (commands) from the controller SMC, and sends serial data (status) to the SMC. The minimum time between edges of the MDC is 160 ns. There is no maximum time between edges.

The minimum cycle time (time between two consecutive rising or two consecutive falling edges) is 400 ns. These modest timing requirements allow this interface to be easily driven by the I/O port of a microcontroller.

The data on the MDIO line is latched on the rising edge of the MDC. The frame structure and timing of the data is shown in Figure 4-6 and Figure 4-7.

The timing relationships of the MDIO signals are further described in Section 6.1, "Serial Management Interface (SMI) Timing," on page 48.

FIGURE 4-6: MDIO TIMING AND FRAME STRUCTURE - READ CYCLE

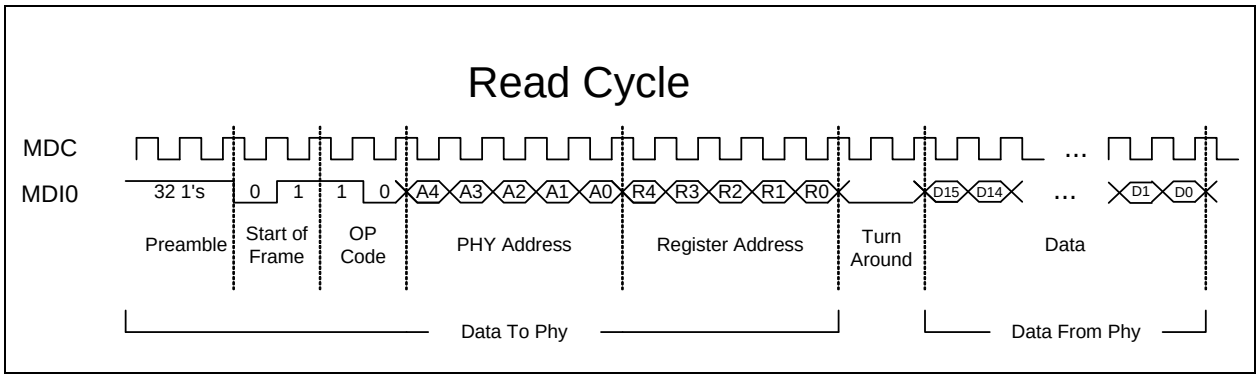


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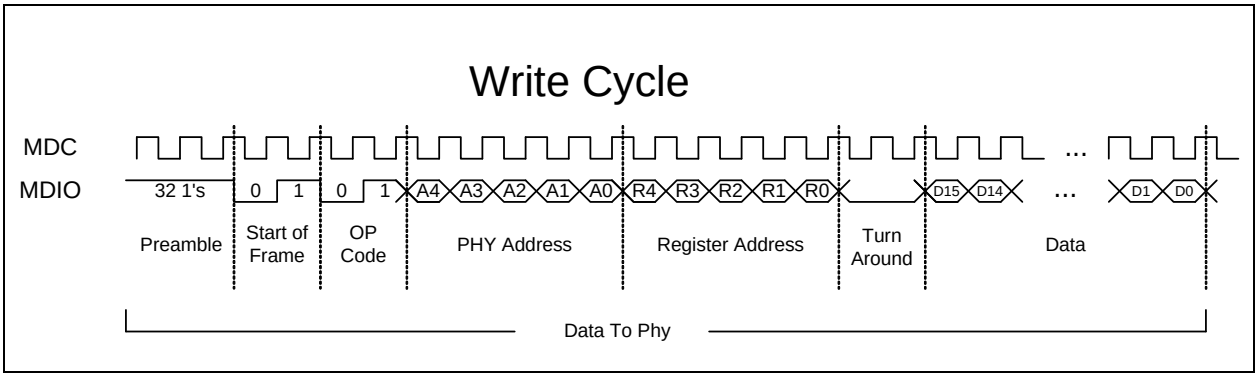
FIGURE 4-7: MDIO TIMING AND FRAME STRUCTURE - WRITE CYCLE



5.0 REGISTERS

TABLE 5-1: CONTROL REGISTER: REGISTER 0 (BASIC)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	Loopback	Speed Select	A/N Enable	Power Down	Isolate	Restart A/N	Duplex Mode	Collision Test	Reserved						

TABLE 5-2: STATUS REGISTER: REGISTER 1 (BASIC)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
100Base-T4	100Base-TX Full Duplex	100Base-TX Half Duplex	10Base-T Full Duplex	10Base-T Half Duplex	Reserved					A/N Complete	Remote Fault	A/N Ability	Link Status	Jabber Detect	Extended Capability

TABLE 5-3: PHY ID 1 REGISTER: REGISTER 2 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY ID Number (Bits 3-18 of the Organizationally Unique Identifier - OUI)															

TABLE 5-4: PHY ID 2 REGISTER: REGISTER 3 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY ID Number (Bits 19-24 of the Organizationally Unique Identifier - OUI)						Manufacturer Model Number						Manufacturer Revision Number			

TABLE 5-5: AUTO-NEGOTIATION ADVERTISEMENT: REGISTER 4 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Next Page	Reserved	Remote Fault	Reserved	Pause Operation		100Base-T4	100Base-TX Full Duplex	100Base-TX	10Base-T Full Duplex	10Base-T	IEEE 802.3 Selector Field				

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TABLE 5-6: AUTO-NEGOTIATION LINK PARTNER BASE PAGE ABILITY REGISTER: REGISTER 5 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Next Page	Acknowledge	Remote Fault	Reserved		Pause	100Base-T4	100Base-TX Full Duplex	100Base-TX	10Base-T Full Duplex	10Base-T	IEEE 802.3 Selector Field				

TABLE 5-7: AUTO-NEGOTIATION EXPANSION REGISTER: REGISTER 6 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											Parallel Detect Fault	Link Partner Next Page Able	Next Page Able	Page Received	Link Partner A/N Able

TABLE 5-8: AUTO-NEGOTIATION LINK PARTNER NEXT PAGE TRANSMIT REGISTER: REGISTER 7 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Note: Next Page capability is not supported.

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TABLE 5-9: REGISTER 8 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEEE Reserved															

TABLE 5-10: REGISTER 9 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEEE Reserved															

TABLE 5-11: REGISTER 10 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEEE Reserved															

TABLE 5-12: REGISTER 11 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEEE Reserved															

TABLE 5-13: REGISTER 12 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEEE Reserved															

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TABLE 5-14: REGISTER 13 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEEE Reserved															

TABLE 5-15: REGISTER 14 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEEE Reserved															

TABLE 5-16: REGISTER 15 (EXTENDED)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEEE Reserved															

TABLE 5-17: SILICON REVISION REGISTER 16: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Silicon Revision				Reserved					

TABLE 5-18: MODE CONTROL/ STATUS REGISTER 17: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		EDPWRDOWN	RSVD	LOWSQEN	MDPREBP	FARLOOPBACK	RSVD		ALTINT	RSVD		PHYADBP	Force Good Link Status	ENERGYON	RSVD

RSVD = Reserved

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TABLE 5-19: SPECIAL MODES REGISTER 18: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	MIIMODE	Reserved						MODE			PHYAD				

TABLE 5-20: RESERVED REGISTER 19: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

TABLE 5-21: REGISTER 24: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

TABLE 5-22: REGISTER 25: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

TABLE 5-23: SYMBOL ERROR COUNTER REGISTER 26: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol Error Counter															

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TABLE 5-24: SPECIAL CONTROL/STATUS INDICATIONS REGISTER 27: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AMDIXCTRL	Reserved	CH_SELECT	Reserved	SQEOFF	Reserved						XPOL	Reserved			

TABLE 5-25: SPECIAL INTERNAL TESTABILITY CONTROL REGISTER 28: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

TABLE 5-26: INTERRUPT SOURCE FLAGS REGISTER 29: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								INT7	INT6	INT5	INT4	INT3	INT2	INT1	Reserved

TABLE 5-27: INTERRUPT MASK REGISTER 30: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								Mask Bits							Reserved

TABLE 5-28: PHY SPECIAL CONTROL/STATUS REGISTER 31: VENDOR-SPECIFIC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			Autodone	Reserved					Enable 4B5B	Reserved	Speed Indication			Reserved	Scramble Disable

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5.1 SMI Register Mapping

The following registers are supported (register numbers are in decimal):

TABLE 5-29: SMI REGISTER MAPPING

Register #	Description	Group
0	Basic Control Register	Basic
1	Basic Status Register	Basic
2	PHY Identifier 1	Extended
3	PHY Identifier 2	Extended
4	Auto-Negotiation Advertisement Register	Extended
5	Auto-Negotiation Link Partner Ability Register	Extended
6	Auto-Negotiation Expansion Register	Extended
16	Silicon Revision Register	Vendor-specific
17	Mode Control/Status Register	Vendor-specific
18	Special Modes	Vendor-specific
20	Reserved	Vendor-specific
21	Reserved	Vendor-specific
22	Reserved	Vendor-specific
23	Reserved	Vendor-specific
26	Symbol Error Counter Register	Vendor-specific
27	Control / Status Indication Register	Vendor-specific
28	Special internal testability controls	Vendor-specific
29	Interrupt Source Register	Vendor-specific
30	Interrupt Mask Register	Vendor-specific
31	PHY Special Control/Status Register	Vendor-specific

5.2 SMI Register Format

The mode key is as follows:

- RW = Read/write,
- SC = Self clearing,
- WO = Write only,
- RO = Read only,
- LH = Latch high, clear on read of register,
- LL = Latch low, clear on read of register,
- NASR = Not Affected by Software Reset
- X = Either a 1 or 0.

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TABLE 5-30: REGISTER 0 - BASIC CONTROL

Address	Name	Description	Mode	Default
0.15	Reset	1 = software reset. Bit is self-clearing. For best results, when setting this bit do not set other bits in this register. The configuration (as described in Section 5.4.9.2) is set from the register bit values, and not from the mode pins.	RW/ SC	0
0.14	Loopback	1 = loopback mode, 0 = normal operation	RW	0
0.13	Speed Select	1 = 100Mbps, 0 = 10Mbps. Ignored if Auto Negotiation is enabled (0.12 = 1).	RW	Set by MODE[2:0] bus
0.12	Auto-Negotiation Enable	1 = enable auto-negotiate process (overrides 0.13 and 0.8) 0 = disable auto-negotiate process	RW	Set by MODE[2:0] bus
0.11	Power Down	1 = General power down mode, 0 = normal operation	RW	0
0.10	Isolate	1 = electrical isolation of PHY from MII 0 = normal operation	RW	0
0.9	Restart Auto-Negotiate	1 = restart auto-negotiate process 0 = normal operation. Bit is self-clearing.	RW/ SC	0
0.8	Duplex Mode	1 = Full duplex, 0 = Half duplex. Ignored if Auto Negotiation is enabled (0.12 = 1).	RW	Set by MODE[2:0] bus
0.7	Collision Test	1 = enable COL test, 0 = disable COL test	RW	0
0.6:0	Reserved		RO	0

TABLE 5-31: REGISTER 1 - BASIC STATUS

Address	Name	Description	Mode	Default
1.15	100Base-T4	1 = T4 able, 0 = no T4 ability	RO	0
1.14	100Base-TX Full Duplex	1 = TX with full duplex, 0 = no TX full duplex ability	RO	1
1.13	100Base-TX Half Duplex	1 = TX with half duplex, 0 = no TX half duplex ability	RO	1
1.12	10Base-T Full Duplex	1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability	RO	1
1.11	10Base-T Half Duplex	1 = 10Mbps with half duplex 0 = no 10Mbps with half duplex ability	RO	1
1.10:6	Reserved			
1.5	Auto-Negotiate Complete	1 = auto-negotiate process completed 0 = auto-negotiate process not completed	RO	0
1.4	Remote Fault	1 = remote fault condition detected 0 = no remote fault	RO/ LH	0
1.3	Auto-Negotiate Ability	1 = able to perform auto-negotiation function 0 = unable to perform auto-negotiation function	RO	1
1.2	Link Status	1 = link is up, 0 = link is down	RO/ LL	X
1.1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO/ LH	X
1.0	Extended Capabilities	1 = supports extended capabilities registers 0 = does not support extended capabilities registers	RO	1

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TABLE 5-32: REGISTER 2 - PHY IDENTIFIER 1

Address	Name	Description	Mode	Default
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively. OUI=00800Fh	RW	0007h

TABLE 5-33: REGISTER 3 - PHY IDENTIFIER 2

Address	Name	Description	Mode	Default
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the OUI.	RW	C0h
3.9:4	Model Number	Six-bit manufacturer's model number.	RW	0Ch
3.3:0	Revision Number	Four-bit manufacturer's revision number.	RW	4h

TABLE 5-34: REGISTER 4 - AUTO NEGOTIATION ADVERTISEMENT

Address	Name	Description	Mode	Default
4.15	Next Page	1 = next page capable, 0 = no next page ability This Phy does not support next page ability.	RO	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = remote fault detected, 0 = no remote fault	RW	0
4.12	Reserved			
4.11:10	Pause Operation	00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device	R/W	00
4.9	100Base-T4	1 = T4 able, 0 = no T4 ability This Phy does not support 100Base-T4.	RO	0
4.8	100Base-TX Full Duplex	1 = TX with full duplex, 0 = no TX full duplex ability	RW	Set by MODE[2:0] bus
4.7	100Base-TX	1 = TX able, 0 = no TX ability	RW	1
4.6	10Base-T Full Duplex	1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability	RW	Set by MODE[2:0] bus
4.5	10Base-T	1 = 10Mbps able, 0 = no 10Mbps ability	RW	Set by MODE[2:0] bus
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	00001

TABLE 5-35: REGISTER 5 - AUTO NEGOTIATION LINK PARTNER ABILITY

Address	Name	Description	Mode	Default
5.15	Next Page	1 = "Next Page" capable, 0 = no "Next Page" ability This Phy does not support next page ability.	RO	0
5.14	Acknowledge	1 = link code word received from partner 0 = link code word not yet received	RO	0
5.13	Remote Fault	1 = remote fault detected, 0 = no remote fault	RO	0
5.12:11	Reserved		RO	0

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TABLE 5-35: REGISTER 5 - AUTO NEGOTIATION LINK PARTNER ABILITY (CONTINUED)

Address	Name	Description	Mode	Default
5.10	Pause Operation	1 = Pause Operation is supported by remote MAC, 0 = Pause Operation is not supported by remote MAC	RO	0
5.9	100Base-T4	1 = T4 able, 0 = no T4 ability. This Phy does not support T4 ability.	RO	0
5.8	100Base-TX Full Duplex	1 = TX with full duplex, 0 = no TX full duplex ability	RO	0
5.7	100Base-TX	1 = TX able, 0 = no TX ability	RO	0
5.6	10Base-T Full Duplex	1 = 10Mbps with full duplex 0 = no 10Mbps with full duplex ability	RO	0
5.5	10Base-T	1 = 10Mbps able, 0 = no 10Mbps ability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	00001

TABLE 5-36: REGISTER 6 - AUTO NEGOTIATION EXPANSION

Address	Name	Description	Mode	Default
6.15:5	Reserved		RO	0
6.4	Parallel Detection Fault	1 = fault detected by parallel detection logic 0 = no fault detected by parallel detection logic	RO/ LH	0
6.3	Link Partner Next Page Able	1 = link partner has next page ability 0 = link partner does not have next page ability	RO	0
6.2	Next Page Able	1 = local device has next page ability 0 = local device does not have next page ability	RO	0
6.1	Page Received	1 = new page received 0 = new page not yet received	RO/ LH	0
6.0	Link Partner Auto-Negotiation Able	1 = link partner has auto-negotiation ability 0 = link partner does not have auto-negotiation ability	RO	0

TABLE 5-37: REGISTER 16 - SILICON REVISION

Address	Name	Description	Mode	Default
16.15:10	Reserved		RO	0
16.9:6	Silicon Revision	Four-bit silicon revision identifier.	RO	0001
16.5:0	Reserved		RO	0

TABLE 5-38: REGISTER 17 - MODE CONTROL/STATUS

Address	Name	Description	Mode	Default
17.15:14	Reserved	Write as 0; ignore on read.	RW	0
17.13	EDPWRDOWN	Enable the Energy Detect Power-Down mode: 0 = Energy Detect Power-Down is disabled 1 = Energy Detect Power-Down is enabled	RW	0
17.12	Reserved	Write as 0, ignore on read	RW	0
17.11	LOWSQEN	The Low_Squelch signal is equal to LOWSQEN AND EDPWRDOWN. Low_Squelch = 1 implies a lower threshold (more sensitive). Low_Squelch = 0 implies a higher threshold (less sensitive).	RW	0

TABLE 5-38: REGISTER 17 - MODE CONTROL/STATUS (CONTINUED)

Address	Name	Description	Mode	Default
17.10	MDPREBP	Management Data Preamble Bypass: 0 – detect SMI packets with Preamble 1 – detect SMI packets without preamble	RW	0
17.9	FARLOOPBACK	Force the module to the FAR Loop Back mode, i.e. all the received packets are sent back simultaneously (in 100Base-TX only). This bit is only active in RMII mode. In this mode the user needs to supply a 50MHz clock to the PHY. This mode works even if MII Isolate (0.10) is set.	RW	0
17.8:7	Reserved	Write as 0, ignore on read.	RW	00
17.6	ALTINT	Alternate Interrupt Mode. 0 = Primary interrupt system enabled (Default). 1 = Alternate interrupt system enabled. See Section 5.3, "Interrupt Management," on page 40.	RW	0
17.5:4	Reserved	Write as 0, ignore on read.	RW	00
17.3	PHYADBP	1 = PHY disregards PHY address in SMI access write.	RW	0
17.2	Force Good Link Status	0 = normal operation; 1 = force 100TX- link active; **Note:** This bit should be set only during lab testing	RW	0
17.1	ENERGYON	ENERGYON – indicates whether energy is detected on the line (see Section 5.4.5.2, "Energy Detect Power-Down," on page 43); it goes to “0” if no valid energy is detected within 256ms. Reset to “1” by hardware reset, unaffected by SW reset.	RO	X
17.0	Reserved	Write as 0. Ignore on read.	RW	0

TABLE 5-39: REGISTER 18 - SPECIAL MODES

Address	Name	Description	Mode	Default
18.15	Reserved	Write as 0, ignore on read.	RW	0
18.14	MIIMODE	**MII Mode**: Reflects the mode of the digital interface: 0 – MII interface. 1 – RMII interface **Note:** When writing to this register, the default value of this bit must always be written back.	RW, NASR	Note 5-1
18.13:8	Reserved	Write as 0, ignore on read.	RW, NASR	000000
18.7:5	MODE	PHY Mode of operation. Refer to Section 5.4.9.2, "Mode Bus – MODE[2:0]," on page 46 for more details.	RW, NASR	XXX EVB8700 default 111
18.4:0	PHYAD	PHY Address. The PHY Address is used for the SMI address and for the initialization of the Cipher (Scrambler) key. Refer to Section 5.4.9.1, "Physical Address Bus - PHYAD[4:0]," on page 46 for more details.	RW, NASR	PHYAD EVB8700 default 11111

Note 5-1 The default value of this field is determined by the strapping of the COL/RMII/CRS_DV pin. Refer to Section 4.6.3, "MII vs. RMII Configuration," on page 21 for additional information.

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TABLE 5-40: REGISTER 26 - SYMBOL ERROR COUNTER

Address	Name	Description	Mode	Default
26.15:0	Sym_Err_Cnt	100Base-TX receiver-based error register that increments when an invalid code symbol is received including IDLE symbols. The counter is incremented only once per packet, even when the received packet contains more than one symbol error. The 16-bit register counts up to 65,536 (2^{16}) and rolls over to 0 if incremented beyond that value. This register is cleared on reset, but is not cleared by reading the register. It does not increment in 10Base-T mode.	RO	0

TABLE 5-41: REGISTER 27 - SPECIAL CONTROL/STATUS INDICATIONS

Address	Name	Description	Mode	Default
27.15	AMDIXCTRL	HP Auto-MDIX control 0 - Auto-MDIX enable 1 - Auto-MDIX disabled (use 27.13 to control channel)	RW	0
27.14	Reserved	Reserved	RW	0
27.13	CH_SELECT	Manual Channel Select 0 - MDI -TX transmits RX receives 1 - MDIX -TX receives RX transmits	RW	0
27.12	Reserved	Write as 0. Ignore on read.	RW	0
27:11	SQEOFF	Disable the SQE (Signal Quality Error) test (Heartbeat): 0 - SQE test is enabled. 1 - SQE test is disabled.	RW, NASR	0
27.10:5	Reserved	Write as 0. Ignore on read.	RW	000000
27.4	XPOL	Polarity state of the 10Base-T: 0 - Normal polarity 1 - Reversed polarity	RO	0
27.3:0	Reserved	Reserved	RO	XXXXb

TABLE 5-42: REGISTER 28 - SPECIAL INTERNAL TESTABILITY CONTROLS

Address	Name	Description	Mode	Default
28.15:0	Reserved	Do not write to this register. Ignore on read.	RW	N/A

TABLE 5-43: REGISTER 29 - INTERRUPT SOURCE FLAGS

Address	Name	Description	Mode	Default
29.15:8	Reserved	Ignore on read.	RO/ LH	0
29.7	INT7	1 = ENERGYON generated 0 = not source of interrupt	RO/ LH	X
29.6	INT6	1 = Auto-Negotiation complete 0 = not source of interrupt	RO/ LH	X
29.5	INT5	1 = Remote Fault Detected 0 = not source of interrupt	RO/ LH	X
29.4	INT4	1 = Link Down (link status negated) 0 = not source of interrupt	RO/ LH	X
29.3	INT3	1 = Auto-Negotiation LP Acknowledge 0 = not source of interrupt	RO/ LH	X
29.2	INT2	1 = Parallel Detection Fault 0 = not source of interrupt	RO/ LH	X

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TABLE 5-43: REGISTER 29 - INTERRUPT SOURCE FLAGS (CONTINUED)

Address	Name	Description	Mode	Default
29.1	INT1	1 = Auto-Negotiation Page Received 0 = not source of interrupt	RO/ LH	X
29.0	Reserved	Ignore on read.	RO/ LH	0

TABLE 5-44: REGISTER 30 - INTERRUPT MASK

Address	Name	Description	Mode	Default
30.15:8	Reserved	Write as 0; ignore on read.	RO	0
30.7:1	Mask Bits	1 = interrupt source is enabled 0 = interrupt source is masked	RW	0
30.0	Reserved	Write as 0; ignore on read	RO	0

TABLE 5-45: REGISTER 31 - PHY SPECIAL CONTROL/STATUS

Address	Name	Description	Mode	Default
31.15:13	Reserved	Write as 0, ignore on read.	RW	0
31.12	Autodone	Auto-negotiation done indication: 0 = Auto-negotiation is not done or disabled (or not active) 1 = Auto-negotiation is done **Note:** This is a duplicate of register 1.5, however reads to register 31 do not clear status bits.	RO	0
31.11:10	Reserved	Write as 0, ignore on Read.	RW	XX
31.9:7	Reserved	Write as 0, ignore on Read.	RW	0
31.6	Enable 4B5B	0 = Bypass encoder/decoder. 1 = enable 4B5B encoding/decoding. MAC Interface must be configured in MII mode.	RW	1
31.5	Reserved	Write as 0, ignore on Read.	RW	0
31.4:2	Speed Indication	HCDSPEED value: [001]=10Mbps Half-duplex [101]=10Mbps Full-duplex [010]=100Base-TX Half-duplex [110]=100Base-TX Full-duplex	RO	XXX
31.1	Reserved	Write as 0; ignore on Read	RW	0
31.0	Scramble Disable	0 = enable data scrambling 1 = disable data scrambling,	RW	0

5.3 Interrupt Management

The Management interface supports an interrupt capability that is not a part of the IEEE 802.3 specification. It generates an active low asynchronous interrupt signal on the nINT output whenever certain events are detected as setup by the Interrupt Mask Register 30.

The Interrupt system on the Microchip LAN8700/8700I has two modes, a Primary Interrupt mode and an Alternative Interrupt mode. Both systems will assert the nINT pin low when the corresponding mask bit is set, the difference is how they de-assert the output interrupt signal nINT.

The Primary interrupt mode is the default interrupt mode after a power-up or hard reset, the Alternative interrupt mode would need to be setup again after a power-up or hard reset.

5.3.1 PRIMARY INTERRUPT SYSTEM

bit The Primary Interrupt system is the default interrupt mode, (Bit 17.6 = ‘0’). The Primary Interrupt System is always selected after power-up or hard reset.

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bit To set an interrupt, set the corresponding mask bit in the interrupt Mask register 30 (see Table 5-46). Then when the event to assert nINT is true, the nINT output will be asserted.

When the corresponding Event to De-Assert nINT is true, then the nINT will be de-asserted.

TABLE 5-46: INTERRUPT MANAGEMENT

Mask	Interrupt Source Flag		Interrupt Source		Event to Assert nINT	Event to De-Assert nINT
30.7	29.7	ENERGYON	17.1	ENERGYON	Rising 17.1(5-2)	Falling 17.1 or Reading register 29
30.6	29.6	Auto-Negotiation complete	1.5	Auto-Negotiate Complete	Rising 1.5	Falling 1.5 or Reading register 29
30.5	29.5	Remote Fault Detected	1.4	Remote Fault	Rising 1.4	Falling 1.4, or Reading register 1 or Reading register 29
30.4	29.4	Link Down	1.2	Link Status	Falling 1.2	Reading register 1 or Reading register 29
30.3	29.3	Auto-Negotiation LP Acknowledge	5.14	Acknowledge	Rising 5.14	Falling 5.14 or Read register 29
30.2	29.2	Parallel Detection Fault	6.4	Parallel Detection Fault	Rising 6.4	Falling 6.4 or Reading register 6, or Reading register 29 or Re-Auto Negotiate or Link down
30.1	29.1	Auto-Negotiation Page Received	6.1	Page Received	Rising 6.1	Falling of 6.1 or Reading register 6, or Reading register 29 Re-Auto Negotiate, or Link Down.

Note 5-2 If the mask bit is enabled and nINT has been de-asserted while ENERGYON is still high, nINT will assert for 256 ms, approximately one second after ENERGYON goes low when the Cable is unplugged. To prevent an unexpected assertion of nINT, the ENERGYON interrupt mask should always be cleared as part of the ENERGYON interrupt service routine

Note: The ENERGYON bit 17.1 is defaulted to a ‘1’ at the start of the signal acquisition process, therefore the Interrupt source flag 29.7 will also read as a ‘1’ at power-up. If no signal is present, then both 17.1 and 29.7 will clear within a few milliseconds.

5.3.2 ALTERNATE INTERRUPT SYSTEM

The Alternative method is enabled by writing a ‘1’ to 17.6 (ALTINT).

To set an interrupt, set the corresponding bit of the in the Mask Register 30, (see Table 5-47).

To Clear an interrupt, either clear the corresponding bit in the Mask Register (30), this will de-assert the nINT output, or Clear the Interrupt Source, and write a ‘1’ to the corresponding Interrupt Source Flag. Writing a ‘1’ to the Interrupt Source Flag will cause the state machine to check the Interrupt Source to determine if the Interrupt Source Flag should clear or stay as a ‘1’. If the Condition to De-Assert is true, then the Interrupt Source Flag is cleared, and the nINT is also de-asserted. If the Condition to De-Assert is false, then the Interrupt Source Flag remains set, and the nINT remains asserted.

For example 30.7 is set to ‘1’ to enable the ENERGYON interrupt. After a cable is plugged in, ENERGYON (17.1) goes active and nINT will be asserted low.

To de-assert the nINT interrupt output, either.

1. Clear the ENERGYON bit (17.1), by removing the cable, then writing a ‘1’ to register 29.7.

   - Or -

2. Clear the Mask bit 30.1 by writing a ‘0’ to 30.1.

TABLE 5-47: ALTERNATIVE INTERRUPT SYSTEM MANAGEMENT TABLE

Mask	Interrupt Source Flag		Interrupt Source		Event to Assert nINT	Condition to De-Assert.	Bit to Clear nINT
30.7	29.7	ENERGYON	17.1	ENERGYON	Rising 17.1	17.1 low	29.7
30.6	29.6	Auto-Negotiation complete	1.5	Auto-Negotiate Complete	Rising 1.5	1.5 low	29.6
30.5	29.5	Remote Fault Detected	1.4	Remote Fault	Rising 1.4	1.4 low	29.5
30.4	29.4	Link Down	1.2	Link Status	Falling 1.2	1.2 high	29.4
30.3	29.3	Auto-Negotiation LP Acknowledge	5.14	Acknowledge	Rising 5.14	5.14 low	29.3
30.2	29.2	Parallel Detection Fault	6.4	Parallel Detection Fault	Rising 6.4	6.4 low	29.2
30.1	29.1	Auto-Negotiation Page Received	6.1	Page Received	Rising 6.1	6.1 low	29.1

Note: The ENERGYON bit 17.1 is defaulted to a ‘1’ at the start of the signal acquisition process, therefore the Interrupt source flag 29.7 will also read as a ‘1’ at power-up. If no signal is present, then both 17.1 and 29.7 will clear within a few milliseconds.

5.4 Miscellaneous Functions

5.4.1 CARRIER SENSE

The carrier sense is output on CRS. CRS is a signal defined by the MII specification in the IEEE 802.3u standard. The PHY asserts CRS based only on receive activity whenever the PHY is either in repeater mode or full-duplex mode. Otherwise the PHY asserts CRS based on either transmit or receive activity.

The carrier sense logic uses the encoded, unscrambled data to determine carrier activity status. It activates carrier sense with the detection of 2 non-contiguous zeros within any 10 bit span. Carrier sense terminates if a span of 10 consecutive ones is detected before a /J/K/ Start-of Stream Delimiter pair. If an SSD pair is detected, carrier sense is asserted until either /T/R/ End–of-Stream Delimiter pair or a pair of IDLE symbols is detected. Carrier is negated after the /T/ symbol or the first IDLE. If /T/ is not followed by /R/, then carrier is maintained. Carrier is treated similarly for IDLE followed by some non-IDLE symbol.

5.4.2 COLLISION DETECT

A collision is the occurrence of simultaneous transmit and receive operations. The COL output is asserted to indicate that a collision has been detected. COL remains active for the duration of the collision. COL is changed asynchronously to both RX_CLK and TX_CLK. The COL output becomes inactive during full duplex mode.

COL may be tested by setting register 0, bit 7 high. This enables the collision test. COL will be asserted within 512 bit times of TX_EN rising and will be de-asserted within 4 bit times of TX_EN falling.

In 10M mode, COL pulses for approximately 10 bit times (1us), 2us after each transmitted packet (de-assertion of TX_EN). This is the Signal Quality Error (SQE) signal and indicates that the transmission was successful. The user can disable this pulse by setting bit 11 in register 27.

5.4.3 ISOLATE MODE

The PHY data paths may be electrically isolated from the MII by setting register 0, bit 10 to a logic one. In isolation mode, the PHY does not respond to the TXD, TX_EN and TX_ER inputs. The PHY still responds to management transactions.

Isolation provides a means for multiple PHYs to be connected to the same MII without contention occurring. The PHY is not isolated on power-up (bit 0:10 = 0).

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5.4.4 LINK INTEGRITY TEST

The LAN8700/LAN8700i performs the link integrity test as outlined in the IEEE 802.3u (Clause 24-15) Link Monitor state diagram. The link status is multiplexed with the 10Mbps link status to form the reportable link status bit in Serial Management Register 1, and is driven to the LINK LED.

The DSP indicates a valid MLT-3 waveform present on the RXP and RXN signals as defined by the ANSI X3.263 TP-PMD standard, to the Link Monitor state-machine, using internal signal called DATA_VALID. When DATA_VALID is asserted the control logic moves into a Link-Ready state, and waits for an enable from the Auto Negotiation block. When received, the Link-Up state is entered, and the Transmit and Receive logic blocks become active. Should Auto Negotiation be disabled, the link integrity logic moves immediately to the Link-Up state, when the DATA_VALID is asserted.

Note that to allow the line to stabilize, the link integrity logic will wait a minimum of 330 μsec from the time DATA_VALID is asserted until the Link-Ready state is entered. Should the DATA_VALID input be negated at any time, this logic will immediately negate the Link signal and enter the Link-Down state.

When the 10/100 digital block is in 10Base-T mode, the link status is from the 10Base-T receiver logic.

5.4.5 POWER-DOWN MODES

There are 2 power-down modes for the Phy:

5.4.5.1 General Power-Down

This power-down is controlled by register 0, bit 11. In this mode the entire PHY, except the management interface, is powered-down and stays in that condition as long as bit 0.11 is HIGH. When bit 0.11 is cleared, the PHY powers up and is automatically reset.

5.4.5.2 Energy Detect Power-Down

This power-down mode is activated by setting bit 17.13 to 1. In this mode when no energy is present on the line the PHY is powered down, except for the management interface, the SQUELCH circuit and the ENERGYON logic. The ENERGYON logic is used to detect the presence of valid energy from 100Base-TX, 10Base-T, or Auto-negotiation signals

In this mode, when the ENERGYON signal is low, the PHY is powered-down, and nothing is transmitted. When energy is received - link pulses or packets - the ENERGYON signal goes high, and the PHY powers-up. It automatically resets itself into the state it had prior to power-down, and asserts the nINT interrupt if the ENERGYON interrupt is enabled. The first and possibly the second packet to activate ENERGYON may be lost.

When 17.13 is low, energy detect power-down is disabled.

5.4.6 RESET

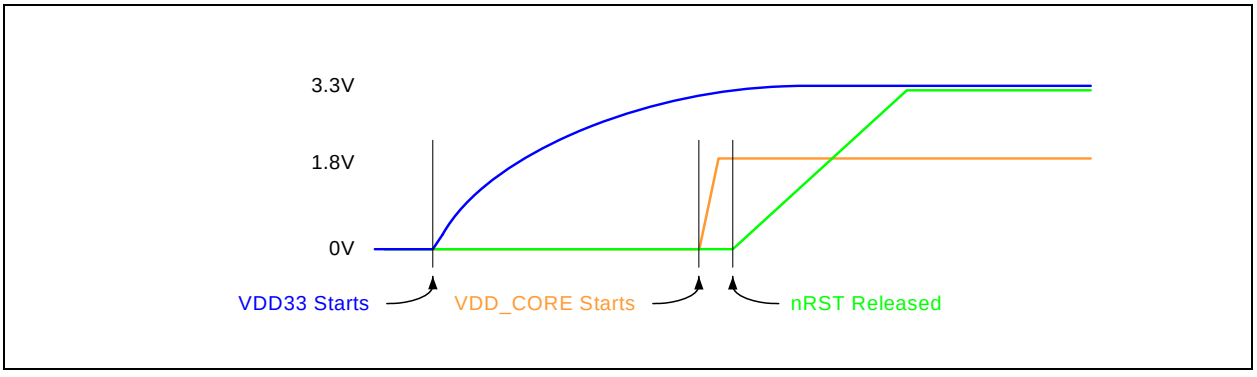
The PHY has 3 reset sources:

Hardware reset (HWRST): connected to the nRST input. At power up, nRST must not go high until after the VDDIO and VDD_CORE supplies are stable, as shown in Figure 5-1.

To initiate a hardware reset, nRST must be held LOW for at least 100 us to ensure that the Phy is properly reset, as shown in Figure 6-10.

During a Hardware reset, an external clock ***must*** be supplied to the CLKIN signal.

FIGURE 5-1: RESET TIMING DIAGRAM



Software (SW) reset: Activated by writing register 0, bit 15 high. This signal is self- clearing. After the register-write, internal logic extends the reset by 256µs to allow PLL-stabilization before releasing the logic from reset.

The IEEE 802.3u standard, clause 22 (22.2.4.1.1) states that the reset process should be completed within 0.5s from the setting of this bit.

Power-Down reset: Automatically activated when the PHY comes out of power-down mode. The internal power-down reset is extended by 256µs after exiting the power-down mode to allow the PLLs to stabilize before the logic is released from reset.

These 3 reset sources are combined together in the digital block to create the internal “general reset”, SYSRST, which is an asynchronous reset and is active HIGH. This SYSRST directly drives the PCS, DSP and MII blocks. It is also input to the Central Bias block in order to generate a short reset for the PLLs.

The SMI mechanism and registers are reset only by the Hardware and Software resets. During Power-Down, the SMI registers are not reset. Note that some SMI register bits are not cleared by Software reset – these are marked “NASR” in the register tables.

For the first 16us after coming out of reset, the MII will run at 2.5 MHz. After that it will switch to 25 MHz if auto-negotiation is enabled.

5.4.7 LED DESCRIPTION

The PHY provides four LED signals. These provide a convenient means to determine the mode of operation of the Phy. All LED signals are either active high or active low.

The four LED signals can be either active-high or active-low. Polarity depends upon the Phy address latched in on reset. The LAN8700/LAN8700i senses each Phy address bit and changes the polarity of the LED signal accordingly. If the address bit is set as level “1”, the LED polarity will be set to an active-low. If the address bit is set as level “0”, the LED polarity will be set to an active-high.

The ACTIVITY LED output is driven active when CRS is active (high). When CRS becomes inactive, the Activity LED output is extended by 128ms.

The LINK LED output is driven active whenever the PHY detects a valid link. The use of the 10Mbps or 100Mbps link test status is determined by the condition of the internally determined speed selection.

The SPEED100 LED output is driven active when the operating speed is 100Mbit/s or during Auto-negotiation. This LED will go inactive when the operating speed is 10Mbit/s or during line isolation (register 31 bit 5).

The Full-Duplex LED output is driven active low when the link is operating in Full-Duplex mode.

5.4.8 LOOPBACK OPERATION

The LAN8700/LAN8700i may be configured for near-end loopback and far loopback.

5.4.8.1 Near-end Loopback

Near-end loopback is a mode that sends the digital transmit data back out the receive data signals for testing purposes as indicated by the blue arrows in Figure 5-2.The near-end loopback mode is enabled by setting bit register 0 bit 14 to logic one.

A large percentage of the digital circuitry is operational near-end loopback mode, because data is routed through the PCS and PMA layers into the PMD sublayer before it is looped back. The COL signal will be inactive in this mode, unless collision test (bit 0.7) is active. The transmitters are powered down, regardless of the state of TXEN.

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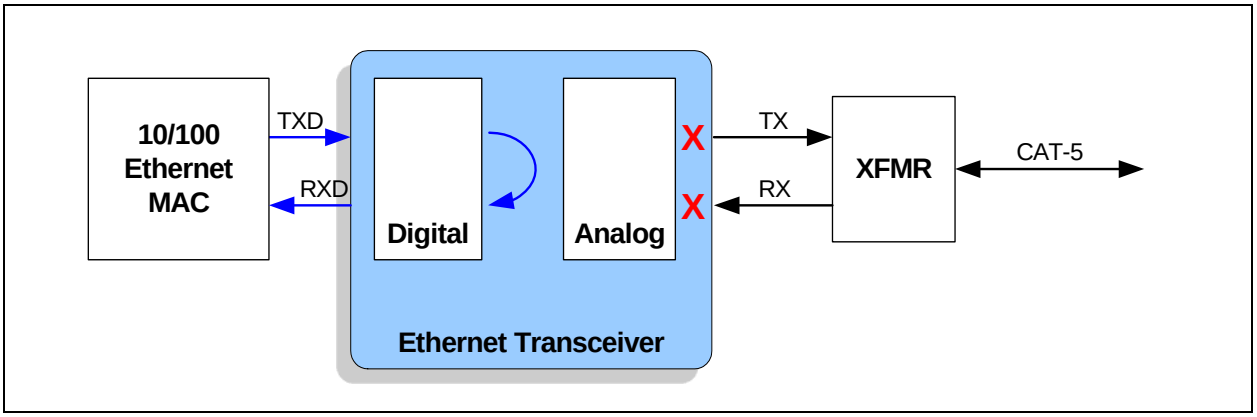
FIGURE 5-2: NEAR-END LOOPBACK BLOCK DIAGRAM

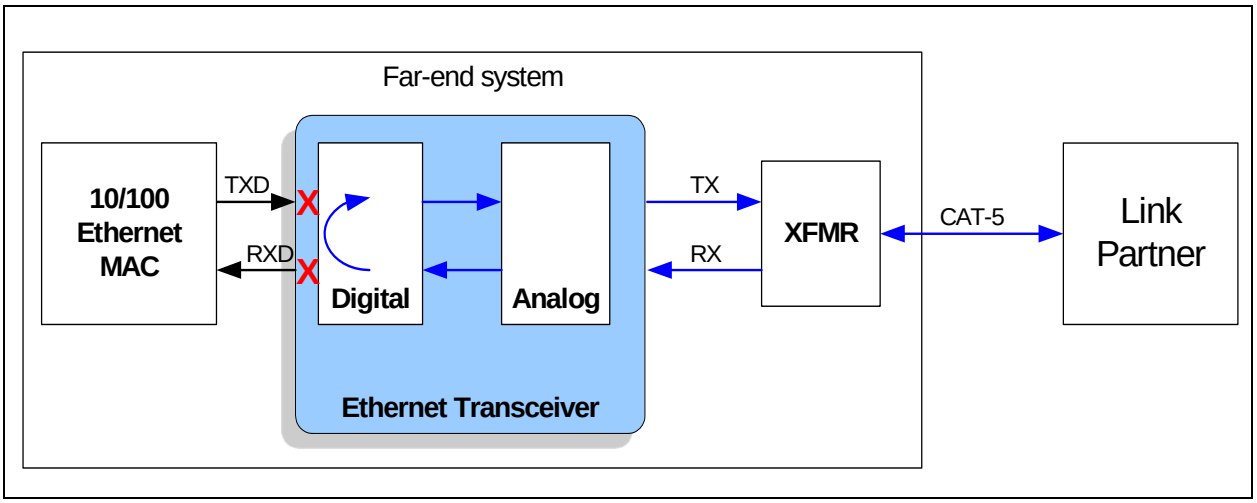


5.4.8.2 Far Loopback

Far loopback is a special test mode for MDI (analog) loopback as indicated by the blue arrows in Figure 5-3. The far loopback mode is enabled by setting bit register 17 bit 9 to logic one. In this mode, data that is received from the link partner on the MDI is looped back out to the link partner. The digital interface signals on the local MAC interface are isolated.

Note:	This special test mode is only available when operating in RMII mode.

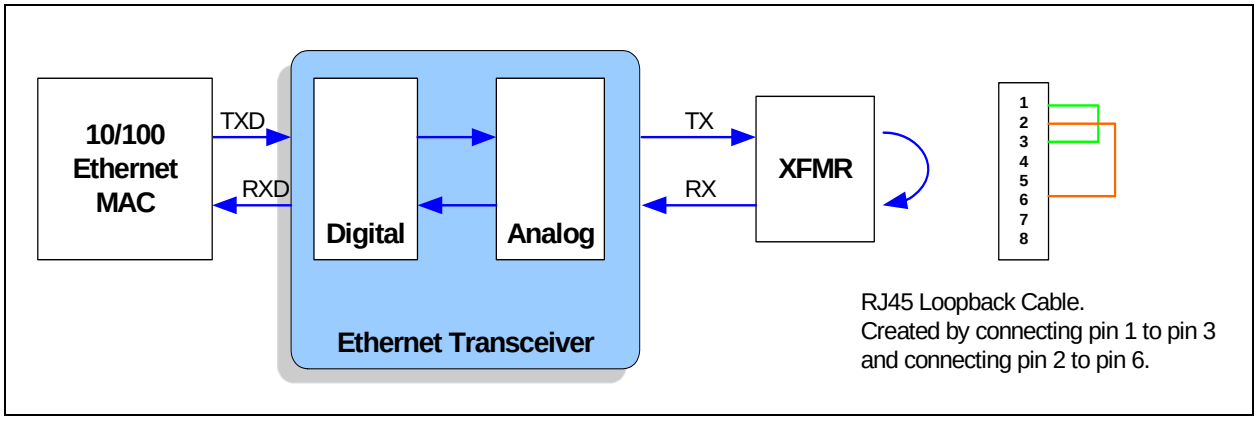
FIGURE 5-3: FAR LOOPBACK BLOCK DIAGRAM



5.4.8.3 Connector Loopback

The LAN8700/LAN8700i maintains reliable transmission over very short cables, and can be tested in a connector loopback as shown in Figure 5-4. An RJ45 loopback cable can be used to route the transmit signals an the output of the transformer back to the receiver inputs, and this loopback will work at both 10 and 100.

FIGURE 5-4: CONNECTOR LOOPBACK BLOCK DIAGRAM



5.4.9 CONFIGURATION SIGNALS

The PHY has 11 configuration signals whose inputs should be driven continuously, either by external logic or external pull-up/pull-down resistors.

5.4.9.1 Physical Address Bus - PHYAD[4:0]

The PHYAD[4:0] signals are driven high or low to give each PHY a unique address. This address is latched into an internal register at end of hardware reset. In a multi-PHY application (such as a repeater), the controller is able to manage each PHY via the unique address. Each PHY checks each management data frame for a matching address in the relevant bits. When a match is recognized, the PHY responds to that particular frame. The PHY address is also used to seed the scrambler. In a multi-PHY application, this ensures that the scramblers are out of synchronization and disperses the electromagnetic radiation across the frequency spectrum.

5.4.9.2 Mode Bus – MODE[2:0]

The MODE[2:0] bus controls the configuration of the 10/100 digital block. When the nRST pin is deasserted, the register bit values are loaded according to the MODE[2:0] pins. The 10/100 digital block is then configured by the register bit values. When a soft reset occurs (bit 0.15) as described in Table 5-30, the configuration of the 10/100 digital block is controlled by the register bit values, and the MODE[2:0] pins have no affect.

TABLE 5-48: MODE[2:0] BUS

Mode [2:0]	Mode Definitions	Default Register Bit Values	
		Register 0	Register 4
		[13,12,10,8]	[8,7,6,5]
000	10Base-T Half Duplex. Auto-negotiation disabled.	0000	N/A
001	10Base-T Full Duplex. Auto-negotiation disabled.	0001	N/A
010	100Base-TX Half Duplex. Auto-negotiation disabled. CRS is active during Transmit & Receive.	1000	N/A
011	100Base-TX Full Duplex. Auto-negotiation disabled. CRS is active during Receive.	1001	N/A
100	100Base-TX Half Duplex is advertised. Auto-negotiation enabled. CRS is active during Transmit & Receive.	1100	0100
101	Repeater mode. Auto-negotiation enabled. 100Base-TX Half Duplex is advertised. CRS is active during Receive.	1100	0100

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TABLE 5-48: MODE[2:0] BUS (CONTINUED)

Mode [2:0]	Mode Definitions	Default Register Bit Values	
		Register 0	Register 4
		[13,12,10,8]	[8,7,6,5]
110	Power Down mode. In this mode the PHY will wake-up in Power-Down mode. The PHY cannot be used when the MODE[2:0] bits are set to this mode. To exit this mode, the MODE bits in Register 18.7:5 (see Table 5-39) must be configured to some other value and a soft reset must be issued.	N/A	N/A
111	All capable. Auto-negotiation enabled.	X10X	1111

6.0 AC ELECTRICAL CHARACTERISTICS

The timing diagrams and limits in this section define the requirements placed on the external signals of the Phy.

6.1 Serial Management Interface (SMI) Timing

The Serial Management Interface is used for status and control as described in Section 4.13.

FIGURE 6-1: SMI TIMING DIAGRAM

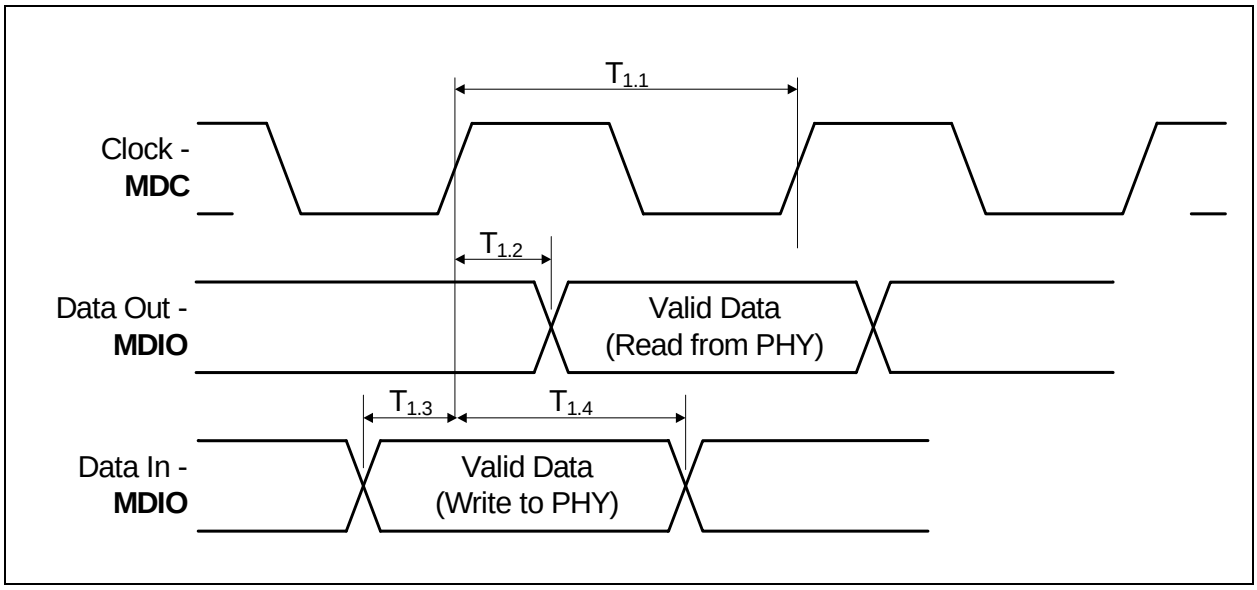

TABLE 6-1: SMI TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T1.1	MDC minimum cycle time	400			ns	
T1.2	MDC to MDIO (Read from PHY) delay	0		300	ns	
T1.3	MDIO (Write to PHY) to MDC setup	10			ns	
T1.4	MDIO (Write to PHY) to MDC hold	10			ns	

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6.2 MII 10/100Base-TX/RX Timings

6.2.1 MII 100BASE-T TX/RX TIMINGS

6.2.1.1 100M MII Receive Timing

FIGURE 6-2: 100M MII RECEIVE TIMING DIAGRAM

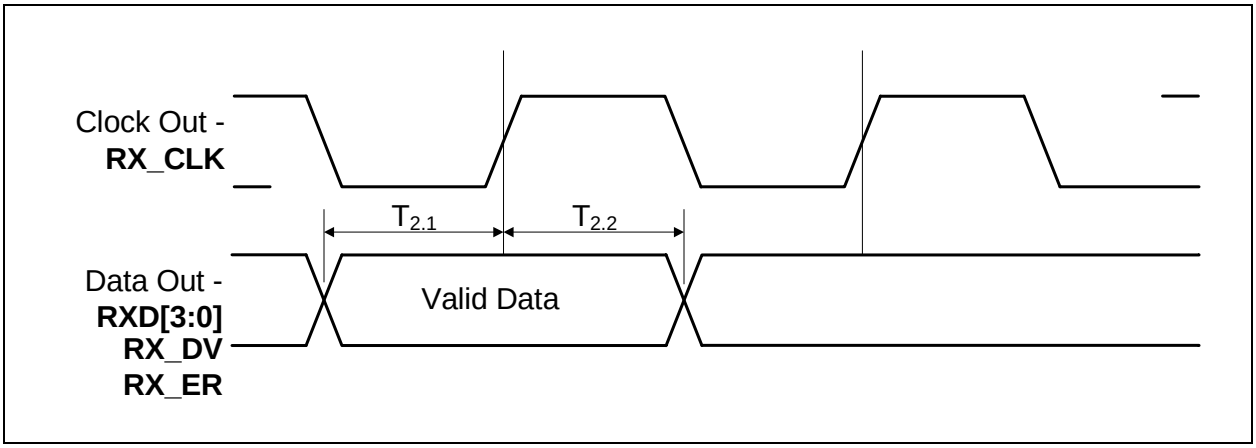

TABLE 6-2: 100M MII RECEIVE TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T2.1	Receive signals setup to RX_CLK rising	10			ns	
T2.2	Receive signals hold from RX_CLK rising	10			ns	
	RX_CLK frequency		25		MHz	
	RX_CLK Duty-Cycle		40		%	

6.2.1.2 100M MII Transmit Timing

FIGURE 6-3: 100M MII TRANSMIT TIMING DIAGRAM

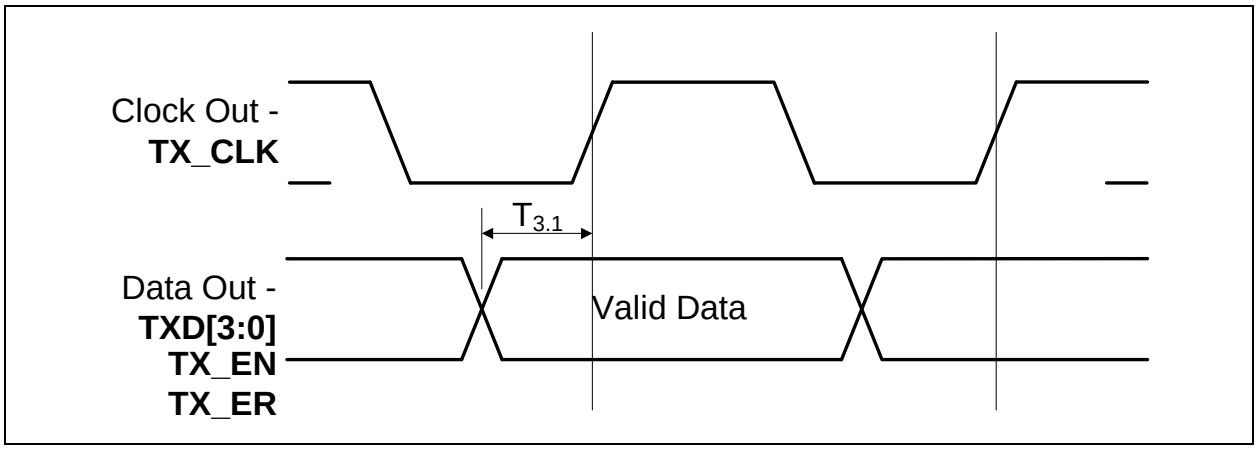

TABLE 6-3: 100M MII TRANSMIT TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T3.1	Transmit signals required setup to TX_CLK rising	12			ns	
	Transmit signals required hold after TX_CLK rising	0			ns	
	TX_CLK frequency		25		MHz	
	TX_CLK Duty-Cycle		40		%	

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6.2.2 MII 10BASE-T TX/RX TIMINGS

6.2.2.1 10M MII Receive Timing

FIGURE 6-4: 10M MII RECEIVE TIMING DIAGRAM

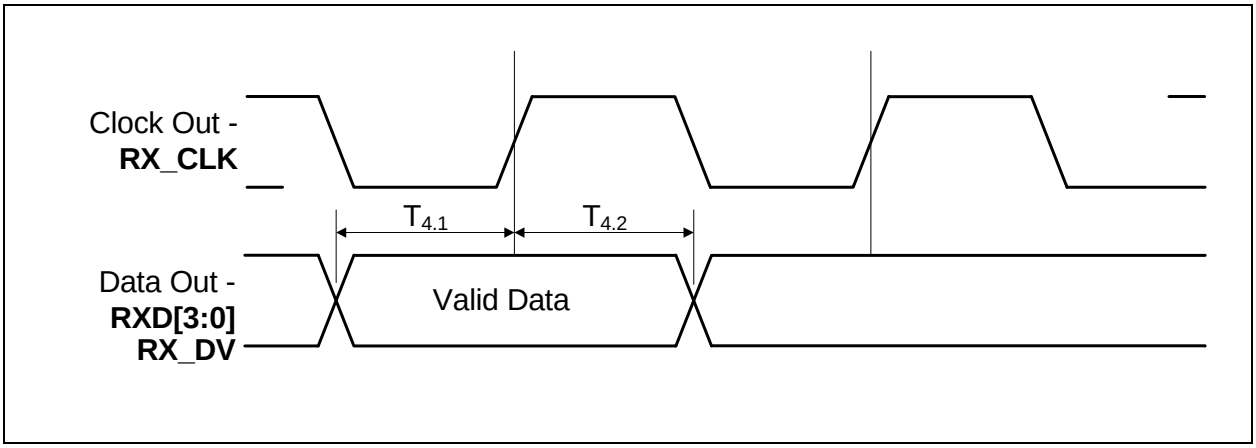

TABLE 6-4: 10M MII RECEIVE TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T4.1	Receive signals setup to RX_CLK rising	10			ns	
T4.2	Receive signals hold from RX_CLK rising	10			ns	
	RX_CLK frequency		2.5		MHz	
	RX_CLK Duty-Cycle		40		%	

6.2.2.2 10M MII Transmit Timing

FIGURE 6-5: 10M MII TRANSMIT TIMING DIAGRAMS

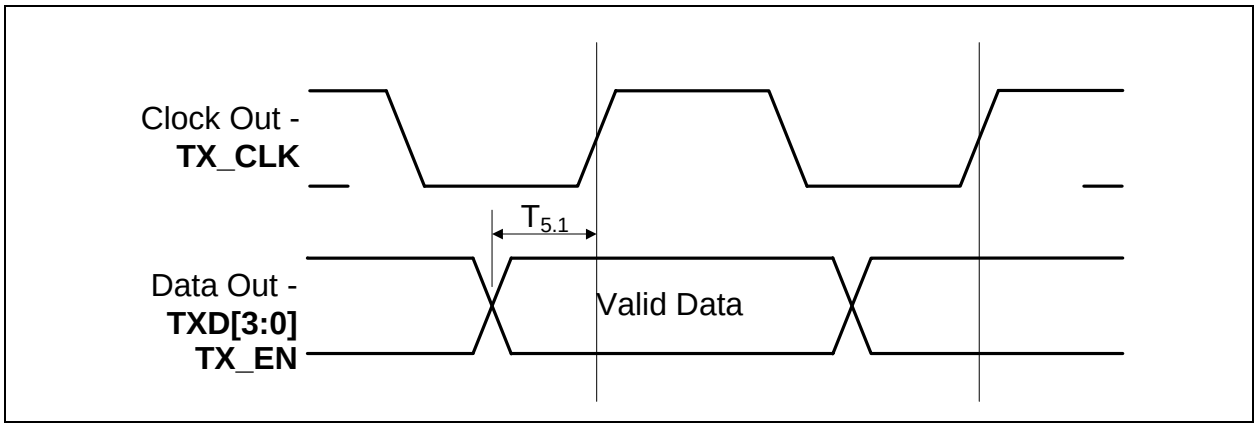

TABLE 6-5: 10M MII TRANSMIT TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T5.1	Transmit signals required setup to TX_CLK rising	12			ns	
	Transmit signals required hold after TX_CLK rising	0			ns	
	TX_CLK frequency		2.5		MHz	
	TX_CLK Duty-Cycle		50		%	

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6.3 RMII 10/100Base-TX/RX Timings

6.3.1 RMII 100BASE-T TX/RX TIMINGS

6.3.1.1 100M RMII Receive Timing

FIGURE 6-6: 100M RMII RECEIVE TIMING DIAGRAM

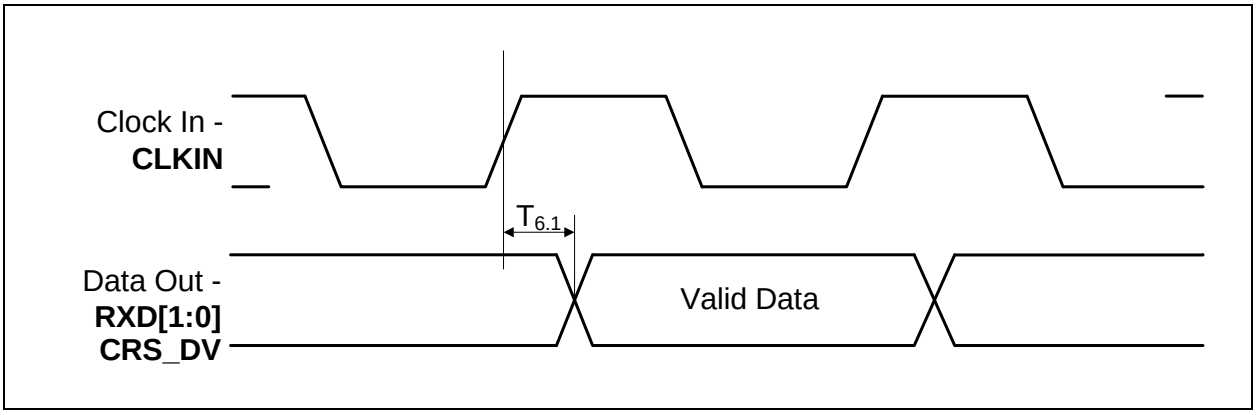

TABLE 6-6: 100M RMII RECEIVE TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T6.1	Output delay from rising edge of CLKIN to receive signals output valid	2		10	ns	
	CLKIN frequency		50		MHz	

6.3.1.2 100M RMII Transmit Timing

FIGURE 6-7: 100M RMII TRANSMIT TIMING DIAGRAM

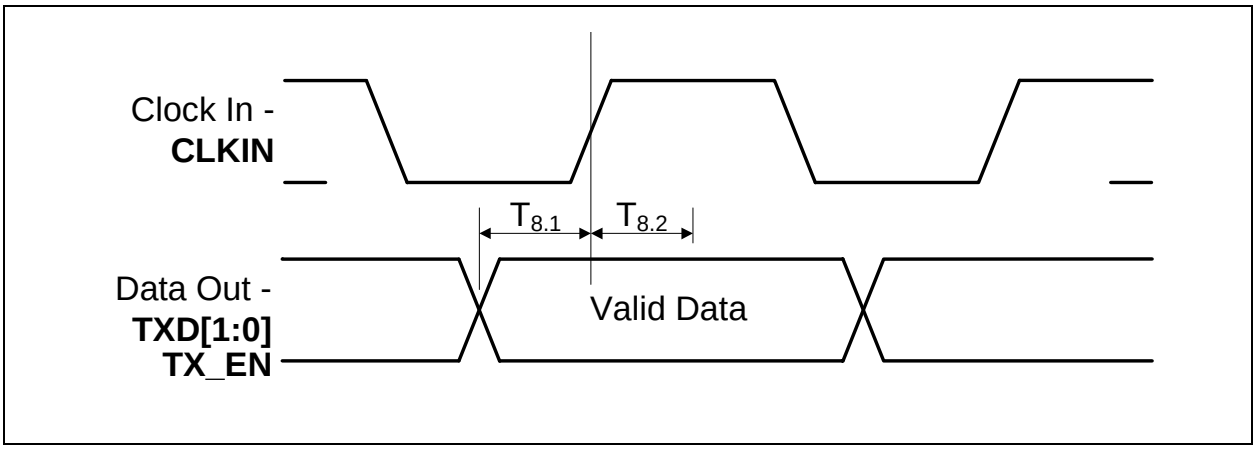

TABLE 6-7: 100M RMII TRANSMIT TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T8.1	Transmit signals required setup to rising edge of CLKIN	2			ns	
T8.2	Transmit signals required hold after rising edge of REF_CLK	1.5			ns	
	CLKIN frequency		50		MHz	

6.3.2 RMII 10BASE-T TX/RX TIMINGS

6.3.2.1 10M RMII Receive Timing

FIGURE 6-8: 10M RMII RECEIVE TIMING DIAGRAM

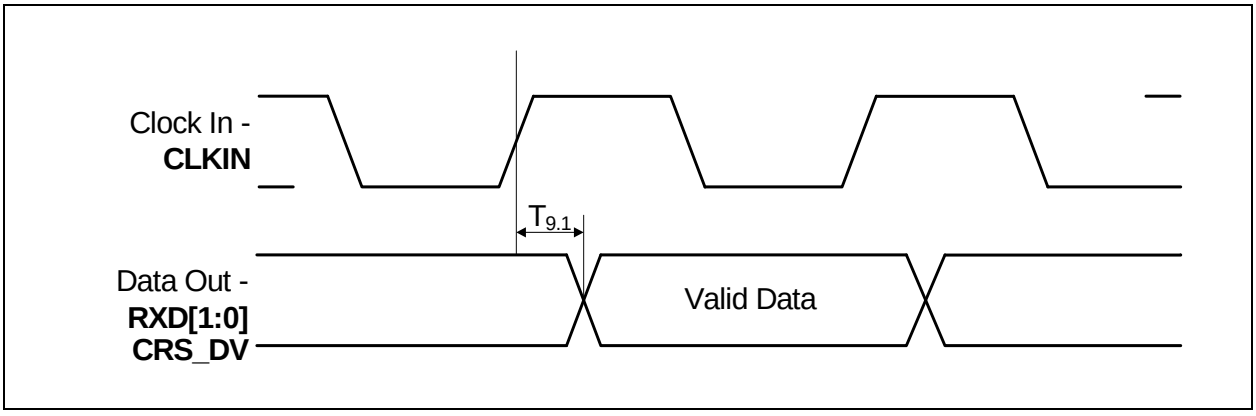

TABLE 6-8: 10M RMII RECEIVE TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T9.1	Output delay from rising edge of CLKIN to receive signals output valid	2		10	ns	
	CLKIN frequency		50		MHz	

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6.3.2.2 10M RMII Transmit Timing

FIGURE 6-9: 10M RMII TRANSMIT TIMING DIAGRAM

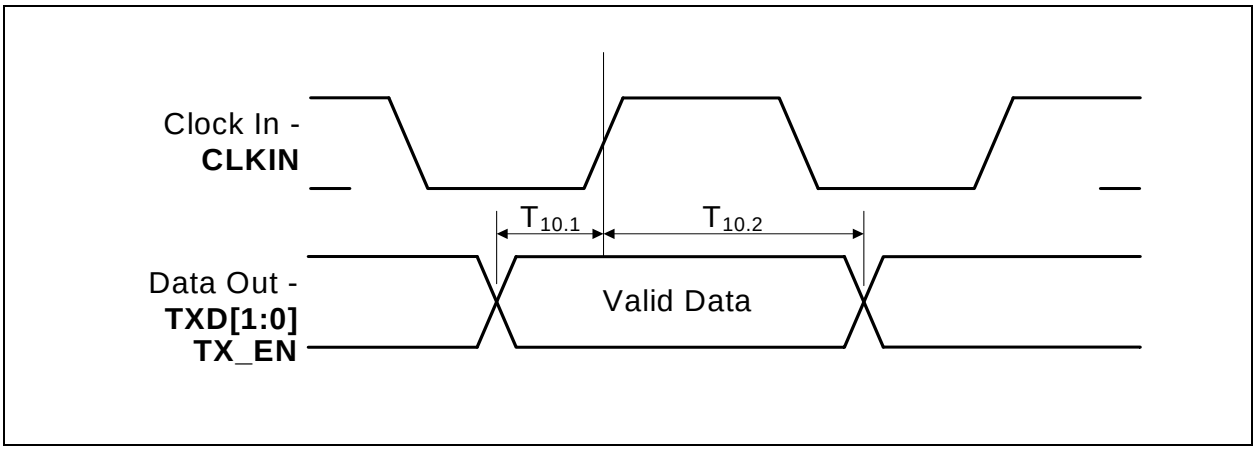

TABLE 6-9: 10M RMII TRANSMIT TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T10.1	Transmit signals required setup to rising edge of CLKIN	4			ns	
T10.2	Transmit signals required hold after rising edge of REF_CLK	2			ns	
	CLKIN frequency		50		MHz	

6.4 RMII CLKIN Timing

TABLE 6-10: RMII CLKIN (REF_CLK)TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
	CLKIN frequency		50		MHz	
	CLKIN Frequency Drift			± 50	ppm	
	CLKIN Duty Cycle	40		60	%	
	CLKIN Jitter			150	psec	p-p – not RMS

6.5 Reset Timing

FIGURE 6-10: RESET TIMING DIAGRAM

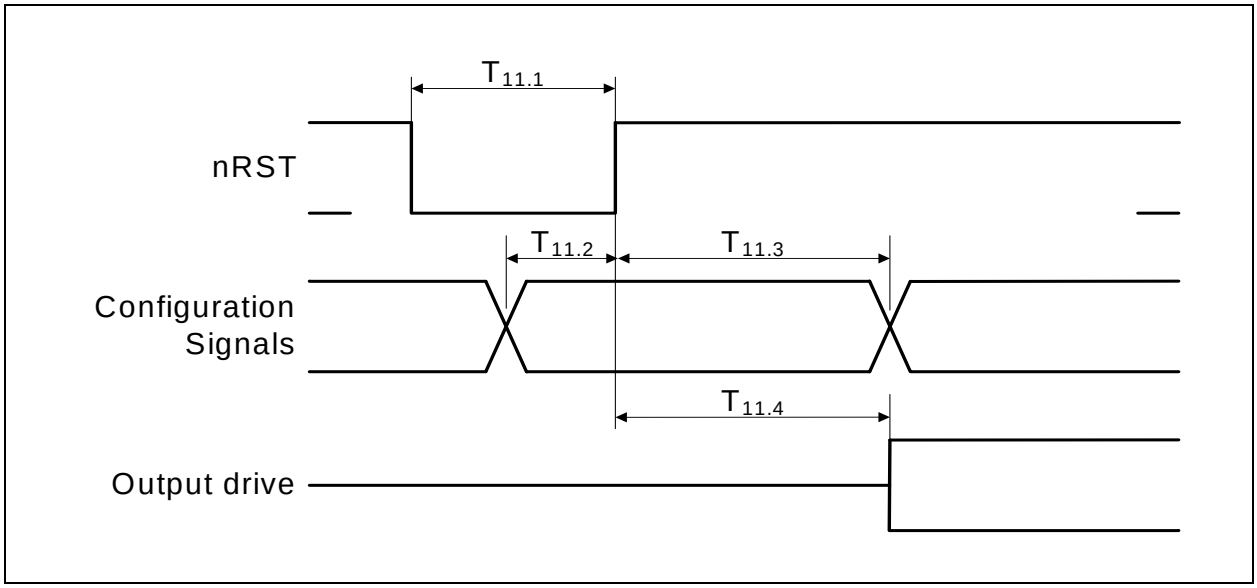

TABLE 6-11: RESET TIMING VALUES

Parameter	Description	MIN	TYP	MAX	Units	Notes
T11.1	Reset Pulse Width	100			us	
T11.2	Configuration input setup to nRST rising	200			ns	
T11.3	Configuration input hold after nRST rising	2			ns	
T11.4	Output Drive after nRST rising	3		800	ns	20 clock cycles for 25 MHz clock - or - 40 clock cycles for 50MHz clock

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6.6 Clock Circuit

LAN8700/LAN8700i can accept either a 25MHz crystal or a 25MHz single-ended clock oscillator (±50ppm) input for operation in MII mode. If the single-ended clock oscillator method is implemented, XTAL2 should be left unconnected and XTAL1/CLKIN should be driven with a nominal 0-3.3V clock signal. The user is required to supply a 50MHz single-ended clock for RMII operation. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum. See Table 6-12 for the recommended crystal specifications.

TABLE 6-12: LAN8700/LAN8700I CRYSTAL SPECIFICATIONS

Parameter	Symbol	MIN	NOM	MAX	Units	Notes
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	±50	PPM	Note 6-1
Frequency Stability Over Temp	F_{temp}	-	-	±50	PPM	Note 6-1
Frequency Deviation Over Time	F_{age}	-	+/-3 to 5	-	PPM	Note 6-2
Total Allowable PPM Budget		-	-	±50	PPM	Note 6-3
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	0.5	-	-	mW	
Equivalent Series Resistance	R_1	-	-	30	Ohm	
Operating Temperature Range		Note 6-4	-	Note 6-5	°C	Note 6-6
LAN8700/LAN8700i XTAL1/CLKIN Pin Capacitance		-	3 typ	-	pF	Note 6-6
LAN8700/LAN8700i XTAL2 Pin Capacitance		-	3 typ	-	pF	Note 6-6

Note 6-1 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependant. Since any particular application must meet the IEEE ±50 PPM Total PPM Budget, the combination of these two values must be approximately ±45 PPM (allowing for aging).

Note 6-2 Frequency Deviation Over Time is also referred to as Aging.

Note 6-3 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as ±100 PPM.

Note 6-4 0°C for commercial version, -40°C for industrial version.

Note 6-5 +70°C for commercial version, +85°C for industrial version.

Note 6-6 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The XTAL1/CLKIN pin, XTAL2 pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. The total load capacitance must be equivalent to what the crystal expects to see in the circuit so that the crystal oscillator will operate at 25.000 MHz.

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7.0 DC ELECTRICAL CHARACTERISTICS

7.1 DC Characteristics

7.1.1 MAXIMUM RATINGS

Stresses beyond those listed in may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 7-1: MAXIMUM CONDITIONS

Parameter	Conditions	MIN	TYP	MAX	Units	Comment
VDD33,VDDIO	Power pins to all other pins.	-0.5		+3.6	V	
Digital IO	To VSS ground	-0.5		+3.6	V	Table 7-5, “MII Bus Interface Signals,” on page 60
VSS	VSS to all other pins	-0.5		+4.0	V	
Operating Temperature	LAN8700-AEZG	0		+70	C	Commercial temperature components.
Operating Temperature	LAN8700i-AEZG	-40		+85	C	Industrial temperature components.
Storage Temperature		-55		+150	C	

TABLE 7-2: ESD AND LATCH-UP PERFORMANCE

Parameter	Conditions	MIN	TYP	MAX	Units	Comments
ESD PERFORMANCE						
All Pins	Human Body Model			±8	kV	Device
System	EN/IEC61000-4-2 Contact Discharge			±8	kV	3rd party system test
System	EN/IEC61000-4-2 Air-gap Discharge			±15	kV	3rd party system test
LATCH-UP PERFORMANCE						
All Pins	EIA/JESD 78, Class II		150		mA	

7.1.1.1 Human Body Model (HBM) Performance

HBM testing verifies the ability to withstand the ESD strikes like those that occur during handling and manufacturing, and is done without power applied to the IC. To pass the test, the device must have no change in operation or performance due to the event. All pins on the LAN8700 provide ±8kV HBM protection.

7.1.1.2 IEN/IEC61000-4-2 Performance

The EN/IEC61000-4-2 ESD specification is an international standard that addresses system-level immunity to ESD strikes while the end equipment is operational. In contrast, the HBM ESD tests are performed at the device level with the device powered down.

Microchip contracts with Independent laboratories to test the LAN8700 to EN/IEC61000-4-2 in a working system. Reports are available upon request. Please contact your Microchip representative, and request information on 3rd party ESD test results. The reports show that systems designed with the LAN8700 can safely dissipate ±15kV air discharges and ±8kV contact discharges per the EN/IEC61000-4-2 specification without additional board level protection.

In addition to defining the ESD tests, EN/IEC61000-4-2 also categorizes the impact to equipment operation when the strike occurs (ESD Result Classification). The LAN8700 maintains an ESD Result Classification 1 or 2 when subjected to an EN/IEC61000-4-2 (level 4) ESD strike.

Both air discharge and contact discharge test techniques for applying stress conditions are defined by the EN/IEC61000-4-2 ESD document.

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7.1.1.2.1 Air Discharge

To perform this test, a charged electrode is moved close to the system being tested until a spark is generated. This test is difficult to reproduce because the discharge is influenced by such factors as humidity, the speed of approach of the electrode, and construction of the test equipment.

7.1.1.2.2 Contact Discharge

The uncharged electrode first contacts the pin to prepare this test, and then the probe tip is energized. This yields more repeatable results, and is the preferred test method. The independent test laboratories contracted by Microchip provide test results for both types of discharge methods.

7.1.2 OPERATING CONDITIONS

TABLE 7-3: RECOMMENDED OPERATING CONDITIONS

Parameter	Conditions	MIN	TYP	MAX	Units	Comment
VDD33	VDD33 to VSS	3.0	3.3	3.6	V	
Input Voltage on Digital Pins		0.0		VDDIO	V	
Voltage on Analog I/O pins (RXP, RXN)		0.0		+3.6V	V	
Ambient Temperature	T_A LAN8700-AEZG	0		70	C	For Commercial Temperature
	T_A LAN8700i-AEZG	-40		+85	C	For Industrial Temperature

7.1.3 POWER CONSUMPTION

7.1.3.1 Power Consumption Device Only

Power measurements taken over the operating conditions specified. See Section 5.4.5 for a description of the power down modes.

TABLE 7-4: POWER CONSUMPTION DEVICE ONLY

Power Pin Group		VDDA3.3 Power Pins (mA)	VDD_CORE Power Pin (mA)	VDDIO Power Pin (mA)	Total Current (mA)	Total Power (mW)
100BASE-T /W TRAFFIC	Max	35.6	41.3	4.7	81.6	269.28
	Typical	33.3	37.4	4.1	74.8	246.84
	Min	31.3	33.4	1.3	66	165.75 Note 7-1
10BASE-T /W TRAFFIC	Max	15.6	22.3	1.1	39	128.7
	Typical	15.3	20.8	0.9	37	122.1
	Min	14.9	19.1	0.1	34.1	83.88 Note 7-1
ENERGY DETECT POWER DOWN	Max	10.5	3.3	0.5	13.85	45.7
	Typical	9.9	2.7	0.4	13.0	42.9
	Min	9.8	2.3	0.3	12.4	37.02 Note 7-1
GENERAL POWER DOWN	Max	0.21	2.92	0.39	3.52	11.62
	Typical	0.124	2.6	0.345	3.07	10.131
	Min	0.038	2.1	0.3	2.44	4.4454 Note 7-1

Note: The current at VDD_CORE is either supplied by the internal regulator from current entering at VDD33, or from an external 1.8V supply when the internal regulator is disabled.

Note 7-1 This is calculated with full flexPWR features activated: VDDIO = 1.8V and internal regulator disabled.

Note 7-2 Current measurements do not include power applied to the magnetics or the optional external LEDs. Current measurements taken with VDDIO = +3.3V, unless otherwise indicated.

7.1.4 DC CHARACTERISTICS - INPUT AND OUTPUT BUFFERS

TABLE 7-5: MII BUS INTERFACE SIGNALS

Name	V_{IH} (V)	V_{IL} (V)	I_{OH}	I_{OL}	V_{OL} (V)	V_{OH} (V)
TXD0	0.68 * VDDIO	0.4 * VDDIO				
TXD1	0.68 * VDDIO	0.4 * VDDIO				
TXD2	0.68 * VDDIO	0.4 * VDDIO				
TXD3	0.68 * VDDIO	0.4 * VDDIO				
TX_EN	0.68 * VDDIO	0.4 * VDDIO				
TX_CLK			-8 mA	+8 mA	+0.4	VDDIO – +0.4
RXD0/MODE0			-8 mA	+8 mA	+0.4	VDDIO – +0.4
RXD1/MODE1			-8 mA	+8 mA	+0.4	VDDIO – +0.4
RXD2/MODE2			-8 mA	+8 mA	+0.4	VDDIO – +0.4
RXD3/nINTSEL			-8 mA	+8 mA	+0.4	VDDIO – +0.4
RX_ER/RXD4			-8 mA	+8 mA	+0.4	VDDIO – +0.4
RX_DV			-8 mA	+8 mA	+0.4	VDDIO – +0.4
RX_CLK/REGOFF			-8 mA	+8 mA	+0.4	VDDIO – +0.4
CRS/PHYAD4			-8 mA	+8 mA	+0.4	VDDIO – +0.4
COL/RMII/CRS_DV			-8 mA	+8 mA	+0.4	VDDIO – +0.4
MDC	0.68 * VDDIO	0.4 * VDDIO				
MDIO	0.68 * VDDIO	0.4 * VDDIO	-8 mA	+8 mA	+0.4	VDDIO – +0.4
nINT/TX_ER/TXD4	0.68 * VDDIO	0.4 * VDDIO	-8 mA	+8 mA	+0.4	3.6

TABLE 7-6: LAN INTERFACE SIGNALS

Name		V_{IH}	V_{IL}	I_{OH}	I_{OL}	V_{OL}	V_{OH}
TXP	See Table 7-12, “100Base-TX Transceiver Characteristics,” on page 62 and Table 7-13, “10BASE-T Transceiver Characteristics,” on page 62.						
TXN							
RXP							
RXN							

TABLE 7-7: LED SIGNALS

Name	V_{IH} (V)	V_{IL} (V)	I_{OH}	I_{OL}	V_{OL} (V)	V_{OH} (V)
SPEED100/PHYAD0	0.68 * VDDIO	0.4 * VDDIO	-12 mA	+12 mA	+0.4	VDDIO – +0.4
LINK/PHYAD1	0.68 * VDDIO	0.4 * VDDIO	-12 mA	+12 mA	+0.4	VDDIO – +0.4
ACTIVITY/PHYAD2	0.68 * VDDIO	0.4 * VDDIO	-12 mA	+12 mA	+0.4	VDDIO – +0.4
FDUPLEX/PHYAD3	0.68 * VDDIO	0.4 * VDDIO	-12 mA	+12 mA	+0.4	VDDIO – +0.4

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TABLE 7-8: CONFIGURATION INPUTS

Name	V_{IH} (V)	V_{IL} (V)	I_{OH}	I_{OL}	V_{OL} (V)	V_{OH} (V)
SPEED100/PHYAD0	0.68 * VDDIO	0.4 * VDDIO	-12 mA	+12 mA	+0.4	VDDIO – +0.4
LINK/PHYAD1	0.68 * VDDIO	0.4 * VDDIO	-12 mA	+12 mA	+0.4	VDDIO – +0.4
ACTIVITY/PHYAD2	0.68 * VDDIO	0.4 * VDDIO	-12 mA	+12 mA	+0.4	VDDIO – +0.4
FDUPLEX/PHYAD3	0.68 * VDDIO	0.4 * VDDIO	-12 mA	+12 mA	+0.4	VDDIO – +0.4
CRS/PHYAD4	0.68 * VDDIO	0.4 * VDDIO	-8 mA	+8 mA	+0.4	VDDIO – +0.4
RXD0/MODE0	0.68 * VDDIO	0.4 * VDDIO				
RXD1/MODE1	0.68 * VDDIO	0.4 * VDDIO				
RXD2/MODE2	0.68 * VDDIO	0.4 * VDDIO				
RX_CLK/REGOFF	0.68 * VDDIO	0.4 * VDDIO				
COL/RMII/CRS_DV			-8 mA	+8 mA	+0.4	VDDIO – +0.4

TABLE 7-9: GENERAL SIGNALS

Name	V_{IH} (V)	V_{IL} (V)	I_{OH}	I_{OL}	V_{OL} (V)	V_{OH} (V)
nINT/TX_ER/TXD4			-8 mA	+8 mA	+0.4	VDDIO – +0.4
nRST	0.68 * VDDIO	0.4 * VDDIO				
CLKIN/XTAL1 (Note 7-3)	+1.40 V	0.4 * VDDIO				
XTAL2	-	-				
NC						

Note 7-3 These levels apply when a 0-3.3V Clock is driven into CLKIN/XTAL1 and XTAL2 is floating. The maximum input voltage on XTAL1 is VDDIO + 0.4V.

TABLE 7-10: ANALOG REFERENCES

Name	Buffer Type	V_{IH}	V_{IL}	I_{OH}	I_{OL}	V_{OL}	V_{OH}
EXRES1	AI						

TABLE 7-11: INTERNAL PULL-UP / PULL-DOWN CONFIGURATIONS

Name	Pull-up or Pull-down
SPEED100/PHYAD0	Pull-up
LINK/PHYAD1	Pull-up
ACTIVITY/PHYAD2	Pull-up
FDUPLEX/PHYAD3	Pull-up
CRS/PHYAD4	Pull-up
RXD0/MODE0	Pull-up
RXD1/MODE1	Pull-up
RXD2/MODE2	Pull-up
RXD3/nINTSEL	Pull-up
nINT/TX_ER/TXD4	Pull-up
nRST	Pull-up
COL/RMII/CRS_DV	Pull-down
MDIO	Pull-down
MDC	Pull-down
RX_CLK/REGOFF	Pull-down

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TABLE 7-11: INTERNAL PULL-UP / PULL-DOWN CONFIGURATIONS (CONTINUED)

Name	Pull-up or Pull-down
RX_ER/RXD4	Pull-down
RX_DV	Pull-down
TX_EN	Pull-down

Note: For VDDIO operation below +2.5V, Microchip recommends designs add external strapping resistors in addition the internal strapping resistors to ensure proper strapped operation.

TABLE 7-12: 100BASE-TX TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	MIN	TYP	MAX	Units	Notes
Peak Differential Output Voltage High	V_{PPH}	950	-	1050	mVpk	Note 7-4
Peak Differential Output Voltage Low	V_{PPL}	-950	-	-1050	mVpk	Note 7-4
Signal Amplitude Symmetry	V_{SS}	98	-	102	%	Note 7-4
Signal Rise & Fall Time	T_{RF}	3.0	-	5.0	nS	Note 7-4
Rise & Fall Time Symmetry	T_{RFS}	-	-	0.5	nS	Note 7-4
Duty Cycle Distortion	D_{CD}	35	50	65	%	Note 7-5
Overshoot & Undershoot	V_{OS}	-	-	5	%	
Jitter				1.4	nS	Note 7-6

Note 7-4 Measured at the line side of the transformer, line replaced by 100Ω (± 1%) resistor.

Note 7-5 Offset from 16 nS pulse width at 50% of pulse peak.

Note 7-6 Measured differentially.

TABLE 7-13: 10BASE-T TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	MIN	TYP	MAX	Units	Notes
Transmitter Peak Differential Output Voltage	V_{OUT}	2.2	2.5	2.8	V	Note 7-7
Receiver Differential Squelch Threshold	V_{DS}	300	420	585	mV	

Note 7-7 Min/max voltages ensured as measured with 100Ω resistive load.

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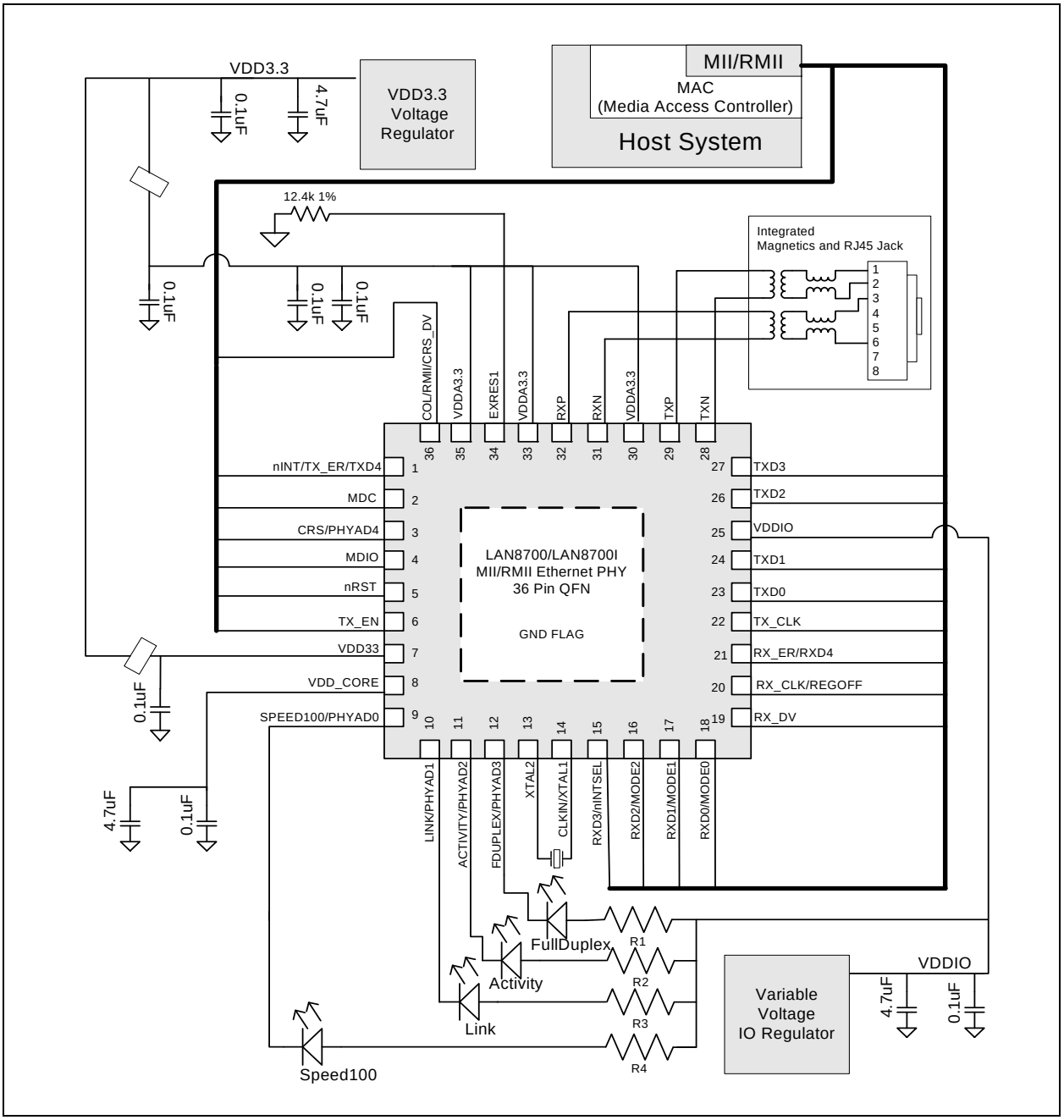
8.0 APPLICATION NOTES

8.1 Application Diagram

FIGURE 8-1: SIMPLIFIED APPLICATION DIAGRAM (SEE Section 8.4, "Reference Designs")



Note:	R5 on the Crystal is used to control the crystal drive strength into the PHY clock generator. This resistance can be fine tuned to meet the requirements of each crystal manufacturer.

8.2 Magnetics Selection

For a list of magnetics selected to operate with the Microchip LAN8700, please refer to the Application note “AN 8-13 Suggested Magnetics”.

http://ww1.microchip.com/downloads/en/appnotes/en562793.pdf

8.3 Application Notes

Application examples are given in pdf format on the Microchip LAN8700 web site. The link to the web site is shown below.

http://www.microchip.com/wwwproducts/en/LAN8700

Please check the web site periodically for the latest updates.

8.4 Reference Designs

The LAN8700 Reference designs are available on the Microchip LAN8700 web site link below.

http://www.microchip.com/wwwproducts/en/LAN8700

The reference designs are available in four variations:

a) MII with +3.3V IO
b) RMII with +3.3V IO
c) MII with +1.8V IO
d) RMII with +1.8V IO.

Features

- Industrial temperature PHY and Magnetics
- 8 pin SOIC for user configurable Magnetics
- On board LED indicators for Speed 100
- Full Duplex
- RJ-45 Connector LEDs for Link and Activity
- Interfaces Through 40-pin Connector as Defined in the MII Specification
- Powered by 5.0V from the 40-Pin MII Connector
- Standard RJ45 Connector with LED indicators for Link and Activity
- Includes Probe Points on All MII Data and Control Signals for Troubleshooting
- Includes 25MHz Crystal for Internal PHY Reference; RX_CLK is Supplied to the 40-Pin Connector
- Supports user configuration options including PHY address selection
- Integrated 3.3V Regulator

Applications

The EVB8700 Evaluation board simplifies the process of testing and evaluating an Ethernet Connection in your application. The LAN8700 device is installed on the EVB board and all associated circuitry is included, along with all configuration options.

The Benefits of adding an external MII interface are:

- Easier system and software development
- Verify MAC to PHY interface
- Support testing of FPGA implementations of MAC
- Assist interoperability test of various networks
- Verify MII compliance
- Verify performance of HP AutoMDIX feature
- Verify Variable IO compliance

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9.0 PACKAGE OUTLINE, TAPE AND REEL

FIGURE 9-1: 36-PIN QFN PACKAGE, 6 X 6 X 0.9MM BODY, 0.5MM PITCH

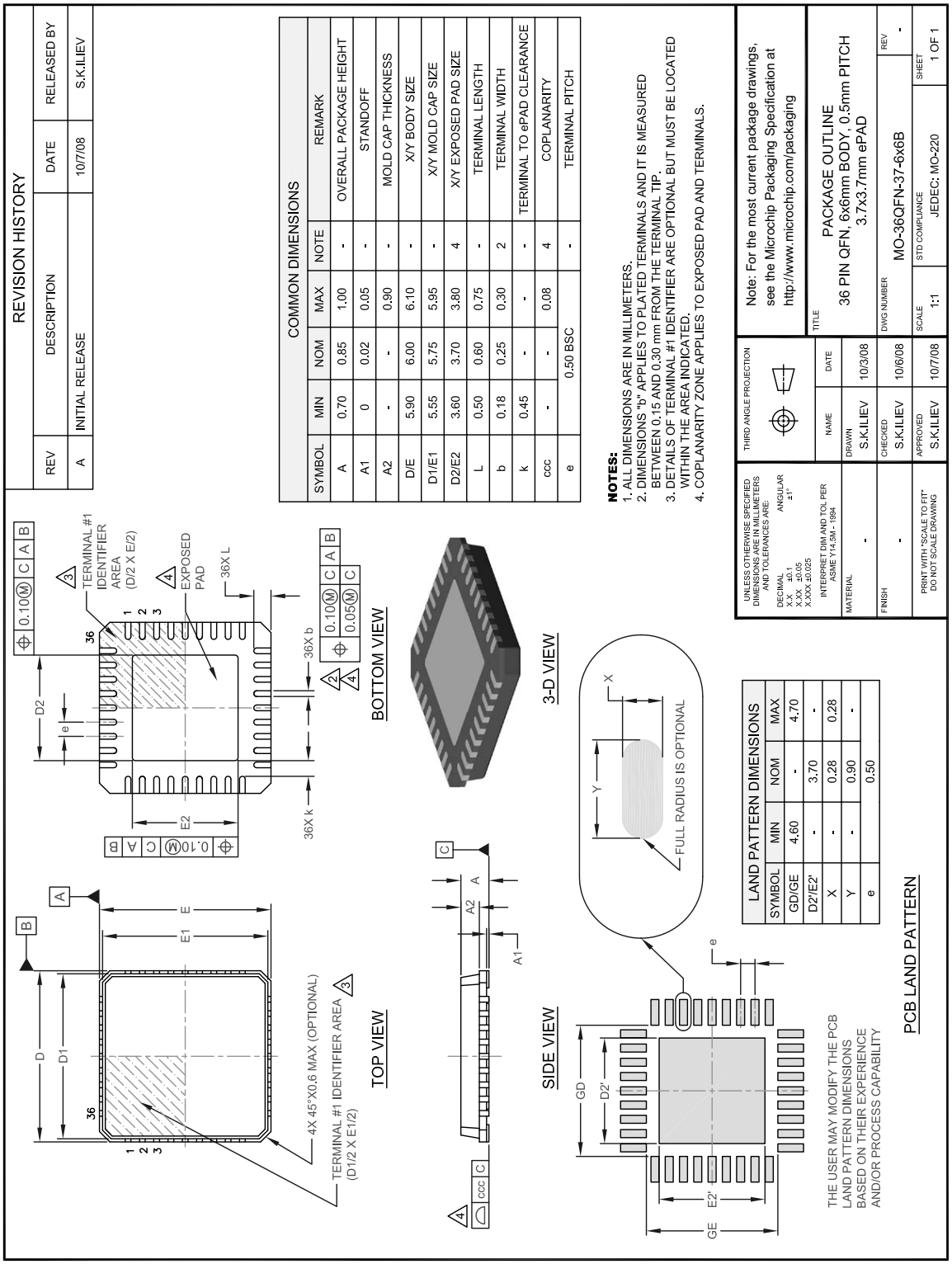
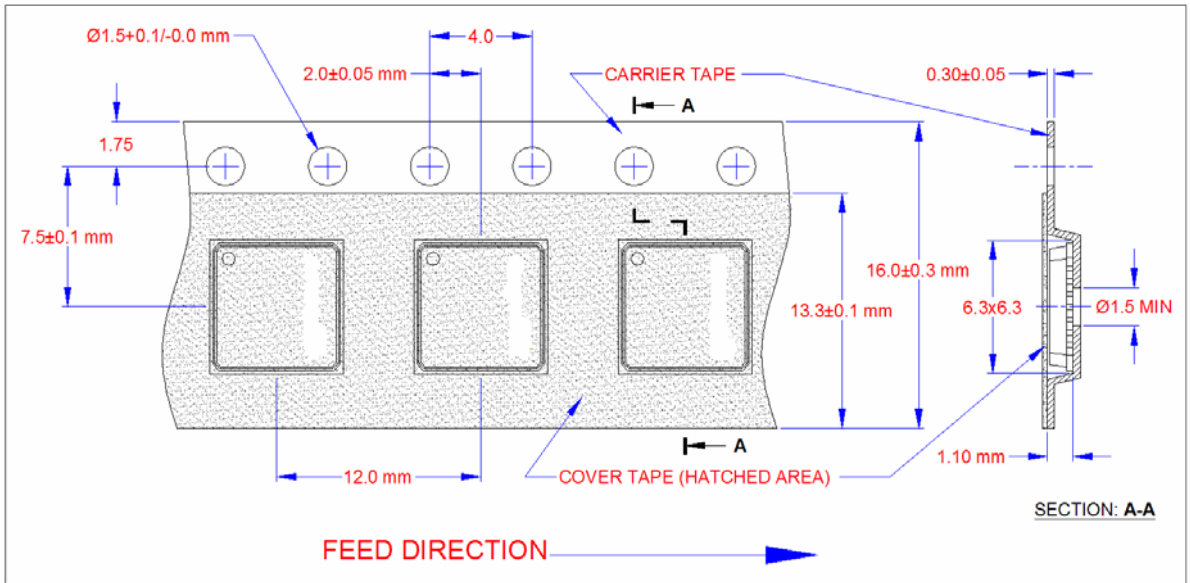


FIGURE 9-2: QFN, 6X6 TAPE & REEL



QFN-6x6: TAPING DIMENSIONS AND PART ORIENTATION	UNIT: MM

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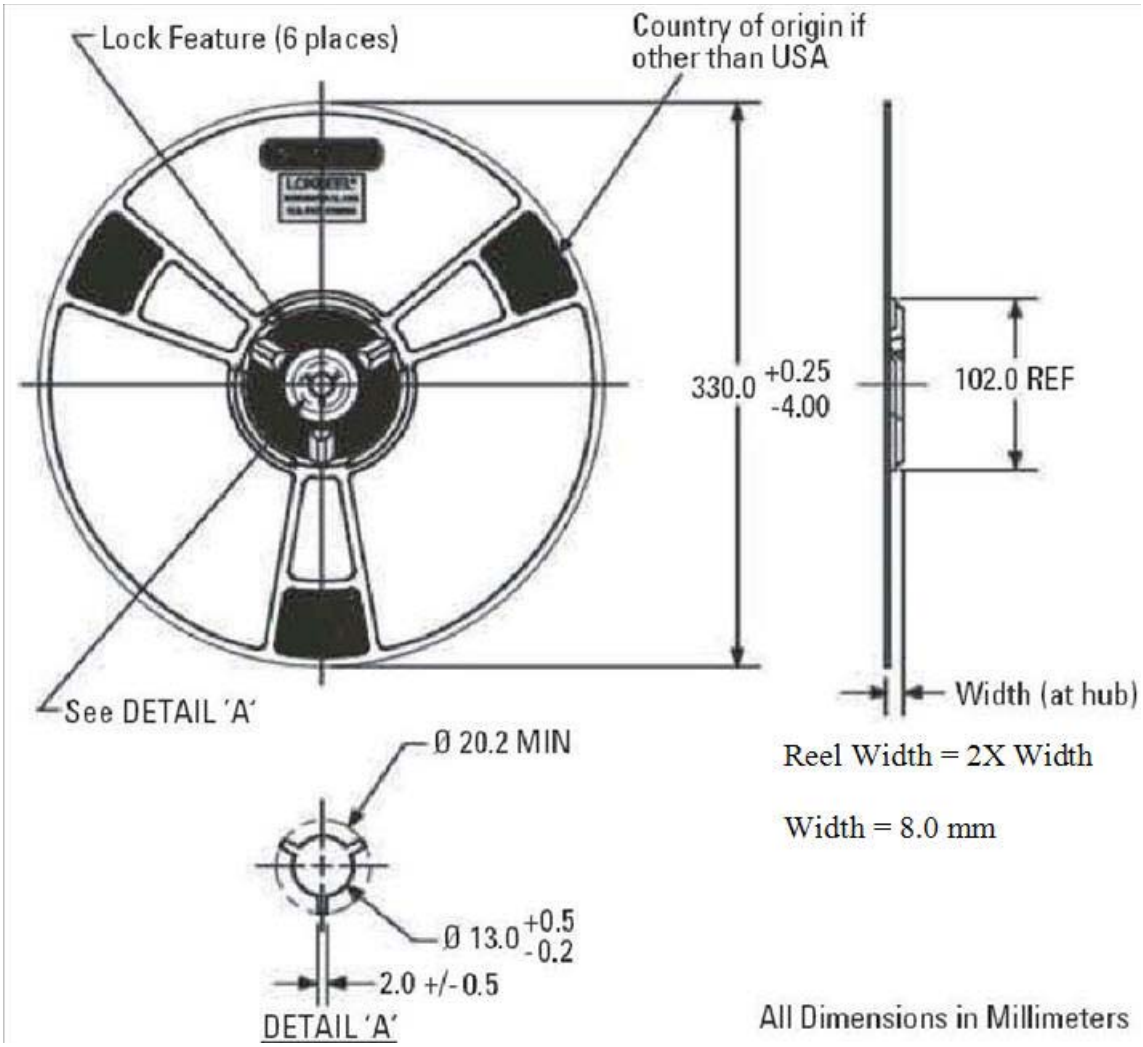
FIGURE 9-3: REEL DIMENSIONS



Note:	Standard reel size is 3000 pieces per reel.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002260A (08-25-16)	Replaces previous SMSC version Rev. 2.3 (04-12-11)	
Rev. 2.3 (04-12-11)	Section 6.5, "Reset Timing," on page 56	Corrected T11.4 minimum value to 3ns. Corrected T11.3 to 2ns.
	Table 5-39, “Register 18 - Special Modes,” on page 38	• Updated MIIMODE bit description and added note: “When writing to this register, the default value of this bit must always be written back.” • Added note regarding default MIIMODE value.
	Section 4.6.3, "MII vs. RMII Configuration," on page 21	Updated section to remove information about register control of the MII/RMII mode.
	Section 5.4.8.2, "Far Loopback," on page 45	Updated section to remove information about register control of the MII/RMII mode.
Rev. 2.2 (12-04-09)	Table 6-1, "SMI Timing Values"	Updated T1.2 maximum to 300ns.
Rev. 2.1 (03-06-09)	Section 5.4.6, "Reset"	Removed reference to internal POR system. Added note the nRST should be low until VDDIO and VDD_CORE are stable. Added Figure.
	Table 5-34, "Register 4 - Auto Negotiation Advertisement"	Corrected bit value for Asymmetric and Symmetric PAUSE.
	Section 6.3, "RMII 10/100Base-TX/RX Timings"	Improved timing values.
	Section 5.4.8, "Loopback Operation"	Enhanced this section.
	Section 4.6.3, "MII vs. RMII Configuration"	Added information about register bit 18.14.
	Section 6.6, "Clock Circuit"	Added section on clock, with crystal specification table.
	Figure 1-1, "LAN8700/LAN8700i System Block Diagram"	Removed GPIO from the LED block.
	Section 4.11, "PHY Address Strapping and LED Output Polarity Selection"	Removed reference to GP01 pin in third paragraph.
	Table 5-45, "Register 31 - PHY Special Control/Status"	Renamed Bits 7-9 as Reserved.
	Table 5-28, "PHY Special Control/Status Register 31: Vendor-Specific"	Renamed Bits 7-9 as Reserved.
Rev. 2.0 (07-15-08)	Section 9.0, "Package Outline, Tape and Reel"	Tape and reel drawings and ordering info added.
Rev. 1.9 (03-18-08)	Figure 6-7, "100M RMII Transmit Timing Diagram"	Replaced figure.

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TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
	Table 6-5, "10M MII Transmit Timing Values"	Removed the text “T5.2” in the “Parameter” column.
	Figure 6-5, "10M MII Transmit Timing Diagrams"	Replaced figure.
	Table 6-3, "100M MII Transmit Timing Values"	Removed the text “T3.2” in the “Parameter” column.
	Figure 6-3, "100M MII Transmit Timing Diagram"	Replaced figure.
	Table 6-11, "Reset Timing Values"	Changed the MIN value for T11.3: From: “400” To: “10”
	Table 6-4, "10M MII Receive Timing Values"	Deleted last row in table.
	Section 4.6.2.1, "Reference Clock"	First sentence of second paragraph changed: From: “between 35% and 65%” To: “between 40% and 60%”
Rev. 1.8 (02-14-08)	Table 6-7, "100M RMII Transmit Timing Values"	Changed value of T8.1 and T8.2.
	Table 6-6, "100M RMII Receive Timing Values"	Changed value of T6.1.
Rev. 1.6 (12-11-07)	Section 4.9, "Internal +1.8V Regulator Disable"	Added information about not applying VDD_CORE before VDD33 is at 2.64V.
	Table 3-8, "Power Signals"	Updated description of VDD_CORE for information on using external 1.8V supply.
	Table 3-1, "MII Signals"	Updated description of RX_CLK/REGOFF to add power supply sequencing information.
	Table 5-33, "Register 3 - PHY Identifier 2"	Updated Revision Number to match the LAN8700C silicon.
Rev. 1.5 (10-04-07)	Section 8.0, "Application Notes"	Table 8-1, "Simplified Application Diagram (see Section 8.4, "Reference Designs")" has been updated. In addition, the following cross reference added to caption: (see Section 8.4, "Reference Designs").
Rev. 1.4 (09-17-07)	Section 7.1.4, "DC Characteristics - Input and Output Buffers"	Changed VIH to 0.68*VDDIO. Changed VIL to 0.4*VDDIO.
Rev. 1.3 (06-27-07)	Table 6-9, "10M RMII Transmit Timing Values"	Moved parameter T10.2 in Table 6-9, "10M RMII Transmit Timing Values" from MAX column to MIN column.
	Table 6-5, "10M MII Transmit Timing Values"	Moved parameter T5.2 in Table 6-5, "10M MII Transmit Timing Values" from MAX column to MIN column.
Rev. 1.2 (05-29-07)	Table 5-48, "MODE[2:0] Bus"	Added description when the MODE[2:0] bits are set to 110.

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
	Table 5-30, "Register 0 - Basic Control"	Corrected Default value for bit 0.11 to the value of 0. This bit does not get set when the MODE[2:0] bits are set to 110.
	Section 5.4.9.2, "Mode Bus – MODE[2:0]"	Added detail about MODE[2:0] pins having no affect at soft reset.
	Table 5-30, "Register 0 - Basic Control"	Added note to reset description (bit 0.15).
	Table 3-5, "General Signals"	AT nRST, added note that register bit values are loaded from the Mode pins upon deassertion.
	Table 7-11, "Internal Pull-Up / Pull-Down Configurations"	Added RX_DV to table.
	Table 3-1, "MII Signals"	Added note that RX_DV and RX_ER cannot be high during reset.
	Table 6-7, "100M RMII Transmit Timing Values"	Moved parameter T8.2 from MAX column to MIN column.
Rev. 1.1 (04-17-07)	Table 7-4, "Power Consumption Device Only"	Changed column headings to add clarity regarding source of current. Added Note.
	Table 3-4, "Boot Strap Configuration Inputs (Note 3-1)"	Removed RX_CLK/REGOFF because it made Note 3-1 false.
	Table 5-40, "Register 26 - Symbol Error Counter"	Added this table to describe the register.
	Table 5-29, "SMI Register Mapping"	Added Register 26.
	Table 5-23, "Symbol Error Counter Register 26: Vendor-Specific"	Changed description from Reserved to Symbol Error Counter.
Rev. 1.0 (04-04-07)	Table 5-30, “Register 0 - Basic Control,” on page 35	Table modified: Default column for “Power Down” and “Isolate”.
	Section 4.6.3, "MII vs. RMII Configuration," on page 21	Fixed a typo, GPO0/MII is on the 187, COL/RMII/CRS_DV is on the 8700.
	Section 8.1, "Application Diagram," on page 63	Added support components to crystal in application diagram circuit. also added a note to the bottom to indicate that purpose of R5 added.
	Table 5-33, “Register 3 - PHY Identifier 2,” on page 36	Corrected reg3 values.
	Section 4.9.1, "Disable the Internal +1.8V Regulator," on page 24	Changed paragraph to correctly reflect operation VDDIO and VDDA latch 1.8V regulator. 1.8v strap above VIH or below VIL.

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