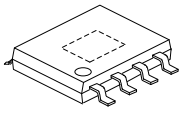
0.8V REFERENCE ULTRA LOW DROPOUT LINEAR REGULATOR



HSOP-8

■ DESCRIPTION

The UTC **LADLD30** is a typical LDO with the features of very low dropout voltage as low as 0.25V at output current 3A.

For normal operation, tow supply voltages are necessary. One called control voltage from other equipment can shutdown the output voltage and it should pull and hold the voltage of EN pin less than 0.3V. Another one is the main supply voltage whose purpose is for main power conversion, to keep the power dissipation low, and to make the dropout voltage lower.

Internally, in the UTC **LADLD30**, there're many functions which can be seen in the block figure to prevent the IC from being damaged. Internal Power-On-Reset (POR) circuit can control the tow supply voltages to prevent fault operations of the circuit; the thermal shutdown circuit is able to protect the device from over thermal operation, and a current limit function will keep the device work safely under current over-loads.

The UTC **LADLD30** can be used as an ideal to provide well supply voltage in the applications, such as front-side-bus termination on motherboard, NB applications, front side bus V_{TT} (1.2V/3A) and note book PC applications.

■ FEATURES

* Low Dropout V_D=0.25V(typ.)@ I_{OUT}=3A
* Low ESR Output Capacitor
* V_{REF}=0.8V
* ±1.5% over Line, Load and Temperature Output Accuracy
* Fast Transient Response
* Output Voltage Adjustable through External Resistors
* POR(Power-On-Reset) controlling V_{CNTL} and V_{IN}
* With internal Soft-Start
* Internal Current Limit Protection
* Internal Under Voltage Protection
* Hysteretic Thermal Shutdown
* With Power-OK Output (with a Delay Time)
* For Standby or Suspend Mode: Shutdown

■ ORDERING INFORMATION

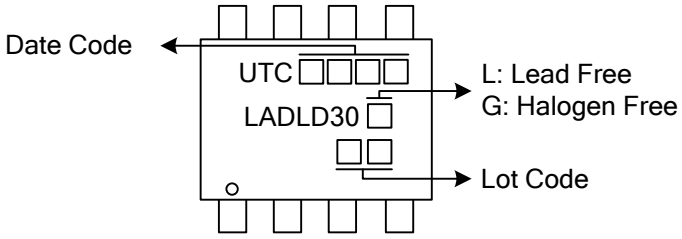
Ordering Number		Package	Packing
Lead Free	Halogen Free		
LADLD30L-SH2-R	LADLD30G-SH2-R	HSOP-8	Tape Reel

xx: Output Voltage, refer to Marking Information.

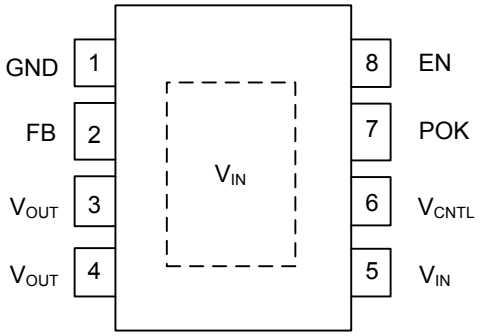
LADLD30L-SH2-R
- (1) Packing Type
- (2) Package Type
- (3) Lead Free
- (4) Output Voltage Code

(1) R: Tape Reel
(2) SH2: HSOP-8
(3) G: Halogen Free, L: Lead Free
(4) AD: Output Voltage :ADJ

■ MARKING INFORMATION



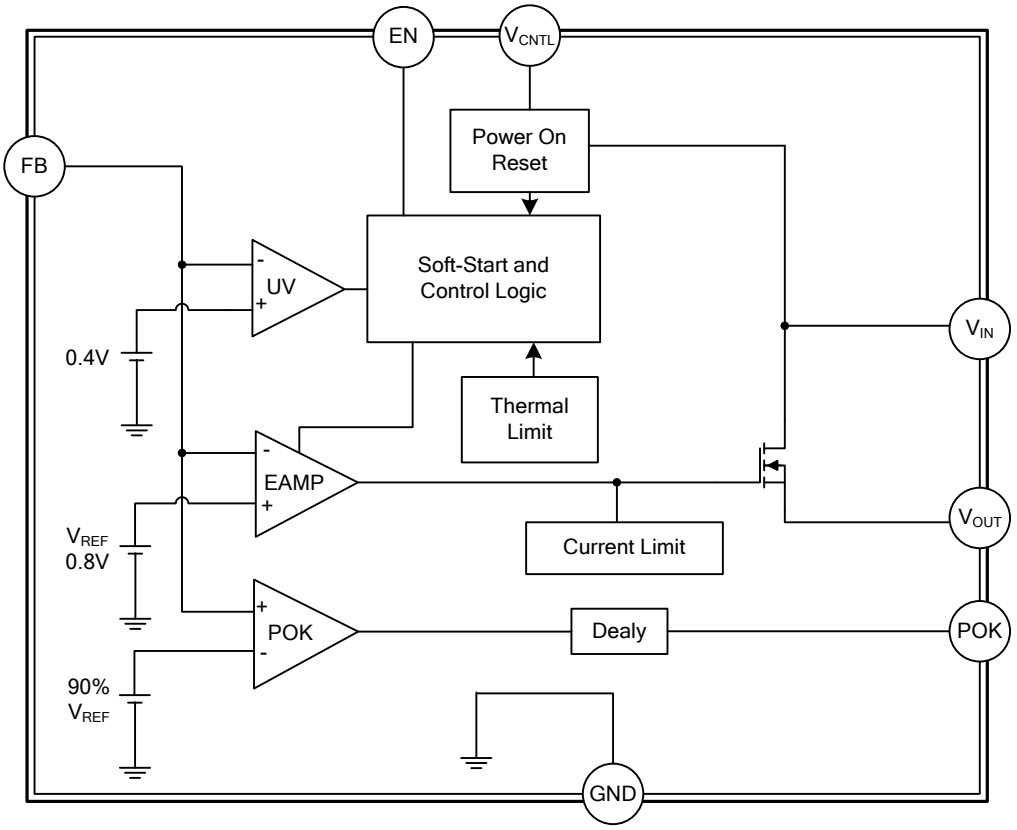
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground pin.
2	FB	There's an external resistor divider connected to this pin which is necessary to give the feedback voltage to the regulator. The external circuit is combined as the follow: between V_{OUT} and FB is R1(connected with a bypass capacitor which can improve the load transient response),and between FB and ground is R2.The value of R2 and R1 are recommended between 100Ω~10kΩ.So the output voltage is equals: $V_{OUT}=0.8\cdot(1+\frac{R1}{R2})(V)$
3 4	V_{OUT}	The output voltage pin of the regulator. There should be set an output capacitor to compensate for closed-loop and also to improve transient responses. It's necessary to connect Pin 3 and Pin 4 together by wide tracks.
5	V_{IN}	This pin is the main supply input. It's necessary to connect the Exposed Pad and V_{IN} together for lower dropout voltage. Monitoring this pin's voltage can reset Power-On.
6	V_{CNTL}	Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.
7	POK	Output pin for Power-OK signal output. Being an open drain output, through senescing FB voltage, this pin can show the users the output voltage's states. That's this pin will be low under any of these tow situations: the rising FB voltage is not above the V_{POK} threshold; the falling FB voltage is below the V_{PNOK} threshold. That indicates the output voltage is not ready for users.
8	EN	Input Enable control pin. The output voltage can be shut down when this pin is below 0.3V. This pin's voltage can be set higher than V_{CNTL} voltage by an internal 10μA current source, and then the regulator will begin working normally.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (V_{CNTL} to GND)	V_{CNTL}	-0.3 ~ +7	V
Supply Voltage (V_{IN} to GND)	V_{IN}	-0.3 ~ +3.3	V
EN and FB to GND	$V_{I/O}$	-0.3 ~ V_{CNTL}+0.3	V
POK to GND	V_{POK}	-0.3 ~ +7	V
Power Dissipation	P_D	3	W
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 1)	θ_{JA}	42	°C/W
Junction to Case (Note 2)	θ_{JC}	18	°C/W

Note: 1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of HSOP-8 is soldered directly on the PCB.
2. The Thermal Pad Temperature is measured on the PCB copper area connected to the thermal pad of package.

■ OPERATING CONDITIONS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage	Control	V_{CNTL}	3.1 ~ 6	V
Supply Voltage	Input	V_{IN}	1.1 ~ 3.3	V
Output Voltage	V_{CNTL}=3.3±5%	V_{OUT}	0.8 ~ 1.2	V
	V_{CNTL}=5.0±5%		+0.8 ~ V_{IN}-0.2	V
Output Current		I_{OUT}	0 ~ 4	A
Junction Temperature		T_J	-25 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

(Refer to the typical application circuit. These specifications apply over, V_{CNTL} = 5V, V_{IN} = 1.5V, V_{OUT} = 1.2V and T_a = 0 to 70°C, unless otherwise specified. Typical values refer to T_a = 25°C).

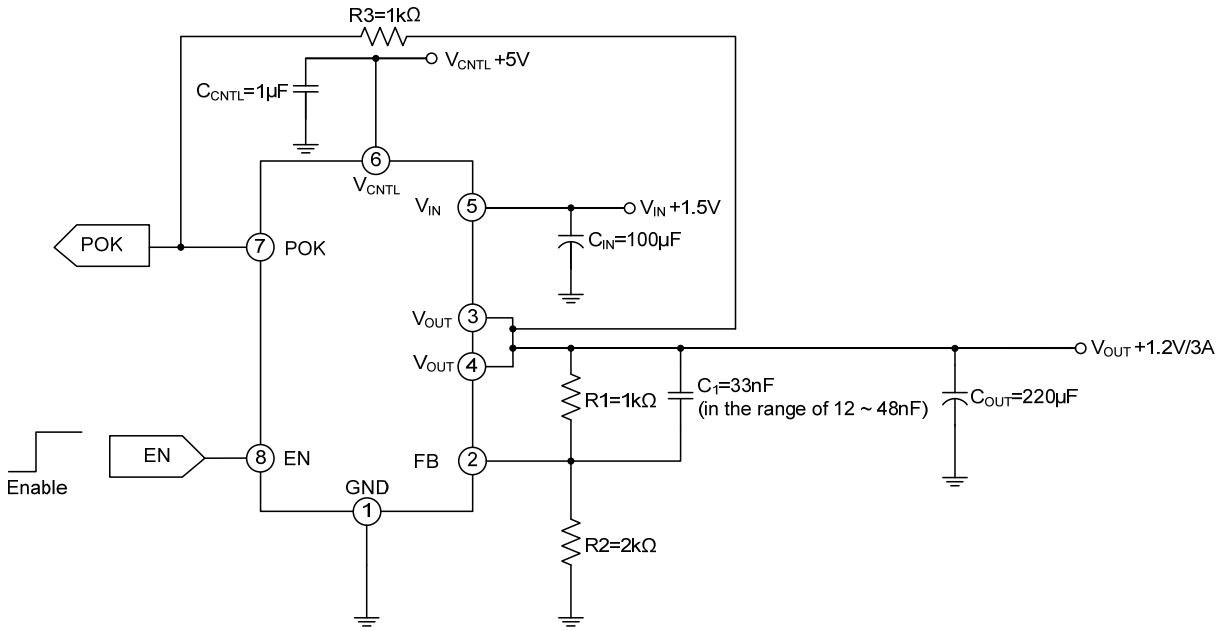
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CNTL} Nominal Supply Current		I_{CNTL}	EN = V_{CNTL}	0.4	1	2	mA
V_{CNTL} Shutdown Current		I_{SD}	EN = GND		180	380	μA
POR Threshold	V_{CNTL}	V_{THR}	V_{CNTL} Rising	2.7	2.9	3.1	V
	V_{IN}		V_{IN} Rising	0.8	0.9	1.0	V
POR Hysteresis	V_{CNTL}	V_{HYS}			0.4		V
	V_{IN}				0.5		V
Reference Voltage		V_{REF}	FB =V_{OUT}		0.8		V
Output Voltage Accuracy			I_{OUT}=0A~3A, T_J= -25 ~125°C	-1.5		+1.5	%
Line Regulation		$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	V_{CNTL}=3.3~5V		0	0.13	%/V
Load Regulation		$\frac{\Delta V_{OUT}}{V_{OUT}}$	I_{OUT}=0A~3A		0.06	0.15	%
Current Limit		I_{LIMIT}	V_{CNTL}=5V, T_J= 25°C	4.8	5.7	6.6	A
			V_{CNTL}=5V, T_J= -25 ~ +125°C	4			A
			V_{CNTL}=3.3V, T_J= 25°C	4.6	5.5	6.4	A
			V_{CNTL}=3.3V, T_J= -25 ~ +125°C	3.8			A
Dropout Voltage		V_D	V_{CNTL}=5V, I_{OUT}=3A, T_J= 25°C		0.17	0.25	V
			V_{CNTL}=5V, I_{OUT}=3A, T_J= -50~+125°C			0.3	V

■ ELECTRICAL CHARACTERISTICS(Cont.)

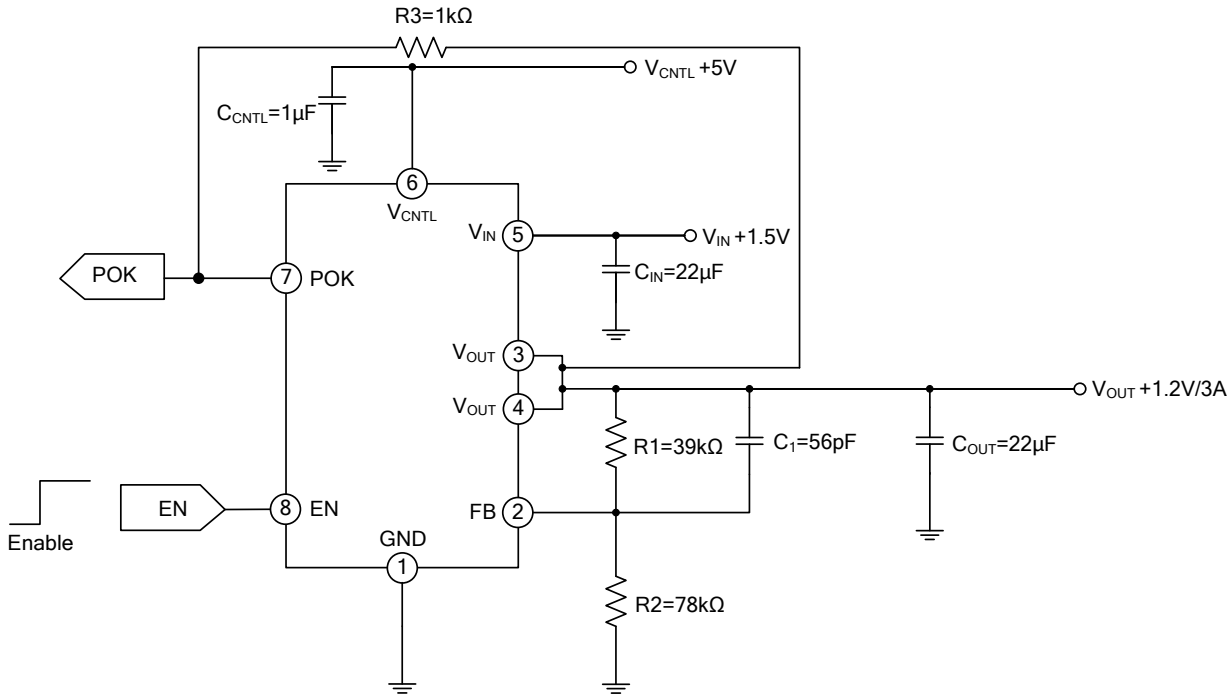
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Over Temperature Shutdown	OTS	T_J Rising		150		°C
Over Temperature Hysteresis	OTH			50		°C
Under-Voltage Threshold		V_{FB} Falling		0.4		V
EN Logic High Threshold Voltage		V_{EN} Rising	0.3	0.4	0.5	V
EN Hysteresis				30		mV
EN Pin Pull-Up Current		EN=GND		10		μA
Soft-Start Interval	T_{SS}			2		ms
POK Threshold Voltage for Power OK	V_{POK}	V_{FB} Rising	90%	92%	94%	V_{REF}
POK Threshold Voltage for Power Not OK	V_{PNOK}	V_{FB} Falling	79%	81%	83%	V_{REF}
POK Low Voltage		POK sinks 5mA		0.25	0.4	V
POK Delay Time	T_{DELAY}		1	3	10	ms

■ TYPICAL APPLICATION CIRCUIT

1. Using an Output Capacitor with ESR≥18mΩ



2. Using an MLCC as the Output Capacitor



V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)
1.05	43	137.6	47
1.5	27	30.86	82
1.8	15	12	150

■ APPLICATION INFORMATION

1. Power Sequencing

When there's no main voltage applied at V_{IN}, it is suggested not to apply a voltage to V_{OUT} for a long time. Because the internal parasitic diode (between V_{OUT} to V_{IN}) will conduct and dissipate power, there's no protection.

2. Output Capacitor

A proper output capacitor to maintain stability and improve transient response over temperature and current is necessary. Proper ESR (equivalent series resistance) and capacitance of the output capacitor should be selected properly for stability of the normal operation and good load transient response.

Many kinds of capacitors can be used as an output capacitor, such as ultra-low-ESR capacitors (like ceramic chip capacitors), low-ESR bulk capacitors (like solid Tantalum, POSCap, and Aluminum electrolytic capacitors). And also the value of the output capacitors' can be increased without limit.

In the applications with large stepping load current, the low-ESR bulk capacitors are normally recommended.

Decoupling ceramic capacitors are recommended to be placed at the load and ground pins very closely and also the impedance of the layout must be minimized.

3. Input Capacitor

In order to prevent the input rail from dropping, the proper input capacitor to supply current surge during stepping load transients is required. Because the limited slew rate of the surge currents, more parasitic inductance needs more input capacitance.

Ultra-low-ESR capacitors (>100mF, ESR<300mW) is recommended for the input capacitor.

4. Feedback Network

The following figure shows the feedback network between V_{OUT} GND and FB pins. Working with the internal error amplifier, the feedback network can provide proper frequency response for the UTC LADLD30.