

SANYO	No.1774E	LA7530N
		IF Signal Processing (VIF + SIF) Circuit for TV / VCR Use

The LA7530N is an IC containing the VIF section and SIF section on a single chip in the DIP20S package. The use of the small-sized package serves to make VTR tuner units smaller.

As compared with the LA7530, the LA7530N is provided with 2 pins for IF AGC, permitting higher AGC speed. The LA7530N can substitute for the LA7530, but the LA7530 cannot substitute for the LA7530N. For 9V supply, use the LA7533.

Functions

- VIF section: VIF AMP, VIDEO DET, PEAK IF AGC, B/W NOISE CANCELLER, RF AGC, AFT, VIDEO MUTE.
- SIF section: SIF LIMITER AMP, FM DET, SND MUTE.

Features

- High-gain VIF amp requiring no preamp.
- Higher AGC speed.
- Adjustment-free FM detector because of ceramic discriminator-used quadrature detection.
- Possible to mute video, sound for VTR.
- Small-sized package.
- Minimum number of external parts required.

Maximum Ratings at $T_a = 25^\circ\text{C}$

Maximum Supply Voltage	$V_{CC \text{ max}}$	14	V
Flow-out Current	$I_{16 \text{ max}}$	5	mA
Maximum Applied Voltage	$V_{20 \text{ max}}$	V_{CC}	V
Allowable Power Dissipation	$P_d \text{ max}$	1.1	W
Operating Temperature	T_{opr}	-20 to +70	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

$T_a \leq 40^\circ\text{C}$

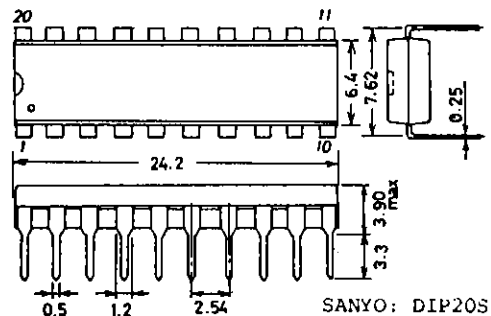
Operating Conditions at $T_a = 25^\circ\text{C}$

Recommended Supply Voltage	V_{CC}	12	V
Operating Voltage Range	$V_{CC \text{ op}}$	9 to 13.2	V

Package Dimensions

(unit : mm)

3021B



SANYO: DIP20S

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LA7530N

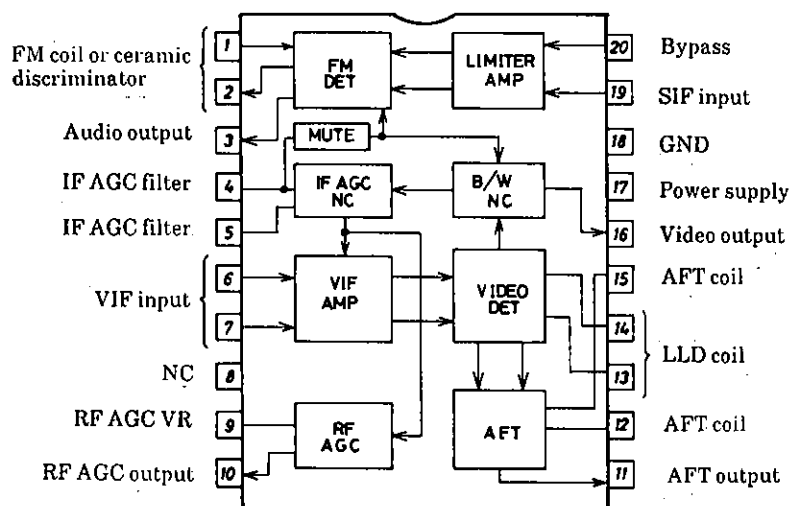
Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, $f_p = 58.75\text{MHz}$, $f_s = 54.25\text{MHz}$ (VIF),
 $f_o = 4.5\text{MHz}$ (SIF)

			min	typ	max	unit
Total Circuit Current	I_{17}	DC	47	58	74	mA
Maximum RF AGC Voltage	V_{10H}	DC	8.5	8.9	9.2	V
Minimum RF AGC Voltage	V_{10L}	DC			0.5	V
Quiescent Video Output Voltage	V_{16}	DC	5.7	6.1	6.5	V
Quiescent AFT Output Voltage	V_{11}	DC	4.5	6.5	7.5	V
Input Sensitivity	V_i	$f_m = 400\text{Hz}$, 40%AM, $V_o = 0.8\text{Vp-p}$	30	36	42	dB μ
AGC Range	GR	$f_m = 400\text{Hz}$, 40%AM, $V_o = 0.8\text{Vp-p}$	57	65		dB
Maximum Allowable Input	$V_i \text{ max}$	$f_m = 15\text{kHz}$, 78%AM, $V_o = \pm 1\text{dB}$	100	200		mVrms
Video Output Amplitude	V_o (VIDEO)	$V_i = 10\text{mVrms}$, $f_m = 15\text{kHz}$, 78%AM	1.9	2.2	2.5	Vp-p
Output S/N	S/N	$V_i = 10\text{mVrms}$ CW	48	54		dB
Carrier Leak	CL	$V_i = 100\text{mVrms}$, $f_m = 15\text{kHz}$, 78%AM	50	55		dB
Maximum AFT Voltage	V_{11H}	$V_i = 10\text{mVrms}$ CW SWEEP	11	11.4		V
Minimum AFT Voltage	V_{11L}	$V_i = 10\text{mVrms}$ CW SWEEP		0.5	1.0	V
AFT Detection Sensitivity	S_f	$V_i = 10\text{mVrms}$ CW SWEEP	80	110	150	mV/kHz
White Noise Threshold Level	V_{WTH}	$V_i = 10\text{mVrms}$ SWEEP	6.4	6.8	7.2	V
White Noise Clamp Level	V_{WCL}	$V_i = 10\text{mVrms}$ SWEEP	4.2	4.6	5.0	V
Black Noise Threshold Level	V_{BTH}	$V_i = 10\text{mVrms}$ SWEEP	2.1	2.4	2.7	V
Black Noise Clamp Level	V_{BCL}	$V_i = 10\text{mVrms}$ SWEEP	3.8	4.2	4.6	V
SIF Output Signal Voltage	V_o (SIF)	P/S = 20dB	80	140	210	mVrms
Frequency Characteristic	f_c	-3dB	5	7		MHz
Differential Gain	DG	$V_i = -27\text{dBm}$ (peak) 87.5% VIDEOMOD		3		%
Differential Phase	DP	$V_i = -27\text{dBm}$ (peak) 87.5% VIDEOMOD		3		deg
Input Resistance	R_i		1.0	1.5	2.0	k Ω
Input Capacitance	C_i			3.0	6.0	pF
SIF Limiting Voltage	V_i (lim)	-3dB		200	500	μVrms
Detection Output Voltage	V_o (DET)	$V_i = 100\text{mVrms}$, $f_m = 400\text{Hz}$, $\Delta f = \pm 25\text{kHz}$	450	680	850	mVrms
Total Harmonic Distortion	THD (DET)	$V_i = 100\text{mVrms}$, $f_m = 400\text{Hz}$, $\Delta f = \pm 25\text{kHz}$		0.5	1.3	%
AM Rejection	AMR	$V_i = 100\text{mVrms}$, $f_m = 400\text{Hz}$, $\Delta f = \pm 25\text{kHz}$, 30%AM	50	60		dB

Usage Note : 1. Protective circuits must be inserted when using this IC with lines directly connecting the IC pins to external circuits.
 (For example, this applies to pins 12 and 15.)

2. A 1000pF capacitor must be connected between either pin 5 and ground or between pin 5 and pin 8 to prevent VIF amplifier oscillation.

Equivalent Circuit Block Diagram



[illegible]

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