Ordering number : ENA0490

LA5774MP

ON Semiconductor®

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Monolithic Linear IC

Separately-excited Step-down Switching Regulator (Variable Type)

Overview

The LA5774MP is a Separately-excited step-down switching regulator (variable type).

Functions

- Low-ESR capacitor with increased reliability applicable as the output smoothing capacitor.
- High efficiency.
- Four external parts.
- Time-base generator (160kHz) incorporated.
- Current limiter incorporated.
- Thermal shutdown circuit incorporated.
- Soft start circuit incorporated.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Input voltage	V_{IN} max		30	V
Maximum Output current	I_O max		3	A
SW pin application reverse voltage	V_{SW}		-1	V
Allowable power dissipation	Pd max	Mounted on a substrate.*	3.9	W
Operating temperature	Topr		-30 to +125	°C
Storage temperature	Tstg		-40 to +150	°C

* Specified substrate : 76.1×114.3×1.6mm^3 : Copper foil ratio 60% FR4

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage range	V_{IN}		4.5 to 28	V

Electrical Characteristics at Ta = 25°C, V_O = 3.3V

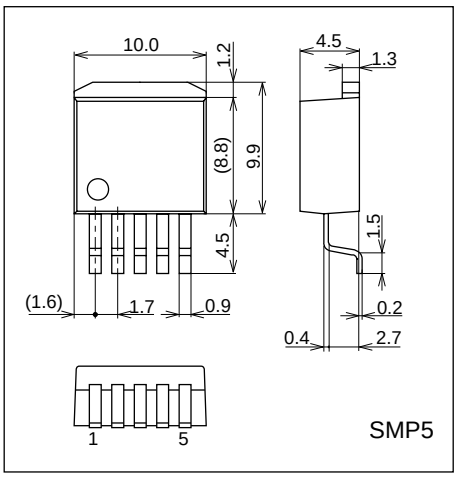
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage	V_{OS}	V_{IN} = 15V, I_O = 1.0A	1.235	1.26	1.285	V
Efficiency	η	V_{IN} = 15V, I_O = 1.0A		78		%
Switching frequency	f	V_{IN} = 15V, I_O = 1.0A	128	160	192	kHz
Line regulation	ΔV_OLINE	V_{IN} = 8 to 20V, I_O = 1A		40	100	mV
Load regulation	ΔV_OLOAD	V_{IN} = 15V, I_O = 0.5 to 1.5A		10	30	mV
Output voltage temperature coefficient	$\Delta V_O/\Delta Ta$	Designed target value. *		±0.5		mV/°C
Ripple attenuation factor	RREJ	f = 100 to 120Hz		45		dB
Current limiter operating voltage	I_S	V_{IN} = 15V	3.1			A
Thermal shutdown operating temperature	TSD	Designed target value. *		165		°C
Thermal shutdown Hysteresis width	ΔTSD	Designed target value. *		15		°C

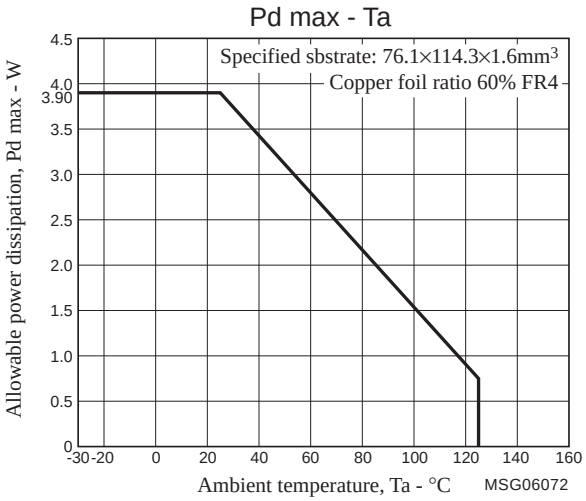
* Design target value: No measurement made.

Package Dimensions

unit : mm (typ)

3275

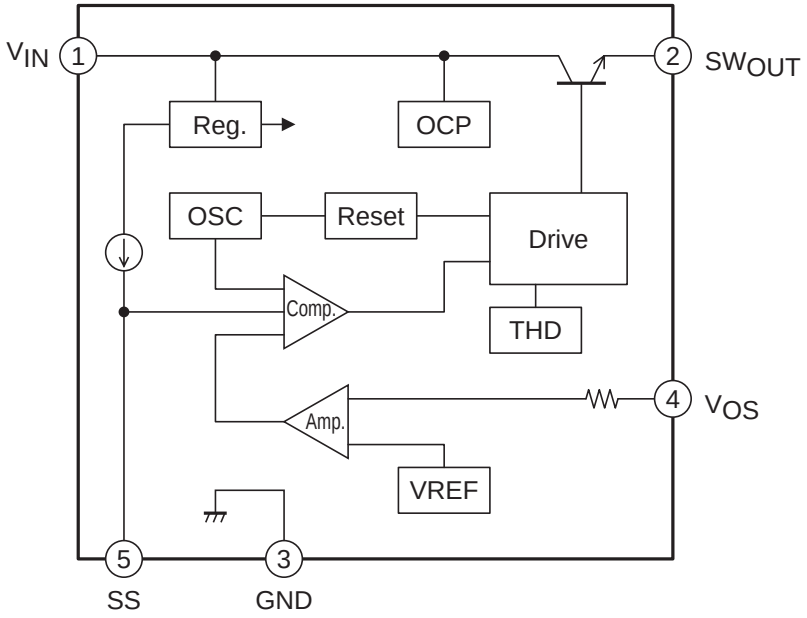




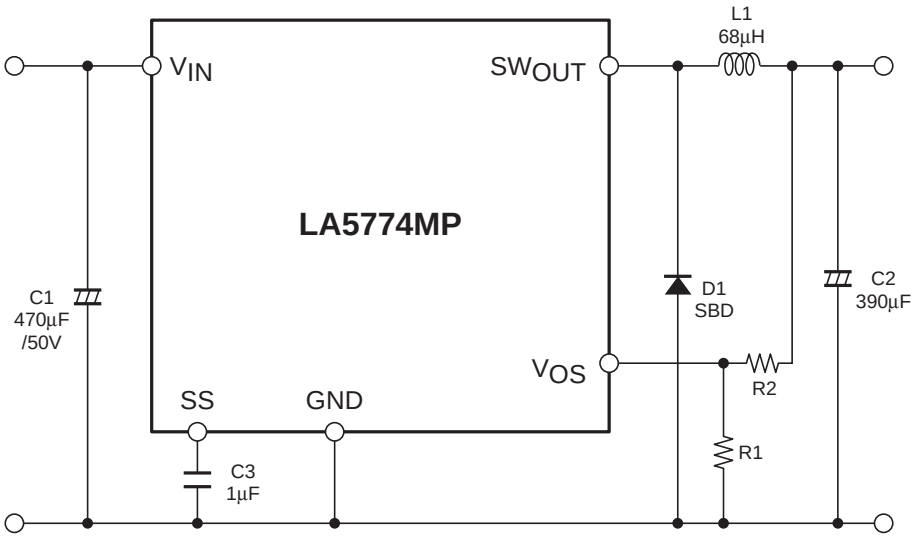
Pin Assignment

(1) V_{IN} (2) SW_{OUT} (3) GND (4) V_{OS} (5) SS

Block Diagram



Application Circuit Example



Notes: C3 is for the soft start function. Delete C3 and keep the SS pin open when the soft start function is not necessary.

Description of Functional Settings

1. Calculation equation to set the output voltage
   This IC controls the switching output so that the V_{OS} pin voltage becomes 1.26V (typ).
   The equation to set the output voltage is as follows:

$$V_O = \left(1 + \frac{R2}{R1}\right) \times 1.26V(typ)$$

   The VOS pin has the inrush current of 1μA (typ). Therefore, the error becomes larger when R1 and R2 resistance values are large.

2. Start delay function
   The SS pin has the internally-connected 22μA (typ) constant-current supply. When the voltage of SS pin exceeds the threshold voltage, the regulator starts operation. As the threshold voltage is 0.62V (typ), the start delay time can be calculated as follows:
   ex. For setting at 1μF

$$Td = \frac{C \times V}{i} = \frac{1\mu F \times 0.62}{22\mu A} = 28.2\ ms$$

3. Soft start function
   The internal PWM waveform has the voltage value as shown in the right.
   If down-conversion from the voltage of V_{IN} = 15 V to V_{IN} = 3.3V is to be made, for example, the PWM-ON duty has the value as shown below.



PWM wave

$$PWMduty = \frac{V_{OUT}}{V_{IN} - Vsat + VF} = 23\ \%$$

   (Note that calculation is made with Vsat = 1V and VF = 0.2V)

   The output voltage of error amplifier, which is 3.3 V, is the value with PWM = 23%, as calculated in the above equation, so that this voltage is determined as follows:

$$\boldsymbol{Ver = (\Delta VPWM) \times PWMduty + VPWML = 0.88V \times 0.23 + 0.62V = 0.82V}$$

   (ΔVPWM is the PWM amplitude value or 0.88V(typ) while VPWML is the lower limit voltage of PWM waveform or 0.62V(typ))

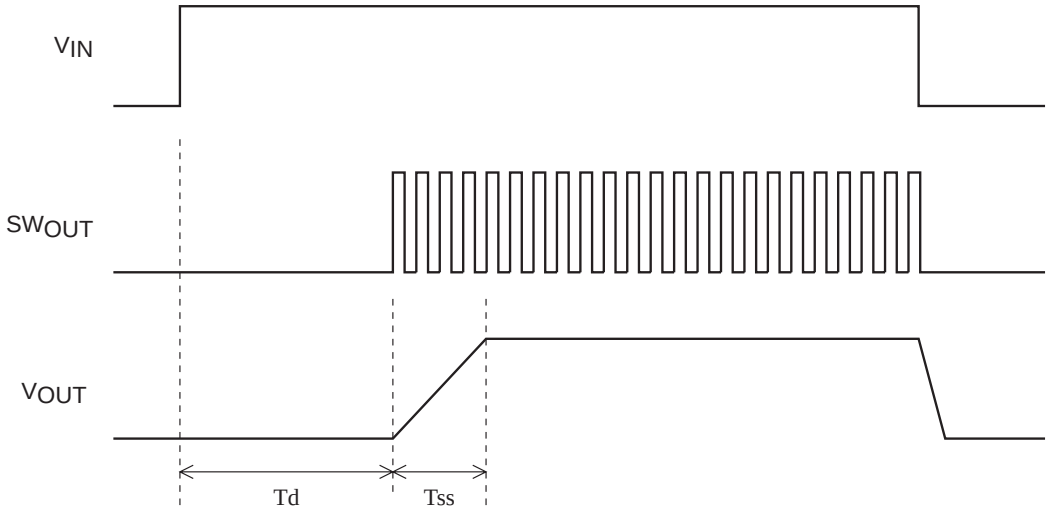
   SS pin and error amplifier output voltages are designed to prefer the lower voltages, so that V_{OUT} will reach the designed regulation voltage in timing when the SS pin voltage exceeds the error amplifier output.
   Therefore, the soft start time is calculated as follows:

$$Tss = \frac{C \times \Delta VPWM \times PWMduty}{i} = \frac{C \times 0.88 \times PWMduty}{22\mu A}$$

   For the set conditions of C = 1μF and PWMduty = 23%:

$$Tss = \frac{1\mu F \times 0.88V \times 0.23}{22\mu A} = 9.2ms$$

Timing Chart



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