Ordering number: EN4024

Monolithic Linear IC

SANYO No. 4024

LA4534M

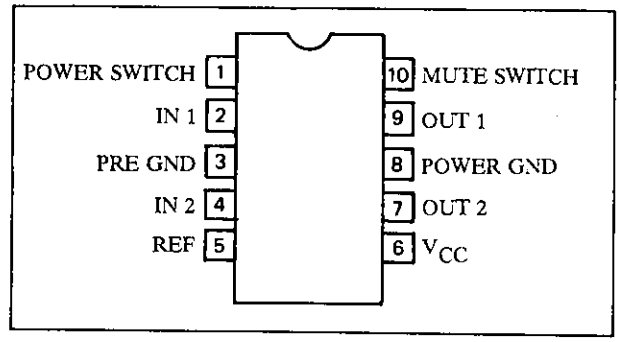
3V CD Headphone-stereo Power Amp

The LA4534M is a low noise, low distortion headphone-stereo power IC designed for use in a portable CD.

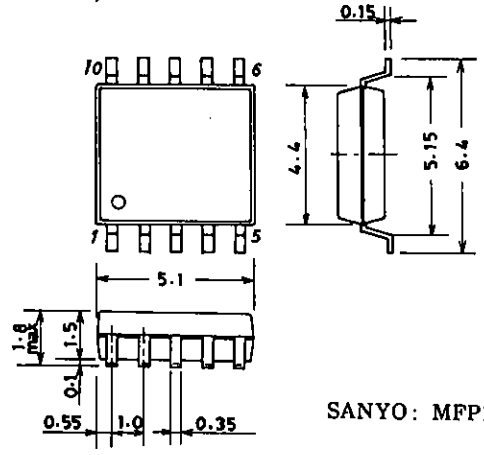
Features

- Low power consumption
- Can drive 16-Ω load
- Excellent performance with reduced supply voltage
- Excellent ripple rejection
- Power switch function, built-in muting circuit
- Low noise (7 μV),low gain (11 dB)

Pinout



Package Dimensions 3086A
(unit: mm)



SANYO: MFP10S

Maximum Ratings at Ta = 25°C

				unit
Maximum Supply Voltage	V_{CC} max	Quiescent time	4.5	V
Allowable Power Dissipation	Pd max		300	mW
Operating Temperature	Topg		-20 to +75	°C
Storage Temperature	Tstg		-40 to +125	°C

Operating Conditions at Ta = 25°C

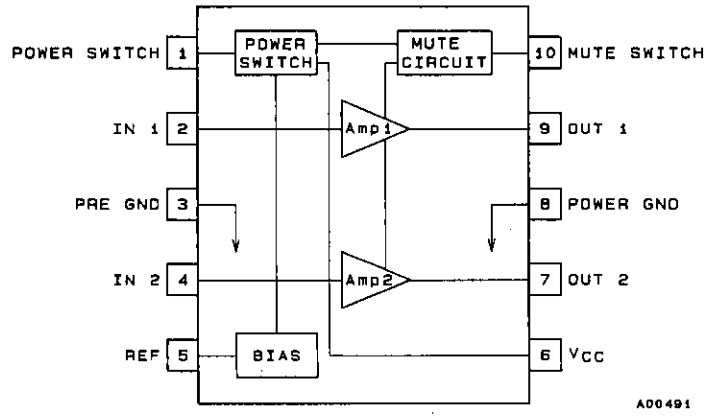
			unit
Recommended Supply Voltage	V_{CC}	3.0	V
Operating Voltage Range	V_{CC} op	1.6 to 4.0	V
Recommended Load Impedance	R_L	16 to 32	Ω

Operating Characteristics at Ta = 25°C, R_L = 16 Ω, Rg = 600 Ω, Measurements taken with specified circuit

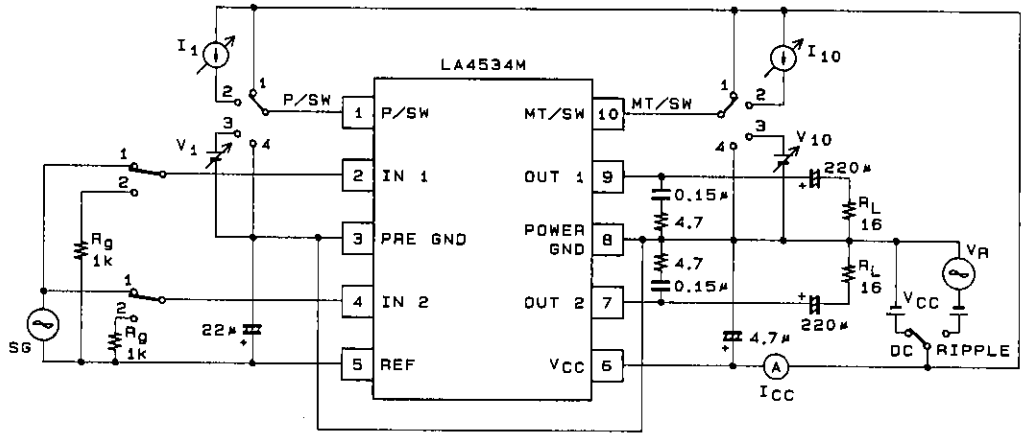
			min	typ	max	unit
Quiescent Current	Icco (1)	V_{CC} = 2.4 V, Quiescent time		5.4	10	mA
	Icco (2)	V_{CC} = 4.5 V, Pin 10 to GND		1.1	2.0	mA
	Icco (3)	V_{CC} = 4.5 V, Pin 1 to GND			1.0	μA
Voltage Gain	VG (1)	V_{CC} = 2.4 V, f = 1 kHz, V_O = -10 dBm	9	11	13	dB
	VG (2)	V_{CC} = 1.6 V, f = 1 kHz, V_O = -20 dBm	9	11	13	dB
Voltage Gain Variations	ΔVG (1)	V_{CC} = 2.4 V, f = 1 kHz, V_O = -10 dBm			1.0	dB
	ΔVG (2)	V_{CC} = 1.6 V, f = 1 kHz, V_O = -20 dBm			1.0	dB
Total Harmonic Distortion	THD	V_{CC} = 2.0 V, f = 1 kHz, P_O = 1 mW		0.08	0.24	%
Output Power	P_O	V_{CC} = 3.0 V, f = 1 kHz, THD = 10%	25	50		mW
Crosstalk	CT	V_{CC} = 2.4 V, f = 1 kHz, Rg = 1 kΩ, V_O = -10 dBm	40	50		dB
Ripple Rejection	SVRR	V_{CC} = 1.6 V, f = 100 Hz, Rg = 1 kΩ, V_R = -20 dBm, BPF = 100 Hz	50	70		dB
Output Noise Voltage	V_{NO}	V_{CC} = 4.5 V, Rg = 1 kΩ, BPF = 20 Hz to 20 kHz		7	20	μV
Power Off Effect	V_O (off)	V_{CC} = 1.6 V, f = 100 Hz, Pin 1 to GND, Vi = -10 dBm			-80	dBm
Mute Effect	V_O (MT)	V_{CC} = 1.6 V, f = 100 Hz, Pin 10 to GND, Vi = -10 dBm			-80	dBm
Power On Current Sensitivity	I1 (on)	V_{CC} = 1.5 V, V5 ≥ 0.85 V		0.05	1.0	μA
Power Off Voltage Sensitivity	V1 (off)	V_{CC} = 1.5 V, V5 ≤ 0.1 V	0.5	0.6		V
Mute Off Current Sensitivity	I10 (off)	V_{CC} = 1.5 V, V5 ≥ 0.85 V		0.2	1.0	μA
Mute On Voltage Sensitivity	V10 (on)	V_{CC} = 1.5 V, V5 ≤ 0.1 V	0.5	0.65		V

Note) Quiescent current is the current flowing into pin 6. Current flowing into pin 1 or 10 is the maximum value and calculated from the equation (V pin -0.5 V)/16 [V/kΩ], increasing total current.

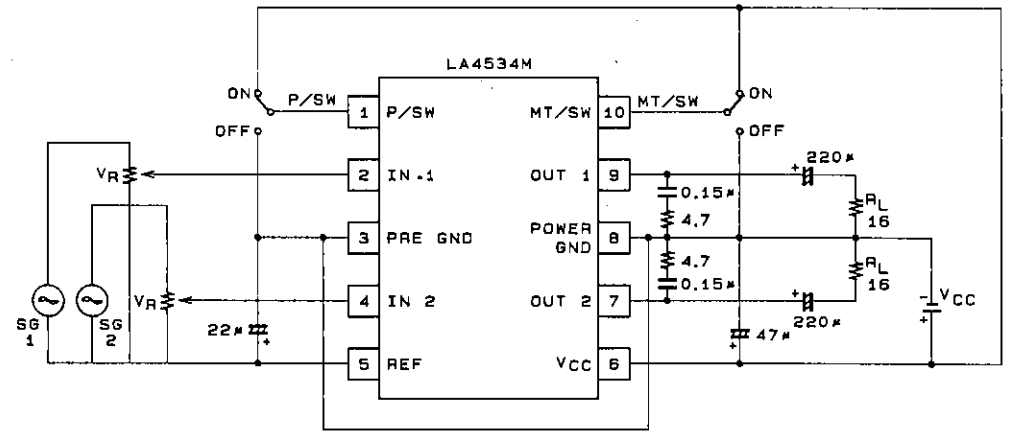
Block Diagram



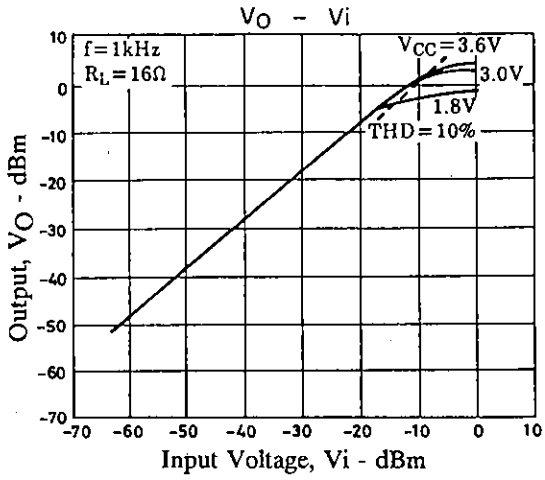
Test Circuit

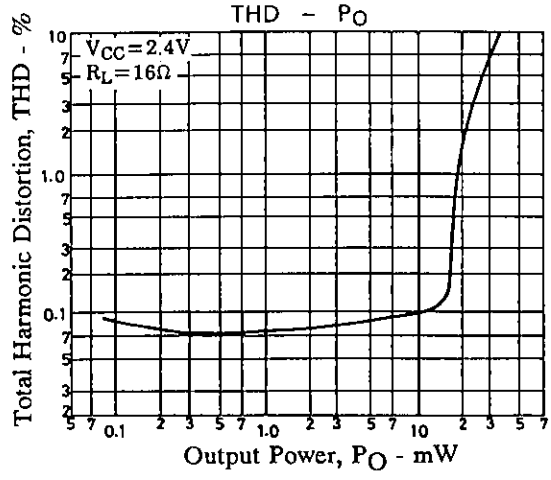


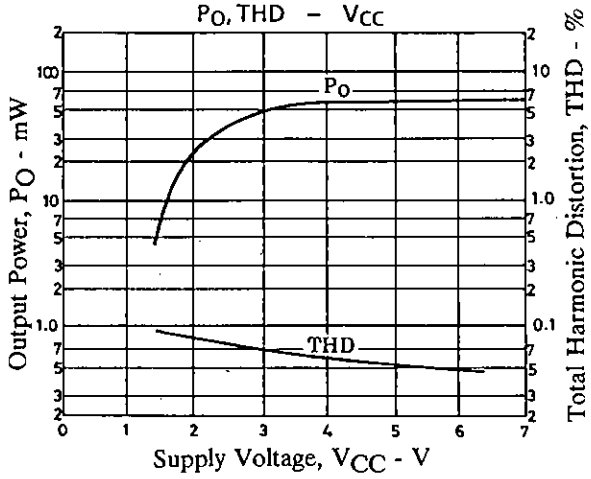
Typical Application

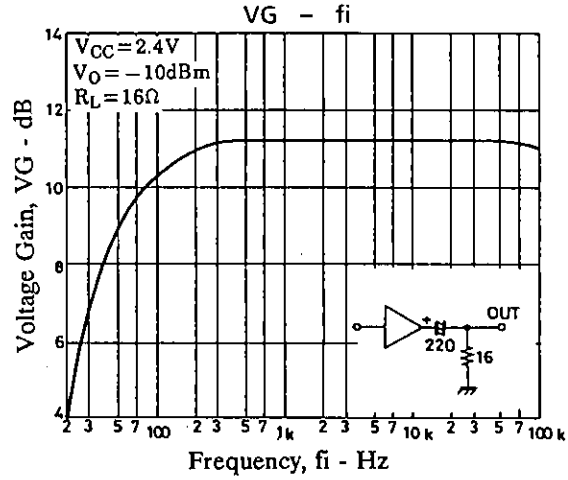


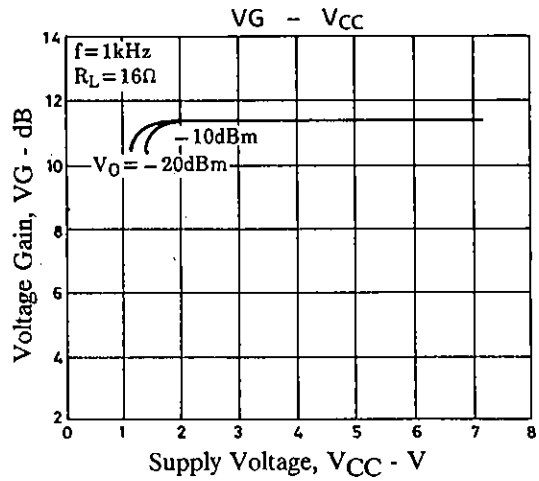
Unit (resistance: Ω, capacitance: F)

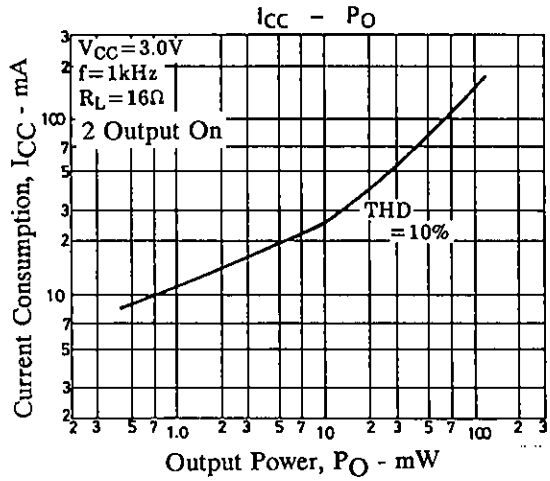

VO – Vi
f=1kHz
RL=16Ω
VCC=3.6V
3.0V
1.8V
THD=10%
Output, VO - dBm
Input Voltage, Vi - dBm

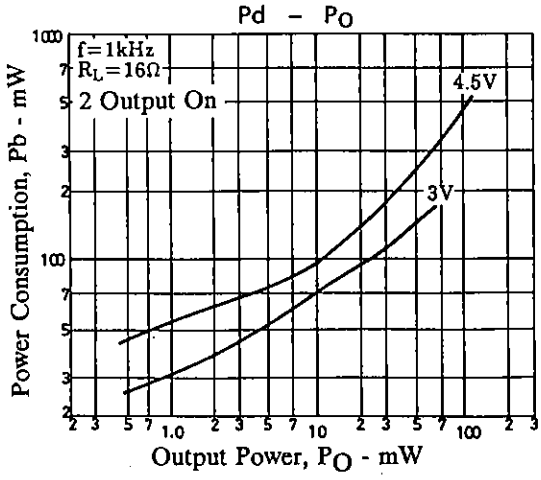

THD – PO
VCC=2.4V
RL=16Ω
Total Harmonic Distortion, THD - %
Output Power, PO - mW

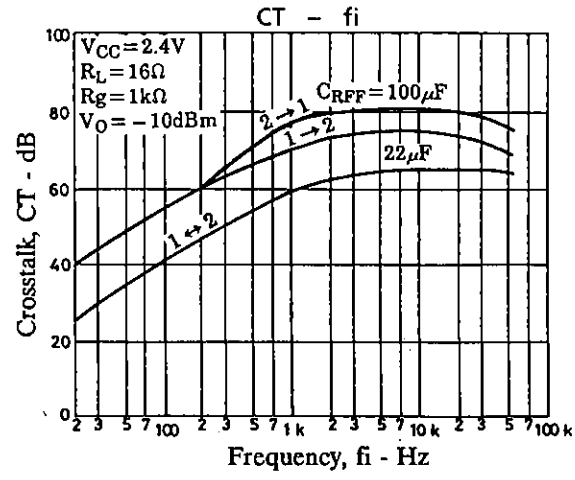

PO, THD – VCC
PO
THD
Output Power, PO - mW
Total Harmonic Distortion, THD - %
Supply Voltage, VCC - V


VG – fi
VCC=2.4V
VO=–10dBm
RL=16Ω
OUT
220
16
Voltage Gain, VG - dB
Frequency, fi - Hz

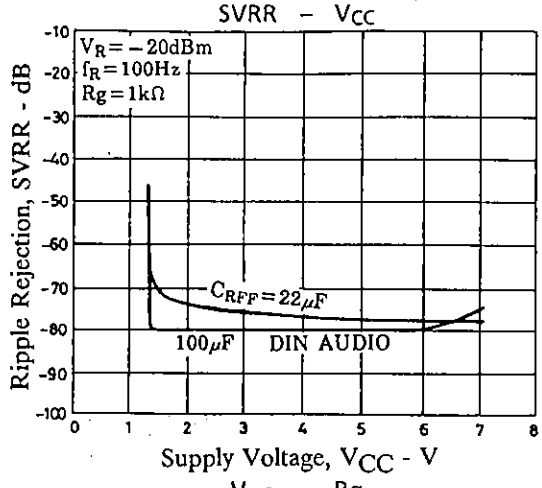

VG – VCC
f=1kHz
RL=16Ω
–10dBm
VO=–20dBm
Voltage Gain, VG - dB
Supply Voltage, VCC - V


ICC – PO
VCC=3.0V
f=1kHz
RL=16Ω
2 Output On
THD
=10%
Current Consumption, ICC - mA
Output Power, PO - mW

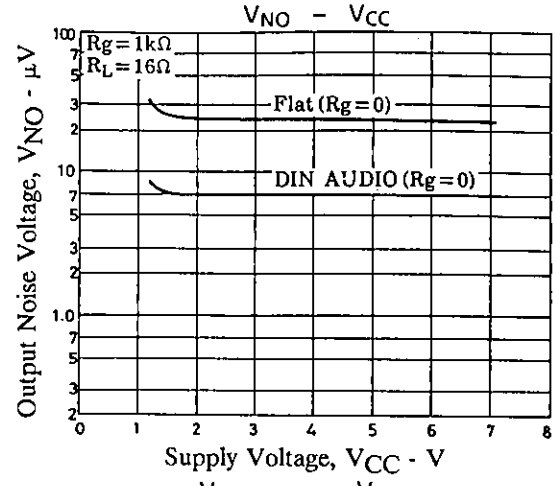

Pd – PO
f=1kHz
RL=16Ω
2 Output On
4.5V
3V
Power Consumption, Pb - mW
Output Power, PO - mW


CT – fi
VCC=2.4V
RL=16Ω
Rg=1kΩ
VO=–10dBm
CRFF=100μF
2→1
1→2
22μF
1↔2
Crosstalk, CT - dB
Frequency, fi - Hz

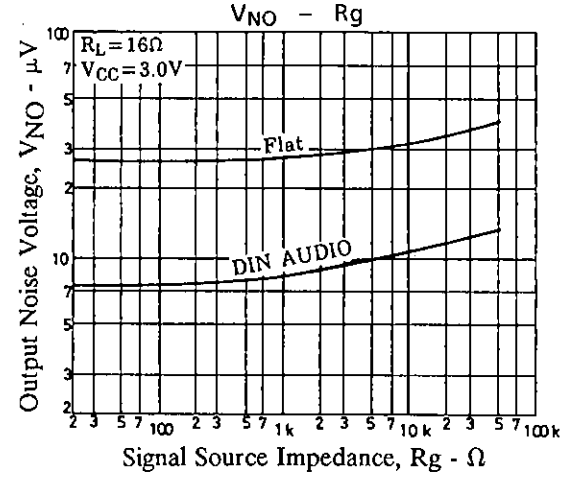
SVRR – V_{CC}



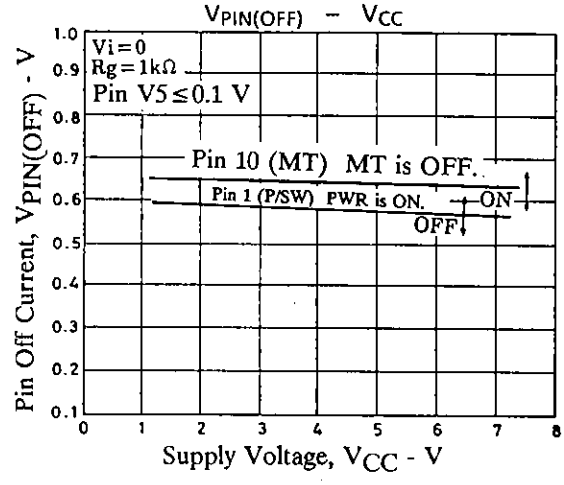
V_{NO} – V_{CC}



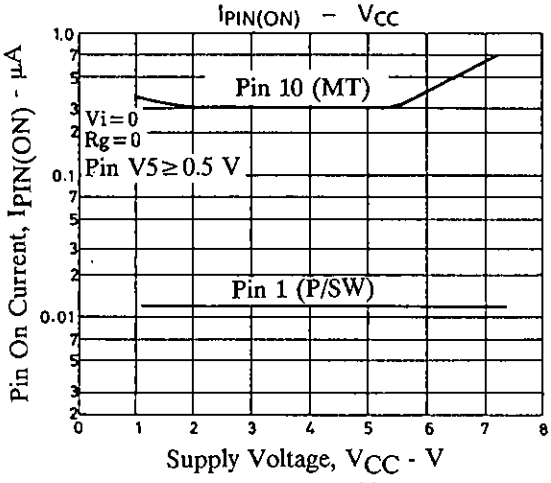
V_{NO} – Rg



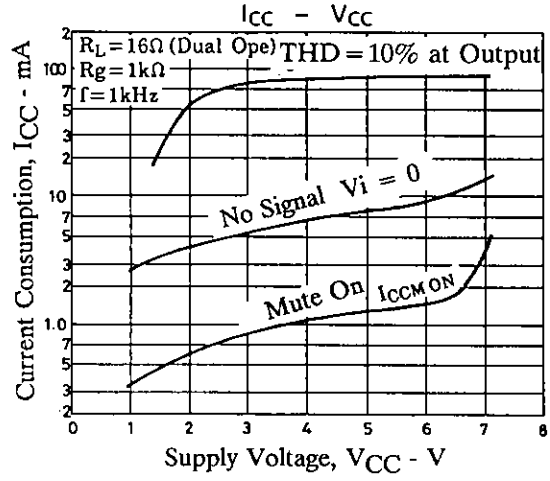
$V_{PIN(OFF)}$ – V_{CC}



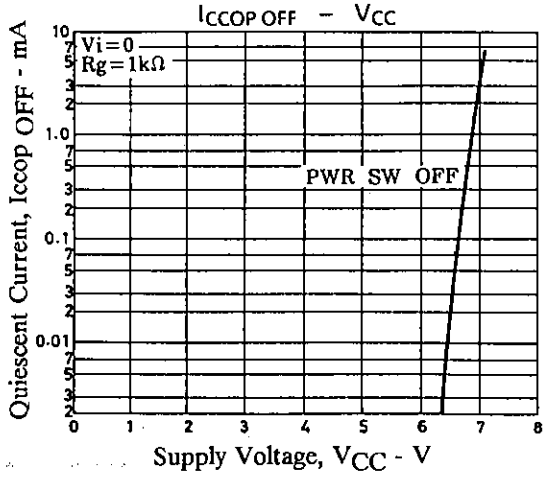
$I_{PIN(ON)}$ – V_{CC}



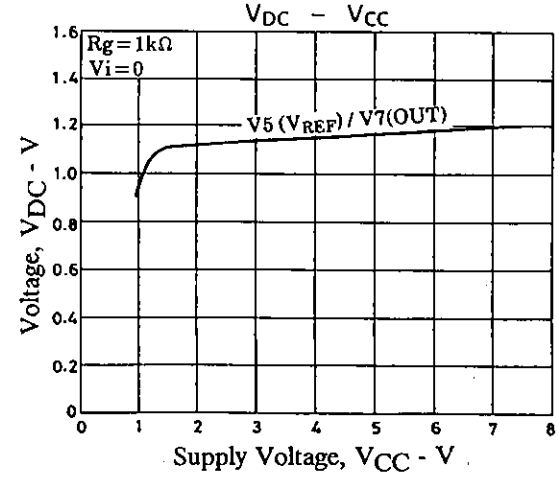
I_{CC} – V_{CC}

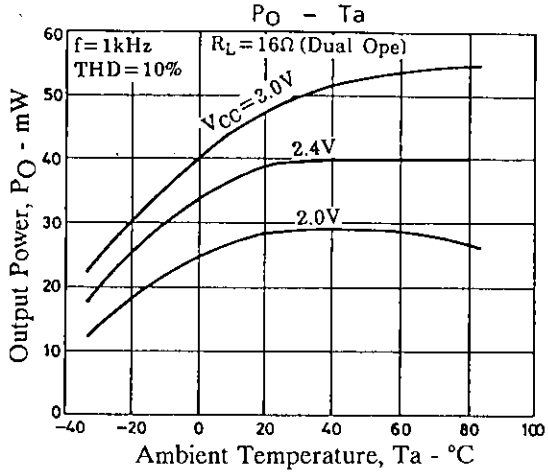


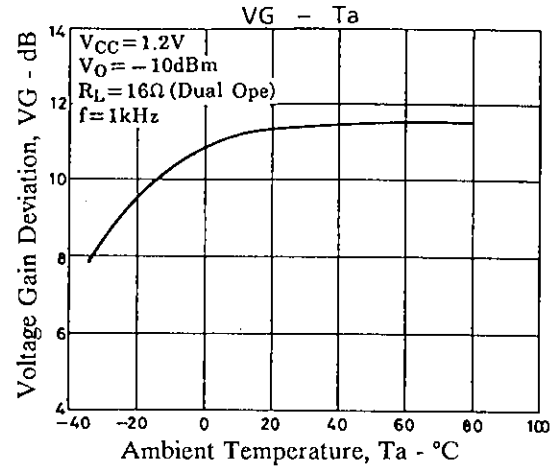
$I_{CCOP\,OFF}$ – V_{CC}

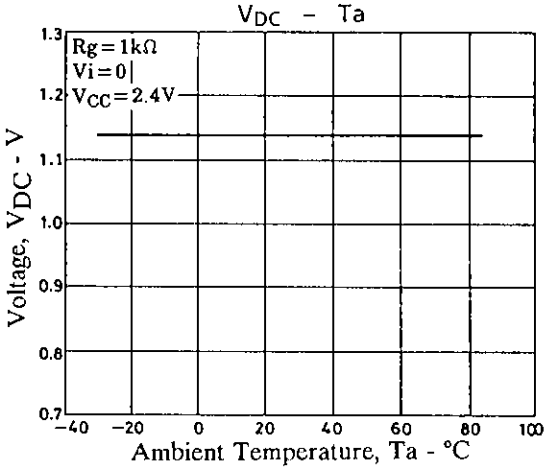


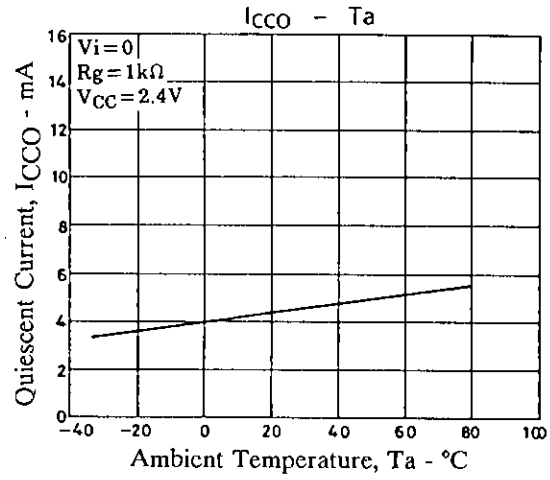
V_{DC} – V_{CC}



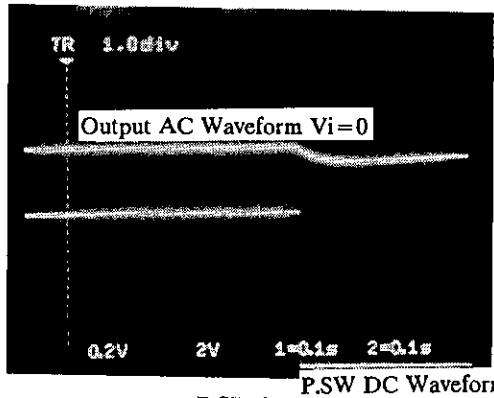




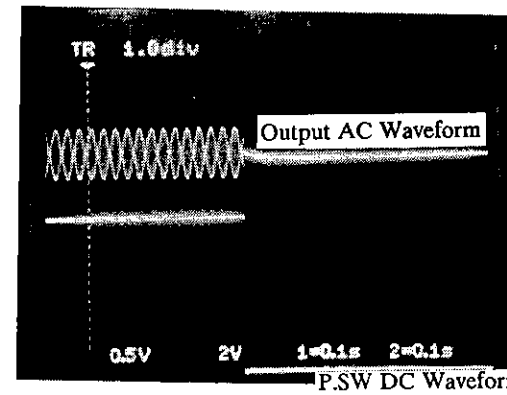




P.SW OFF

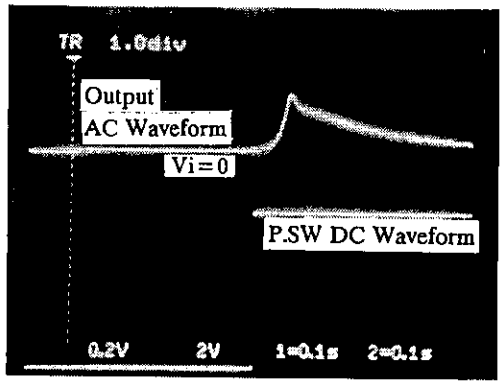


P.SW OFF

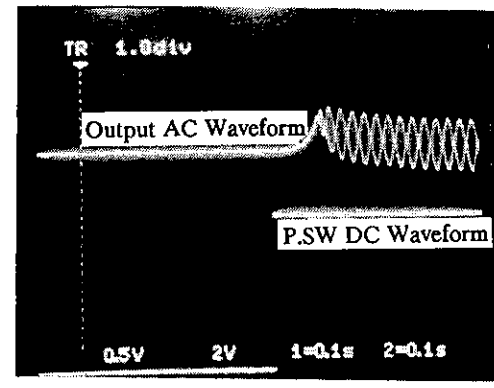


P. SW OFF

P.SW ON

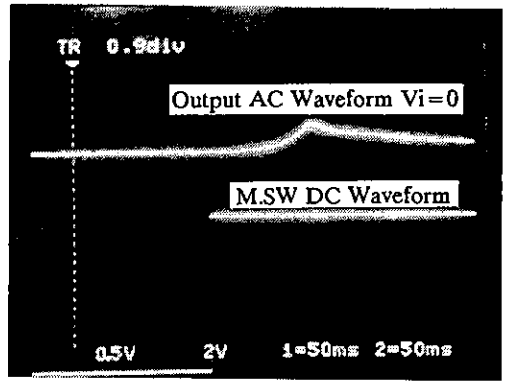


P.SW ON

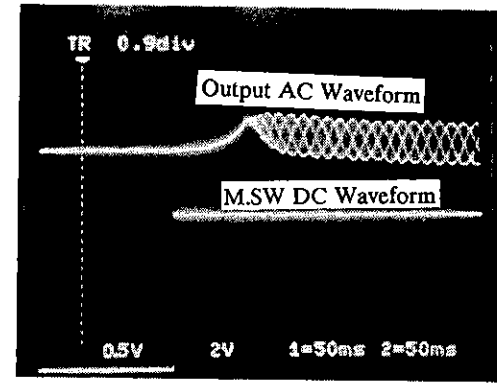


P.SW ON

M.SW OFF

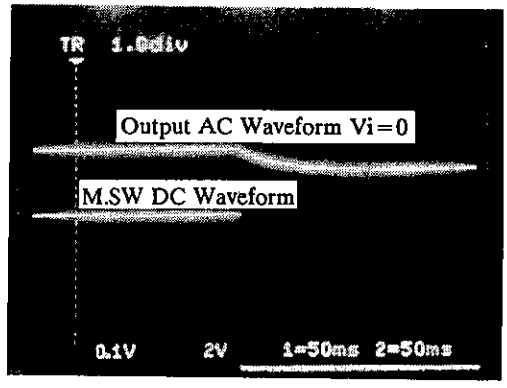


M.SW OFF

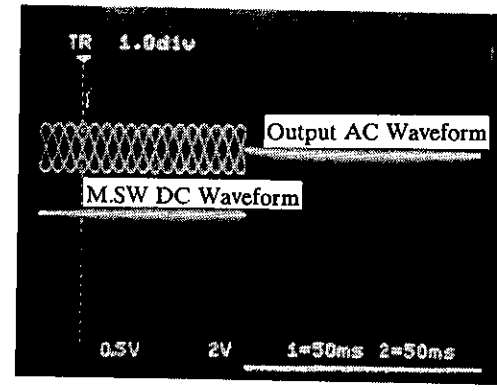


M.SW OFF

M.SW ON



M.SW ON

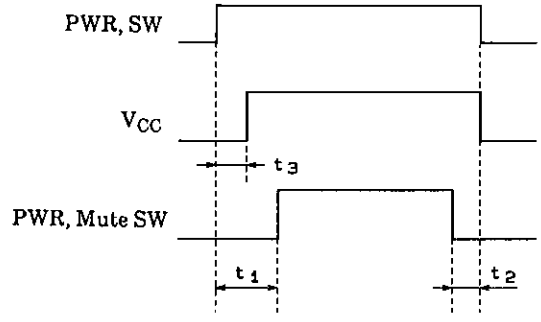


M.SW ON

Note on Application

Minimizing pop noise

The switching sequence shown below will generate minimum pop noises.



A00500

For minimum pop noise, the PWR mute switch should be turned on t1 (approx. 0.1 sec) after power-on and turned off t2 (approx. 0.1 sec) before power-off. That is, turn on and off the PWR mute switch while both power and V_{CC} are on.

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