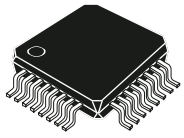
L99LD01

High efficiency constant current LED driver for automotive applications

Datasheet - production data



LQFP32
7x7 mm

GAPG1506151117CFT

Features

Max V_{BATT}	40	V
Operation supply battery voltage V_{BATT}	5.6 - 24	V
Oscillator frequency range	100 - 500	kHz

- Automotive qualified
- Constant current operation
- Current LED settable by external sensing resistor and adjustable via SPI
- Converter switching frequency adjustable by external resistor (R_{SF})
- EMC reduction by internal spread spectrum dither oscillator
- Low frequency PWM dimming operation.
- Maximum input current limiter
- Maximum switching duty cycle limiter
- Slope compensation adjustable by external resistor (R9)
- Battery overvoltage shut down protection (ext. R3, R4 resistors required)
- Led chain OV detection (ext. R5, R6)
- Multiplexed output for monitoring and control of LED temperature (external NTC resistor required), voltage of LED chain, and low frequency PWM
- SPI communication serial interface transceiver (SDI, SDO, SCK, CSN)
- Regulated output for micro supply 5 V ± 2 % -20 mA
- Parameter programming and settings of internal memory registers by the dedicated SPI interface:
  - LED current reference adjusting (± 66.7 %)
  - Maximum input current limiter reference adjusting (± 55.5 %)
  - Random dither frequency sweeping, modulation frequency and deviation percentage
- Power on reset pin output
- ESD protection

Applications

Automotive day time running light, LED HeadLamps

Description

L99LD01 is a precise constant current DC–DC converter LED driver for automotive applications, dedicated to the control of high-brightness LED headlights and housed in a LQFP32™ package.

The device is designed to be used in Boost, Buck-Boost and Fly back converter topologies. An internal random dither oscillator works in low frequency modulation, allowing the RF spectrum of the switching frequency to spread so to reduce EMC emissions. The slope compensation ensures good converter loop stability whatever is the duty cycle needed by the application.

The converter is able to work either in full power mode or in low frequency dimming mode.

The device includes an internal low drop voltage regulator, that can be used to supply a microcontroller, and a reset pin**,** that is useful for resetting the microcontroller at the start up and every time that the regulated output voltage falls down below an established voltage threshold.

This is information on a product in full production. www.st.com

Contents

1 Block diagram and pin description 6

2 Functional description 8

2.1 Operating modes 8

2.1.1 Operation with an external microcontroller 8

2.1.2 Stand alone operation 9

2.1.3 Start-up fail 9

2.1.4 Normal mode 10

2.1.5 Software limp home 10

2.1.6 Limp home mode 10

2.2 Protections and functions 16

2.2.1 LED current adjust and temperature control 16

2.2.2 Slope compensation 17

2.2.3 LED chain overvoltage detection 18

2.2.4 Battery overvoltage shutdown 19

2.2.5 Regulators thermal shut down 19

2.2.6 Reset 19

2.2.7 Watchdog 20

2.2.8 Standby and wake up by ENABLE pin 20

2.2.9 Frequency setting and dither effect 21

2.2.10 Start up LED overvoltage management 23

2.2.11 Programming the over/under voltage threshold 27

2.2.12 Input overvoltage programming 29

3 SPI functional description 31

3.1 Serial peripheral interface (ST SPI standard) 31

3.2 Signal description 32

3.3 SPI protocol 32

3.3.1 SDI, SDO format 32

3.3.2 Global status byte description 33

3.3.3 Operating code definition 34

3.4 Address mapping 37

3.5 Control registers (RAM) 38

3.6 Status registers 41

4 Electrical specifications 44
4.1 Absolute maximum ratings 44

5 Electrical characteristics 46

6 SPI electrical characteristics 54
6.1 DC characteristics 54
6.2 AC characteristics 54
6.3 Dynamic characteristics 55

7 Application circuits 59

8 Package information 65
8.1 ECOPACK® 65
8.2 LQFP32™ package information 65

9 Order codes 67

10 Revision history 68

List of tables

Table 1. Pin description . . . 7
Table 2. Limp home mode: recovery paths . . . 11
Table 3. Suggested K_L value and overvoltage thresholds . . . 29
Table 4. Command byte (8 bit) . . . 33
Table 5. Input data byte . . . 33
Table 6. Global status byte . . . 33
Table 7. Output data byte . . . 33
Table 8. Global status byte . . . 34
Table 9. Operation code definition . . . 34
Table 10. RAM memory map . . . 37
Table 11. ROM memory map . . . 37
Table 12. Internal oscillator frequency deviation settings . . . 39
Table 13. Internal oscillator frequency modulation settings . . . 39
Table 14. Watchdog timer status . . . 42
Table 15. Absolute maximum ratings . . . 44
Table 16. Thermal data . . . 45
Table 17. VS and V_{CC1} pin characteristics . . . 46
Table 18. V_{CC2} and C5V pin characteristics . . . 47
Table 19. NRES and LMODE pin characteristics . . . 48
Table 20. G1 driver 1 pin characteristics . . . 48
Table 21. G2 pin characteristics (driver2) . . . 48
Table 22. Converter oscillator and RSF pin characteristics . . . 49
Table 23. PWM_L, PWM, MOUT pin characteristics . . . 49
Table 24. ISENSE+, ISENSE- pin, and O.T.A. characteristics . . . 49
Table 25. SC pin characteristics . . . 51
Table 26. VLED pin characteristics . . . 51
Table 27. INP_OV pin characteristics (input overvoltage shut down) . . . 52
Table 28. NTC pin characteristics . . . 52
Table 29. ENABLE, LHM pin characteristics . . . 52
Table 30. Power on reset . . . 52
Table 31. Watchdog and timers parameters . . . 53
Table 32. SPI DC characteristics . . . 54
Table 33. SPI AC characteristics . . . 54
Table 34. SPI dynamic characteristics . . . 55
Table 35. LQFP32™ mechanical data . . . 66
Table 36. Device summary . . . 67
Table 37. Document revision history . . . 68

List of figures

Figure 1. Block diagram . . . 6
Figure 2. Connection diagram (top view – not in scale) . . . 6
Figure 3. Operating modes, main states . . . 11
Figure 4. Normal start up vs V_S ramp up and V_{CC1} voltage dips . . . 13
Figure 5. V_{CC1_FAIL} or V_{CC1} reset under voltage ($V_S > V_{SMIN}$) at start up . . . 14
Figure 6. V_{CC1} reset under voltage at start up ($V_S < V_{SMIN}$) and fast V_S ramp down . . . 15
Figure 7. Slow vs ramp down . . . 16
Figure 8. Internal structure of the slope compensation circuit . . . 18
Figure 9. Operation with a standalone LIN and ENABLE . . . 21
Figure 10. Operation with PM device and ENABLE (FSO active Low) . . . 21
Figure 11. Internal structure of main converter oscillator . . . 22
Figure 12. Converter frequency range vs R_{SF} and I_{RSF} vs frequency . . . 23
Figure 13. Correct start UP with no LED overvoltage failure . . . 25
Figure 14. LED overvoltage after t_{DStart} . . . 25
Figure 15. Device behavior in case the low to high transition of PWM_L signal happens after t_{DStart} expiration . . . 26
Figure 16. LED overvoltage event not caused by a VS overvoltage event . . . 26
Figure 17. LED overvoltage detection due to a possible battery VS overvoltage . . . 27
Figure 18. Behavior of LED overvoltage recovery bit with low on-time of PWM_L . . . 27
Figure 19. LED chain overvoltage thresholds settings. An example for boost and fly back converters 28
Figure 20. Input overvoltage programming . . . 29
Figure 21. Clock polarity and clock phase . . . 31
Figure 22. SPI global error information output . . . 32
Figure 23. SPI write operation . . . 35
Figure 24. SPI read operation . . . 35
Figure 25. SPI read and clear operation . . . 36
Figure 26. SPI read device information . . . 37
Figure 27. Principle of the WD_Status bits . . . 43
Figure 28. Voltage and current conventions . . . 44
Figure 29. SPI timing parameters . . . 56
Figure 30. SPI input and output timing parameters . . . 56
Figure 31. SPI maximum clock frequency . . . 57
Figure 32. NRES pin open drain structure . . . 57
Figure 33. Handshake procedure at start up with microcontroller on board . . . 58
Figure 34. Boost application circuit . . . 59
Figure 35. Fly back application circuit . . . 60
Figure 36. Buck-boost application circuit . . . 61
Figure 37. Stand alone application example for boost topology . . . 62
Figure 38. Reverse battery protection: an example for boost topology . . . 63
Figure 39. External MOS required during PWM dimming . . . 64
Figure 40. LQFP32™ package dimensions . . . 65

1 Block diagram and pin description

Figure 1. Block diagram

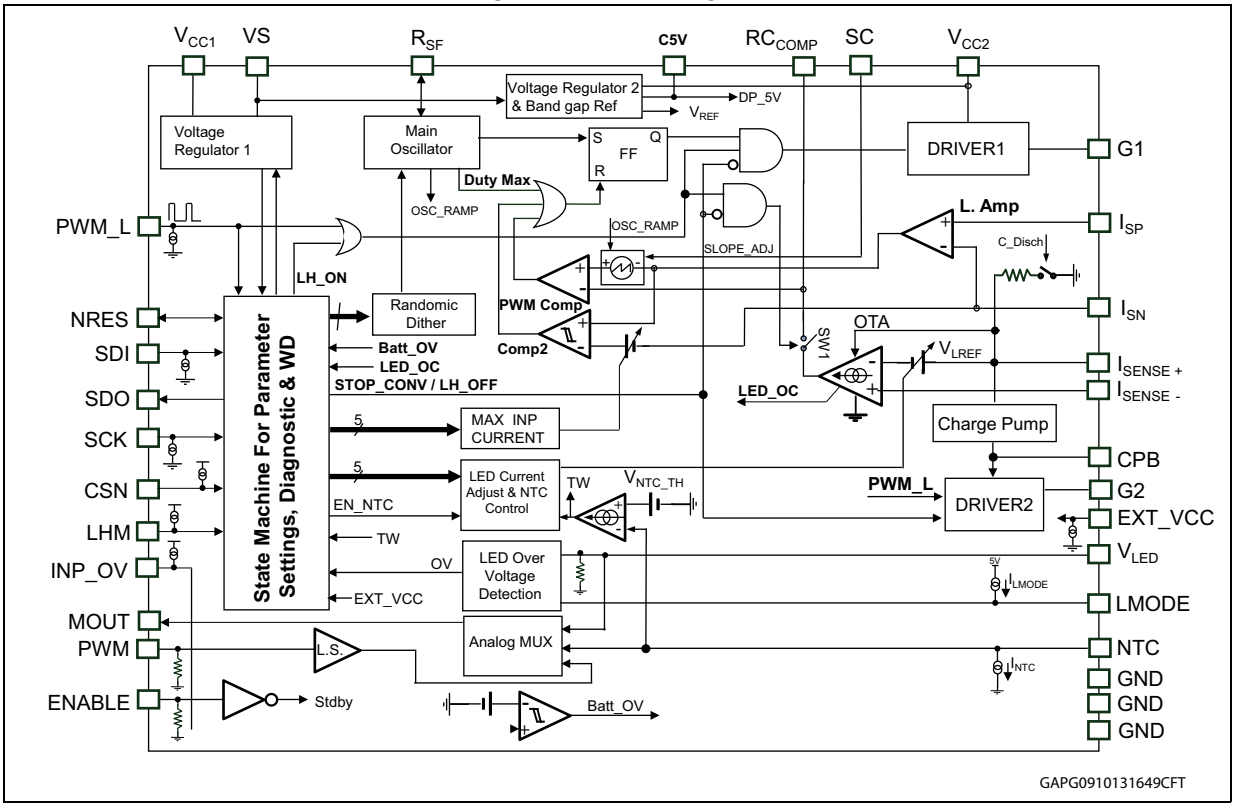


Figure 2. Connection diagram (top view – not in scale)

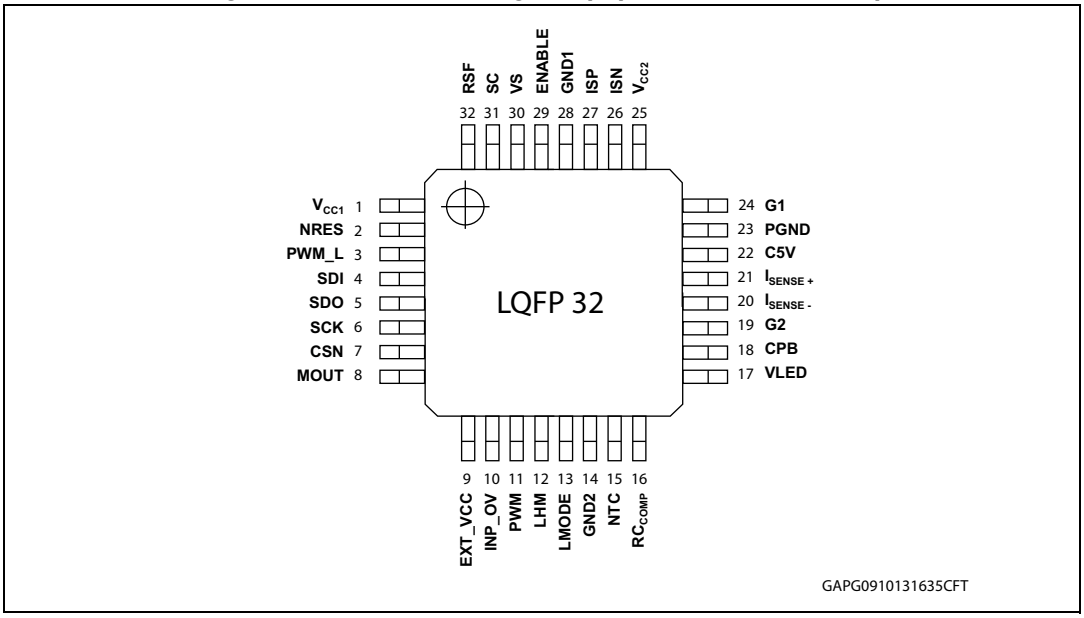


Table 1. Pin description

Pin number	Pin name	Function
1	V_{CC1}	5 V internal voltage regulator 1 output (external capacitor req.)
2	NRES	Reset I/O pin; active low
3	PWM_L	Logic low frequency PWM input
4	SDI	Serial SPI data input
5	SDO	Serial SPI data output
6	SCK	SPI clock
7	CSN	Chip select not
8	MOUT	Multiplexed data output pin
9	EXT_VCC	Internal/external up supply voltage programming pin(1)
10	INP_OV	Battery overvoltage programming pin
11	PWM	Low frequency PWM input (battery compatible)
12	LHM	Limp home mode input pin
13	LMODE	Switch input pin (connect to GND if LED drop voltage is referred to GND or open (5 V) if LED drop is referred to V_S)
14	GND2	GND of controller
15	NTC	Output for external N.T.C. resistor
16	RC_{COMP}	External R C compensation network
17	VLED	Input for LED chain overvoltage detection
18	CPB	Charge pump buffer capacitor
19	G2	Gate 2 output for external PMOS M2
20	I_{SENSE-}	Negative terminal of the LED sense resistor
21	I_{SENSE+}	Positive terminal of the LED sense resistor
22	C5V	Output for 5 V buffer capacitor
23	PGND	Power ground
24	G1	Gate 1 output for external PMOS M1
25	V_{CC2}	10 V voltage regulator 2 output (ext. capacitor required)
26	ISN	Negative terminal of the shunt resistor
27	ISP	Positive terminal of the shunt resistor
28	GND1	GND of controller
29	ENABLE	Enable pin
30	VS	Supply voltage input pin
31	SC	Slope compensation setting resistor
32	RSF	Oscillator frequency setting resistor

1. In case of externally supplied microcontroller, attach this pin to its external supply voltage pin.

2 Functional description

2.1 Operating modes

The device is able to work both with a microcontroller and without it (stand alone configuration).

2.1.1 Operation with an external microcontroller

This way allows parameters to be adjusted and checked by means of the SPI interface.

The adjusted device parameters, stored, i.e., inside the micro EEPROM, can be loaded into device internal registers after the start up phase.

By means of a small 8 pins microcontroller it is possible to implement the following functions:

- Parameters setting:
  - LED current level and maximum input current limit can be adjusted according to the application, the LED characteristic and spreads
  - Dither oscillator parameters as random, frequency modulation and deviation percentage can be programmed
- Flexible PWM operation with duty cycle and frequency managed by the microcontroller
- Diagnostic feedback:
  - Fault condition is sent to the micro when the CSN pin is pulled down
- Advanced LED monitoring:
  - LED voltage drop and temperature are multiplexed and sent to the microcontroller through the dedicated MOUT pin in order to monitor the selected parameter with the A/D of the microcontroller. The multiplexer is driven through a SPI command. This function allows a sophisticated control of the LED status. For example, as an alternative to the default overvoltage detection, it is possible to monitor the LED drop voltage, reduced by the external R5/R6 resistor divider. So taking into account the spread and temperature influence on the LED voltage drop, the microcontroller is able to detect if there is one or more LED shorted. Furthermore, it is possible to monitor the LED chain temperature, by means of the voltage feedback through the dedicated NTC pin. The temperature limit control, operated by the device by default, can be disabled via the SPI and the voltage applied on the NTC pin can be sent back to the microcontroller via the multiplexed output, MOUT, so allowing the microcontroller itself to control the LED chain either acting on the internal current LED register or reducing the low frequency PWM duty cycle.
- In case of V_{R1} over temperature, its output will be switched off, the device enters in limp home mode and a failsafe bit will be set in the internal status register (see details in the following paragraph). In order to restart the normal operation, so clearing the corresponding status register bit, the V_S or ENABLE voltage has to be switched off and then on. The mentioned bit can be cleared by the microcontroller only when it is external supplied.

2.1.2 Stand alone operation

The device operates with default parameters. The overall tolerance depends on the internal references precision and the external resistors tolerance. In details:

- LED current via external sensing resistor:

$$I_{LED} = 150\ mV/R_{SENSE}$$

- Maximum input current via an external shunt resistor.
- Oscillator dither effects are set to its default parameters; a low level on the SDI allows disabling the function.
- Low frequency dimming operation is allowed either by PWM pin or by logic level PWM_L input pin. Connecting the PWM control pin to the supply voltage via a resistor divider, allows the converter to be synchronized to the low frequency PWM generated, i.e., from the smart junction box.
- Connecting the MOUT pin, which by default provides a logic level image of the control input, to the PWM_L input, it is possible to drive the LED according to the PWM frequency and duty cycle of control. (See application circuit of *Figure 38*).
- In case of V_{R1} over temperature, its output will be permanently switched off. The device still continues to work in normal mode but with V_{R1} = OFF.

The L99LD01 can operate in 4 different modes:

- Start-up fail
- Normal mode
- Software limp home
- Limp home

After the power on reset, the device stays in start-up phase until V_{CC1} reaches a specified threshold, V_{CC1_TH}. Then the device enters in normal mode either with microcontroller or standalone, depending on the voltage level on the N_{reset} pin.

Note: The information about the operation with microcontroller or standalone is latched until a new power on reset.

If V_{CC1} does not reach both V_{CC1} fail and V_{CC1_TH} thresholds within a given delay or if a V_{CC1} over temperature event occurs, the device enters in a corresponding state.

2.1.3 Start-up fail

The device enters this mode in case a V_{CC1} under voltage event occurs during start-up phase and $V_S < V_{SMIN}$, provided that a microcontroller is detected. In this case V_{CC1} is turned off.

If V_S remains below V_{SMIN}, then the converter is switched off.

If V_S rises above V_{SMIN}, the converter behaves according to the PWM_L pin.

2.1.4 Normal mode

- Normal mode with microcontroller: the device enters this mode after a successful start up ($V_{CC1} > V_{CC1_TH}$) and a microcontroller is detected. The device keeps this mode as long as the watchdog is retriggered before a timeout event.
- Normal mode in standalone configuration: the device enters this mode if a standalone configuration is detected, independently from V_{CC1} errors. The L99LD01 keeps this mode even in case of watchdog timeouts.

In both cases, the converter behaves according to the PWM_L pin.

2.1.5 Software limp home

This device enters software limp home mode in case the Lh_Sw bit is set (see *Section : Control registers 3*).

The control registers are set to their default values, with the exception of the Lh_Sw bit, which remains unchanged.

The converter behaves according to the signal on the LHM pin:

– Turned on if a high signal is detected at the LHM pin
– Turned off if a low signal is detected at the LHM pin

2.1.6 Limp home mode

The device enters limp home mode, if a microcontroller is detected, in the following cases:

– Watchdog timeout in normal mode
– V_{CC1} under voltage ($V_{CC1} < V_{CC1_TH}$) for more than 2 ms in normal mode
– V_{CC1} is below the V_{CC1_FAIL} threshold for more than 4 ms during start-up
– V_{CC1} is below Vcc1uv for more than 100 ms during start-up and V_S is above V_{SMIN} threshold
– Thermal shutdown of V_{CC1}
– SDI stuck at 0 or 1

In Limp Home mode, all the control registers are set to their default values, except Lh_Sw (see *Section : Control registers 3*), which remains unchanged.

The converter behaves according to the voltage level on the LHM pin:

- Turned on if a High signal is detected at the LHM pin
- Turned off if a Low signal is detected at the LHM pin

Depending on the root cause, the action taken to quit the limp home mode (provided that the limp home condition has disappeared) is different. Some of the recovery paths require the microcontroller to be supplied by external supply.

A power on reset is always possible.

Figure 3. Operating modes, main states

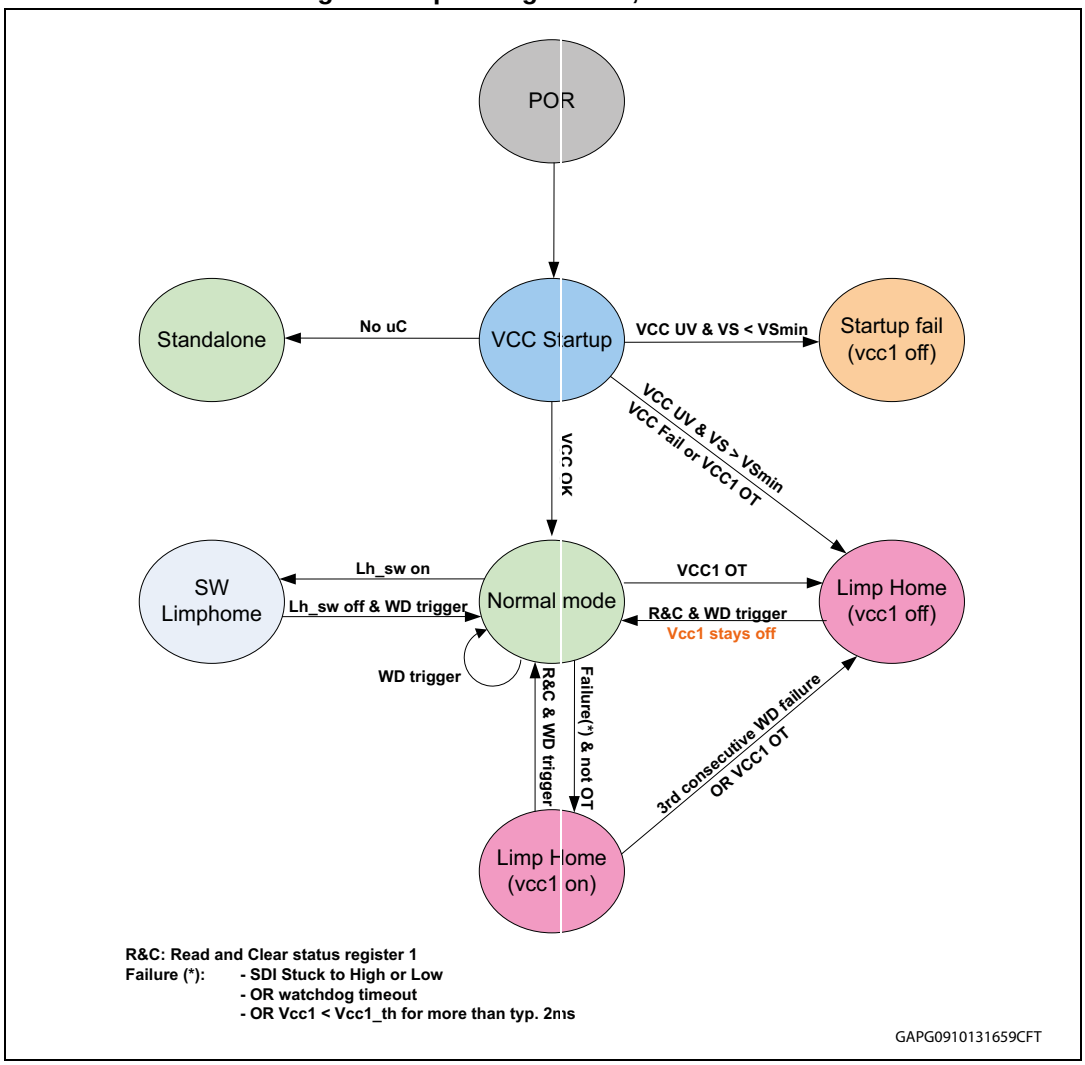


Table 2. Limp home mode: recovery paths

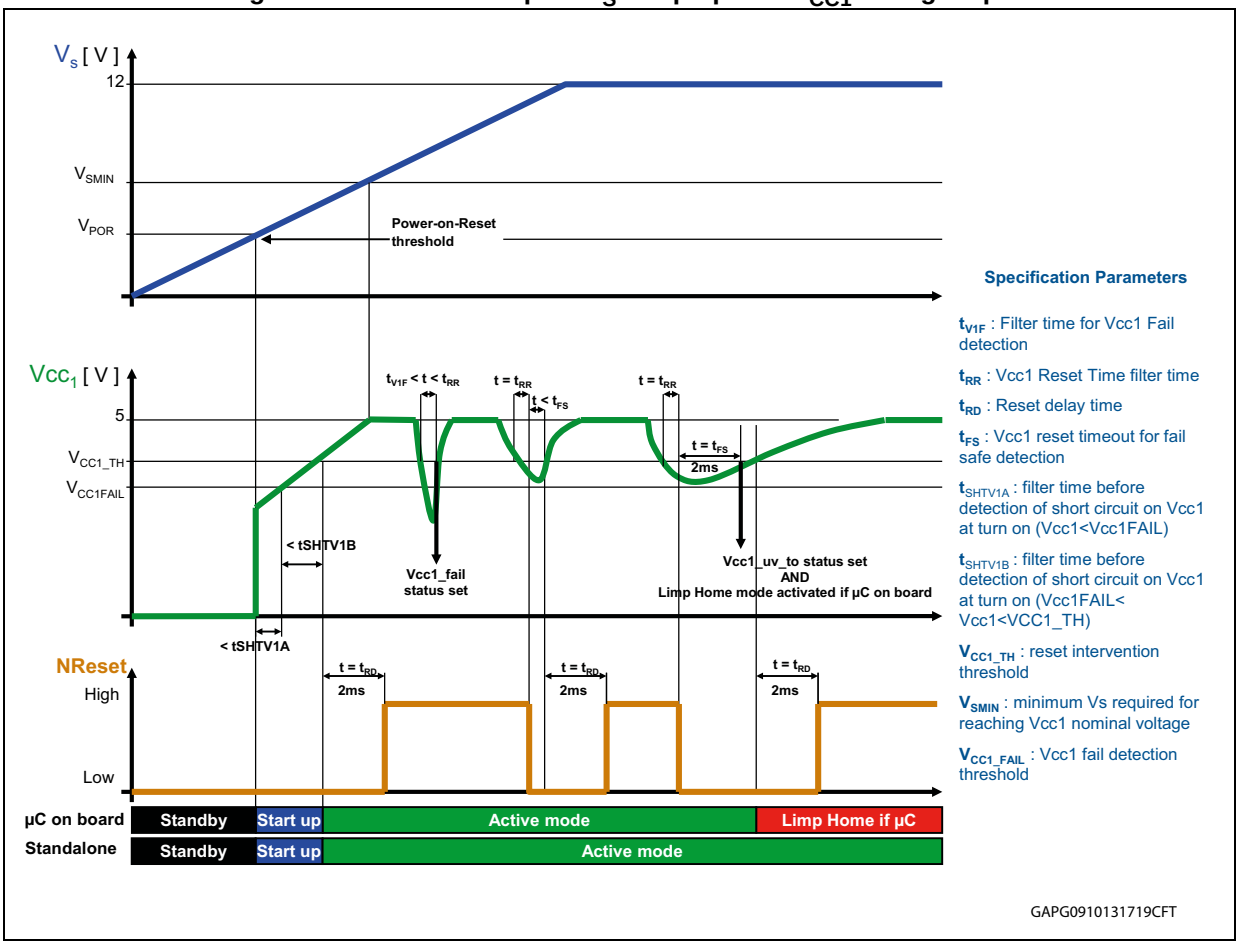
Transition	Root cause	Action to get back to normal mode	Response in the next SPI command
Normal mode → Limp Home V_{CC1} on	WD timeout (1^{st} or 2^{nd} WD timeout)	Read and clear status1 AND WD trigger	Fail Safe bit = 0 WD_Fail bit = 0
	$V_{CC1} < V_{CC1_TH}$ for more than 2 ms		Fail Safe bit = 0 Vcc1_Uv_To bit = 0
	SDI stuck at 0 or 1		Fail Safe bit = 0 SDI_Stuck@ = 0

Table 2. Limp home mode: recovery paths (continued)

Transition	Root cause	Action to get back to normal mode	Response in the next SPI command
Limp home V_{CC1} on → limp home V_{CC1} off	3 consecutive WD timeouts (microcontroller is supplied by V_{CC1})	Power on reset OR toggling of EN pin	Fail Safe bit = 0 WD_Fail bit = 0 Reset bit = 1
	3 consecutive WD timeouts (microcontroller is supplied by another V_{REG})	Read and clear Status1 AND WD trigger	Fail Safe bit = 0 WD_Fail bit = 0
Start up →limp home V_{CC1} off	$V_{CC1} < V_{CC1_FAIL}$ during start up for more than 4 ms	Power on reset	Failsafe bit = 0 Vcc1_Sc bit = 0 Reset bit = 1
	$V_{CC1} < V_{CC1_FAIL}$ during start up for more than 4 ms (microcontroller supplied by another V_{REG})	Read and clear Status1 AND WD trigger OR Toggling of EN pin	Failsafe bit = 0 Vcc1_Sc bit = 0 Vcc1_Fail = 0
	$V_{CC1} < V_{CC1_TH}$ for more than 100 ms during start up AND $V_S > V_{SMIN}$	Power on reset OR toggling of EN pin	Fail Safe bit = 0 Vcc1_Sc bit = 0 Reset bit = 1
	$V_{CC1} < V_{CC1_TH}$ for more than 100 ms during start up AND $V_S > V_{SMIN}$ (microcontroller supplied by another V_{REG})	Read and clear Status1 AND WD trigger	Fail Safe bit = 0 Vcc1_Sc bit = 0
Any state except normal mode standalone→ limp home V_{CC1} off	V_{CC1} over temperature	Read and clear Status1 AND WD trigger	Fail Safe bit = 0 Vcc1_Ot bit = 0
Normal mode → SW limp home	Software limp home is activated	Reset Lh_Sw bit AND WD trigger	Fail Safe bit = 0 Lh_Sw_St = 0

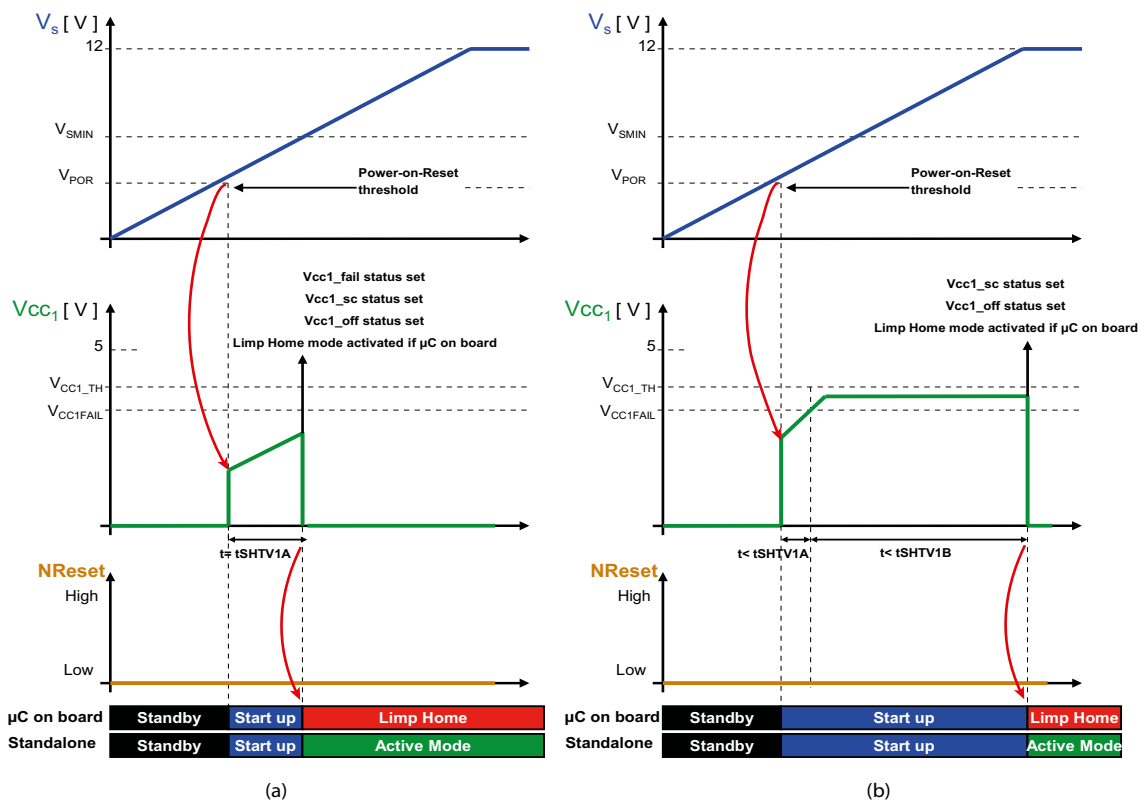
The following *Figure 4*, *Figure 5* (a), (b) and *Figure 6* (a) show the behavior of the device and NRES during start-up in case of normal V_S ramp up or in case of V_{CC1} failures (V_{CC1} fail or reset under voltage), both with microcontroller and standalone. *Figure 6* (b) and *Figure 7* show the behavior at V_S ramp down fast and slow respectively.

Figure 4. Normal start up vs V_S ramp up and V_{CC1} voltage dips



Note: Normal start up with or without microcontroller.

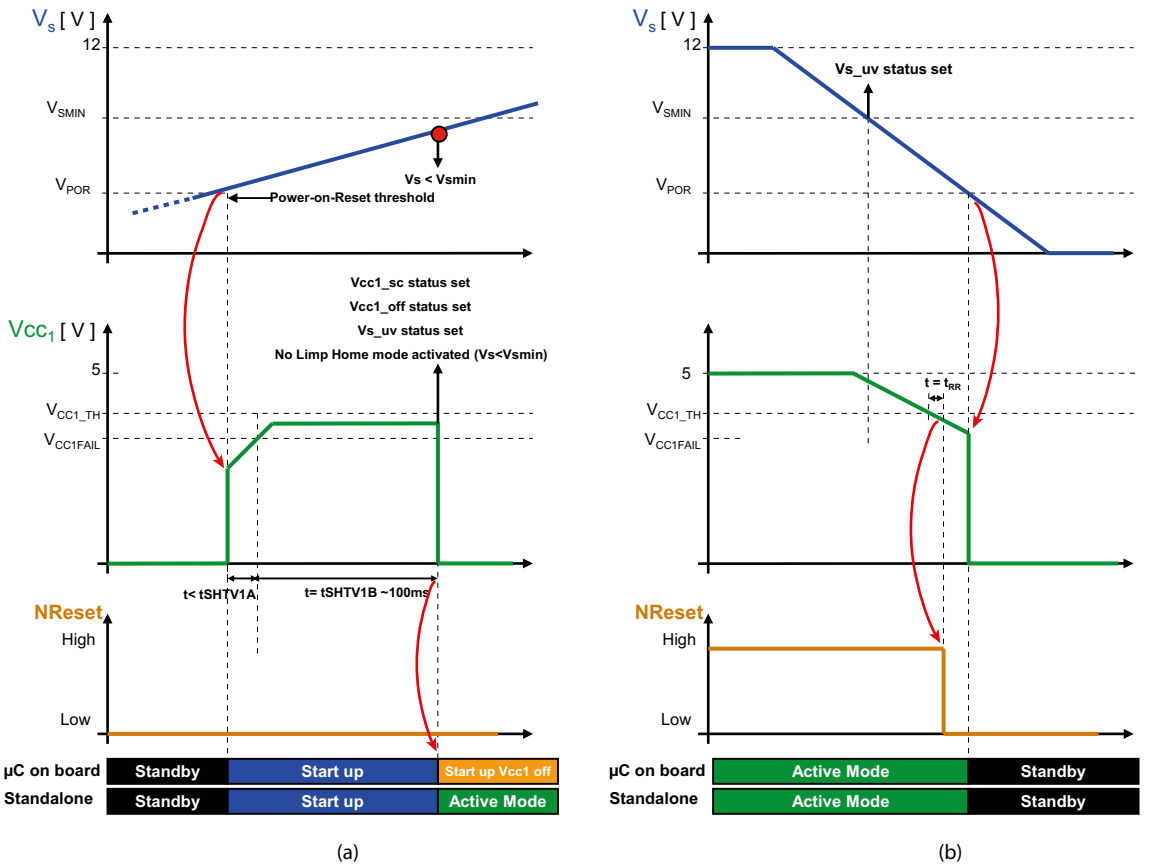
Figure 5. V_{CC1_FAIL} or V_{CC1} reset under voltage ($V_S > V_{SMIN}$) at start up



(a) start up V_{CC1} fail; (b) V_{CC1} under reset threshold during start up, $V_S > V_{SMIN}$

GAPG1410130949CFT

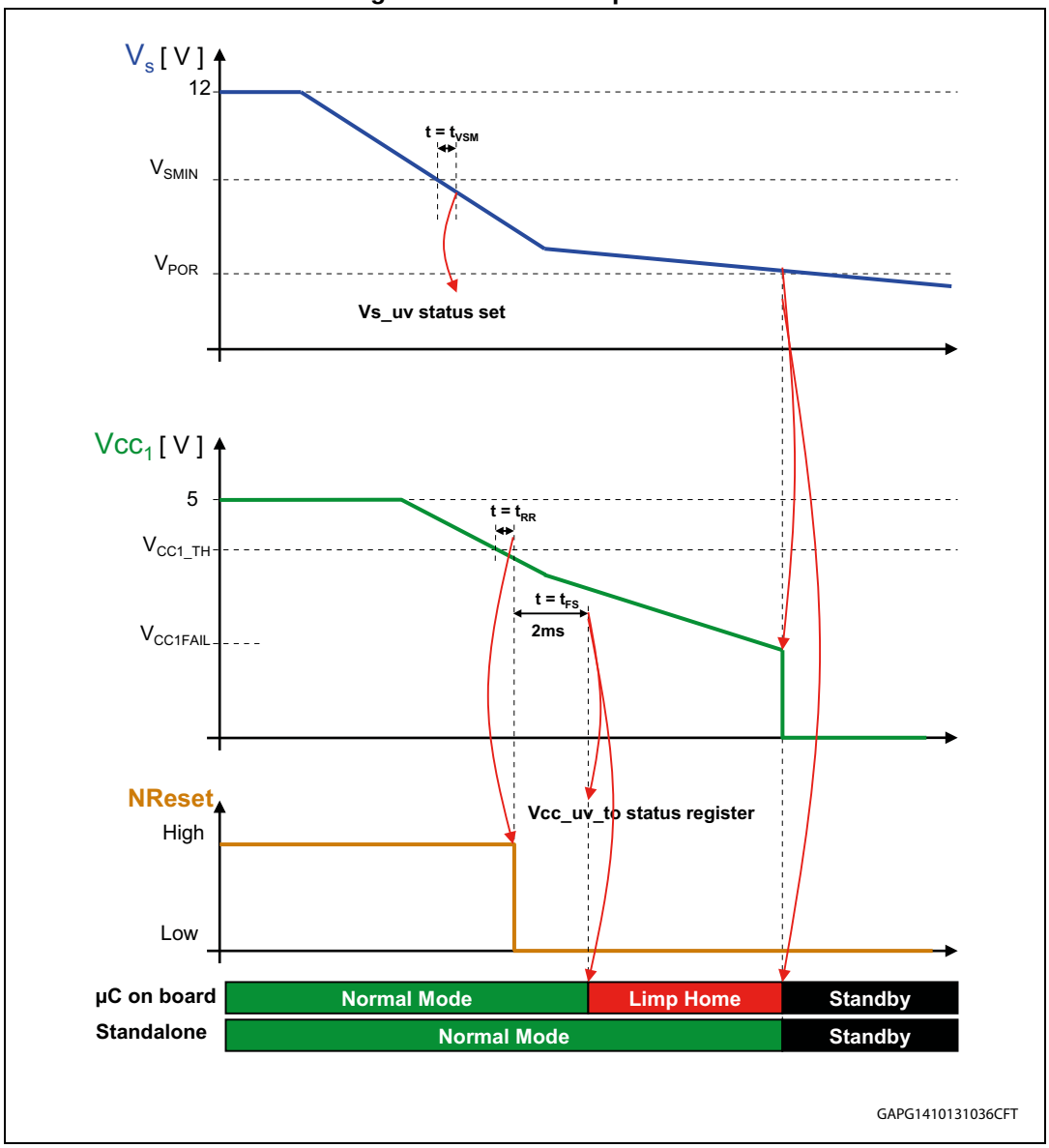
Figure 6. V_{CC1} reset under voltage at start up ($V_S < V_{SMIN}$) and fast V_S ramp down



(a) V_{CC1_UV} during start up; (b) $V_S < V_{SMIN}$ Fast V_S ramp down

GAPG1410130959CFT

Figure 7. Slow vs ramp down



2.2 Protections and functions

2.2.1 LED current adjust and temperature control

The LED current can be adjusted within a range of ± 66.7 %, with respect to the default value set by the LED current sense resistor, via the SPI input, so allowing the end of line calibration. The LED chain temperature measurement is achieved by means of an external NTC resistor connected between the NTC pin and GND. The NTC resistor is supplied through a resistor connected to the 5 V internal regulator output. As soon as the voltage on the NTC resistor becomes lower than the internal threshold, V_{NTC_TH}, (due to an overtemperature in the LED chain) an internal circuitry is activated and the internal LED current reference voltage decreases proportionally, so that the LED current is progressively

reduced (maximum 50 % of the nominal LED current), not allowing the LED temperature to increase over the programmed limit.

Thermal limit intervention is reported by properly setting a bit inside the internal status register.

2.2.2 Slope compensation

Slope compensation is needed to ensure the stability of the control loop with all possible values of duty cycle

$$D = \frac{T_{ON}}{T}$$

$(0 < D < 1)$

especially for duty cycle greater than 0.5. The recommended slope S_{ADD} of the additional ramp is proportional to the inductor current slope during the turn off phase, that is:

$$S_{ADD} = \alpha \cdot S_L$$

where S_{ADD} is the additional slope introduced by the circuit,

$$S_L = \left.\frac{dI_L}{dt}\right|_{OFF}$$

is the off-time inductor slope and

$$0.5 < \alpha < 1$$

S_L is also given by the formula:

$$S_L = \frac{G_{LA} \cdot R_{SHUNT} \cdot (V_{OUT} - V_{IN})}{L}$$

Being G_{LA} the gain of the linear amplifier (see *Chapter 5: Electrical characteristics* for G_{LA} parameter values) and R_{SHUNT} is the resistor across pin I_{SP} and I_{SN} (see *Chapter 7: Application circuits*).

The simplified internal circuit structure for the slope compensation is shown in *Figure 8*.

The additional slope is obtained from the internal oscillator ramp voltage. A fraction of the oscillator voltage ramp is added to the output voltage of the sensing amplifier, which is proportional to the sense resistor voltage drop, and therefore, to the current flowing through power mosfet M1.

The added ramp voltage is

$$V_{ADD} = I \cdot R_{SLOPE}$$

where

$$I = 2 \cdot \frac{V_{OSC}}{R_T}$$

and R_{SLOPE} and R_T are defined in the *Figure 8*, together with their typical values.

Therefore, will result:

$$V_{ADD} = 2 \cdot V_{OSC} \cdot \frac{R_{SLOPE}}{R_T}$$

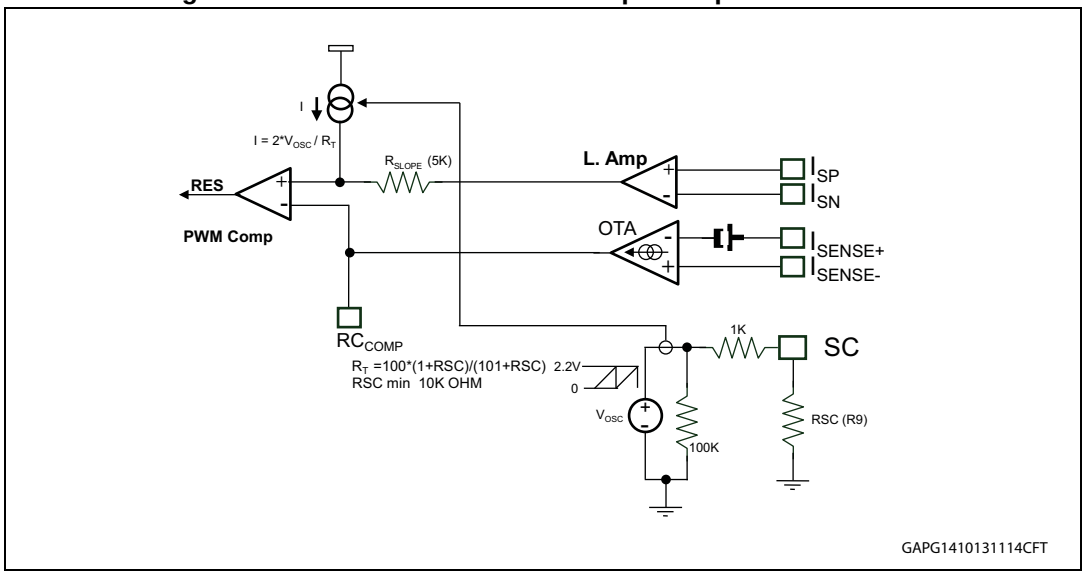
and consequently:

$$S_{ADD} = \frac{V_{ADD}}{T} = \frac{2 \cdot V_{OSC} \cdot R_{SLOPE}}{R_T \cdot T}$$

where T is the period of the converter oscillator.

The additional compensating current slope can be simply adjusted by properly setting the value of the external resistor R9 (and consequently R_T).

Figure 8. Internal structure of the slope compensation circuit



2.2.3 LED chain overvoltage detection

Via the external resistor divider (R5, R6) it is possible to detect LED overvoltage events, by programming a threshold for the maximum drop voltage of the LED chain for a specific LED board (see *Section 2.2.12* for details). In case Boost or Fly back topology is used, the L_{MODE} pin must be connected to GND. In this case the voltage at pin V_{LED} will be referred to ground. Instead, if Buck Boost topology is used, the L_{MODE} pin must be connected to 5 V or left open. An internal pull up current source keep this pin high, and in this case, the voltage applied by the resistor divider R5/R6 at pin V_{LED} will be referred to the battery voltage applied at pin V_S. If a valid overvoltage event occurs, which is detected if the LED drop voltage reaches a value $V_{LED} \geq OV_TH1$, the device is switched off immediately forcing the

pins G1 and G2 to zero voltage and the event is registered in the status register of the SPI interface and read by the micro.

In case of LED overvoltage, immediately after stopping the device, an internal resistor is applied between pin I_{SENSE+} and GND trough the switch “C_disch” (see *Figure 1*), in order to discharge capacitors C1 and C4, avoiding LED flashing when the converter restarts. Any LED_OV event will be written in the GSB (Global Status Byte) bit 7 and also in the SR1 (Status Register 1) bit 18.

2.2.4 Battery overvoltage shutdown

In case supply voltage applied to the V_S pin rises above a maximum voltage threshold, sensed by a resistor divider attached at pin INP_OV, the converter is switched off immediately, forcing outputs pin G1 and G2, to zero voltage. This prevents a LED over current in case of load-dump.

If, following the input overvoltage event, the battery voltage decreases under a second threshold, lower than the former, the converter starts again.

2.2.5 Regulators thermal shut down

Both voltage regulators inside the chip are provided with over temperature detection circuits.

If V_{R1} reaches its maximum temperature, V_{R1} will be switched off. After that, the behavior of the device depends on the application (see *Section 2.2.1: LED current adjust and temperature control*).

If instead, is V_{R2} to reach its maximum temperature (typ 175 °C), then the device will be completely switched off (V_{CC1} and V_{CC2} = 0).

Only the internal temperature monitoring of V_{CC2} remains alive and when the temperature falls down under a second lower temperature threshold (150 °C typ.), the device tries to restart again.

2.2.6 Reset

The NRES pin (active low), generates a reset signal for the microcontroller.

An external pull up resistor (typ. 100 k) maintain normally high the voltage at pin NRES (see *Figure 32*).

Following a power up condition, the NRES pin is forced low while the voltage provided by regulator 1 (V_{CC1}) is below an internal fixed threshold V_{CC1_TH} of typ 4.5 V. After V_{CC1} has reached the above mentioned internal threshold, NRES voltage is kept low for a fixed default time of 2 ms; after that, the NRES pin will be released reaching the normal high state. However, this time can be externally extended by an additional capacitance connected between NRES and GND (see C6 in the application circuits), which is charged by the external pull-up. Depending on the reset-input-threshold of the µP (U_{TR}), the required capacitance for a typical T_{RD} can be calculated as follows:

$$C6 = -T_{RD} / (R_{PU} \cdot \lg(1 - U_{TR} / V_{CC1}))$$

R_{PU} is the pull up resistor (value in ohm)

In case V_{CC1} voltage drops below the internal threshold during the normal functioning, or when the device is put in standby, the NRES pin is forced to low, but after a time interval T_{RR} has expired and kept low until the V_{CC1} has gone back again to the internal threshold (see *Figure 4* for more details).

2.2.7 Watchdog

In case the application uses a microcontroller, during the device power-up a reset pulse is generated periodically every 200 ms (default) for 2.0 ms waiting for microcontroller acknowledgment. Timeout window is selectable by SPI (100 ms or 200 ms) and the reset time could be extended by the external capacitor C6.

- Timeout WD is refreshed by bit toggling.
- After the 1st WD timeout, a reset pulse is generated and the device enters in Limp Home mode. After the second WD timeout, another reset pulse cycle is generated, waiting for microcontroller response.
- After 3 consecutive reset cycles without WD refresh, which means that microcontroller is not responding, the voltage regulator, V_{CC1}, is turned off and the device keeps working in “Limp Home Mode” (see *Figure 33*). Safety critical functions like Low Beam application require the LED Driver to be turned on if the microcontroller fails, while in case of high beam application, it is required the driver to be switched off in case of microcontroller failure. As a consequence, the device operates according to the state of LHM pin which is enabled during the recognition of the microcontroller failure. In particular, if LHM pin is kept low the device will be always OFF. If instead, LHM pin is high or left open, the device will be switched permanently ON, regardless of the status of PWM_L pin.If the application doesn’t use a microcontroller (stand alone operation), the start-up WD control must to be deactivated. This can be done by connecting NRES pin to the battery supply voltage V_S. In such a case the driver will operate in normal mode as above mentioned (see stand alone operation).

2.2.8 Standby and wake up by ENABLE pin

A low consumption mode is required in case of applications directly connected to the battery.

The device enters in standby mode, that is the default operating modes because of an internal pull down, in case of low level signal at the ENABLE pin and it wakes up in case of high level signal.During standby mode, V_{CC1} and V_{CC2} are switched off. *Figure 9* and *Figure 10* show two possible application schematics in case of direct connection to the battery.

In case of *Figure 9* the microcontroller of the application goes in standby when the microcontroller sets the LIN transceiver in standby mode: NSLP = Low→INH goes Low→the DRL driver goes in standby.

The application is waken up from the standby when a wake up source is detected by the LIN transceiver. That means INH goes high and so ENABLE, then the DRL driver restarts and consequently V_{CC1} is activated and supplies the microcontroller.

In case of *Figure 10*, a power management device is present, which supplies the microcontroller. Normally the inverted FSO signal coming from the power management device is high. This output is inverted by an external logic and applied to one of the two input OR diodes and therefore, at the input of the OR the voltage is normally at logical zero.

So in this case the LED driver goes:

- In stand-by mode with a low level on ENABLE pin operated by the microcontroller
- In normal mode with a high level on ENABLE pin operated by the microcontroller

The inverted FSO signal, coming from the power management device ensures, putting trough the inverter and the external OR diode ENABLE pin high, that the LED driver correctly restarts even if the microcontroller fails.

Figure 9. Operation with a standalone LIN and ENABLE

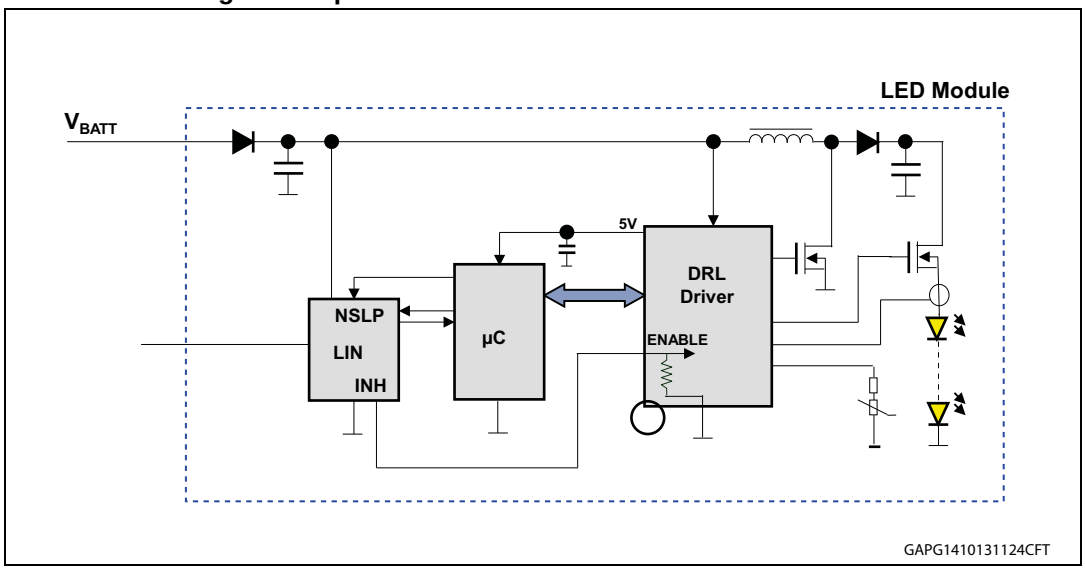
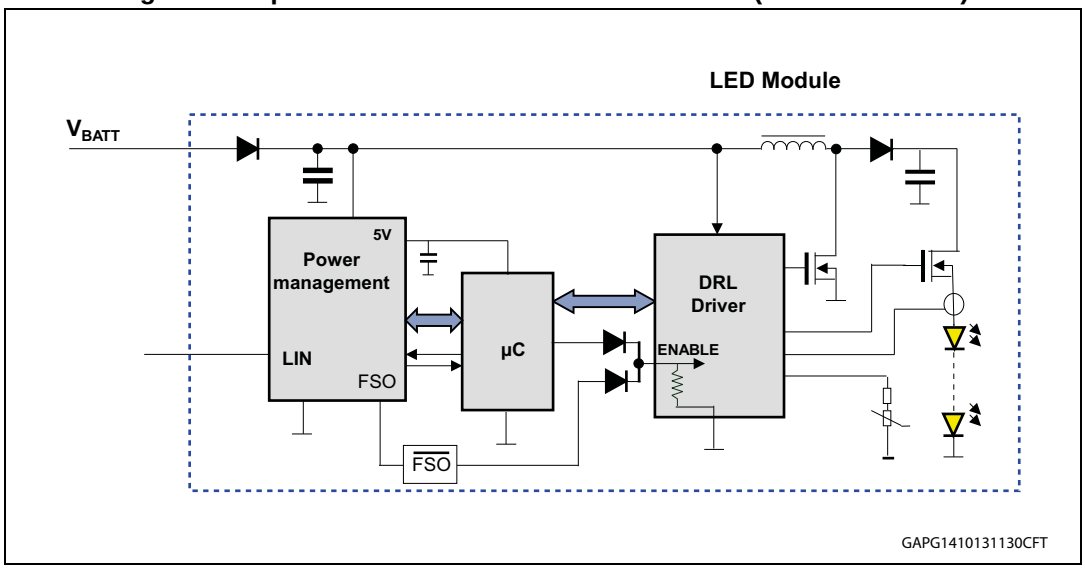


Figure 10. Operation with PM device and ENABLE (FSO active Low)



1. An inverter network is required.

2.2.9 Frequency setting and dither effect

The internal main converter oscillator structure is reported in *Figure 11*.

The external resistor applied between pin R_{SF} and ground is setting the converter working frequency. The voltage applied on pin R_{SF} is the internal reference reported by the source follower structure which is a constant voltage of 1.21 V. The converter frequency is directly related to the current flowing through the R_{SF} pin. *Figure 12* reports the behavior of frequency converter as function of the external resistor R_{SF} and I_{RSF} as function of converter frequency. As above mentioned the converter oscillator spread parameters (dither effect) are adjustable via SPI.

Dither effect is disabled by default during standalone operation, but it is possible enabling it simply connecting the SDI pin to 5 V voltage.

Figure 11. Internal structure of main converter oscillator

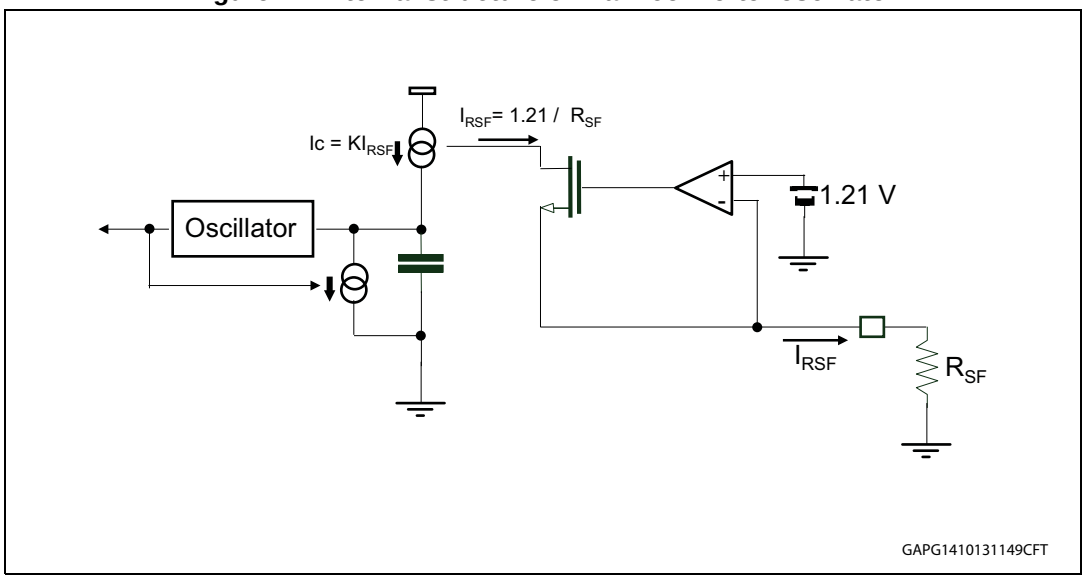
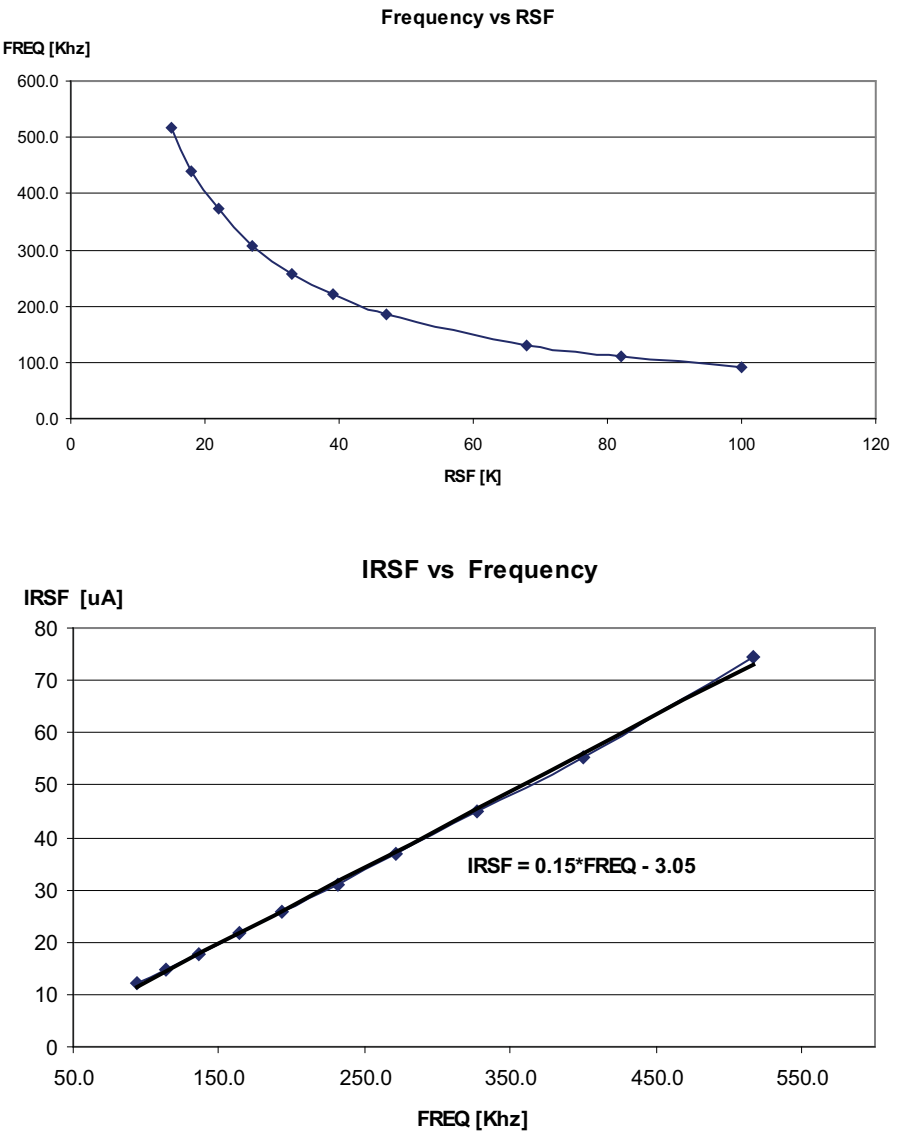


Figure 12. Converter frequency range vs R_{SF} and I_{RSF} vs frequency



2.2.10 Start up LED overvoltage management

The following diagram shows the purpose of delay time windows "t_{DStart}" and "$t_{EnRecov}$".

The first delay window t_{DStart} has been thought to ensure an initial time period for charging the external buffer capacitor of the charge pump C9. When V_S is below V_{SMIN}, the LED overvoltage recovery bit is set. During this time interval, triggered as soon as the battery voltage V_S overcomes V_{SMIN} threshold, the converter remain in a stop condition, independently from PWM_L. When the t_{DStart} is elapsed (typ. 5 ms), the converter is released and behaves according to the PWM_L signal provided, that no failure occurs.

If no LED overvoltage comes during the 2nd time interval $t_{EnRecov}$, LED ov recovery bit is reset.

If a LED overvoltage failure occurs afterwards, the failure will be latched and the converter is stopped until a read and clear of the status register 1.

Note that during t_{DStart}, the converter is stopped to enable the buffer capacitor C9 to charge at a sufficient voltage to correctly drive the mosfet M2. This delay prevents the converter to turn on, while M2 stays off, avoiding a LED overvoltage event.

If the application uses a big capacitor[(a)], it is recommended to keep the PWM_L signal low after a power on reset or after a V_S under voltage, until C9 is totally charged, to avoid a LED overvoltage. *Figure 13* shows the device behavior in case of no LED overvoltage failure, after t_{DStart}.

If C9, after t_{DStart} time, should be not enough charged to allow correct driving operation, a possible LED overvoltage will appear when, the converter will be released. *Figure 14* shows what happens in this case.

After t_{DStart}, the converter is released while the C9 capacitor is only partially charged. Consequently, V_{LED} increases up to LED OV_TH1 and a LED overvoltage event is detected during the $t_{EnRecov}$ phase. The LED_Ov_Rec bit is not reset at the end of the $t_{EnRecov}$ phase due to the LED overvoltage event. The discharge path is activated until V_{LED} crosses LED OV_TH2. Then, the LED_Ov_Rec bit is reset, the converter is released, and the buffer capacitor C9 is now fully charged, enabling the dimming mosfet M2 to turn on.

Figure 15 shows the case of LED_Ov_Rec bit during a start up with a rising edge on PWM_L = High after the expiration of t_{DStart}. In this case, the $t_{EnRecov}$ phase starts only when the PWM_L signal goes High. *Figure 16* shows the case of LED overvoltage event, which could appear during normal functioning.

The LED overvoltage status bit is set (latched) and the discharge path is activated until V_{LED} crosses LED OV_TH2. The converter is stopped, independently from PWM_L, until a read and clear command of the status register 1 (LED_Ov_Rec bit is reset).

If a LED overvoltage failure event occurs during V_S overvoltage, (battery OV), the discharge path for the output capacitor is inhibited and the LED overvoltage status bit is not set.

When the V_S overvoltage event disappears, (V_S crosses V_S OV_TH2), the LED overvoltage status bit is set (latched) and the discharge path is activated until V_{LED} crosses LED OV_TH2. The converter is stopped, independently from PWM_L, until the LED ov status bit is cleared (read and clear of the status register 1). *Figure 17* shows such a case.

Finally *Figure 18* shows how will be managed the LED_Ov_Rec bit in case signal PWM_L has a low on-time. In this case the LED_Ov_Rec bit is reset when the cumulated running time of $t_{EnRecov}$ exceeds typ. 5 ms. This feature enables a single recovery of a LED overvoltage event, due to a too fast regulation loop (set by the resistor and capacitor connected to RCCOMP pin), even in PWM operation with low on-time. However, a proper choice of RC network values, avoiding fast transients on the LED string voltage, when the converter is switched ON, it is carefully recommended

a. More than 22 nF

Figure 13. Correct start UP with no LED overvoltage failure

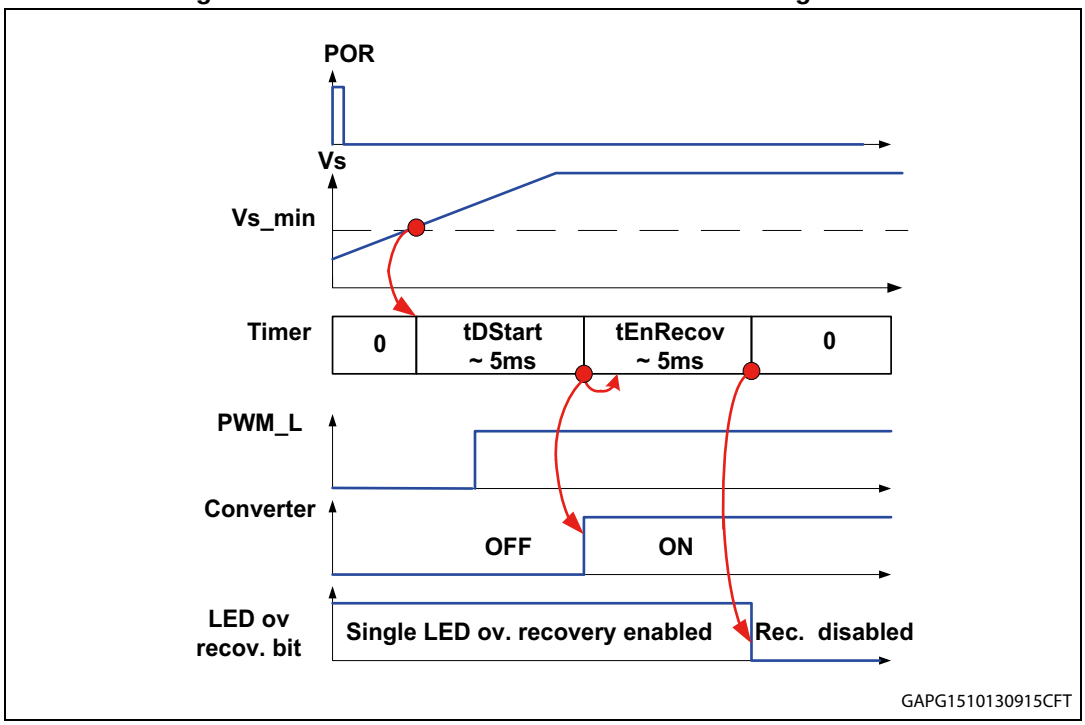


Figure 14. LED overvoltage after t_{DStart}

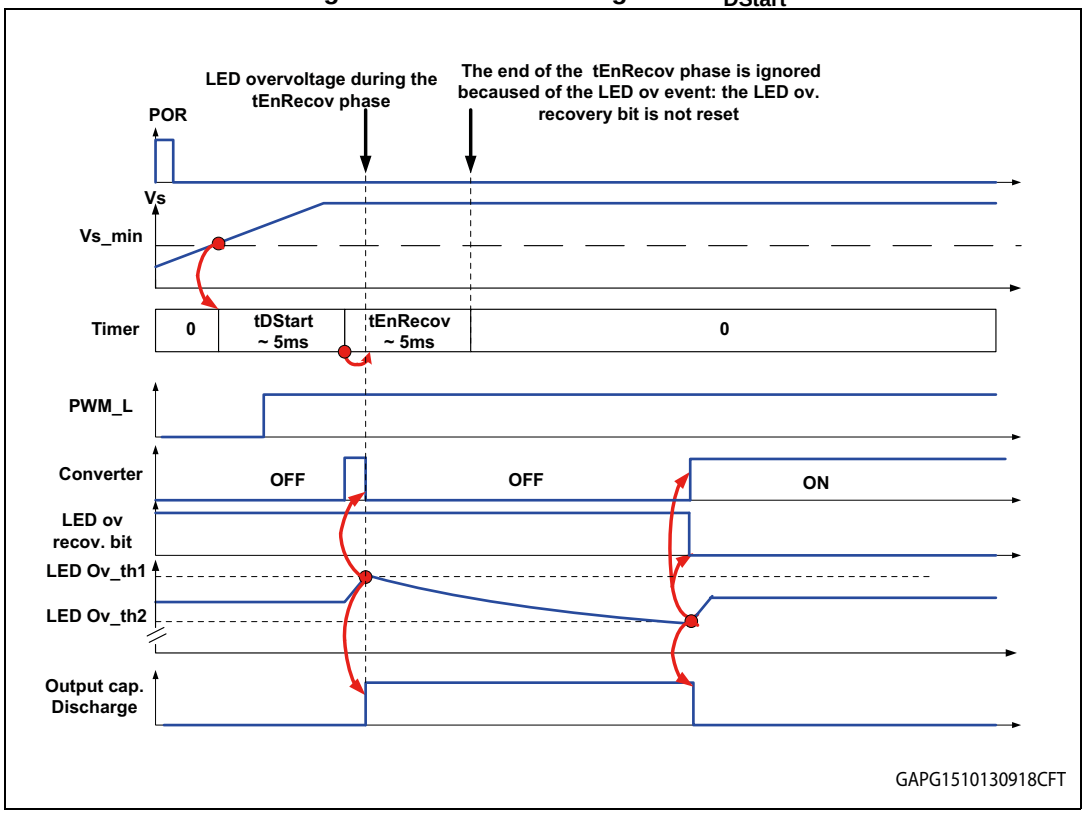


Figure 15. Device behavior in case the low to high transition of PWM_L signal happens after t_{DStart} expiration

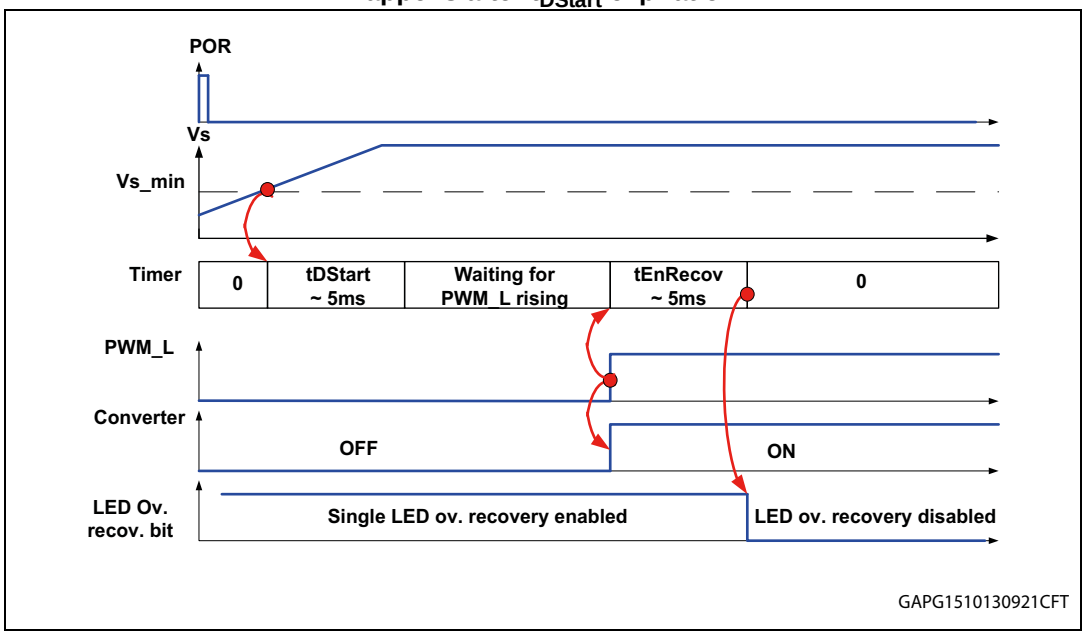


Figure 16. LED overvoltage event not caused by a VS overvoltage event

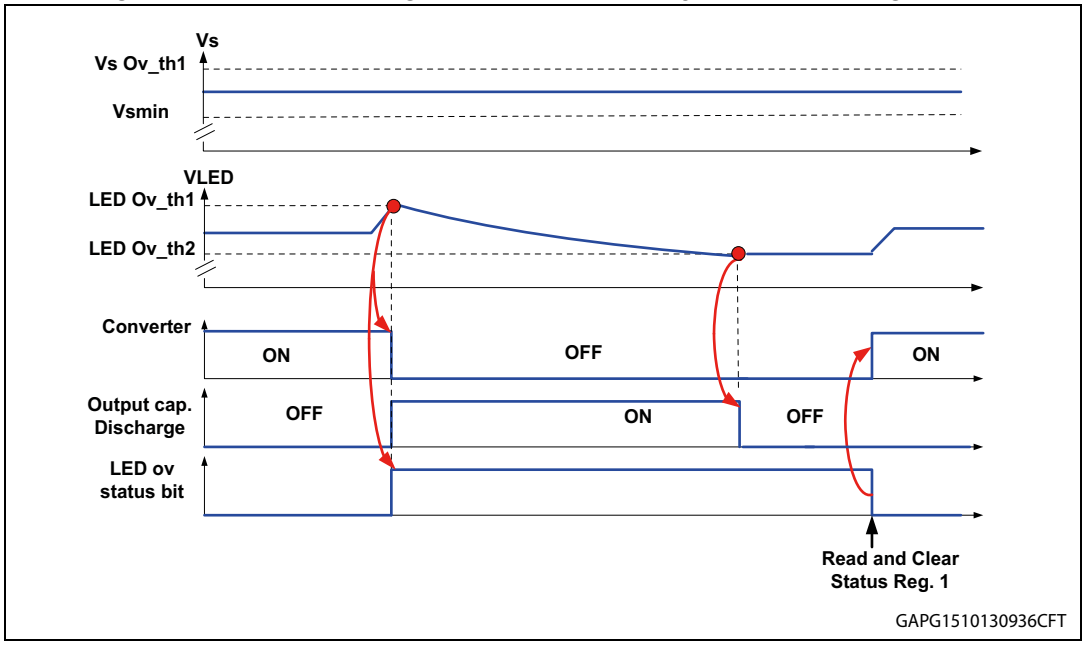


Figure 17. LED overvoltage detection due to a possible battery VS overvoltage

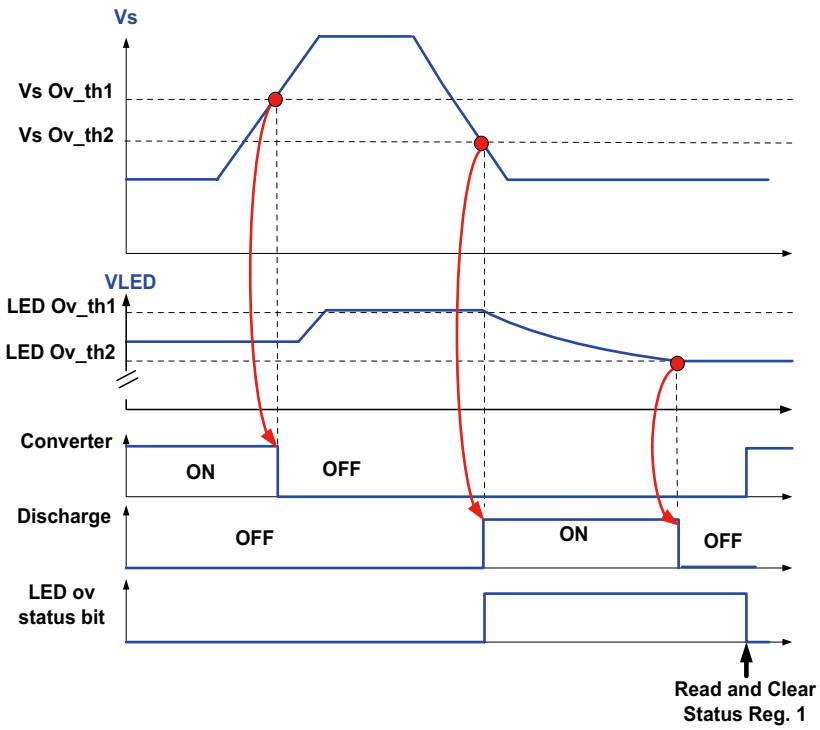
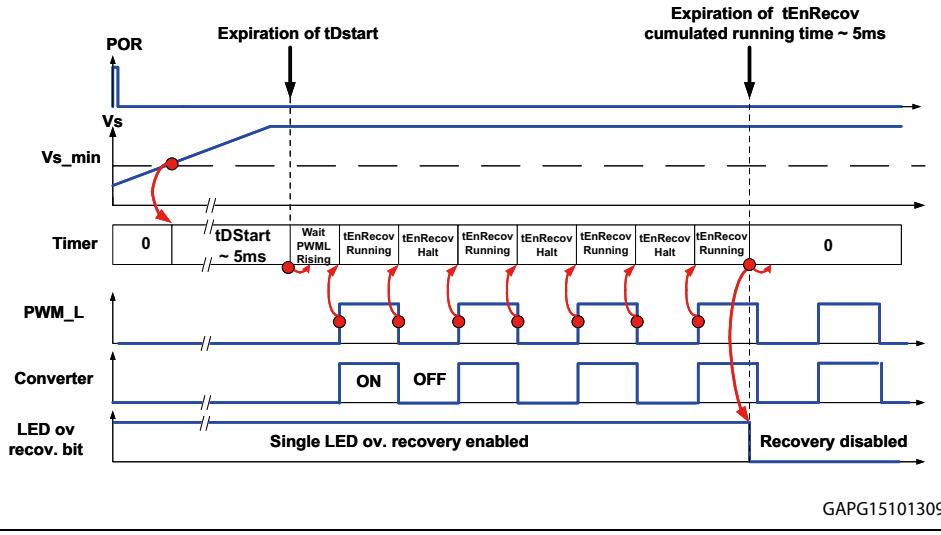


Figure 18. Behavior of LED overvoltage recovery bit with low on-time of PWM_L



2.2.11 Programming the over/under voltage threshold

The voltage across the LED string is continuously sensed by the external resistor divider R5/R6 and reported inside the chip trough the apposite pin $V_{LED.}$ Considering negligible the voltage drop due to the sense resistor and the V_{DS} of external mosfet M2 respect to the LED

voltage string, according to the equation reported below, the LED overvoltage thresholds are given by the following formulas:

V_{LED_OV} = OV_TH1 / K_L; being K_L = R6 / (R5+R6);

OV_TH1 is the reference for the OV internal comparator. Typical value for OV_TH1 is 3.5 V.

LED OV event makes the converter and also mosfet M2 immediately switched OFF, in order to prevent any damage to the LED string or to the driver. Furthermore, following an OV event, the LED_OV status register is set and an internal load is applied between I_{SENSE+} pin and ground in order to fast discharge the voltage across capacitor C4.

In the boost topology application, if a short circuit between the source of external mosfet M2 and GND occurs, an uncontrolled current could flow. In order to avoid this situation, a maximum LED current protection has been inserted, which continuously monitors the voltage across the sense resistor R_{SENSE}. If this voltage reaches a value in excess of an internal fixed threshold of (see *Table 24* - LED over current protection threshold parameter), the status bit LED_OC (led over current) is set and the converter and also mosfet M2 will be immediately switched OFF.

Following a stop of the converter due to an OV event, the device can not be restarted before of C4 discharge (V_{LED} is below OV_TH2).

After an OV event, the converter could restart if a read and clear command of the LED_OV status bit is done. *Table 3* summarizes the suggested value of K_L resistor ratio, supposing to have a LED_OV event, when the voltage across LED string, reaches a value in excess of 50 % of its nominal value.

Figure 19. LED chain overvoltage thresholds settings. An example for boost and fly back converters

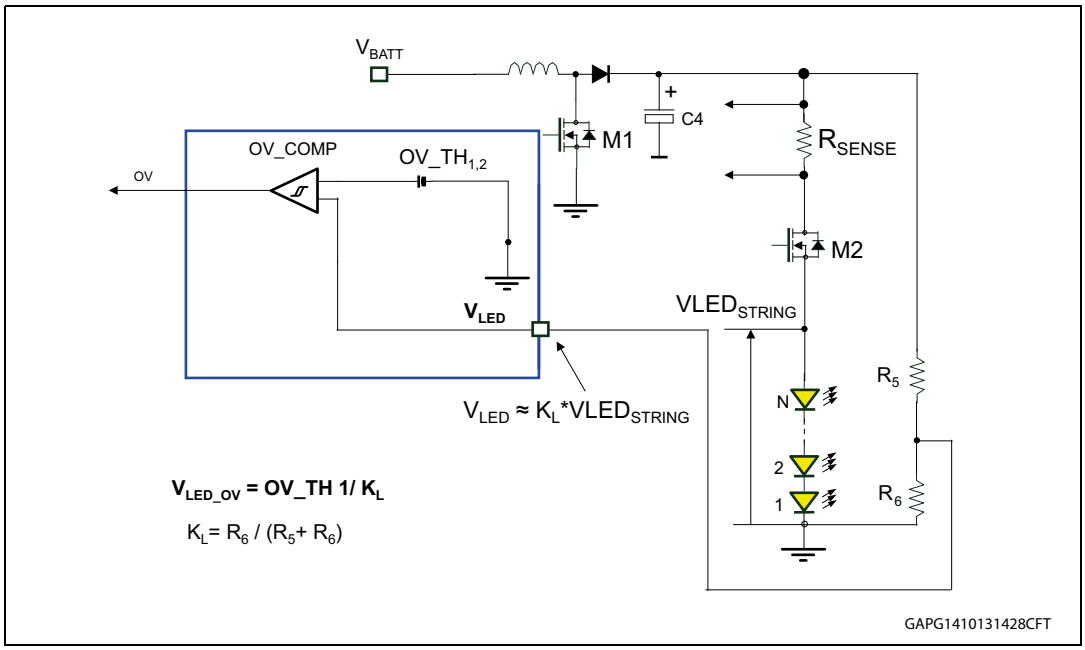


Table 3. Suggested K_L value and overvoltage thresholds

N Number of LED	K_L	LED CHAIN nominal DROP N*V_F [V]	overvoltage V_{LED_OV} [V]
1(1)	0.583	4	6
2(1)	0.292	8	12
3(1)	0.194	12	18
4(1)	0.146	16	24
5	0.117	20	30
6	0.097	24	36
7	0.083	28	42
8	0.073	32	48
9	0.065	36	54(2)
10	0.0583	40	60(2)

1. Not Applicable on boost converter topology, since the chain LED Drop must be always larger as the maximum battery voltage.
2. Theoretical value; effective value will be clamped to 52 V (typ) by the OV protection.

2.2.12 Input overvoltage programming

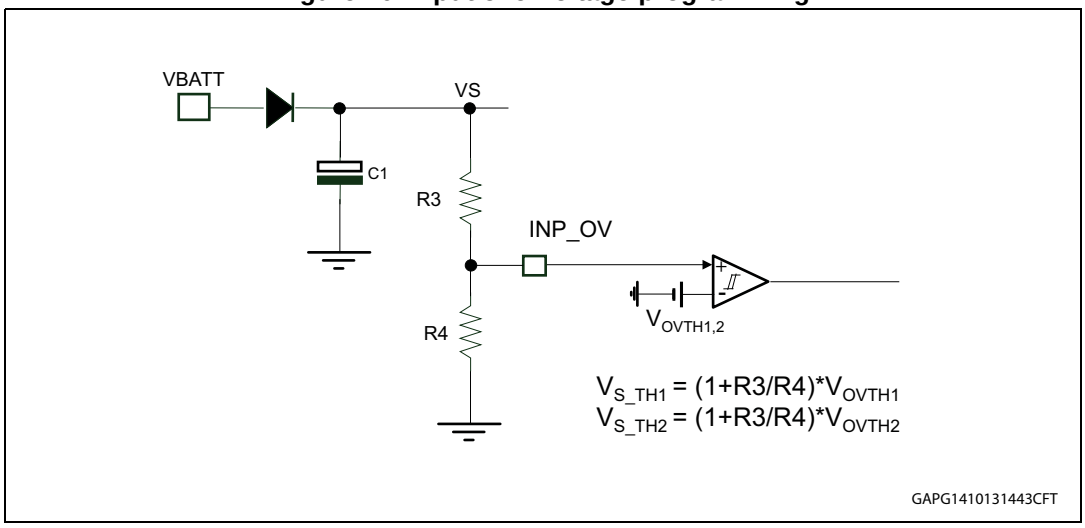
Supply overvoltage is programmed by the external partition ratio K_l = R3/R4

According to the *Figure 20* input overvoltage thresholds depend on the internal reference voltages V_{OVTH1} and V_{OVTH2} (being $V_{OVTH2} < V_{OVTH1}$)

Typical values of these internally generated references are 3.5 V and 3 V.

When the Battery voltage reaches a value in excess to V_{S_TH1} the converter is immediately stopped. When the battery voltage, going down, reaches a value just lower to V_{S_TH2}, the converter restarts again.

Figure 20. Input overvoltage programming



As an example, if we want V_{S_TH1} = 20 V, according to the formula of *Figure 20*, R3/R4 will result equal to 4.7 and consequently the deactivation threshold V_{S_TH2} will result ~ 17 V.[b]

b. Notice that the deactivation threshold must be always greater than the maximum allowed battery value in normal conditions.

3 SPI functional description

3.1 Serial peripheral interface (ST SPI standard)

The SPI communication is based on a standard ST-SPI 24-bit interface, using CSN, SDI, SDO and SCK signal lines.

Input data are shifted into SDI, MSB first while output data are shifted out on SDO, MSB first.

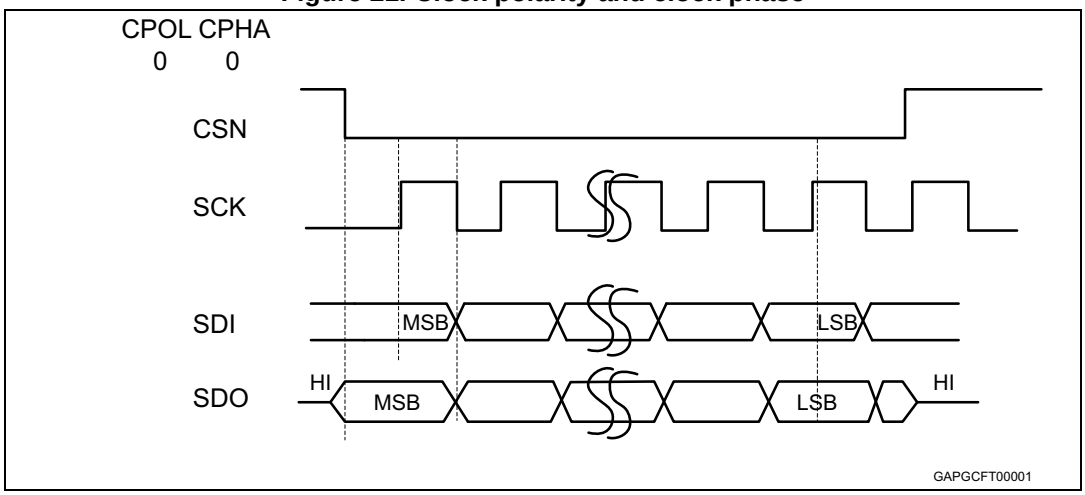
During active mode, the SPI:

- Triggers the watchdog
- Controls the modes and status of all internal modules (incl. input and output drivers)
- Provides driver output diagnostic
- Provides device diagnostic (incl. over temperature warning, device operation status)

Note: During standby modes, the SPI is generally deactivated.

The SPI can be driven by a microcontroller with its SPI peripheral running in following mode:

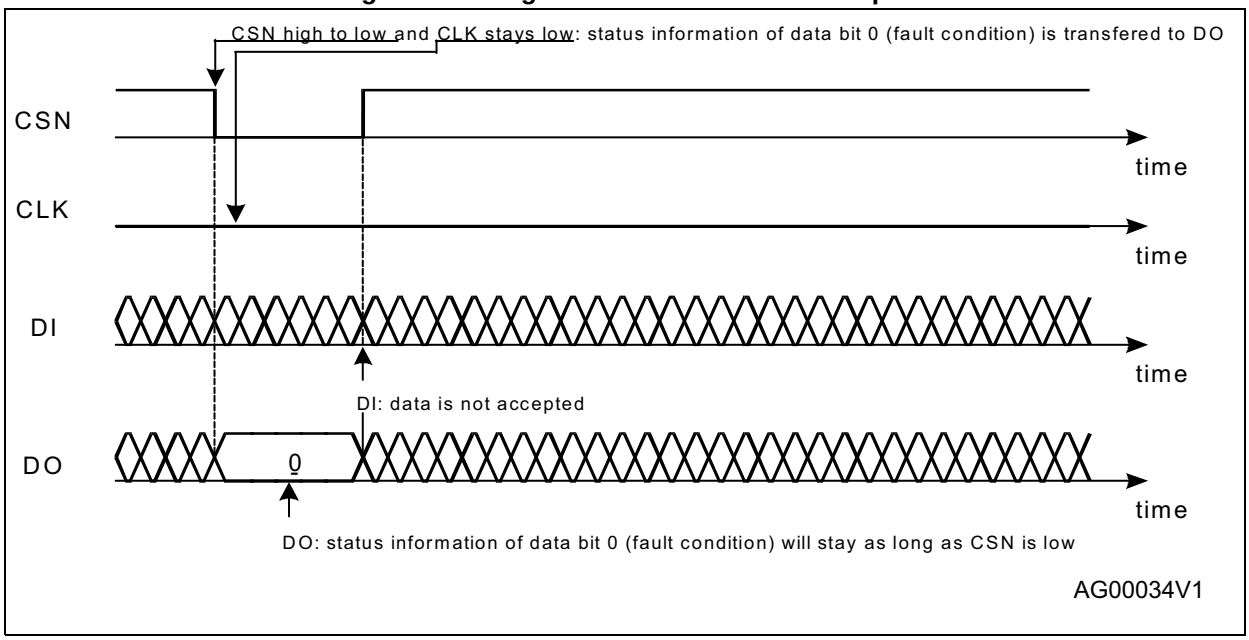
Figure 21. Clock polarity and clock phase



According to the standard, a generic input bit is sampled by the low to high transition of the clock CLK and a generic output bit changes synchronously to the high to low transition of CLK.

This device is not limited to micro controller through a built-in SPI. Only three CMOS-compatible output pins and one input pin will be needed to communicate with the device. A fault condition can be detected by setting CSN low. If CSN = 0, the DO pin will reflect the global error flag (fault condition) of the device (see *Figure 22*). This operation does not cause a communication error bit in the global status byte to be set.

Figure 22. SPI global error information output



3.2 Signal description

- Serial Clock (SCK): this input signal provides the timing of the serial interface. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK). Data on Serial Data Out (SDO) is shifted out at the falling edge of Serial Clock (SCK).
- Serial Data Input (SDI): This input is used to transfer data serially into the device. It receives the data to be written. Values are latched on the rising edge of Serial Clock (SCK).
- Serial Data Output (SDO): this output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK). SDO also reflects the status of the <Global Error Flag> (Bit 7 of the <Global Status Register>) while CSN is low and no clock signal is present
- Chip Select Not (CSN): when this input signal is High, the device is deselected and Serial Data Output (SDO) is high impedance. Driving this input Low enables the communication. The communication must start and stop on a Low level of Serial Clock (SCK).

3.3 SPI protocol

3.3.1 SDI, SDO format

SDI format during each communication frame starts with a command byte.

It begins with two bits of operating code (OC0, OC1) which specify the type of operation (read, write, read and clear status, read device information) and is followed by a 6 bit address (A0:A5). The command byte is followed by an input data byte (D0:D15).

At the beginning of each communication the master device read the contents of the <SPI-frame-ID> register (ROM address 3Eh) of the slave device. This 8 bit register indicates the SPI frame length (24 bit) and the availability of additional features.

Each communication frame consists of a command byte which is followed by 2 data bytes.

The data returned on SDO within the same frame always starts with the <Global Status Byte>. It provides general status information about the device. It is followed by 2 data bytes (i.e. "in-frame-response").

For write cycles the <Global Status Byte> is followed by the previous content of the addressed register.

Table 4. Command byte (8 bit)

Bit	23	22	21	20	19	18	17	16
Name	OC1	OC0	A5	A4	A3	A2	A1	A0

Table 5. Input data byte

	Data Byte 1								Data Byte 0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

SDO format during each communication frame starts with a specific byte called Global Status Byte (see *Section 3.3.2*). This byte is followed by two output data byte (D0:D7, D8:D15).

Table 6. Global status byte

Bit	23	22	21	20	19	18	17	16
Name	GEF	Comm_Err	Not (chip reset or Comm_Error)	LED overload	Temp. warning	Overvoltage	V_{CC1} Error	Fail safe

Table 7. Output data byte

	Data Byte 1								Data Byte 0							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

3.3.2 Global status byte description

The data shifted out on SDO during each communication starts with a specific byte called Global Status Byte. This one is used to inform the microcontroller about global faults which can be happened on the channel part (like thermal warning, OVL,...) or on the SPI interface (like communication error,...). This specific register has the following format.

Table 8. Global status byte

Bit	Name	Description
23	Global Error Flag (GEF)	This bit is an OR combination of the remaining bits of the register OR (Vs_uv) OR (Lmode_err)
22	Comm_Err	The right number of SPI clocks within any valid spi command is 24. If not, then this bit is set to '1'. This bit goes to '0' automatically after any valid spi command
21	Not (Chip reset OR Comm Err)	After a POR phase this bit is active ('0'). It becomes inactive ('1') after the first valid spi command, provided that any communication error occurs.
20	LED Overload	This bit is set when an LED overcurrent event is detected
19	Temp. warning	Temperature Warning for the LED
18	Overvoltage	LED chain overvoltage or Vs overvoltage via INP_OV (Led_Ov OR Vs_Overvoltage)
17	V_{CC1} Error	This bit is an OR combination of all the errors related to V_{CC1}
16	Fail Safe	This bit is set if the device is in a limp home mode (Data In stuck at '0' or '1', watchdog time out, software limp home), V_{CC1} undervoltage for more than 2 ms in active mode.

3.3.3 Operating code definition

The SPI interface features four different addressing modes which are listed in *Table 10*.

Table 9. Operation code definition

OC1	OC0	Meaning
0	0	Write operation
0	1	Read operation
1	0	Read and clear status operation
1	1	Read device information

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device.

A <Read and Clear Mode> operation is used to read a status register and subsequently clears its content.

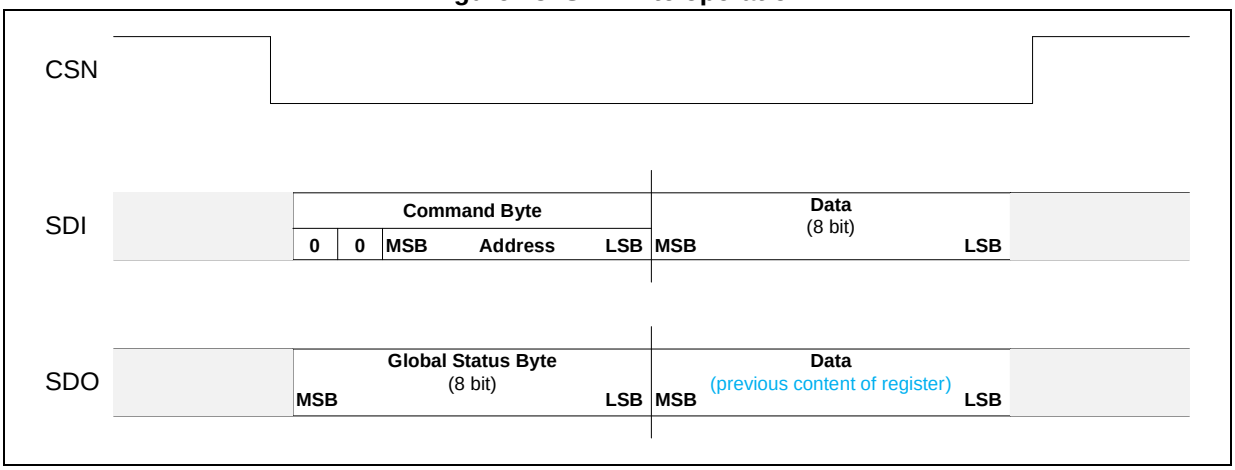
The <Read Device Information> allows access to the ROM area which contains device related information such as <ID-Header>, <Product Code>, <Silicon Version> and <SPI-frame-ID>.

Write mode

The write mode of the device allows writing the content of the input data byte into the addressed register. Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

During the same sequence outgoing data are shifted out MSB first on the falling edge of the CSN pin and subsequent bits on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte and the second to the previous content of the addressed register.

Figure 23. SPI write operation

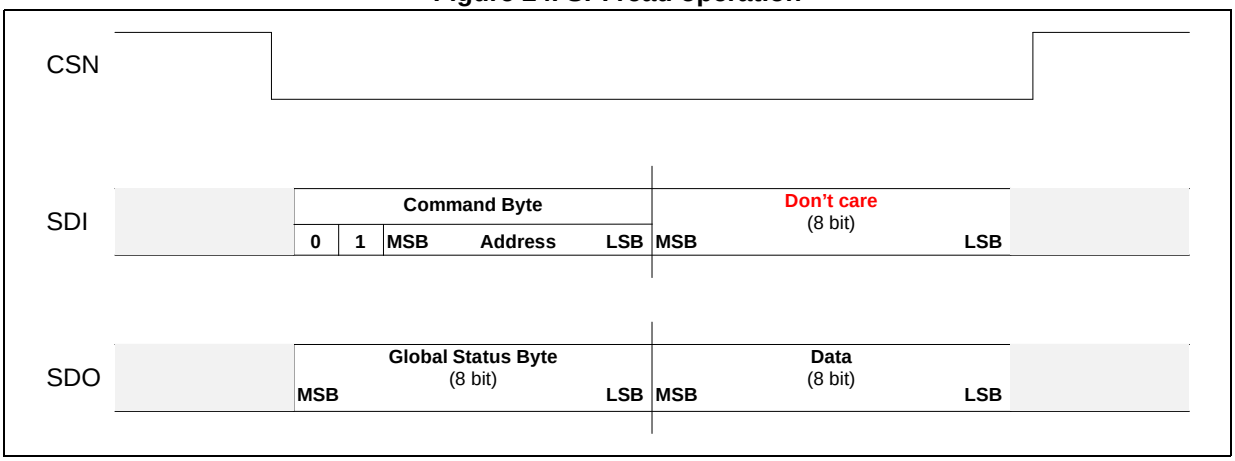


Read mode

The read mode of the device allows to read and to check the state of any register. Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte and the second to the content of the addressed register. In case of a read mode on an unused address, the ‘global status/error’ byte on the SDO pin is following by 00H byte.

In order to avoid inconsistency between the Global status byte and the status register, the status register contents are frozen during SPI communication.

Figure 24. SPI read operation



Read and clear status command

The read and clear status operation is used to clear the content of the addressed status register (see *Section : Status registers 1*). A read and clear status operation with address

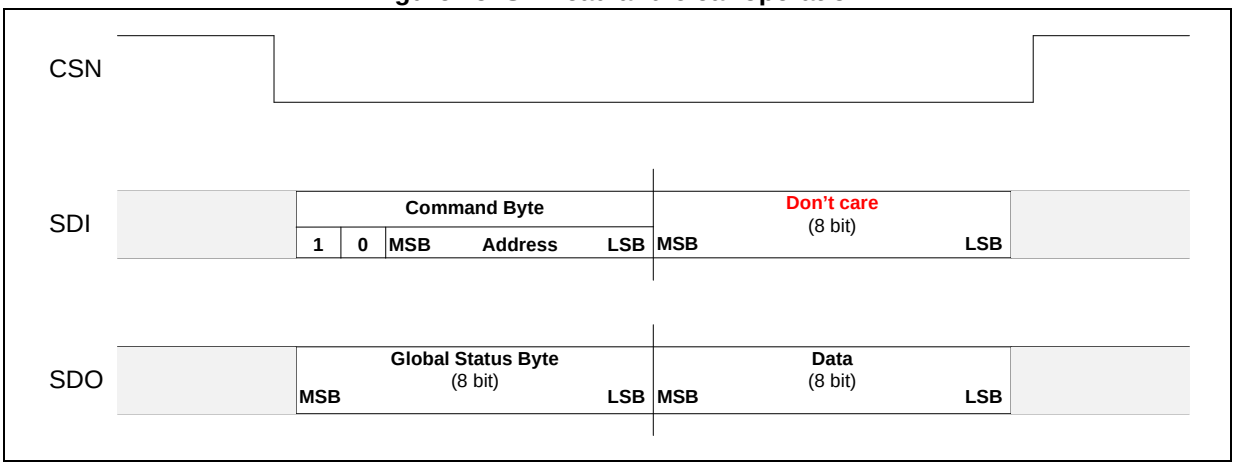
3Fh clears all status registers simultaneously and reads back the configuration register (GLOBCTR).

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which register content is read then erased while the data byte is ‘don’t care’.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte and the second to the content of the addressed register.

In order to avoid inconsistency between the Global status byte and the status register, the status register contents are frozen during SPI communication.

Figure 25. SPI read and clear operation



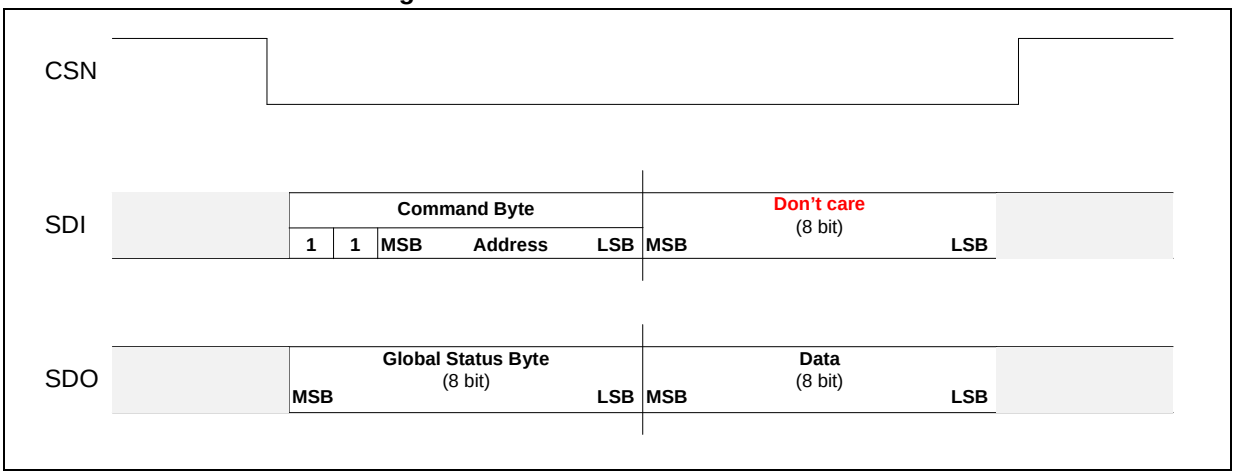
Read device information

Specific information can be read but not modified during this mode.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which information is read while the data byte is ‘don’t care’.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte and the second to the content of the addressed register.

Figure 26. SPI read device information



3.4 Address mapping

Table 10. RAM memory map

Address	Name	Access	Content
00h	Reserved	Read/write	Reserved
01h	Control register 1	Read/write	Mux settings, WD period and retrigger
02h	Control register 2	Read/write	Spread spectrum settings, max input current and LED current settings
03h	Control register 3	Read/write	SW Limp Home, OTA/driver and converter delay control
04h	Status register 1	Read	Detailed status information
05h	Status register 2	Read	WD status, operation mode and LMode error
3E	Trimming and test	Read	Trimming bus and test mode select
3F	Configuration reg.	Read/write	WD retrigger bit

Table 11. ROM memory map

Address	Name	Access	Content
00h	ID header	Read only	4300h (ASSP ST_SPI)
01h	Version	Read only	0100h
02h	Product code 1	Read only	3100h (dec. 49)
03h	Product code 2	Read only	5100h (ASCII 'Q')
3Eh	SPI frame ID	Read only	4200h (Watchdog available, 24 bit ST-SPI)

3.5 Control registers (RAM)

Control registers 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										Mux[[1:0]		Mux_En	En_Ntc	WD_Period	WD_trig

Address: 0x01h

Type: R/W

Reset: 0000 0000 0000 1110b

Bit [6:15] Reserved

Bit [5:4] Mux[1:0]:
00 (default): the signal on the PWM pin is reflected on Mout pin
01: the signal on the V_{LED} is reflected on Mout pin
10: the signal on NTC is selected
11: the signal on Lmode pin is selected

Bit [3] Mux_En:
0: the Mout pin is inactive (tristate)
1: the Mout pin is active (default)

Bit [2] En_Ntc:
When set, the current fold back feature enabled in case of LED overtemperature conditions.
This bit is ignored in case of any LIMP MODE and the LED temperature monitoring is activated (the NTC control is internal)

Bit [1] WD_Period:
0: WD timeout = 100 ms
1: WD timeout = 200 ms (default)

Bit [0] WD_trig:
This bit must be toggled within the WD period to refresh the WD

Control registers 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fdev[2:0]			Fmod[1:0]		Dith_En	Led_Curr[4:0]					Max_Curr[4:0]				

Address: 0x02h

Type: R/W

Reset: 0101 1110 0001 1111b

Bit [15:13] Fdev[2:0]: frequency deviation of the internal oscillator (see *Table 12*)

Bit [12:11] Fmod[1:0]: frequency modulation of the internal oscillator (see *Table 13*)

Bit [10] Dith_En: enable or disable random dither effect.
If this bit is set Dithering is enabled;
If the bit is reset, the dithering is disabled

Bit [9:5] Led_Curr[4:0]: these bits set the LED current.
The LED current is given by:
0.05 + (0.2 * Led_Curr[4:0]d) / 31) / (R_{SENSE}) [A] (typ)
Where Led_Curr[4:0]d = decimal value of Led_Curr[4:0]

Bit [4:0] Max_Curr[4:0]: these bits set the maximum input current.
The internal current limiter voltage threshold is:
1 + (2.5 * Max_Curr[4:0]d) / 31 in [V] (typ)
Considering the gain of the amplifier of 10, the current limitation is:
(1 + 2.5 * Max_Curr[4:0]d / 31) / (10 R_{SHUNT}) (typ);
Where Max _Curr[4:0]d = decimal value of Max_Curr[4:0]

Table 12. Internal oscillator frequency deviation settings

Fdev[2]	Fdev[1]	Fdev[0]	Frequency deviation
0	0	0	0 %
0	0	1	5 %
0	1	0	10 %
0	1	1	15 %
1	0	0	20 %
1	0	1	25 %
1	1	0	30 %

Table 13. Internal oscillator frequency modulation settings

Fmod[1]	Fmod[0]	Frequency modulation
0	0	1.95 kHz
0	1	3.9 kHz
1	0	7.8 kHz
1	1	15.6 kHz

Control registers 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			Lh_Sw	Ctrl_Ota[3:0]				Ctrl_Drv[3:0]							

Address: 0x03h

Type: R/W

Reset: 0000 1000 0000 0000b

Bit [15:13] Reserved

Bit [12] Lh_Sw:

The device goes in Limp Home mode without WD supervision (V_{CC1} stays on) when the bit is set

Bit [11:8] Ctrl_Ota[3:0]: these bits set the delay between a rising edge of the PWM_L signal and a connection of the output of the operation transconductance amplifier.

The delay is given by Ctrl_Ota[3:0]d * 3.3 µs (typ.)

Where Ctrl_Ota[3:0]d is the decimal value of Ctrl_Ota[3:0]

The default of these bits are loaded from the corresponding control bus

Bit [7:4] Ctrl_Drv[3:0]: these bits set the delay between a rising edge of the PWM_L signal and the activation of the converter

The delay is given by:

Ctrl_Drv[3:0]d * 1.67 µs (typ.)

Where Ctrl_Drv[3:0]d is the decimal value of Ctrl_Drv[3:0]

The default of these bits are loaded from the corresponding control bus

Bit [3:0] Ctrl_Sw[3]: these bits set the delay between the falling edge of the PWM_L signal and the turn off of the dimming mosfet M2.

The delay is given by:

Ctrl_Sw[3:0]d * 1.67 µs (typ.)

Where Ctrl_Sw[3:0]d is the decimal value of Ctrl_Sw[3:0]

The default of these bits are loaded from the corresponding control bus.

3.6 Status registers

Status registers 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			Lmode_Err	Vs_Ov	Vs_Uv	Led_Temp_War	Led_Oc	Led_Ov	Vcc1_Off	Vcc1_Fail	Vcc1_Uv_To	Vcc1_Ot	Vcc1_Sc	SDI_stuck@	WD_fail
—			R(1)	R	R(1)	R/C(2)			R	R/C(2)					

1. “Read only”, real time bit.
2. These bits are latched until a “Read and Clear” access.

Address: 0x04h

Type: R/C

Bit [15:13] Reserved

Bit [12] Lmode_Err: this bit is set if a mismatch between the signal on LMODE pin and VLED pin is detected.

Bit [11] Vs_Ov: is set if an overvoltage event at the supply line is detected

Bit [10] Vs_Uv: is set if an under voltage event at the supply line is detected

Bit [9] Led_Temp_Warn: temperature warning for the LED

Bit [8] Led_Oc: Is set if an over current event across the LED chain is detected

Bit [7] Led_Ov: is set if an overvoltage event across the LED chain is detected

Bit [6] Vcc1_Off: when set, this bit indicated that V_{CC1} is off

Bit [5] Vcc1_Fail
Indicates that:
V_{CC1} is below V_{CC1_FAIL} threshold for typ. 2 µs in active mode
V_{CC1} is below V_{CC1_FAIL} threshold for more than 4 ms typ. during start up

Bit [4] Vcc1_Uv_To: this bit is set in active mode if V_{CC1} is below the reset threshold for more than typ. 2 ms

Bit [3] Vcc1_Ot: set if an overtemperature condition has been detected on V_{CC1}

Bit [2] Vcc1_Sc: indicates a short circuit on V_{CC1}.
This bit is set if V_{CC1} stays below the V_{CC1_FAIL} threshold 4 ms (typ.) after the power on reset or below the reset threshold 100 ms after the POR (Power On Reset)

Bit [1] SDI_stuck@

Bit [0] WD_fail

Status registers 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							Led_Ov_Rec	Ext_Vcc	PWM_L	Standalone	LHM	Lh_Sw_St	WD_Status[2:0]		
—							R	R(1)		R	R(1)	R	R(2)		

1. “Read only”, real time bit.
2. “Read only” bit. These bits are cleared by a WD re-trigger.

Address: 0x05h

Type: R

Bit [15:9] Reserved

Bit [8] Led_Ov_Rec
Once this bit is set, the device will make a single trial to recover from an LED overvoltage.

Bit [7] Ext_Vcc: this bit reflects the signal on the Ext_Vcc pin,

Bit [6] PWM_L: this bit reflects the signal on the PWM_L pin

Bit [5] Standalone: this bit is set if the device operates in standalone mode, without microcontroller

Bit [4] LHM: reflects the level at LHM pin

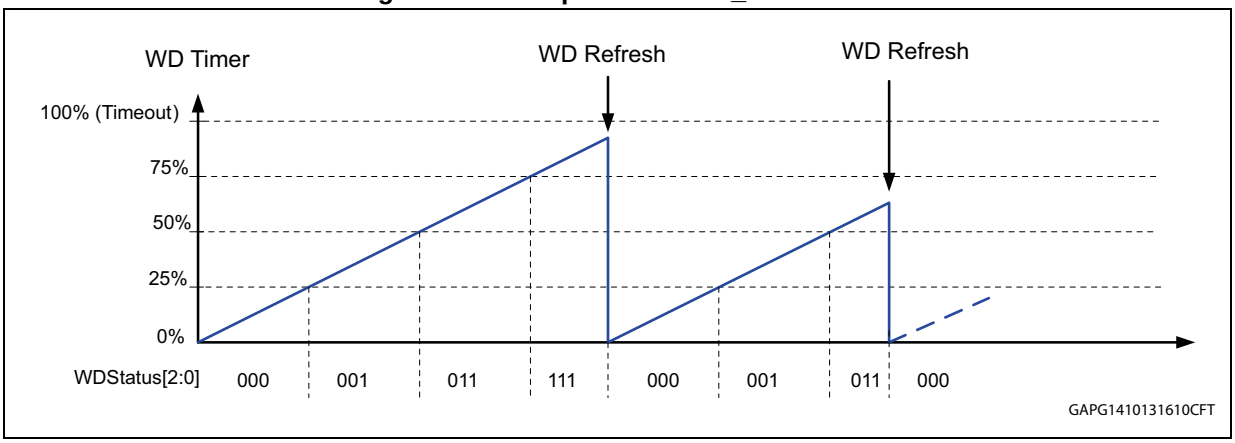
Bit [3] Lh_Sw_St: is set if the software limp home mode is activated

Bit [2:0] WD_status[2:0]: these bits indicate the status of the watchdog timer (see *Table 14* and see *Figure 27*)

Table 14. Watchdog timer status

WD_Status[1]	WD_Status[1]	WD_Status[0]	WD timer status
0	0	0	[0…25 %[
0	0	1	[25 % … 50 %[
0	1	1	[50 % … 75 %[
1	1	1	[75 % … 100 %[

Figure 27. Principle of the WD_Status bits



Trimming and test register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM[5:0]						Trim_Bus[9:0]									
R/W						R									

Address: 0x3Eh

Type: R/W

Reset: 0000 0000 0000 0000b

Bit [15:10] TM[5:0]: test mode selection (refer to the UQ49 test controller)

Bit [9:0] Trim_Bus[9:0]: copy of the data stored in the trimming fuse cells

Configuration register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															WD_Trig
—															R/W

Address: 0x3Fh

Type: R/W

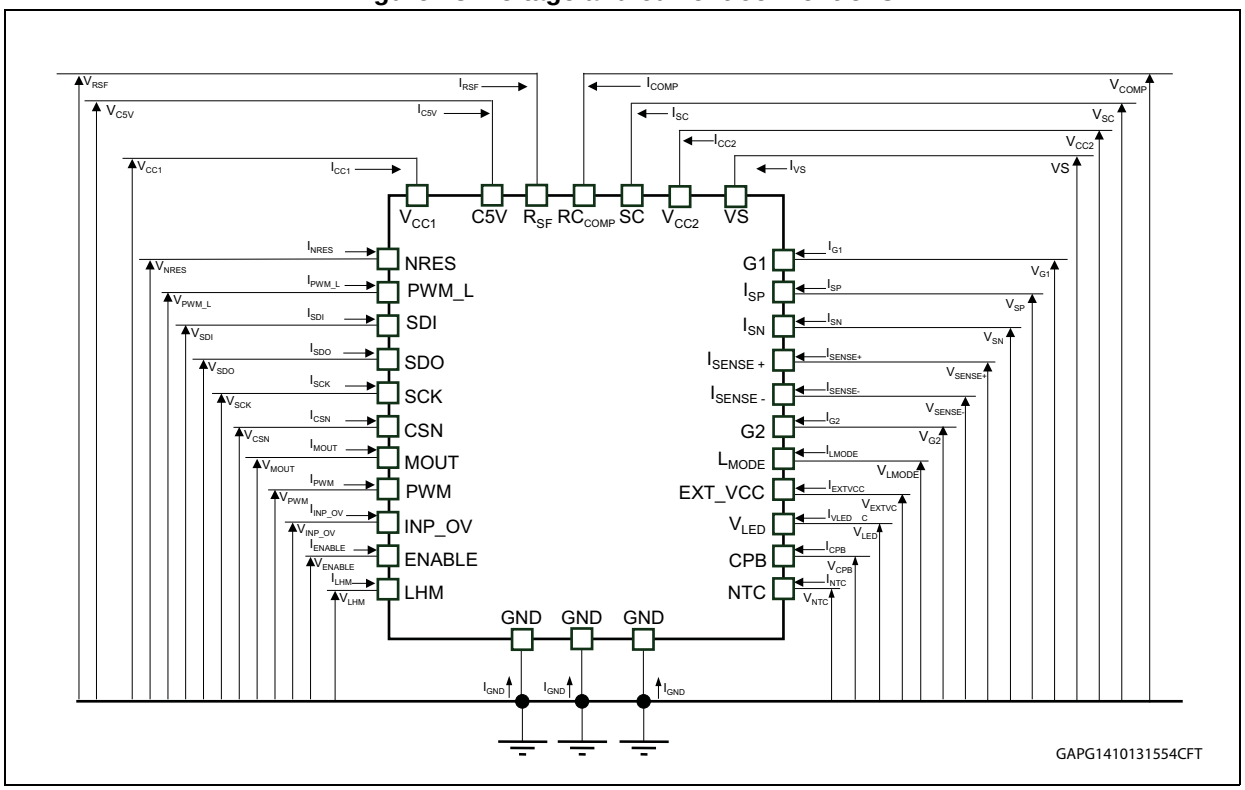
Reset: 0000 0000 0000 0000b

Bit [15:1] Reserved

Bit [0] WD_Trig: this bit must be toggled within the WD period to refresh the WD.
Note that this bit is copied in the Control register 1, bit 0

4 Electrical specifications

Figure 28. Voltage and current conventions



4.1 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 15. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC operating supply voltage	5.6 / 24	V
V_{S_TR}	Transient operating supply voltage (T < 400 ms)	-0.3 / 40	V
V_{SDI}	SPI data input voltage range	-0.3 / +5.3	V
V_{SDO}	SPI data output voltage range	-0.3 / +5.3	V
V_{SCK}	SPI clock voltage range	-0.3 / +5.3	V
V_{CSN}	SPI chip select not voltage range	-0.3 /+5.3	V
V_{NRES}	Reset output pin voltage range	-0.3 ÷ V_S+0.3	V
V_{CC1}	Regulator1 supply voltage output	-0.3 / + 5.5	V
V_{CC2}	Regulator 2 supply voltage output	-0.3 / + 10.5	V
V_{ENABLE}	Enable input pin voltage range	-0.3 ÷ V_S+0.3	V

Table 15. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{SC}	Slope compensation input voltage range	-0.3 / + 5.3	V
V_{LHM}	Limp home mode input pin voltage range	-0.3 ÷ V_S+0.3	V
V_{PWM}	Input L.F. PWM voltage range	-0.3 ÷ V_S+0.3	V
V_{PWM_L}	Logic level L.F. PWM input voltage range	-0.3 / +5.3	V
V_{MOUT}	Multiplexed data output pin voltage range	-0.3 / +5.3	V
V_{G1}	Driver 1 output voltage range	-0.3 / (V_{CC2} + 0.3)	V
V_{G2}	Driver 2 gate output voltage range	-0.3 / min (V_{CPB} + 0.3, 68)	V
V_{EXT_VCC}	External VCC voltage range	-0.3 / 5.3	V
V_{CPB}	External capacitor voltage range	$V_{ISENSE+}$ - 0.8 V / min ($V_{ISENSE+}$ + 16 V, 68 V)	V
$V_{ISENSE+}$	Positive sensing res. voltage range	-0.3 / 55	V
$V_{ISENSE-}$	Negative sensing res. voltage range	$V_{ISENSE+}$ - 5 V / $V_{ISENSE+}$ + 0.3 V	V
V_{SP}	Sensing positive shunt res voltage range	-0.3 / +5.3	V
V_{SN}	Sensing negative shunt res voltage range	-0.3 / +5.3	V
V_{INP_OV}	overvoltage input pin voltage range	-0.3 ÷ V_S+0.3	V
V_{RSF}	External set frequency resistor voltage range	-0.3 / 5.5	V
V_{C5V}	C5V ext capacitor voltage range	-0.3 / 5.5	V
$V_{RC\ COMP}$	External RC network input pin voltage range	-0.3 / 5.5	V
V_{NTC}	External NTC resistor input voltage range	-0.3 / 5.5	V
V_{LED}	LED chain drop voltage detection input range	-0.3 / + 65	V
V_{LMODE}	LED Mode switch voltage range	-0.3 / +5.3	V
V_{ESD}	Electrostatic discharge (HBM R = 1.5 kΩ; C = 100 pF)	± 2	kV
V_{ESD}	CDM model all pin	500	V
V_{ESD}	CDM for corner pin	750	V
Tj	Junction operating temperature	-40 to 150	°C
Tstg	Storage temperature	-55 to 150	°C

Table 16. Thermal data

Symbol	Parameter	Value	Unit
$R_{Thj\text{-}case}$	Thermal resistance junction to case	27	°C/W
$R_{Thj\text{-}amb}$	Thermal resistance junction to ambient	90	°C/W

5 Electrical characteristics

Values specified in this section are for 5.6 V ≤ V_S ≤ 24 V; -40 °C ≤ Tj ≤ 150 °C, unless otherwise specified

Table 17. VS and V_{CC1} pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_S	Operative battery voltage		5.6		24	V
I_S	Supply current consumption in continuous mode (L.F. PWM = 100 %)	V_S = 13.5 V; F_{REQ} = 300 kHz; I_{CC1} = I_{CC2} = I_{C5V} = 0			20	mA
I_{S_STBY}	Supply current consumption in stand by mode	Enable = Low; LHM,CSN,PWM, INP_OV = open; V_{NRES} ≤ 5.5 V; V_S = 13.5 V; T_j = 25 ºC			12	µA
V_{SMIN}	Minimum V_S required for reaching V_{CC1} nominal value	V_S ramp up	4.8	5.2	5.6	V
V_{SMIN_HYS}	V_{SMIN} hysteresis	V_S ramp down		0.2		V
t_{VSM}	V_{SMIN} filtering time		13	16	23	µs
V_{CC1}	D.C. logic supply output voltage	1 < -I_{CC1} < 10 mA	4.9	5	5.1	V
-I_{CC1}	Output current capability	V_S = 13.5 V; V_{CC1} = V_{CC1_1mA} - 0.1 V(1)	50			mA
V_{CC1_DROP}	Min voltage drop of V_{CC1} respect to V_S: V_{CC1_DROP} = min (V_S - V_{CC1})	-I_{CC1} = 10 mA			500	mV
V_{CC1_LINE}	Line regulation voltage	-I_{CC1} = 10 mA; $V_{CC1@5.6}$ – $V_{CC1@24}$			5	mV
V_{CC1_LOAD}	Load regulation voltage	-I_{CC1} = 1 to 10 mA; V_S = 13.5 V			10	mV
V_{CC1_FAIL}	V_{CC1} fail detection threshold(2)	V_S ≥V_{SMIN}; V_{CC1} rising	2.4	2.6	2.8	V
		V_S ≥V_{SMIN}; V_{CC1} falling	1.9	2.1	2.3	V
$t_{LMODERR}$	Filtering time for LMODE error		13	16	23	µs
t_{OC}	Filtering time for LED overcurrent		13	16	23	µs
t_{LEDOV}	Filtering time for LED overvoltage		12	15	22	µs
t_{WD1}	1st watchdog time-out period		85	100	135	ms
t_{WD2}	2nd watchdog time-out period		170	200	275	ms
t_{V1F}	Internal filtering time for v_{cc1} fail detection	V_S ≥ V_{SMIN}	1.7	2	2.75	µs
t_{SHTV1A}	Time to detect a short on V1 regulator at turn-on	V_S ≥ V_{SMIN}; V_{CC1} < V_{CC1_FAIL}; t ≥ t_{SHTV1A}		4		ms
t_{SHTV1B}	Time to detect a short on V1 regulator at turn-on	V_S ≥ V_{SMIN}; V_{CC1_FAIL} ≤ V_{CC1} ≤ V_{CC1_TH}; t ≥ t_{SHTV1B}		100		ms

Table 17. VS and V_{CC1} pin characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
CV_{CC1}	Load capacitance	A good quality (Low ESR) capacitor is recommended	1	10		µF
V_{CC1_OT}	Regulator 1 over temperature detection level		150	175	190	°C
$V_{CC1_OT_HYS}$	Hysteresis		20	25	30	°C
t_{V1OT}	Filtering time for regulator 1 over temperature detection		0.75	1	1.55	ms

1. V_{CC1_1mA} is V_{CC1} at I_{LOAD} = 1 mA; V_S = 13.5 V.
2. Minimum V_{CC1} voltage for keep RAM data.

Table 18. V_{CC2} and C5V pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC2}	D.C. logic supply output voltage	$1 \le -I_{CC2} \le 10$ mA; V_S = 13.5 V; V_{PWM_L} = 0	9.5	10	10.5	V
$-I_{CC2}$	Output current capability	V_S = 13.5 V; $V_{CC2} = V_{CC2_1mA}$ - 0.1 V(1); V_{PWM_L} = 0	20			mA
V_{CC2_DROP}	Drop voltage to V_S: $V_{CC2_DROP} = (V_S - V_{CC2})$	$-I_{CC2}$ = 1 mA; V_{CC2} = 9.5 V; V_{PWM_L} = 0			100	mV
$-I_{CC2_SHT}$	Short output current limitation	$0 \le V_{CC2} \le V_{CC2_1mA}$; V_S = 13.5 V; V_{PWM_L} = 0			100	mA
CV_{CC2}	Load capacitance	A good quality (Low ESR) capacitor is recommended for correct managing gate peaks current during switching On and OFF of G1	10			µF
V_{CC2_OT}	Regulator 2 over temperature detection level		150	175	190	°C
$V_{CC2_OT_HYS}$	Over temperature detection level hysteresis		20	25	30	°C
V_{C5V}	Internal 5 V output voltage	$0 \le -I_{C5V} \le 2.5$ mA	4.75	5	5.25	V
$-I_{C5V}$	5 V output current	$V_{C5V} = V_{C5V_1mA}$(2) - 0.1	2.5			mA
$-I_{C5V_SHT}$	Short output current limitation	$0 \le V_{C5V} \le V_{C5V_1mA}$(3) (pulsed s.c. no continuous short)			50	mA
C_{5V}	Load capacitance See *Figure 34*		1			µF

1. V_{CC2_1mA} is the value of V_{CC2} at I load = 1 mA, V_S = 13.5 V; T_j = 25 °C.
2. V_{C5V_1mA} is the value of V_{C5V} at external I_{C5V} load = 1 mA, V_S = 13.5 V; T_j = 25 °C.
3. V_{C5V_1mA} is the value of V_{C5V} at external I_{C5V} load = 1 mA, V_S = 13.5 V; T_j = 25 °C.

Table 19. NRES and L_{MODE} pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{CC1_TH}	Reset intervention threshold		4.6	4.7	4.8	V
T_{RR}	V_{CC1} reset filtering time	$V_{CC1} < V_{CC1_TH}$	13	16	23	µs
t_{FS}	V_{CC1} reset time-out for fail safe detection	$V_S \geq V_{SMIN}$; $V_{CC1} < V_{CC1_TH}$; $t \geq t_{FS}$	1.6	2	2.9	ms
T_{RD}	Reset delay time	$V_{CC1} \geq V_{CC1_TH}$	1.6	2	2.9	ms
I_{NRES}	High state reset sink current	$V_{NRES} = V_S$; NRES active	0.5	1.7	3.5	mA
I_{NRES}	High state reset leakage current	$V_{NRES} = V_S$; NRES inactive			300	µA
V_{NRES_L}	Reset I/O low state level	$V_{CC1} \leq V_{CC1_TH}$; I_{NRES} = 1 mA			0.5	V
V_{LMODE_H}	Led mode switch high state input		4			V
V_{LMODE_L}	Led mode switch low state input				1	V
$-I_{LMODE}$	Internal pull up current source	V_{LMODE} = 0	10	18	25	µA

Table 20. G1 driver 1 pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{G1_H}	Gate1 high level		5		V_{CC2}	V
V_{G1_L}	Gate1 low level				0.5	V
$tr_{_G1}$	Gate1 charging rise time	CG = 4.7 nF; V_{GS1} rising from 10 % to 90 %; $V_S \geq 10$ V			40	ns
$tf_{_G1}$	Gate1 discharging fall time	CG = 4.7 nF; V_{GS1} falling from 90 % to 10 %; $V_S \geq 10$ V			40	ns

Table 21. G2 pin characteristics (driver2)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{G2_H}	High state output V_{G2} voltage	PWM_L = High; $V(I_{SENSE+})$ = 30 V	$V(I_{SENSE+})$ +10		$V(I_{SENSE+})$ +14	V
V_{G2_L}	Low state output voltage V_{G2}	PWM_L = Low; $V(I_{SENSE+})$ = 30 V			0.05	V
$-I_{G2_H}$	Gate 2 high state output current	PWM_L = High; V_{GS_M2} = 6 V(1); C_{GS_M2} = 1 nF; $V(I_{SENSE+})$ = 30 V	200			µA
I_{G2_L}	Gate 2 low state output current	PWM_L = Low; V_{GS_M2} = 6 V(2); C_{GS_M2} = 1 nF; $V(I_{SENSE+})$ = 30 V	200			µA

1. I_{G2_H} current is measured when the voltage across gate and source of Mosfet M2 (V_{GS_M2}) reaches a value of 6 V during its rising transient.
2. I_{G2_L} current is measured when the voltage across gate and source of Mosfet M2 (V_{GS_M2}) reaches a value of 6 V during its falling transient.

Table 22. Converter oscillator and R_{SF} pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{RSF}	Voltage at pin R_{SF}	I_{RSF} = 42 µA	1.12	1.21	1.25	V
F_O	DC-DC converter frequency range	See *Figure 12*	100		520	kHz
F_{O_S}	Oscillator frequency spread at 125 kHz	I_{RSF} = 17 µA ($F_O \approx$ 125 kHz)	100	125	150	kHz
F_{O_S}	Oscillator frequency spread at 300 kHz	I_{RSF} = 42 µA ($F_O \approx$ 300 kHz)	240	300	360	kHz
F_{O_S}	Oscillator frequency spread at 470 kHz	I_{RSF} = 67 µA ($F_O \approx$ 470 kHz)	420	470	520	kHz
Duty cycle max	DC-DC converter max duty cycle limit			90		%
Duty cycle min	DC-DC converter min duty cycle limit			10		%
F_{MOD}	Modulation frequency of the internal oscillator	See *Section 3.5: Control registers (RAM)* F_{MOD}[0:1]	1.95, 3.9, 7.8, 15.6			kHz
D% = $\Delta F_0 / F_0$	Frequency deviation factor	See *Section 3.5: Control registers (RAM)* F_{DEV}[0:2]	0 to ±35 (step ±5 %)			%

Table 23. PWM_L, PWM, MOUT pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
TON_{PWM_L}	Minimum PWM_L on time	Q_G = 9 nC	100			µs
PWM_L_{LOW}	Low level PWM_L input voltage				1	V
PWM_L_{HIGH}	High level PWM_L input voltage		4			V
$I_{PWM_L_PD}$	Pull down current source		20	28	35	µA
PWM_{LOW}	Low level PWM input voltage				1	V
PWM_{HIGH}	High level PWM input voltage		4			V
R_{PWM_PD}	Pull Down resistor		50	230	500	kΩ
V_{MOUT_H}	High state output voltage (digital mode)	$-I_{MOUT}$ = 0.1 mA	4			V
V_{MOUT_L}	Low state output voltage (digital mode)	I_{MOUT} = 0.1 mA			1	V
Z_{MOUT}	Analogue mode output impedance			10		kΩ

Table 24. I_{SENSE+}, I_{SENSE-} pin, and O.T.A. characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Units
$V_{ISENSE+}$ $V_{ISENSE-}$	Common mode input range		V_S - 0.3		49	V
($V_{ISENSE+}$ - $V_{ISENSE-}$)	Operative differential input voltage range		-1		0.3	V

Table 24. I_{SENSE+}, I_{SENSE-} pin, and O.T.A. characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
$(V_{ISENSE+} - V_{ISENSE-})_TH$	LED over current protection threshold	$V(I_{SENSE}+) = 25$ V; $V_{LREF} = V_{LREF_16}$; $V_{RCCOMP} = 2$ V	V_{LREF} + 0.03	V_{LREF} + 0.08	V_{LREF} + 0.14	V
I_{SENSE_CD}	Current consumption from I_{SENSE+} (LED_OV)	$V_{SENSE+} = V_{SENSE-} = 25$ V	3	5	10	mA
$V_{SENSE_MAX_1}$	Threshold at pin I_{SENSE+} for overvoltage protection (activation)		49.5	52	54	V
$V_{SENSE_MAX_2}$	Threshold at pin I_{SENSE+} for overvoltage protection (de-activation)		25	33	35	V
V_{OFFS}	OTA input offset voltage	$V_{LREF} = 0$ V; $V(I_{SENSE}+) = 25$ V; $V_{RCCOMP} = 2$ V	-10		10	mV
I_{OFFS}	OTA input offset current	$V(I_{SENSE}+) = 25$ V; $V_{RCCOMP} = 2$ V			10	µA
G_M	Transconductance gain	$V(I_{SENSE}+) = 25$ V; $V_{RCCOMP} = 2$ V	0.95	1.2		mS
$-I_{COMP}$	Sourced output current	$V_{LREF} = V_{LREF_16}$; $(V_{ISENSE+} - V_{ISENSE-}) = 0$	50	175		µA
I_{COMP}	Sunk output current	$V_{LREF} = V_{LREF_16}$; $(V_{ISENSE+} - V_{ISENSE-}) = 300$ mV	50	175		µA
		$V_{LREF} = V_{LREF_16}$; $(V_{ISENSE+} - V_{ISENSE-}) = 1$ V	100	300		
V_{COMP}	Output voltage range		0		3.5	V
V_{LREF_16}	Default internal voltage reference for constant LED current regulation	Internal LED current register = 16d; $V_{NTC} = 5$ V; $V_{ISENSE+} = 25$ V	138	150	162	mV
V_{LREF}	Internal voltage reference range-for setting output LED current(1)	$V_{NTC} = 5$ V		(8 + N) / 24 * V_{LREF_16} (2)		mV
V_{LREF_NTC}	Max internal V_{LREF} reduction caused by NTC intervention (thermal LED current reduction)	$V_{NTC} = 0$ V		0.5 * V_{LREF}		mV
V_{LREF_STEP}	Internal voltage reference step			4 / 3 * (V_{LREF_16} / 31)		mV
I_{SP}, I_{SN} pin characteristics						
V_{SP}, V_{SN}	Shunt resistor input voltage range		-0.3		5	V

Table 24. I_{SENSE+}, I_{SENSE-} pin, and O.T.A. characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{SP}-V_{SN}	Differential input voltage range		-0.3		0.5	V
G_{LA_CPK}	Gain of internal linear amplifier	V_{SP} = 100 mV; V_{SN} = 0 V; Pin SC floating	8	9.8	12	
V_{LA_OFFS}	Linear amplifier output offset voltage	V_{SP} = V_{SN} = 0		150	350	mV
V_{CL_31}	Default internal reference for the current limiter(3)	Internal C.L. register = 31		3.5		V
$(V_{SP}$-$V_{SN})_{TH}$	Differential threshold voltage for activate max input current prot.	Internal C.L. register = 31; V_{SC} = 5 V	300	350	400	mV
V_{CL}	Internal C.L. voltage reference range		0.279 * V_{CL_31}		V_{CL_31}	V
V_{CL_STEP}	Internal C.L. voltage reference step			(0.721 * V_{CL_31} / 31)		V

1. Writing into 5 bit LED Current Register via SPI.
2. N is the number corresponding to the 5 bits of LED_CURR control register.
3. Settable by loading the 5 bit C.L. Register via SPI.

Table 25. SC pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{SC_low}	Min ramp voltage at pin SC	I_{SC} = 0		0.2	0.45	V
V_{SC_HIGH}	Max ramp voltage at pin SC	I_{SC} = 0	1.4	2	2.6	V
R_{SC}	Ext. resistor range		10		1000	kΩ

Table 26. V_{LED} pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{LED}	Operative input voltage range for OV detection	L_{MODE} = low	0		5	V
		L_{MODE} = high	V_S		V_S+5	
R_{VLED_PD}	Pull down resistor		0.4	0.8	1.2	mΩ
OV_TH1	LED overvoltage threshold 1 boost application	L_{MODE} = low	3.4	3.5	3.6	V
OV_TH2	LED overvoltage threshold 2 boost application	L_{MODE} = low	2.3	2.5	2.7	V

Table 26. V_{LED} pin characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
OV_TH1_VS	LED overvoltage threshold 1 buck-boost application	L_{MODE} = high	V_S + 3.2	V_S + 3.55	V_S + 3.8	V
OV_TH2_VS	LED overvoltage threshold 2 buck-boost application	L_{MODE} = high	V_S + 2.2	V_S + 2.45	V_S + 2.8	V

Table 27. INP_OV pin characteristics (input overvoltage shut down)

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{INP_OV}	Operative input overvoltage range		0		5	V
$-I_{INP_OV}$	Pull UP current source at input INP_OV	V_{INP_OV} = 0 V	10	18	25	µA
$V_{INP_OV_TH1}$	Internal voltage reference 1		3.4	3.6	3.7	V
$V_{INP_OV_TH2}$	Internal voltage reference 2		2.7	2.9	3.1	V

Table 28. NTC pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{NTC}	Operative NTC voltage range		0		5	V
I_{NTC}	Pull down current source	V_{NTC}=5 V	5	10	15	µA
V_{NTC_TH1}	Reference for current LED thermal regulation, temp ramp up	LED temp ramp up	1.13	1.2	1.27	V
V_{NTC_TH2}	Reference for current LED thermal regulation, temp ramp down	LED temp ramp down	1.38	1.45	1.52	V

Table 29. ENABLE, LHM pin characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{ENABLE_L}	Low level ENABLE input voltage				1	V
V_{ENABLE_H}	High level ENABLE input voltage		4			V
R_{ENABLE_PD}	Enable pull down resistor		50	250	500	kΩ
V_{LHM_L}	Low level limp home mode input pin				1	V
V_{LHM_H}	High level limp home mode input pin		4			V
I_{LHM_PU}	Limp home pin pull up current	V_{HLM} = 0	10	18	25	µA

Table 30. Power on reset

Symbol	Parameter	Test condition	Min	Typ	Max	Units
POR_{TH1}	Internal power on reset threshold	V_{C5V} rising; V_S = 13.5 V; C5V = 10 µF	3.2	3.7	4.2	V
POR_{TH2}	Internal power on reset threshold	V_{C5V} falling; V_S = 13.5 V; C5V = 10 µF	2.7	3.4	3.7	V

Table 31. Watchdog and timers parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Units
t_{WDTO}	Watchdog timeout window			100 or 200(1)		ms
t_{DStart}	Start time window			5		ms
$t_{EnRecov}$				5		ms

1. Selectable by SPI command.

6 SPI electrical characteristics

6.1 DC characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 24 V; all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 32. SPI DC characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Inputs: CSN, CLK, DI						
V_{IL}	Input voltage low level	V_S = 13.5 V			0.3 V_{C5V}	V
V_{IH}	Input voltage high level	V_S = 13.5 V	0.7 V_{C5V}			V
V_{IHYS}	Input hysteresis	V_S = 13.5 V	500			mV
$I_{CSN\ in}$	CSN pull-up current source	V_S = 13.5 V	10	18	25	µA
$I_{CLK\ in}$	CLK pull-down current source	V_S = 13.5 V	20	25	35	µA
$I_{DI\ in}$	DI pull-down current source	V_S = 13.5 V	20	25	35	µA
Output: DO						
V_{OL}	Output voltage low level	I_{OL} = 5 mA; V_S = 13.5 V			0.3 V_{C5V}	V
V_{OH}	Output voltage high level	I_{OH} = -5 mA; V_S = 13.5 V	0.7 V_{C5V}			V

6.2 AC characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 24 V; all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 33. SPI AC characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
C_{OUT}(1)	Output capacitance (DO)		—	—	10	pF
C_{IN}(1)	Input capacitance (DI, CSN, CLK)		—	—	10	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

6.3 Dynamic characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 24 V; all outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

For definition of the parameters please see *Figure 29* and *Figure 30*.

Table 34. SPI dynamic characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{CSNQVL}	DO enable from tristate to low level	CDO = 100 pF; I_{DO} = 1 mA; pull-up load to V_{CC}; V_{CC1} = 5.0 V		100	250	ns
t_{CSNQVH}	DO enable from tristate to high level	CDO = 100 pF; I_{DO} = -1 mA; pull-down load to GND; V_{CC1} = 5.0 V		100	250	ns
t_{CSNQTL}	DO disable from low level to tristate	C_{DO} = 100 pF; I_{DO} = 4 mA; pull-up load to V_{CC}; V_{CC1} = 5.0 V		380	450	ns
t_{CSNQTH}	DO disable from high level to tristate	C_{DO} = 100 pF, I_{DO} = -4 mA; pull-down load to GND; V_{CC1} = 5.0 V		380	450	ns
t_{CLKQV}	CLK falling until DO valid	V_{DO} < 0.3 V_{CC} or V_{DO} > 0.7 V_{CC}; C_{DO} = 5 pF; V_{CC1} = 5.0 V				ns
		V_{DO} < 0.3 V_{CC} or V_{DO} > 0.7 V_{CC}; C_{DO} = 100 pF; V_{CC1} = 5.0 V				ns
t_{SCSN}	CSN setup time, CSN low before rising edge of CLK	V_{CC1} = 5.0 V	400			ns
t_{SDI}	DI setup time, DI stable before rising edge of CLK	V_{CC1} = 5.0 V	200			ns
t_{HCLK}	minimum CLK high time	V_{CC1} = 5.0 V	115			ns
t_{LCLK}	minimum CLK low time	V_{CC1} = 5.0 V	115			ns
t_{HCSN}	minimum CSN high time	V_{CC1} = 5.0 V	4			µs
t_{SCLK}	CLK setup time before CSN rising	V_{CC1} = 5.0 V	400			ns
$t_{r\ DO}$	DO rise time	C_{DO} = 100 pF; V_{CC1} = 5.0 V		80	140	ns
$t_{f\ DO}$	DO fall time	C_{DO} = 100 pF; V_{CC1} = 5.0 V		50	100	ns
$t_{r\ in}$	rise time of input signal DI, CLK, CSN	V_{CC1} = 5.0 V			100	ns
$t_{f\ in}$	fall time of input signal DI, CLK, CSN	V_{CC1} = 5.0 V			100	ns

Figure 29. SPI timing parameters

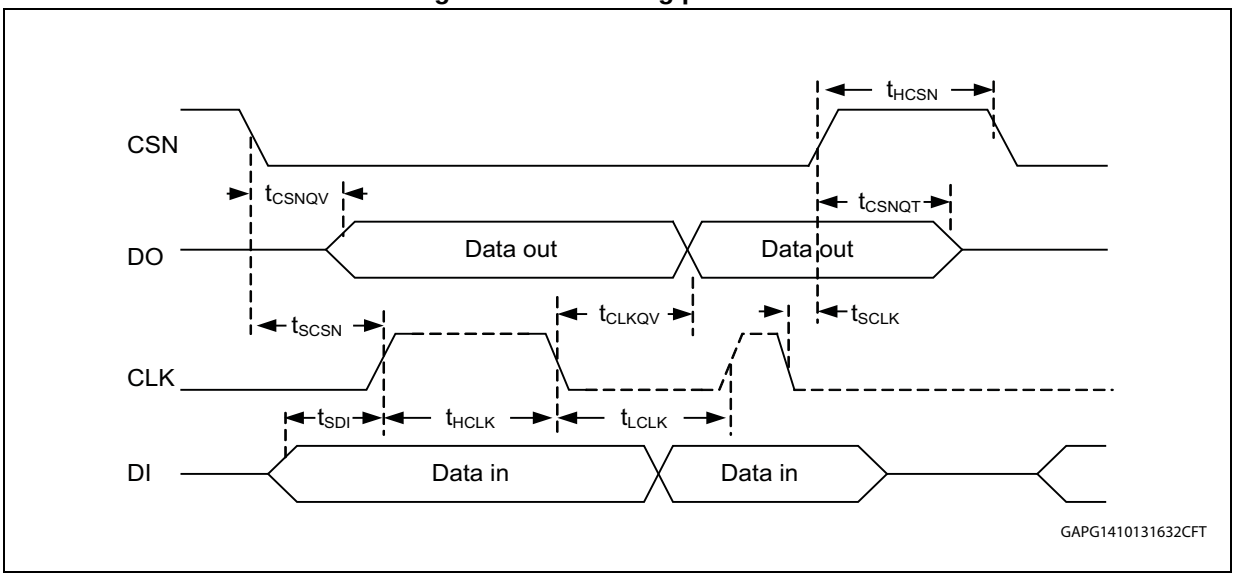


Figure 30. SPI input and output timing parameters

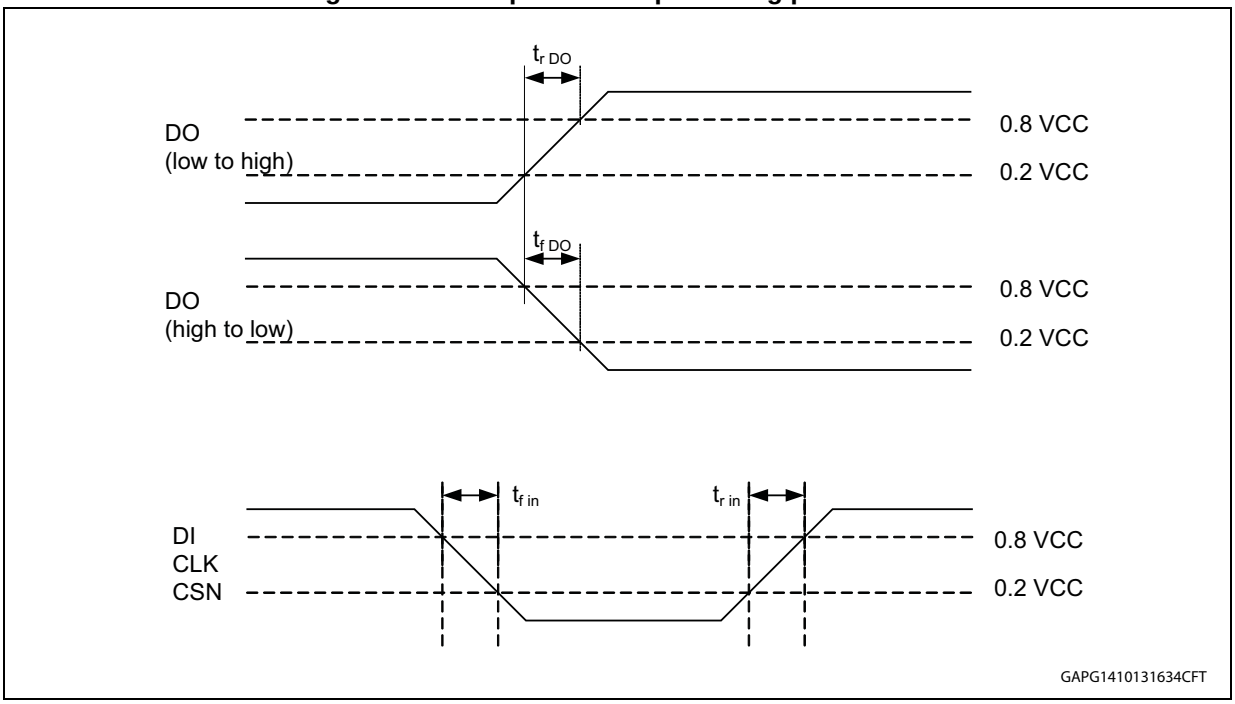
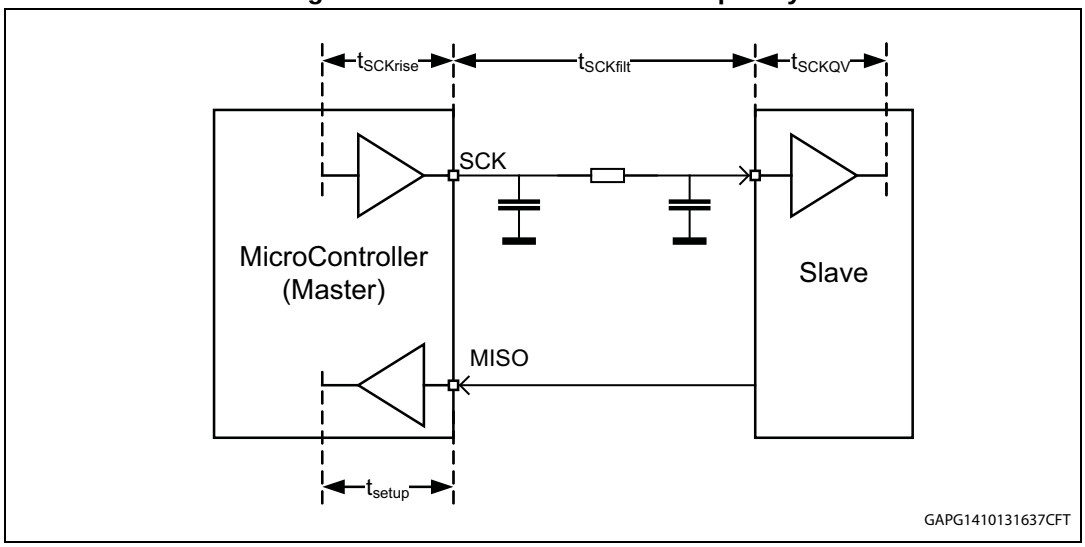


Figure 31. SPI maximum clock frequency



The maximum SPI clock frequency can be calculated as follows (see *Figure 31*):

$t_{CLKQV}(total) = t_{CLKrise}(uC) + t_{CLKfilt}(PCB) + t_{CLKQV}(slave) + t_{setup}(uC)$

$f_{CLK}(max) < ½ \times t_{CLKQV}(total)$

Example:

$t_{CLKQV} = 25\ ns + 100\ ns + 250\ ns + 25\ ns = 400\ ns$

$f_{CLK}(max) < 1.25\ MHz$

Figure 32. NRES pin open drain structure

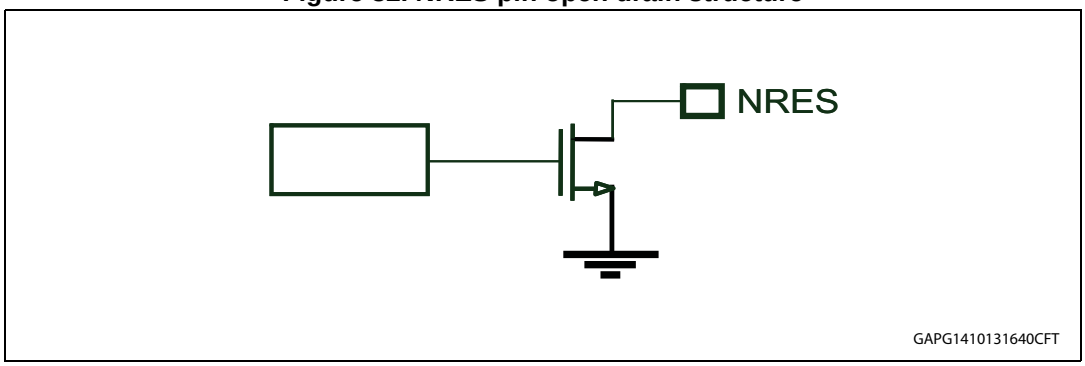
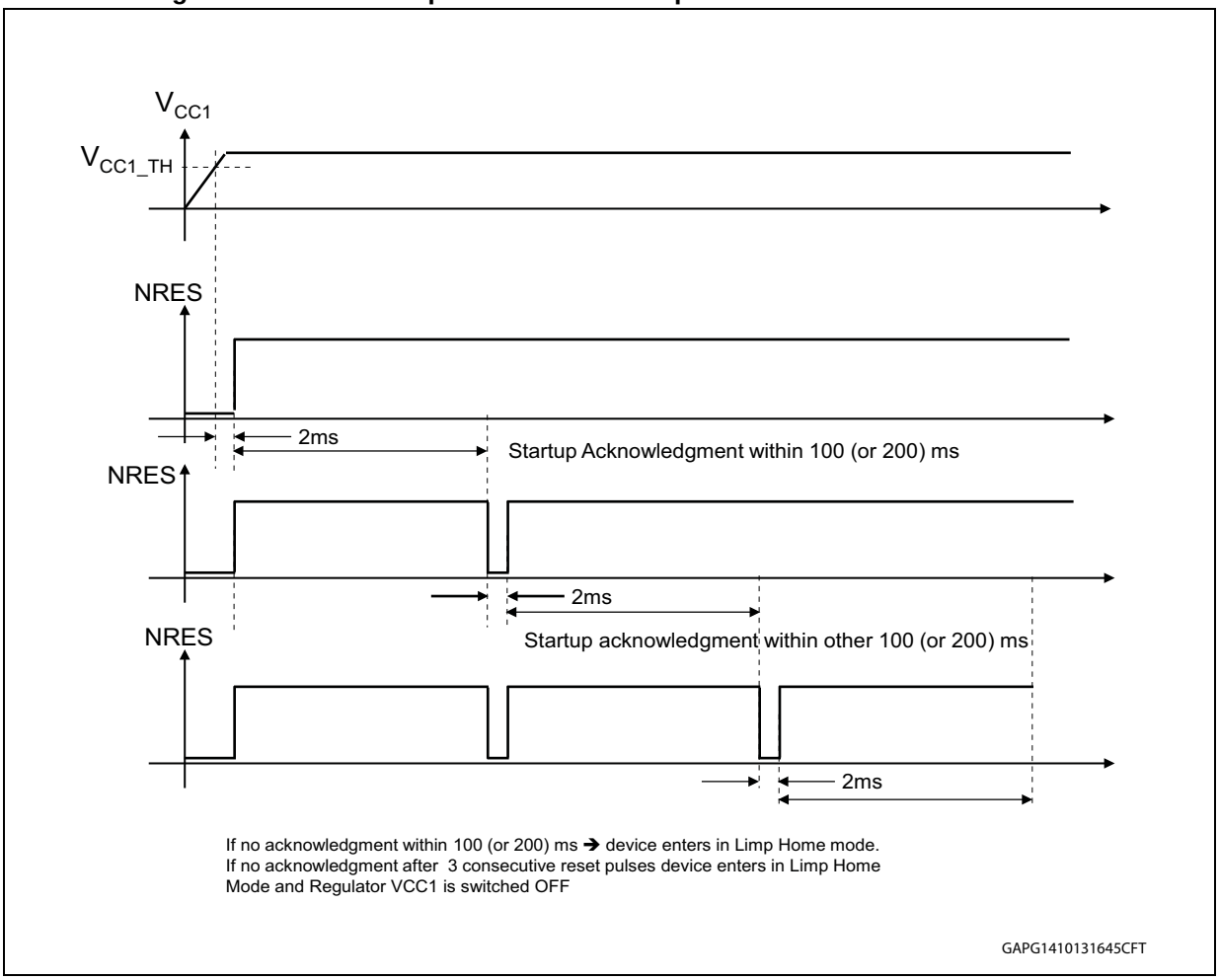


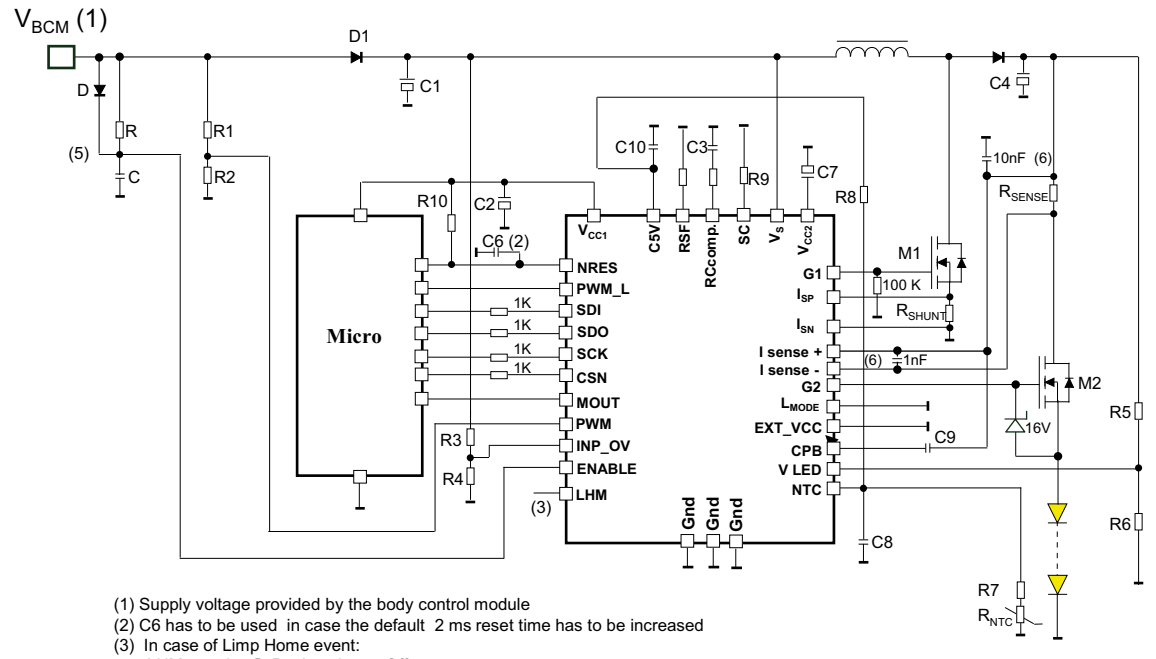
Figure 33. Handshake procedure at start up with microcontroller on board



7 Application circuits

Typical application circuits are shown on the following *Figure 34*, *Figure 35* and *Figure 36*. *Figure 37* shows the case of standalone application. *Figure 38* shows an example for the boost converter topology which uses an external Mosfet M3, for provide reverse battery protection, maintaining at same time a very low drop voltage in the normal functioning, but achieving low dissipation and high efficiency, in case of high power applications (LED headlamps).

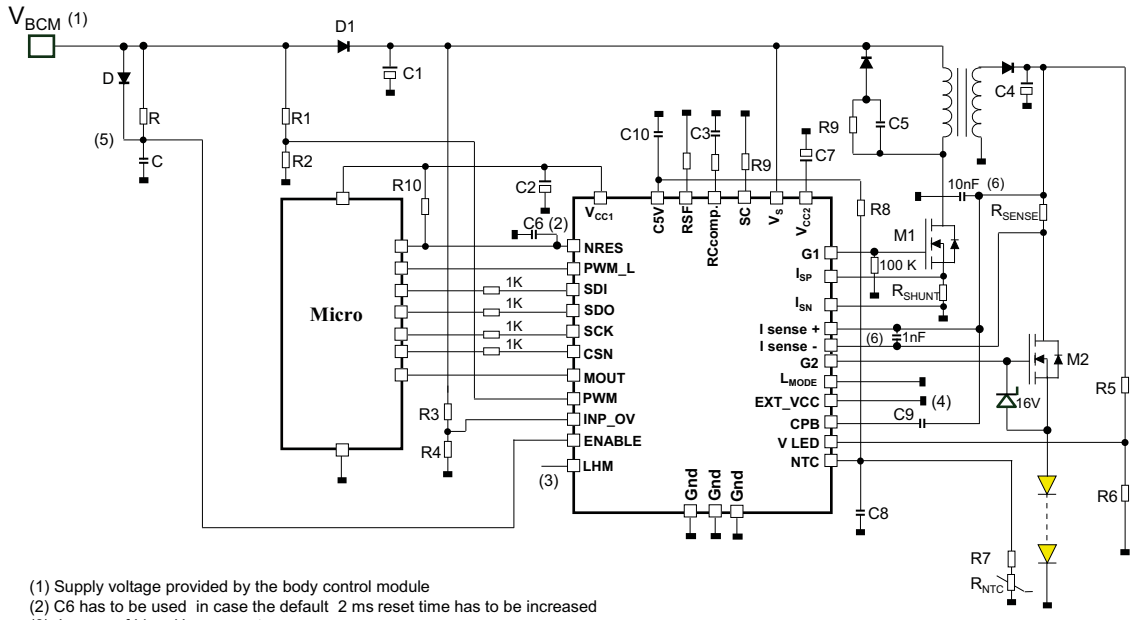
Figure 34. Boost application circuit



(1) Supply voltage provided by the body control module
(2) C6 has to be used in case the default 2 ms reset time has to be increased
(3) In case of Limp Home event:
LHM = gnd ➔ Device always Off
LHM = Open or High ➔ Device always ON
(4) EXT_VCC: Connect this pin to gnd if the uP is supplied by V_{CC1} pin. If the uP is externally supplied by an external 5V supply, connect this pin to the uP external supply
(5) R/C components have to be chosen in order to don't reset the device, during PWM operated by the BCM Voltage
(6) Optional components for noisy filtering

GAPG1410131657CFT

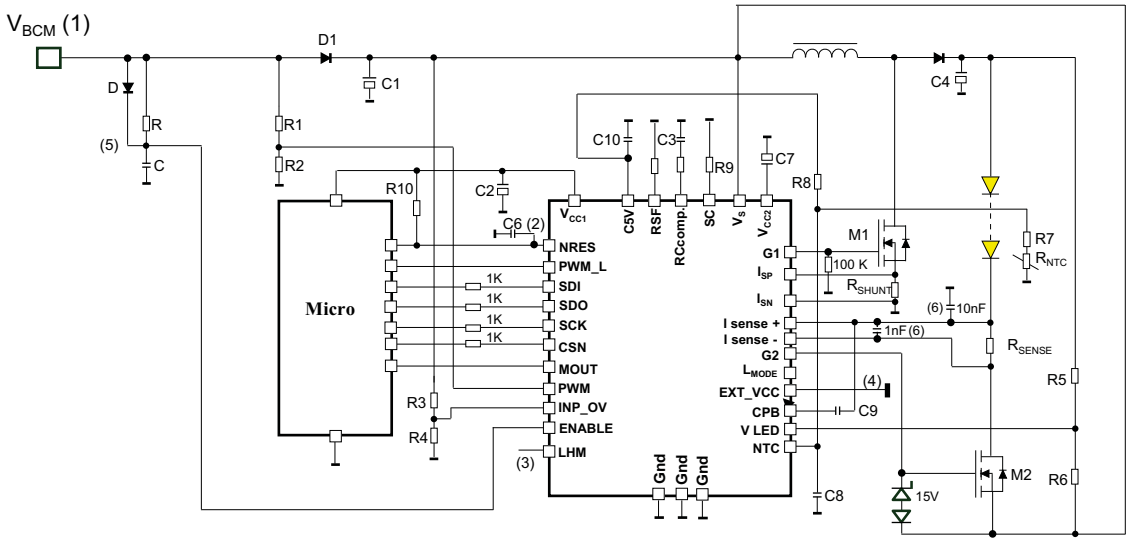
Figure 35. Fly back application circuit



(1) Supply voltage provided by the body control module
(2) C6 has to be used in case the default 2 ms reset time has to be increased
(3) In case of Limp Home event:
LHM = gnd ➔ Device always Off
LHM = Open or High ➔ Device always ON
(4) EXT_VCC: Connect this pin to gnd if the uP is supplied by V_{CC1} pin. If the uP is externally supplied by an external 5V supply, connect this pin to the uP external supply
(5) R/C components have to be chosen in order to don't reset the device, during PWM operated by the BCM Voltage
(6) Optional components for noisy filtering

GAPG1410131703CFT

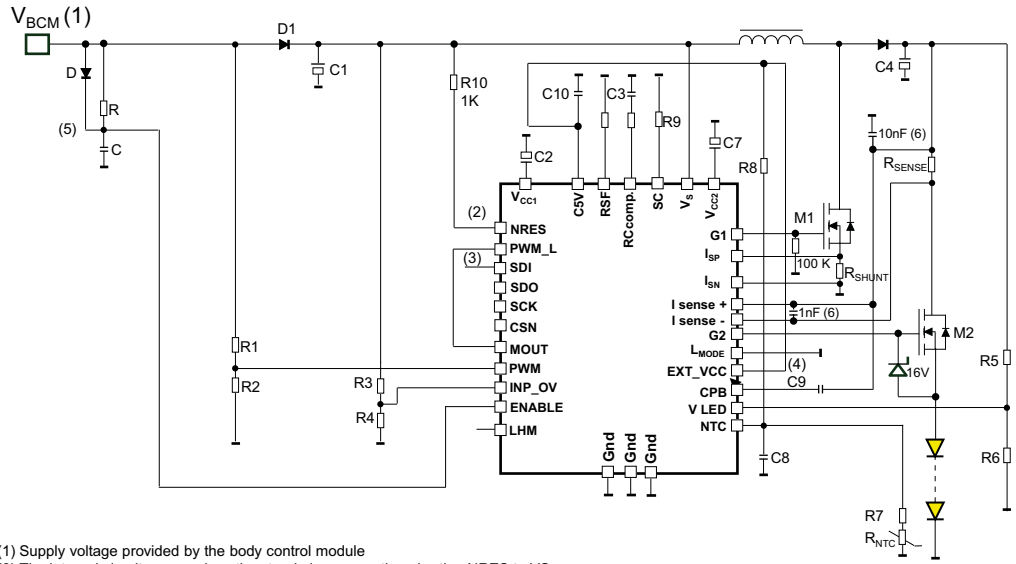
Figure 36. Buck-boost application circuit



(1) Supply voltage provided by the body control module
(2) C6 has to be used in case the default 2 ms reset time has to be increased
(3) In case of Limp Home event:
LHM = gnd ➔ Device always Off
LHM = Open or High ➔ Device always ON
(4) EXT_VCC: Connect this pin to gnd if the uP is supplied by V_{CC1} pin. If the uP is externally supplied by an external 5V supply, connect this pin to the uP external supply
(5) R/C components have to be chosen in order to don't reset the device, during PWM operated by the BCM Voltage
(6) Optional components for noisy filtering

GAPG1410131707CFT

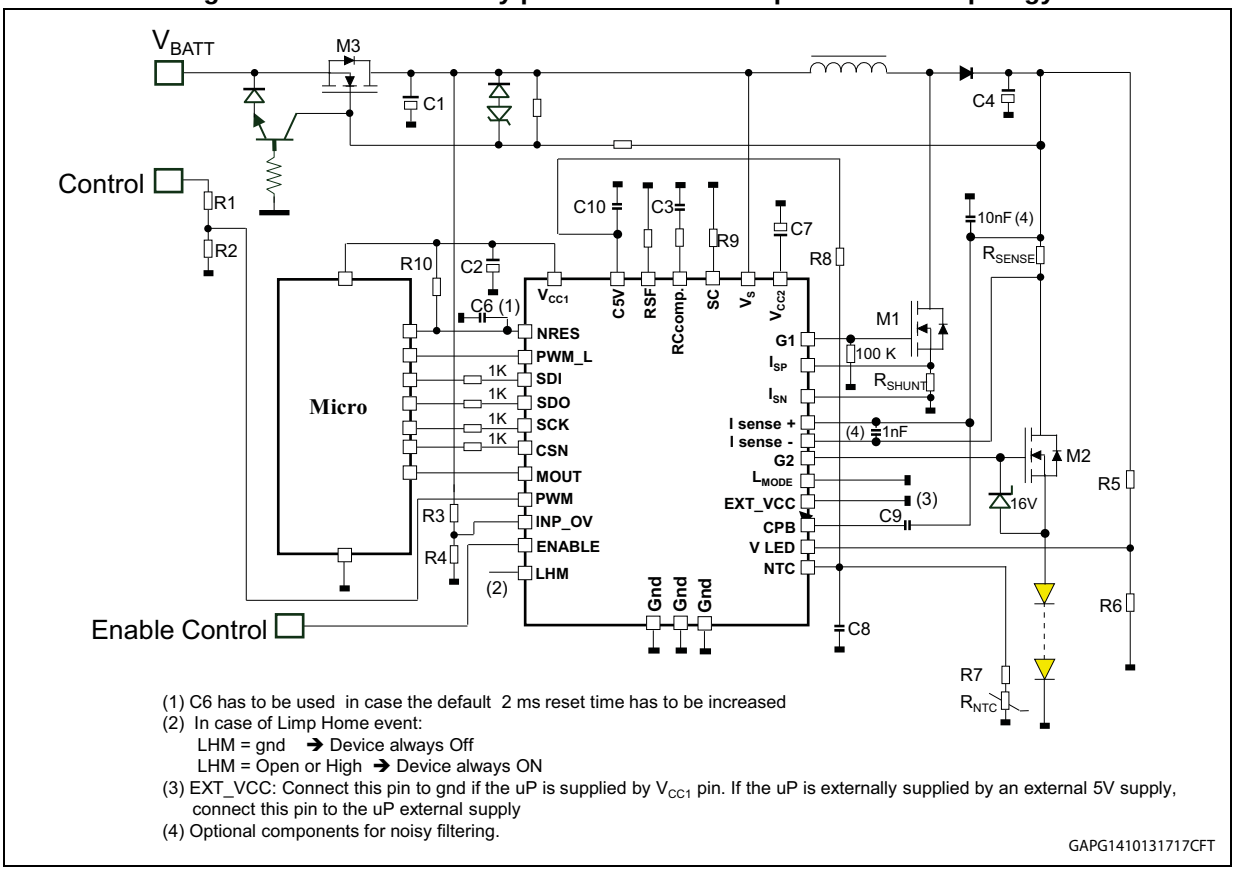
Figure 37. Stand alone application example for boost topology



(1) Supply voltage provided by the body control module
(2) The internal circuitry recognizes the stand alone operation shorting NRES to VS;
(3) Connect this pin to 5V for enabling Dither Effect
(4) EXT_VCC: In stand alone is suggested to connect this pin to C5V
(5) R/C components have to be chosen in order to don't reset the device, during PWM operated by the BCM Voltage
(6) Optional components for noisy filtering

GAPG1410131712CFT

Figure 38. Reverse battery protection: an example for boost topology

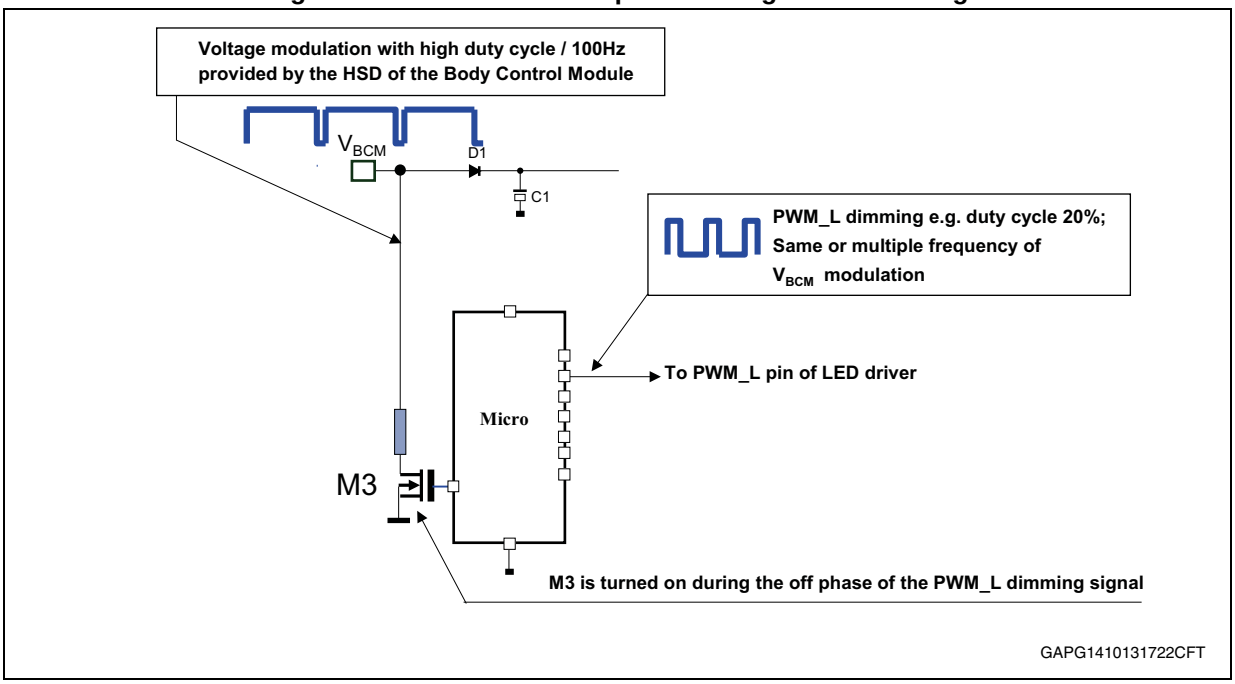


(1) C6 has to be used in case the default 2 ms reset time has to be increased
(2) In case of Limp Home event:
LHM = gnd ➔ Device always Off
LHM = Open or High ➔ Device always ON
(3) EXT_VCC: Connect this pin to gnd if the uP is supplied by V_{CC1} pin. If the uP is externally supplied by an external 5V supply, connect this pin to the uP external supply
(4) Optional components for noisy filtering.

GAPG1410131717CFT

If the DRL module is supplied by a high side driver (HSD) of the body control module (BCM), a minimum current consumption is requested during the off phase of the PWM dimming, so that the HSD of the BCM do not detect a wrong open load condition. This is in charge of the µP which has to draw this “minimum current consumption”, from the supply line (see *Figure 39*).

Figure 39. External MOS required during PWM dimming



8 Package information

8.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.2 LQFP32™ package information

Figure 40. LQFP32™ package dimensions

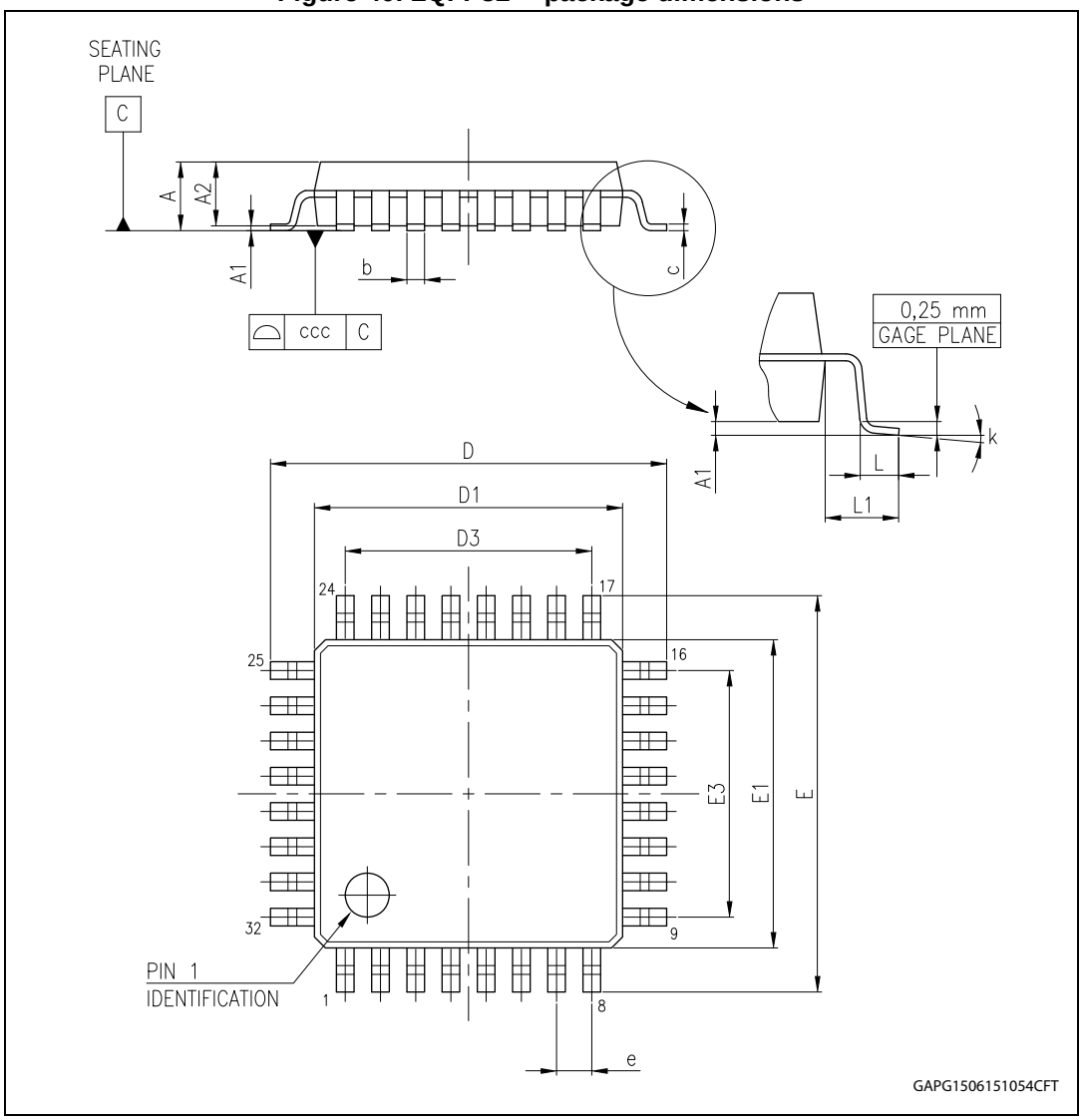


Table 35. LQFP32™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.6
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
D3		5.60	
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
E3		5.60	
L	0.45	0.60	0.75
L1		1.00	
K	0°	3.5°	7°
ccc			0.10

9 Order codes

Table 36. Device summary

Package	Order code
	Tube
LQFP32	L99LD01

10 Revision history

Table 37. Document revision history

Date	Revision	Changes
19-Jun-2014	1	Initial release.
15-Jun-2015	2	Updated *Description* *Table 15: Absolute maximum ratings*: – V_{G1}, V_{G2}, V_{CPB}, $V_{ISENSE-}$: updated values *Table 16: Thermal data*: – $R_{Thj-case}$: updated values *Table 17: VS and V_{CC1} pin characteristics*: – t_{VSM}, t_{V1F}, t_{V1OT}: updated values – V_{CC1_DROP}: updated description – $t_{LMODERR}$, t_{OC}, t_{LEDOV}, t_{WD1}, t_{WD2}: added parameters *Table 19: NRES and LMODE pin characteristics*: – t_{RR}, t_{FS}, t_{RD}: updated values *Table 21: G2 pin characteristics (driver2)*: – V_{G2_H}: updated values *Table 22: Converter oscillator and RSF pin characteristics*: – F_O: updated values – F_{O_S}: updated test conditions and values – Renamed “Duty cycle” symbol in “Duty cycle max”: updated test conditions and values – Renamed “T_{ON_MIN}” symbol in “Duty cycle min”: updated test conditions and values *Table 24: ISENSE+, ISENSE- pin, and O.T.A. characteristics*: – $V_{ISENSE+IR}$, $V_{ISENSE-IR}$: removed parameters – $V_{ISENSE+}$, $V_{ISENSE-}$, $(V_{ISENSE+} - V_{ISENSE-})_TH$, $V_{SENSE_MAX_1}$, V_{LREF_16}: updated values *Table 25: SC pin characteristics*: – V_{SC_low}, V_{SC_HIGH}: updated test conditions and values *Table 26: VLED pin characteristics*: – OV_TH1_VS, OV_TH2_VS: updated test conditions and values Updated *Chapter 8: Package information*
25-Jun-2015	3	*Table 32: SPI DC characteristics*: – $I_{CLK\ in}$, $I_{DI\ in}$: updated maximum value

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved