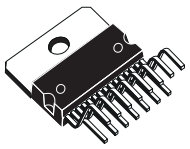
L9947

QUAD HALF-BRIDGE AND SINGLE HIGH-SIDE DRIVER

- LOW CONSUMPTION IN STANDBY MODE (<100µA AT ROM TEMP; < 150µA AT 130°C)
- TWO HALF BRIDGES FOR 3A LOAD (R_{DSON} = 0.25Ω TYP; T_j = 25°C)
- TWO HALF BRIDGES FOR 0.5A LOAD (R_{DSON} = 2.5Ω TYP; T_j = 25°C)
- HIGH SIDE DRIVER FOR 2.5A LOAD (R_{DSON} = 0.45Ω TYP; T_j = 25°C)
- DIRECT CONTROLLED BY µC (MULTIPLEX SYSTEM)
- OUTPUT HIGH/LOW LEVEL DIAGNOSTIC
- OVERCURRENT SWITCH OFF AND DIAGNOSTIC
- OVERTEMPERATURE DIAGNOSTIC BEFORE SWITCH OFF
- OPEN LOAD DIAGNOSTIC



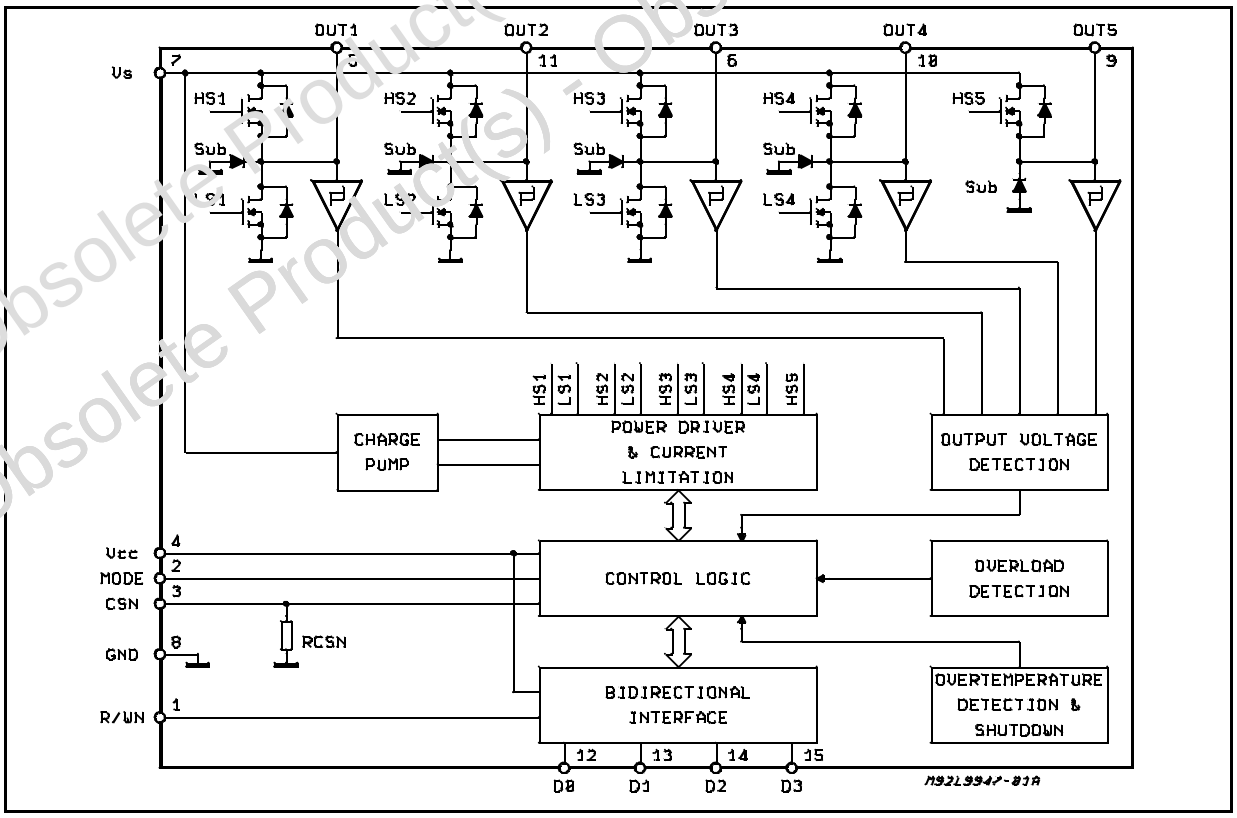
Multiwatt 15

ORDERING NUMBER: L9947S

DESCRIPTION

The L9947 is a bus controlled power interface intended for automotive applications realized in multipower BCD50II technology. Up to three DC motors and one grounded resistive load can be driven with its four half-bridge and one high-side driver power outputs. The microcomputer compatible bidirectional parallel bus allows several interfaces connected on the same bus (multiplex system). The full diagnostic information is available on the bus.

BLOCK DIAGRAM



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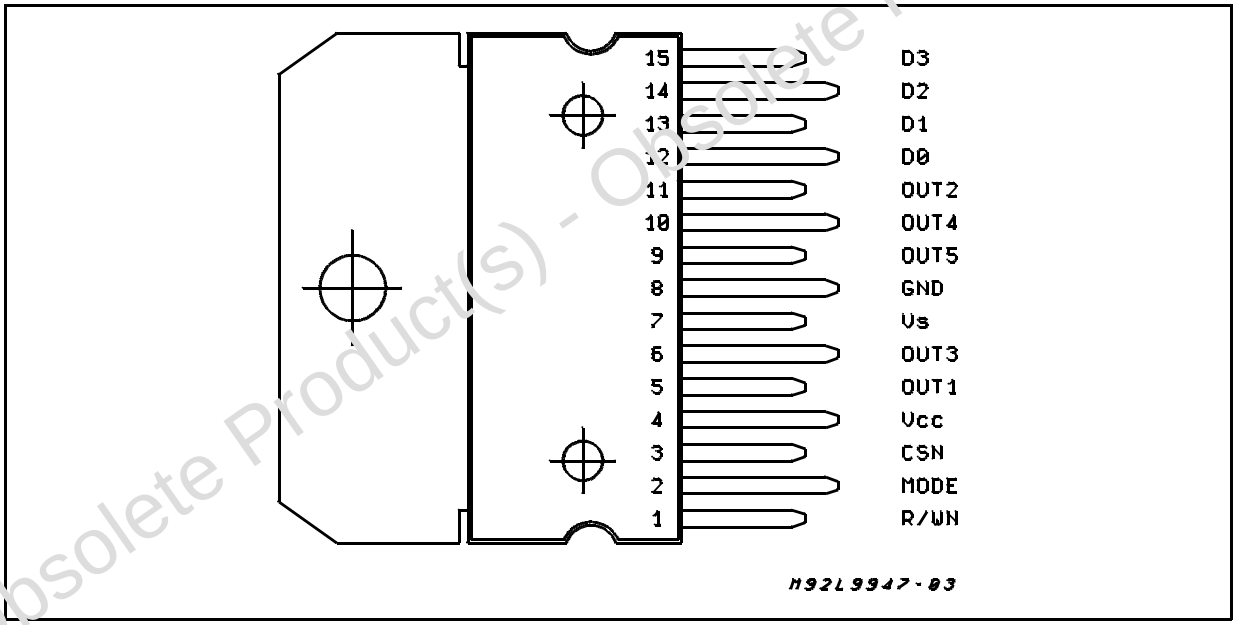
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	26	V
	Single Pulse t_{max} < 400ms	40	V
I_S	Negative Supply Current	-9	A
V_{CC}	Stabilized Supply Voltage	-0.3 to 6V	V
V_{CSN}, $V_{R/WN}$ V_{MODE}	Digital Input Voltage	-0.3 to V_{CC}+0.3	V
$V_{D0\text{ -}D3}$	Digital Input/ Output Voltage	-0.3 to V_{CC}+0.3	V
$I_{OUT1\text{ - }OUT5}$	Output Current Power	internal limited	
T_j	Operating Junction Temperature	-40 to 150	°C
$T_{j\text{ - }SD}$	Thermal Shutdown Junction Temperature	min 150	°C
$T_{j\text{ - }HYS}$	Thermal Junction Temperature Hysteresis	20	K

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient P_{tot} = 25W; free air; DC	38	°C/W
$Z_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient still air; single pulse tp = 20s	10	°C/W

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ELECTRICAL CHARACTERISTICS (V_S = 8 to 16V; V_{CC} = 4.5 to 5.5V; T_j = -40 to 150°C;unless otherwise specified; the voltage are refered to GND and currents are assumed positive, when the current flows into the pin.)

SUPPLY:

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC}	DC Supply Current	V_S = 16V; V_{CC} = 5.5V; (status 8)		5		mA
I_S	DC Supply Current	V_S = 16V; V_{CC} = 5.5V; (status 8)		10		mA
$I_{CC + IS}$	Sum Supply Current (1)	I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0; Standby (status 2) V_S = 14V; V_{CC} = 5.5V; T_j = -40 to 25°C			100	µA
		I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0; Standby (status 2) V_S = 14V; V_{CC} = 5.5V; T_j > 25°C			150	µA
		V_S < 14V; V_{CC} = 5.5V; I_{OUT} = 0; (status 17);			3	mA
V_{SOVT}	Overvoltage Shutdown Threshold		17		25	V

CONTROL INPUTS: CNS, R/WN, MODE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INL}	Input Low Level	V_{CC} = 5V			1.5	V
V_{INH}	Input High Level	V_{CC} = 5V	3.5			V
V_{INHyst}	Input Hysteresis	V_{CC} = 5V;	0.5			V
I_{INL}	Input Current Low	V_{CC} = 5V; V_{IN} = 0	-10		10	µA
I_{INH}	Input Current High (with exception of CSN Input)	V_{CC} = 5V; V_{IN} = 5V	-10		10	µA
R_{CSN}	Input Resistance to GND (pull down at CSN pin)		20			KΩ

DATA INPUT: D0 - D3

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DINL}	Input Low Level	V_{CC} = 5V; MODE = 0			1.5	V
V_{DINH}	Input High Level	V_{CC} = 5V; MODE = 0	3.5			V
$V_{DINHyst}$	Input Hysteresis	V_{CC} = 5V; MODE = 0	0.5			V
I_{DINL}	Input Current Low	V_{CC} = 5V; V_{IN} = 0	-10		10	µA
I_{DINH}	Input Current High	V_{CC} = 5V; V_{IN} = 5V	-10		10	µA

DATA OUTPUT: D0 - D3

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output Low Level	V_{CC} = 5V; I_D = 0.5mA; MODE = 1			0.6	V
V_{DINH}	Input High Level	V_{CC} = 5V; I_D = 0.5mA; MODE = 1	4			V

Note (1): Off-State Leakage Current of each single output ≤25µA, T_j = -40 to 150°C.

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ELECTRICAL CHARACTERISTICS (continued)
OUTPUTS:

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{ON\ OUT1}$	On Resistance to Supply or GND	V_S = 8V; T_j = 125°C; I_{OUT} = ±0.5A			6	Ω
		V_S ≥10V; T_j = 125°C; I_{OUT} = ± 0.5A			3.95	Ω
$R_{ON\ OUT2}$	On Resistance to Supply or GND	V_S = 8V; T_j = 125°C; I_{OUT} = ±0.5A			6	Ω
		V_S ≥ 10V; T_j = 125°C; I_{OUT} = ± 0.5A			3.95	Ω
$R_{ON\ OUT3}$	On Resistance to Supply or GND	V_S = 8V; T_j = 125°C; I_{OUT} = ±2.5A			600	mΩ
		V_S ≥ 10V; T_j = 125°C; I_{OUT} = ± 2.5A			395	mΩ
$R_{ON\ OUT4}$	On Resistance to Supply or GND	V_S = 8V; T_j = 125°C; I_{OUT} = ±2.5A			600	mΩ
		V_S ≥ 10V; T_j = 125°C; I_{OUT} = ± 2.5A			395	mΩ
$R_{ON\ OUT5}$	On Resistance to Supply	V_S = 8V; T_j = 125°C; I_{OUT} = -2A			1.0	Ω
		V_S ≥ 10V; T_j = 125°C; I_{OUT} = -2A			0.7	Ω
$\|I_{OUT1}\|$	Output Current Limitation to Supply or GND	For the function of the short circuit current limitation see the functional description (pag....)	0.67		2	A
$\|I_{OUT2}\|$	Output Current Limitation to Supply or GND		0.67		2	A
$\|I_{OUT3}\|$	Output Current Limitation to Supply or GND		4		12	A
$\|I_{OUT4}\|$	Output Current Limitation to Supply or GND		4		12	A
$\|I_{OUT5}\|$	Output Current Limitation to GND		2.5		7.5	A
I_{OUT1}	Output Current	V_{OUT1}=2.5V; (status 18)	5		15	mA
I_{OUT2}	Output Current	V_{OUT2}=2.5V; (status 18)	5		15	mA
I_{OUT3}	Output Current	V_{OUT3}=2.5V; (status 18)	5		15	mA
I_{OUT4}	Output Current	V_{OUT4}=2.5V; (status 17)	80		500	mA
		V_{OUT4}=V_S -2.5V; (status 16 or 18)	-80		-500	mA
I_{OUT5}	Output Current	V_{OUT5}=V_S -2.5V; (status 18)	-5		-15	mA
V_{OUT1-5}	Output Voltage Detection Thresholds	V_S=13V; (status 11) LOW HIGH HYSTERESIS	 4.9 7.5	 0.4 V_S 0.6 V_S 0.2 V_S	 5.5 8.1	 V V V
T_{JOT}	Overtemperature Detection Thresholds	status 12 - 15		130		°C
		steady state t >20ms	125		<T_{JSD}	°C
t_{ISC}	Overcurrent Switch off Time		50			µs
f_{OSC}	Internal Oscillator Frequency			250		KHz

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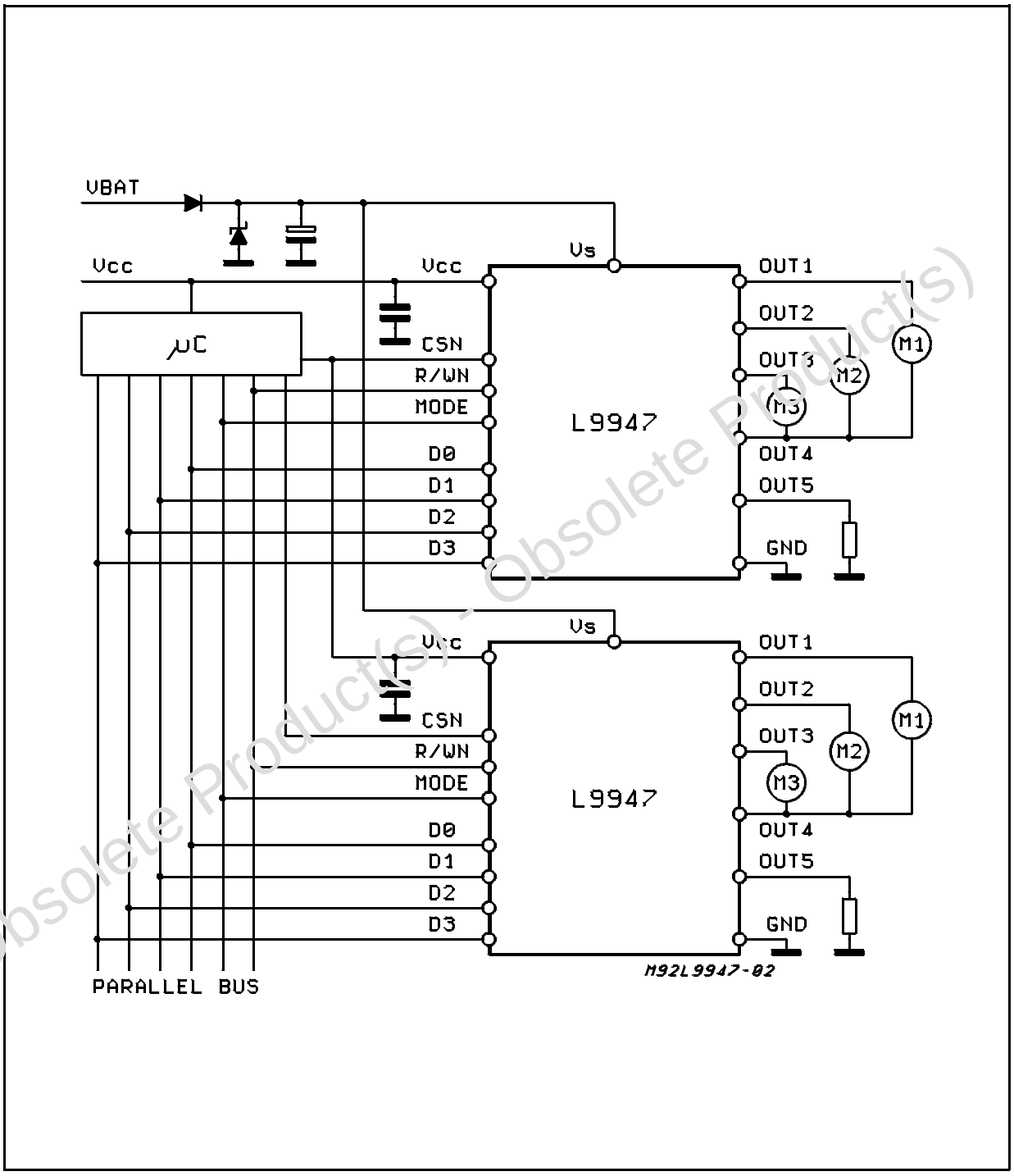
APPLICATION CIRCUIT DIAGRAM

Fogure 1: Recommended Application Circuit.



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FUNCTIONAL DESCRIPTION

The L9947 is a power interface circuit designed for a multiplex system controlled by a parallel µC bus. The bus consists of four bidirectional data wires D0 - D3 and three control wires read/write (R/WN), mode (MODE) and chip select (CSN). The device needs two supply voltages. The first voltage supplies the half bridges, high side driver and its driving part. The second one is a 5V stabilized supply. The function of the device in the typical operating modes is described in the following tables.

Output Activating/write Table 1

Status	CSN	R/WN	MODE	D0	D1	D2	D3	OUT1	OUT2	OUT3	OUT4	OUT5	FUNCTION
1	1	X	X	X	X	X	X	AB	AB	AB	AB	AB	Hold output behavious as programmed before
2	⎍	0	0	0	0	0	0	T	T	T	T	T	All Outputs, Standby mode
3	⎍	0	0	0	0	1	0	SRC	T	T	SNK	T	M1, right
4	⎍	0	0	1	1	0	0	SNK	T	T	SRC	T	M1, left
5	⎍	0	0	1	0	1	0	T	SRC	T	SNK	T	M2, right
6	⎍	0	0	0	1	0	0	T	SNK	T	SRC	T	M2, left
7	⎍	0	0	0	1	1	0	T	T	SRC	SNK	T	M3, right
8	⎍	0	0	1	0	0	0	T	T	SNK	SRC	T	M3, left
9	⎍	0	0	1	1	1	0	SNK	SNK	SNK	SNK	T	Braking
10	⎍	0	0	0	0	0	1	T	T	T	T	SRC	High side driver

Notes:
Where CSN = 0 the device is (for t ≤ 100µs) transparent, in this condition any change of Data D0 .... D3 will lead to the apprpriate output response.
Deselecting the circuit (CSN) the last programmed status will be stored

Diagnostic / read. Table 2:
In readout modes the port D0 .... D3 is acting as an output showing the conditions detected before.

Status	CSN	R/WN	MODE	D0	D1	D2	D3	Function
11	⎍	1	0	OUT1	OUT2	OUT3	OUT4	OUT1, OUT2, OUT3, OUT4;
12	⎍	1	1	0	0	OT	OUT5	• No failure, OT, OUT5;
13	⎍	1	1	1	0	OT	OUT5	• OVC1, OT, OUT5;
14	⎍	1	1	0	1	OT	OUT5	• OVC2, OT, OUT5;
15	⎍	1	1	1	1	OT	OUT5	OVV OT, OUT5; or OVV + OVC1 or OVV + OVC2

Diagnostic / write. Table 3:
Diagnostic modes are used to check the load status for broken or shorted wires.

Status	CSN	R/WN	MODE	D0	D1	D2	D3	OUT1	OUT2	OUT3	OUT4	OUT5	Function
16	⎍	0	1	0	1	0	X	T	T	T	140mA SRC	T	
17	⎍	0	1	1	0	0	X	T	T	T	140mA SNK	T	$I_s+I_{cc} \le 1mA$ for $I_{OUT4} = 0$
18	⎍	0	1	0	1	1	X	10mA SNK	10mA SNK	10mA SNK	140mA SRC	10mA SRC	

Standby and clear / write. Table 4:

Status	CSN	R/WN	MODE	D0	D1	D2	D3	OUT1	OUT2	OUT3	OUT4	OUT5	Function
19	⎍	0	0	1	1	1	1	T	T	T	T	T	Clear
20	0	X	X	X	X	X	X	T	T	T	T	T	Clear, Static CSN = 0 will force clear status and standby after 100µs without respect of data inputs

Symbols:
1: Logic High
0: Logic Low
T: Tristate
X: Don't care

AB: As before
⎍ Low pulse t < 100µs
SRC: Source
SNK: Sink
OT: Overtemperature

OVC1: Overcurrent 1
OVC2: Overcurrent 2
OVV: Overvoltage
OUTX:
- High if output voltage was >0.6V_s during test
- Low if output voltage was < 0.4V_s during test

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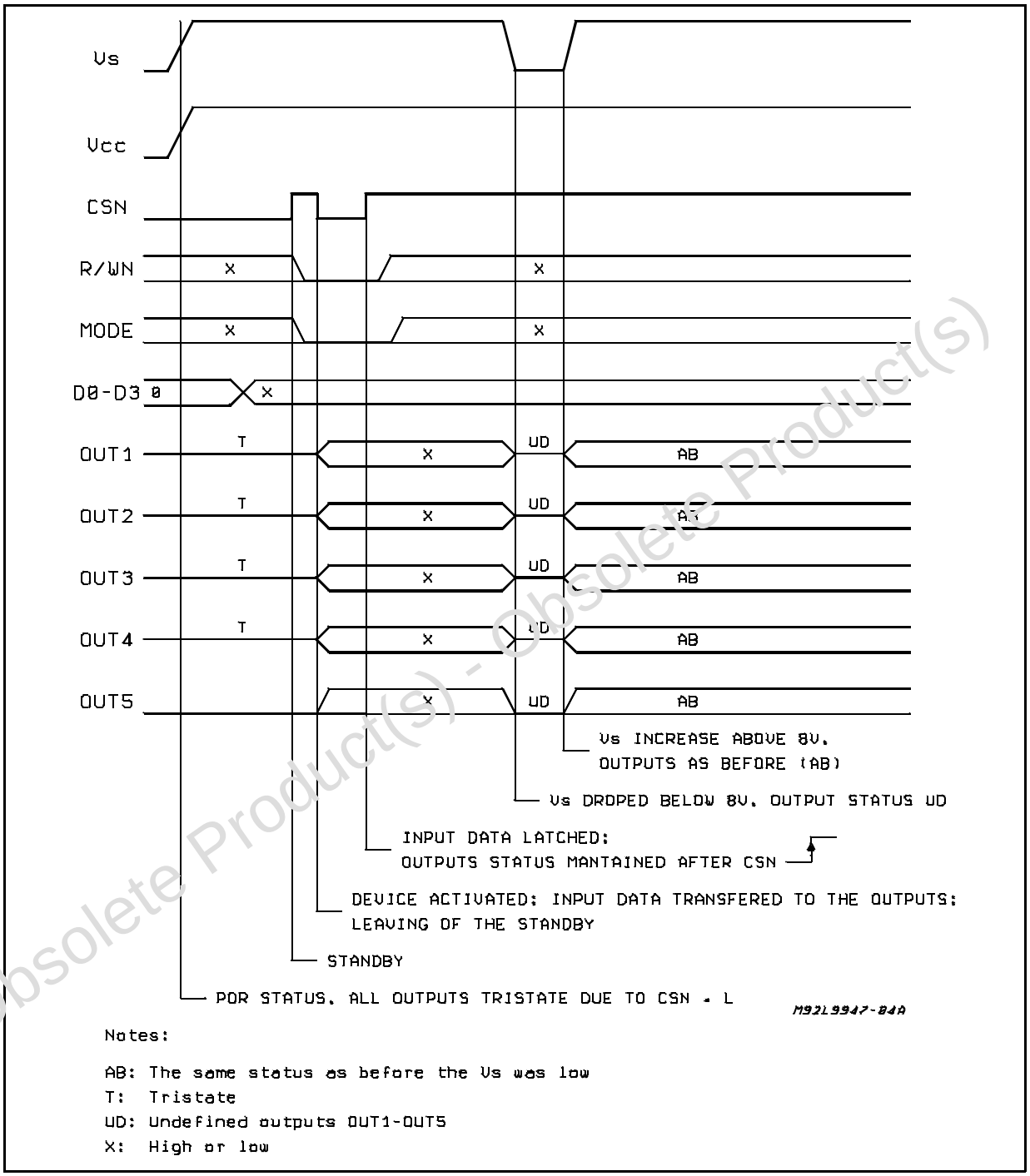
Figure 2: System Startup Sequence



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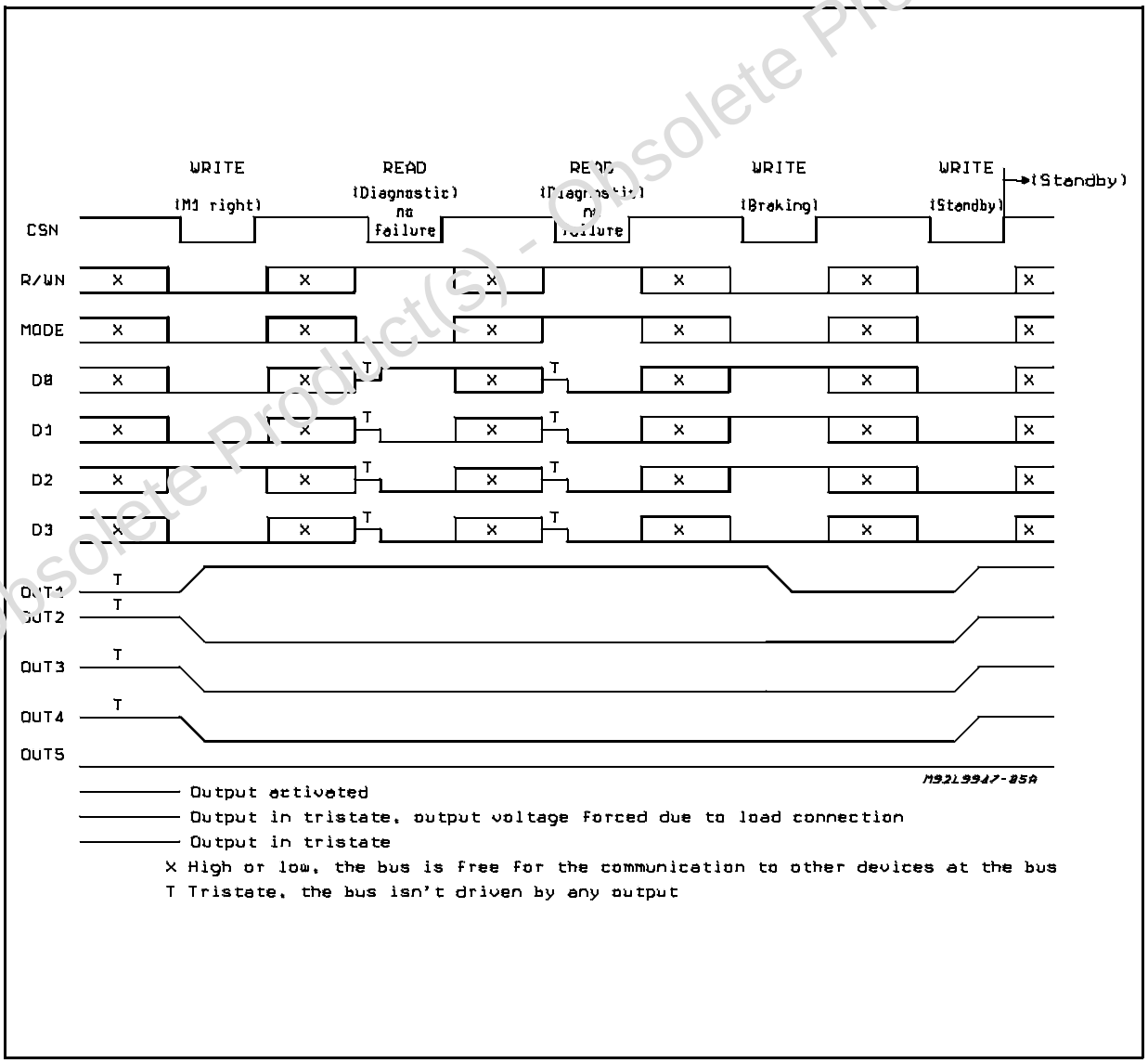
SYSTEM STARTUP (figure 2)

It is not mandatory that Vs is present before Vcc. With the presence of the Vcc the internal logic would be reseted and the system restarts under control of the inputs. If CSN = 0 for more than 100µs after the presence of Vcc the standby mode is activated. Standby is also activated when the CSN and VCC would be high at the same time. When CSN = 0 and Vcc goes up, the device is not controlled by the bus. The outputs remain in tristate but the current consumption is larger than 100µA. A high - low - signal at the CSN - wire is mandatory to control the outputs. There is no undervoltage detection level for the supply voltage VS implemented. The VCC should be supplied from the same voltage supply as the driver of the D0 -D3 pins (eg. µC).

DATA TRANSFER AND OUTPUTS ACTIVATING (Figure 3)
The half bridges of OUT1, OUT2 and OUT3 can be used with OUT4 to drive three bidirectional motors in full bridge configuration as shown in fig.1 Only one motor can be driven in the same time. The µC writes the corresponding word status 1 till 10 at the bus and latch it with a low pulse in the L9947. So the motor is activated. To stop the motor it is useful to insert a braking phase (status 9). In the braking condition there are all low side DMOS of the half bridges switched-on in this case the flyback currents flows through the low side switches instead of the intrinsic diodes of the half bridges. After that, the half bridges could be switched in tristate (T). The high side driver, OUT5 can be switched only when all the half bridges are in tristate status 10.
The µC works always as master and the L9947 Power Interface as slave. That means: the µC starts the communication between the Power Interface and itself with low transition at the CSN line. CSN = 0, R/WN= 0 the L9947 reads the data at the bus and execute the command as shown in tables 1,3,4 (write mode). The high slope of the CSN stores the last command and execute it further. All inputs are disabled if CSN= 1.
So the bus can be used for another device. With CSN = 0 and R/WN = 1 the L9947 writes the status of the diagnostic at the parallel bus until CSN becomes high (table 2; status µ + 15) (read mode). The power outputs maintain the same status as before.

Figure 3: Signal sequence for data transfer to switch M1 right, read the output status, brake the motor and activate the standby mode.



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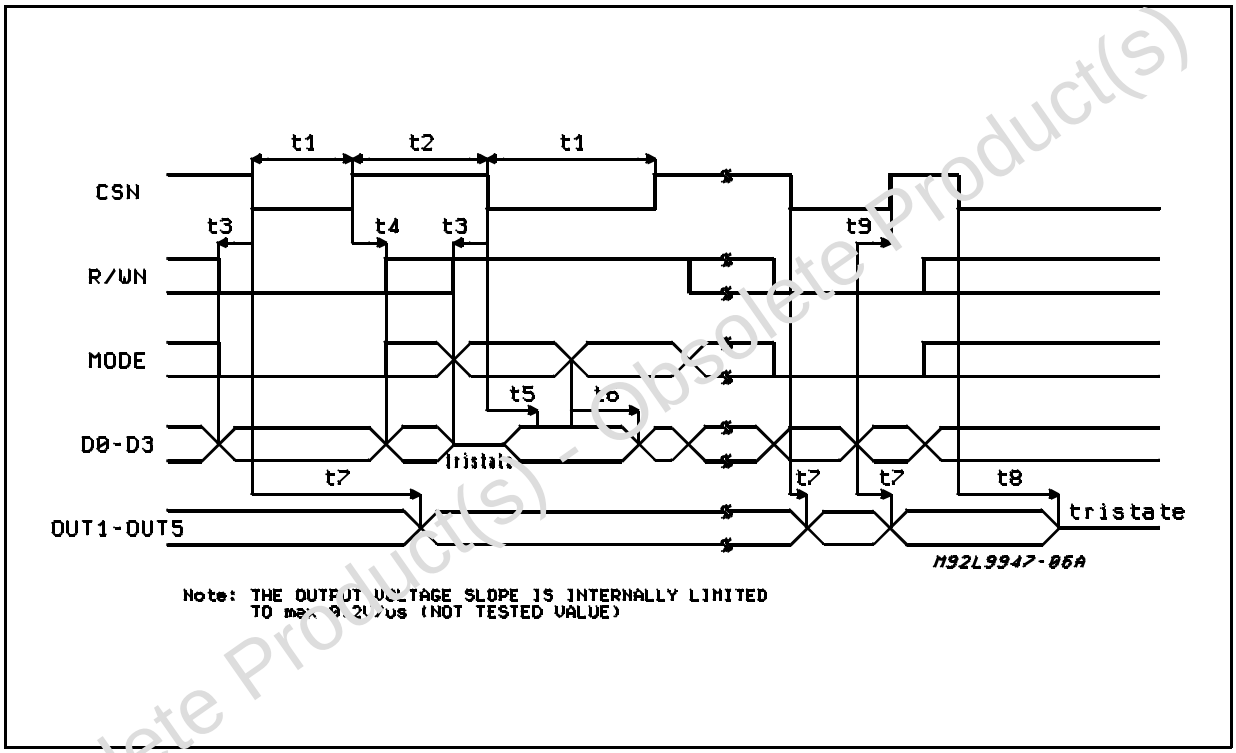
Bus Timing (figure 4)

The bus signal must be defined t_3 = 1µs before CSN goes low. It is allowed to change the level of R/WN during CSN = 0. The other signals could be changed. To store a command it is mandatory to fix the D0 - D3 and MODE signals t_9 = 1µs before the positive edge of CSN.

OVERCURRENT AT OUT1 - OUT5:
The output currents of OUT1 - OUT5 are internally limited. This is realized in the following way:

When the output current reaches a certain level (see pag...) the Gate - Source voltage will be clamped to a lower level. The output current is now limited and follows the output ID, UDS characteristic for this Gate - Source voltage. An internal timer starts when the output voltage drop (Drain - Source) increases above 0.4V_S.
After 100µs typ. the output is switched OFF and the corresponding overcurrent bit (OVC1 or OVC2) will be set. The outputs can be activated again with the next input data word.

Figure 4: Bus and Outputs Timing Diagram



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TIMING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Width of CSN Low	20		90*	µs
t_2	Width of CSN High	10			µs
t_3	Input Signals Before Negative Cdge of CSN	1			µs
t_4	Input Signals After Positive Edge of CSN	1			µs
t_5	Valid Diagnostic Data			10	µs
t_6	Valid Diagnostic Data			10	µs
t_7	Delay Time from Input to Power Output, VS = 13V			300	µs
t_8	CSN = Low Duration (Pulse Length) for CLEAR of latched Data	100			µs
t_9	Input Data Before Positive Edge of CSN Which Should be Latched	1			µs

t_1 and t_5 are derived from the internal oscillator frequency

t_7 varies with the supply voltage V_S, relating to the output voltage slope limitation

(*) for $t_1 \geq 100$µs the latched data will be reseted due to CLEAR (status 20)

Diagnostic (TABLE 2; STATUS 11 - 15):

The diagnostic delivers the information of the output voltage status (high or low) at the outputs OUT1 - OUT5, overcurrent, overvoltage shutdown and over temperature. The output voltage detection is done by hysteresis comparators with thresholds at 0.4VS and 0.6 VS. The overcurrent (OVC) information is latched till a new or repeated write command was received. The OVC1 is set to high with the overcurrent condition at any of the half-bridge outputs. OVC2 error bit will be set with the overcurrent condition at OUT5. The overvoltage (OVV) is high till the supply voltage V_S exceeds the overvoltage threshold of 20V typ.
The overtemperature (OT) is high if the junction temperature is less than typ. 30 Kevin below the thermal shutdown junction temperature (T_{JSD}).

Detection of Load Interruption
(TABLE 3):

The outputs OUT1 - OUT4 are connected by the motors in the application. The output OUT4 can be switched as current source or sink with typ. 140mA current capability (status 16 + 17). The sum of current consumption is <1mA if the output current I_{OUT4} = 0 (status 17). The diagnostic of the output voltage delivers the information if one or more of the half bridges is shorted to V_S or GND or the motor connections are interrupted. In status 18 the outputs OUT1 - OUT3 are switched as current sinks (typ. 10mA), OUt4 and OUt5 as current sources (OUT4 140mA, OUT5 10mA). With this current the influence of leakage currents and oxidized contacts is eliminated.

Standby (TABLE!; STATUS 2):

The L9947 is set in standby mode with the positive edge of CSN when all other inputs are low. All latched data will be cleared and the inputs and outputs are in tristate.
The total current consumption is less than 100µA. CSN=0 quits the standby. All latched data are cleared.

Clear (TABLE 4: STATUS 20):

If the chip select is low for ore than T_{CLR} = 100µs, the internal latched data will be cleared and the outputs become tristate. Repetitive high low edges activate the inputs again. Also a broken CSN-wire activates this clear function due to the internal pull down resistor at CSN input. After a clear, the L9947 goes in standby and can be wake up with a negative edge of CSN.

Thermal Shutdown:

When the junction temperature increases above T_{JSD} the power DMOS transistors are switched off until the junction temperature drops below the value T_{JSD} - T_{JHYST}.

Clamp Current of The Power Outputs:

For output voltages 10V and larger a clamp current of appr. 50µA will flow in the power outputs due to the internal gate-source voltage limitation, when the device is not in standby.

Overvoltage Shutdown:

When the supply voltage VS exceeds the overvoltage threshold V_{SQVT}, typ. 20V the outputs OUT1 - OUT5 go in tristate condition. If the supply voltage goes under the overvoltage shutdown treshold, the status is the same as before the overvoltage condition occurred.

Undervoltage:

In the voltage range 2V <V_{CC} < 4V the internal logic is reseted and all outputs go in tristate. Also ground spikes on the V_{CC} reset the logic. After an internal reset of the logic, the L9947 is controlled again by the inputs.

Ground Interrupt:

The L9947 is protected against interruption. The output OUt5 switches off at ground interruption. The outputs OUT1 - OUt4 are driven in full bridge configuration as shown in the application. There is no path through the load or direct to another ground. Thus, the device protected.

V_{CC} **Interruption**

If the supply voltage V_S is present and V_{CC} is interrupted or not supplied, than two cases can be distinguished:

1 The data pins D0 - D3 are not driven by the µC or they are low. So the outputs OUT1 - OUT5 and D0 - D3 are in tristate.
2 One of the pins D0 - D3 is driven high the µC. This pin supplies the VCC pin by the drain-bulk-diode of the p-channel mos (fig.5). Depending of the CSN, R/WN and MODE inputs some undesiderable functions can occur.

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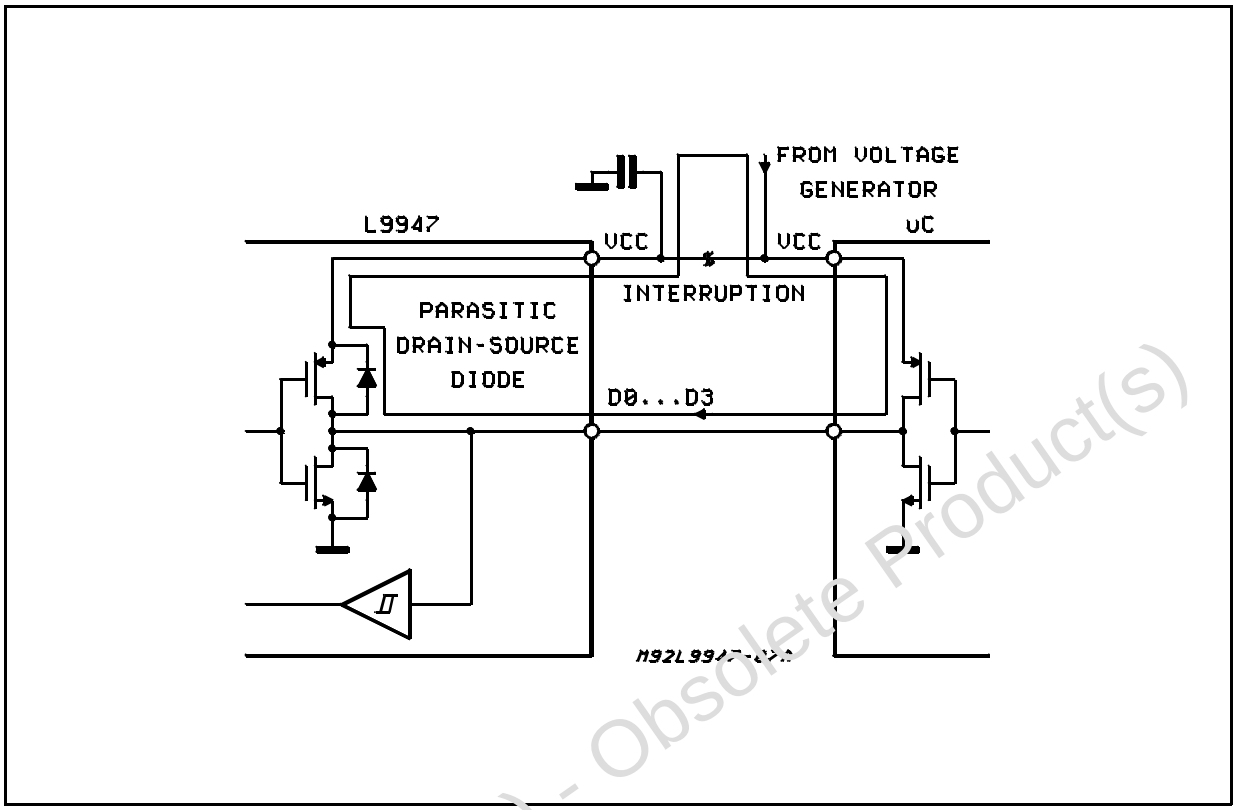
Figure 5: Supply Current Path at V_{CC} Interruption



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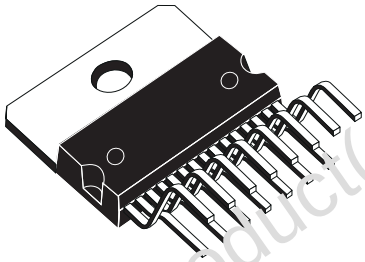
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



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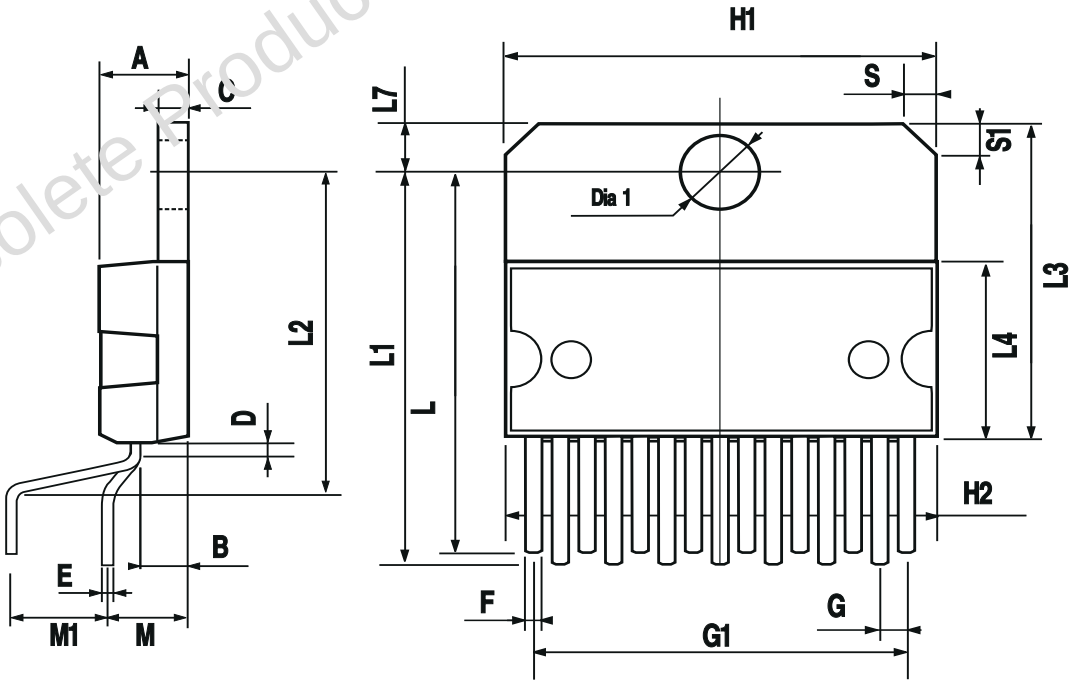

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