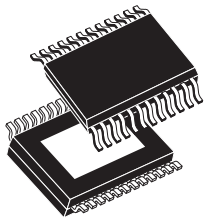
L9942

Integrated stepper motor driver for bipolar stepper motors with microstepping and programmable current profile

PRELIMINARY DATA

Features

- Two full bridges for max. 1.3 A load (R_{DSON} = 500 mΩ)
- Programmable current waveform with look-up table: 9 entries with 5bit resolution
- Current regulation by integrated PWM controller and internal current sensing
- Programmable stepping mode: Full, Half, Mini and Microstepping
- Programmable slew rate for EMC and power dissipation optimisation
- Programmable Fast-, Slow-, Mixed-and Auto-Decay Mode
- Full-Scale Current programmable with 3bit resolution
- Very low current consumption in standby mode I_S < 3µA, typ. $T_j \leq 85$ °C
- All outputs short circuit protected with Openload, Overloadcurrent, Temperature Warning and Thermal Shutdown
- The PWM signal of the internal PWM controller is available as digital output.
- All parameters guaranteed for 7V < Vs < 20V



PowerSSO-24

Applications

Stepper Motor Driver for bipolar Stepper Motors in Automotive Applications like Light Levelling, Bending Light and Throttle Control.

Description

The device is an integrated stepper motor driver for bipolar stepper motors with microstepping and programmable current profile look-up-table to allow a flexible adaptation of the stepper motor characteristics and intended operating conditions. It is possible to use different current profiles depending on target criteria: audible noise, vibrations, rotation speed or torque. The decay mode used in PWM-current control circuit can be programmed to slow-, fast-, mixed-and auto-decay. In autodecay mode device will use slow decay mode if the current for the next step will increase and the fast decay or mixed decay mode if the current will decrease.

Order codes

Part number	Junction Temp range, °C	Package	Packing
L9942	-40 to 150	PowerSSO-24	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Block diagram and Pin information

Figure 1. Block diagram

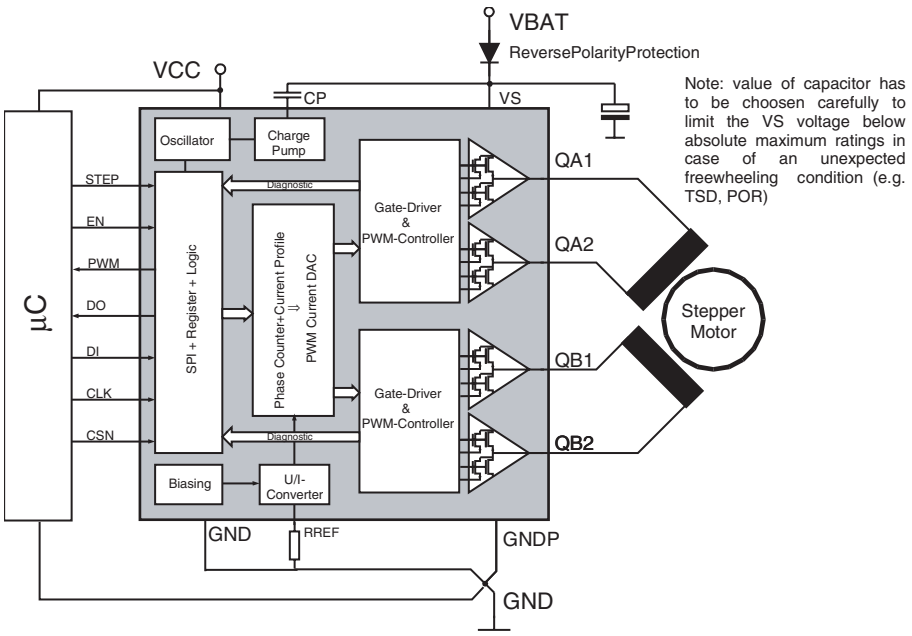
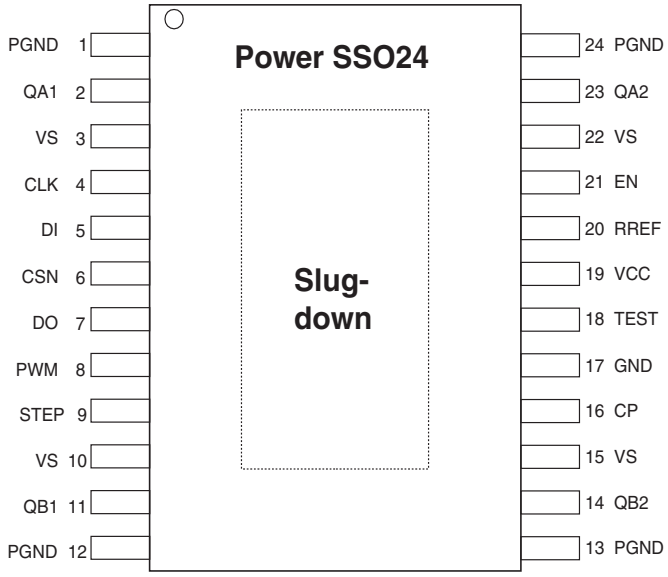


Figure 2. Pin connection (Top view)



All pins with the same name must be externally connected!

All pins PGND are internally connected to the heat slug.

Table 1. Pin Description

Pin	Symbol	Function
1, 12, 13, 24	PGND	**Power ground:** All pins PGND are internally connected to the heat slug. ***Important****:* All pins of PGND must be externally connected!
3, 10, 15, 22	VS	**Power supply voltage (external reverse protection required):** For EMI reason a ceramic capacitor as close as possible to PGND is recommended. ***Important****:* All pins of VS must be externally connected !
2, 23	QA1,QA2	**Fullbridge-outputs An:** The output is built by a highside and a lowside switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal reverse diode (bulk-drain-diode: highside driver from output to VS, lowside driver from PGND to output). This output is over-current protected.
11, 14	QB1,QB2	**Fullbridge-outputs Bn:** The output is built by a highside and a lowside switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal reverse diode (bulk-drain-diode: highside driver from output to VS, lowside driver from PGND to output). This output is over-current protected.
4	CLK	**SPI clock input:** The input requires CMOS logic levels. The CLK input has a pull-down current. It controls the internal shift register of the SPI.
5	DI	**Serial data input:** The input requires CMOS logic levels. The DI input has a pull-down current. It receives serial data from the microcontroller. The data is a 16bit control word and the least significant bit (LSB, bit 0) is transferred first.
6	CSN	**Chip Select Not input** The input requires CMOS logic levels. The CSN input has a pull-up current. The serial data transfer between device and micro controller is enabled by pulling the input CSN to low level.
7	DO	**SPI data output:** The diagnosis data is available via the SPI and it is a tristate-output. The output is CMOS compatible will remain highly resistive, if the chip is not selected by the input CSN (CSN = high)
8	PWM	**PWM output** This CMOS compatible output reflects the current duty cycle of the internal PWM controller of bridge A. It is an high resistance output until VCC has reached minimum voltage ore can switched off via the SPI command.
9	STEP	**Step clock input:** The input requires CMOS logic levels. The STEP input has a pull-down current. It is clock of up and down counter of control register 0. Rising edge starts new PWM cycle to drive motor in next position.
16	CP	**Charge Pump Output:** A ceramic capacitor (e.g.100 nF) to VS can be connected to this pin to buffer the charge-pump voltage.
17	GND	**Ground:** Reference potential besides power ground e.g. for reference resistor RREF. From this pin exist a resistive path via substrate to PGND.
18	TEST	**Test input** The TEST input has a pull-down current. Pin used for production test only. In the application it must be connected to GND.
19	VCC	**Logic supply voltage:** For this input a ceramic capacitor as close as possible to GND is recommended.
20	RREF	**Reference Resistor** The reference resistor is used to generate a temperature stable reference current used for current control and internal oscillator. At this output a voltage of about 1.28V is present. The resistor should be chosen that a current of about 200uA will flow through the resistor.
21	EN	**Enable input:** The input requires CMOS logic levels. The EN input has a pull-down resistor. In standby-mode outputs will be switched off and all registers will be cleared. If EN is set to a logic high level then the device will enter the active mode.

2 Device description

2.1 Dual Power Supply: VS and VCC

The power supply voltage VS supplies the half bridges. An internal charge-pump is used to drive the highside switches. The logic supply voltage VCC (stabilized) is used for the logic part and the SPI of the device. Due to the independent logic supply voltage the control and status information will not be lost, if there are temporary spikes or glitches on the power supply voltage. In case of power-on (VCC increases from under voltage to $V_{POR\ OFF}$ = 2.60 V, typical) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage VCC decreases under the minimum threshold ($V_{POR\ ON}$ = 2.45 V, typical), the outputs are switched to tristate (high impedance) and the internal registers are cleared.

2.2 Standby-Mode

The EN input has a pull-down resistor. The device is in standby mode if EN input isn't set to a logic high level. All latched data will be cleared and the inputs and outputs are switched to high impedance. In the standby mode the current at VS (VCC) is less than 3 µA (1µA) for CSN = high (DO in tristate). If EN is set to a logic high level then the device will enter the active mode. In the active mode the chargepump and the supervisor functions are activated.

2.3 Diagnostic Functions

All diagnostic functions (overload/-current, open load, power supply over-/undervoltage, temperature warning and thermal shutdown) are internally filtered (t_{GL} = 32µs, typical) and the condition has to be valid for a minimum time before the corresponding status bit in the status registers will be set. The filters are used to improve the noise immunity of the device. Open load and temperature warning function are intended for information purpose and will not change the state of the bridge drivers. On contrary, the overload/-current and thermal shutdown condition will disable the corresponding driver (overload/-current) or all drivers (thermal shutdown), respectively. The microcontroller has to clear the status bit to reactivate the bridge driver.

2.4 Over-voltage and Under-voltage Detection

If the power supply voltage VS rises above the over-voltage threshold $V_{SOV\ OFF}$ (typical 20 V), the outputs are switched to high impedance state to protect the load. When the voltage VS drops below the undervoltage threshold $V_{SUV\ OFF}$ (UV-switch-OFF voltage), the output stages are switched to the high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). Error condition is lached and the microcontroller needs to clear the status bits to reactivate the drivers.

2.5 Temperature Warning and Thermal Shutdown

If junction temperature rises above $T_{j\ TW}$ a temperature warning flag is set which is detectable via the SPI. If junction temperature increases above the second threshold $T_{j\ SD}$, the thermal shutdown bit will be set and power DMOS transistors of all output stages are switched off to

protect the device. In order to reactivate the output stages the junction temperature must decrease below Tj SD -Tj SD HYS and the thermal shutdown bit has to be cleared by the microcontroller.

2.6 Inductive Loads

Each half bridge is built by an internally connected highside and a lowside power DMOS transistor. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven without external free-wheeling diodes. In order to reduce the power dissipation during free-wheeling condition the PWMcontroller will switch-on the output transistor parallel to the freewheeling diode (synchronous rectification).

2.7 Cross-current protection

The four half-brides of the device are cross-current protected by an internal delay time depending on the programmed slew rate. If one driver (LS or HS) is turned-off then activation of the other driver of the same half bridge will be automatically delayed by the cross-current protection time .

2.8 PWM Current Regulation

An internal current monitor output of each high-side and low-side transistor sources a current image which has a fixed ratio of the instantaneous load current. This current images are compared with the current limit in PWM control. Range of limit can reach from programmed full scale value (register1 DAC Scale) down belonging LSB value of 5 bit DAC (register1 DAC Phase x). The data of the two 5 bit DACs comes form set up in 9 current profiles (register2 to 6). If signal changes to logic high at pin STEP then 2 currentprofiles are moved in register1 for DAC Phase A and B. Number of profile depends on phase counter reading and direction bit in register0 (*Figure 7*). The bridges are switched on until the load current sensed at HS switch exceeds the limit . Load current comparator signal is used to detect open load or overcurrent condition also.

2.9 Decay modes

During off-time the device will use one of several decay modes programmable by SPI (*Figure 4* top). In slow decay mode HS switches are activated after cross current protection time for synchronous rectification to reduce the power dissipation (*Figure 4* detail A). In fast decay opposite halfbridge will switched on after cross current protection time, that is same like change in the direction. For mixed decay the duration of fast decay period before slow decay can be set to a fixed time (*Figure 4* detail B continuous line) or is triggered by under-run of the load current limit (*Figure 4* detail B dashed line), that can be detected at LS switch. The special mode where the actual phase counter value is taken into account to select the decay mode is called auto decay (e.g. in *Figure 3* Micro Stepping DIR=1). If the absolute value of the current limit is higher as during step before then PWM control uses slow decay mode always. Otherwise one of the fast decay modes is automatic selected for a quick decrease of the load current and so it obtains new lower target value.

2.10 Over Current Detection

The overcurrent detection circuit monitors the load current in each activated output stage. In HS stage it is in function after detection of currentlimit during PWM cycle and in LS stage it works permanently. If the load current exceeds the overcurrent detection threshold for at least tISC = 4 µs, the over-current flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. Error condition is lached and the microcontroller needs to clear the status bits to reactivate the drivers.

2.11 Open Load Detection

The open load detection monitors the activity time of the PWM controller and is available for each phase. If the limit of load current is below around 100mA then open load condition is detectable. Open load bit for a bridge is set in the register6 if this low current limit can't reached after at least 15 consecutive PWM cycles.

Table 2. Truth table

DC2	DC1	DC0	I4	I3	I2	I1	I0	max. IOL
0	0	0	0	x	x	x	x	48mA
0	0	1	0	x	x	x	x	72mA
0	1	0	0	0	x	x	x	56mA
1	1	0	0	0	x	x	x	90mA
1	0	0	0	0	0	x	x	58mA
1	0	1	0	0	0	x	x	87mA
1	1	0	0	0	0	0	1	42mA
1	1	1	0	0	0	0	1	48mA

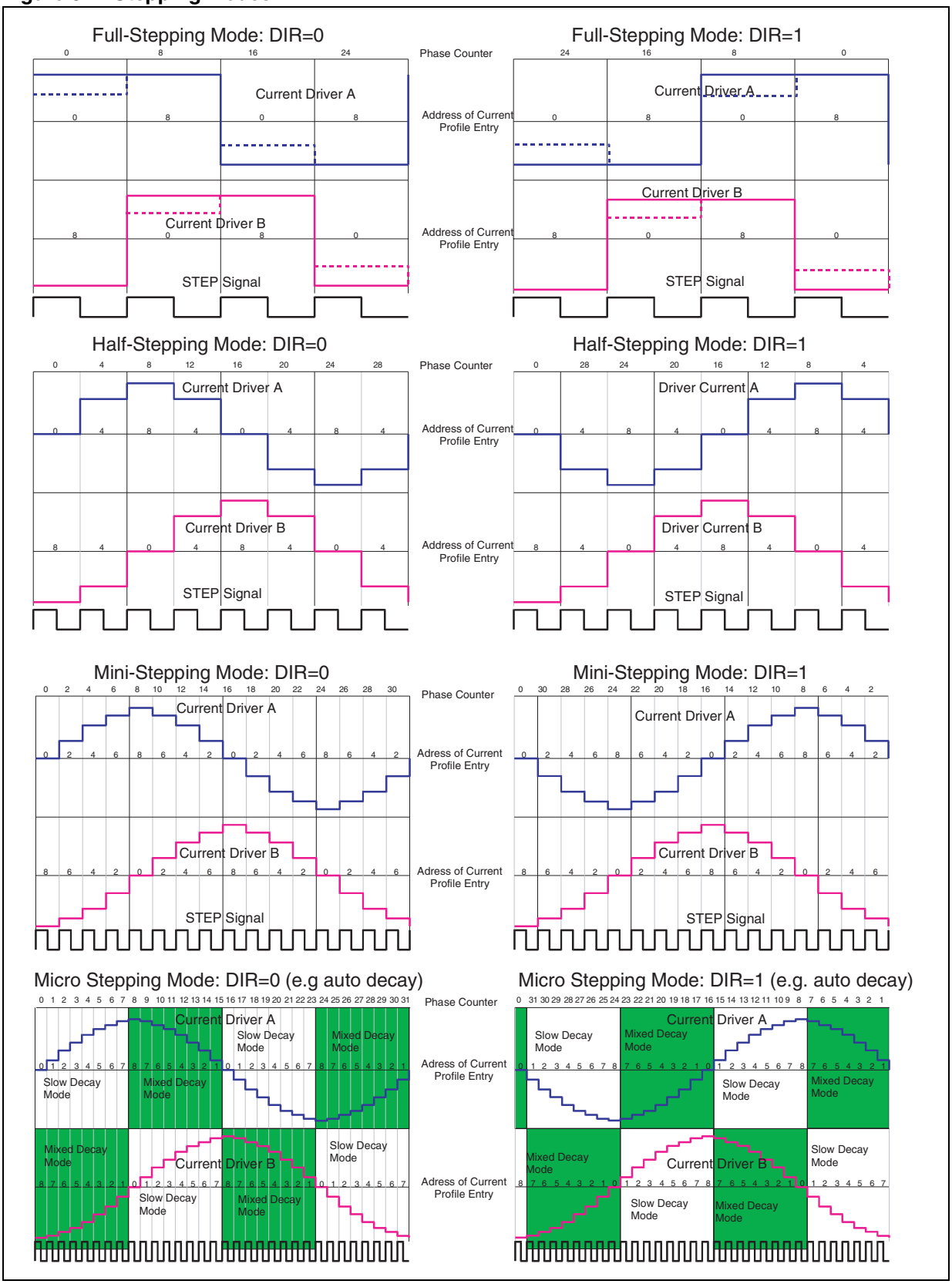
Truth table shows possible profiles for active open load detection. Maximum threshold IOL is shown in left column if x bits are 1 (see also *Figure 7*). Lowest possible limit is e.g. 3.1 mA for DC2=DC1=DC0=0 and it is set only I0=1.

2.12 Stepping Modes

One full revolution can consist of four full steps, eight half steps, sixteen mini steps or 32 microsteps.

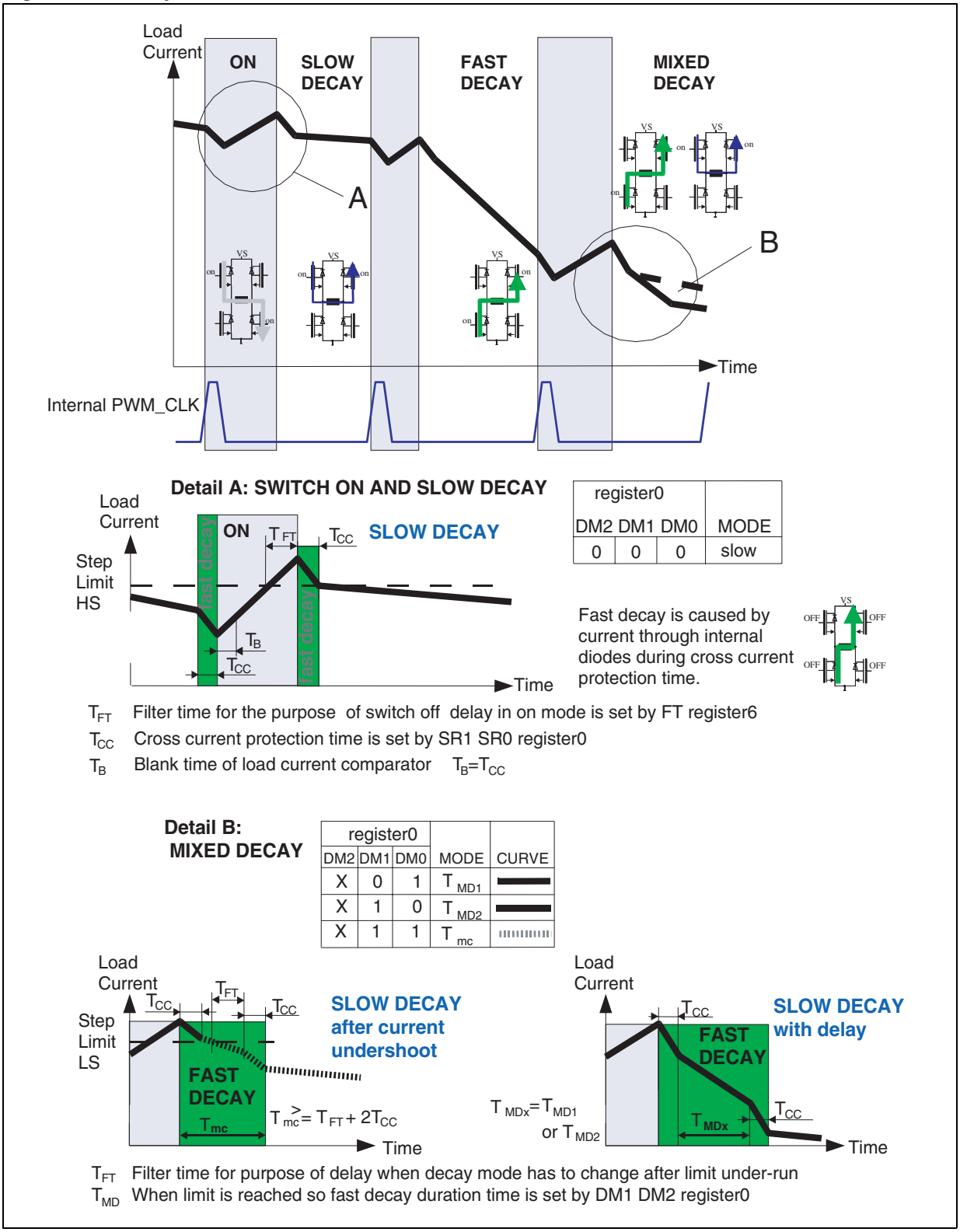
Mode is set up in register 0 and it defines increment size of phase counter. Phase counter value defines address of corresponding currentprofile. Stepping modes with typical profile values can see in *Figure 3* (e.g. also so called 'Two Phase On' shown in dashed line).

Figure 3. Stepping Modes



2.13 Decay Modes

Figure 4. Decay Modes



3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VS	DC supply voltage	-0.3...28	V
	single pulse t_{max} < 400 ms	40	V
VCC	stabilized supply voltage, logic supply	-0.3 to 5.5	V
V_{DI},V_{DO}, V_{CLK} V_{CSN}, V_{STEP} V_{EN}	digital input / output voltage	-0.3 to VCC + 0.3	V
V_{RREF}	current reference resistor	-0.3 to VCC + 0.3	V
V_{CP}	charge pump output	-0.3 to VS + 11	V
V_{Qxn}	(x=A;B n=1;2) output voltage	-0.3 to VS + 0.3	V
I_{Qxn}	(x=A;B n=1;2) output current	±2.5	A

Note: Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit !

3.2 ESD Protection

Table 4. ESD Protection

Parameter	Value	Unit
All pins	±2 [1]	kV
output pins: Qxn (x=A;B n=1;2)	±4 [2]	kV

Note: 1 HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A

2 HBM with all unzapped pins grounded

3.3 Thermal data

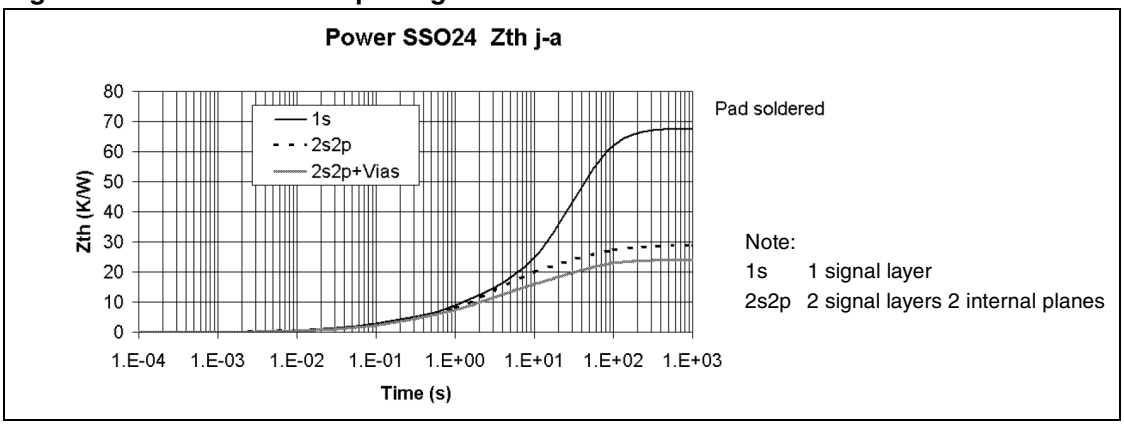
Table 5. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	operating junction temperature	-40 to 150	°C

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ ON}$	temperature warning threshold junction temperature	T_j increasing			150	°C
$T_{jTW\ OFF}$	temperature warning threshold junction temperature		130			°C
$T_{jSD\ ON}$	thermal shutdown thresholdjunction temperature				170	°C
$T_{jSD\ OFF}$	thermal shutdown threshold junction temperature		150			°C
$T_{jSD\ HYS}$	thermal shutdown hysteresis			5		K

Figure 5. Thermal data of package



3.4 Electrical characteristics

3.4.1 Supply

VS = 7 to 16V, VCC = 3.0 to 5.3 V, T_j = -40 to 150 °C, I_{REF} = -200 µA , unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 7. Supply

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I_S	VS DC supply current in active mode	VS = 13.5 V, EN=VCC outputs floating			7	20	mA
	VS quiescent supply current	VS = 13.5 V, TEST, EN = 0V outputs floating	T_j = -40 °C to 25°C		3	10	µA
			T_j = 125 °C		6	20	
I_{CC}	VCC DC supply current in active mode	VCC = 5.0 V EN=VCC, DI=CLK=STEP=0V			1	3	mA
		VCC = 5.0 V TEST; EN = 0V; CSN = VCC no clocks outputs floating	T_j = -40 °C to 25°C		1	3	µA
I_{CC}	VCC quescent suppy current	CSN=VCC no clocks outputs floating	T_j = 125 °C		2	6	µA
		VS = 13.5 V, VCC = 5.0 V	T_j = -40 °C to 25°C		4	13	µA
$I_S + I_{CC}$	Sum quiescent supply current	TEST; EN=0V CSN=VCC no clocks outputs floating	T_j = 125 °C		8	26	
t_{setPOR} [1]	VCC on set up time	EN = 5V, CSN=CLK=0V DO changes from high ohmic to logic level LOW		2			µs

Note: 1 This parameter is guaranteed by design.

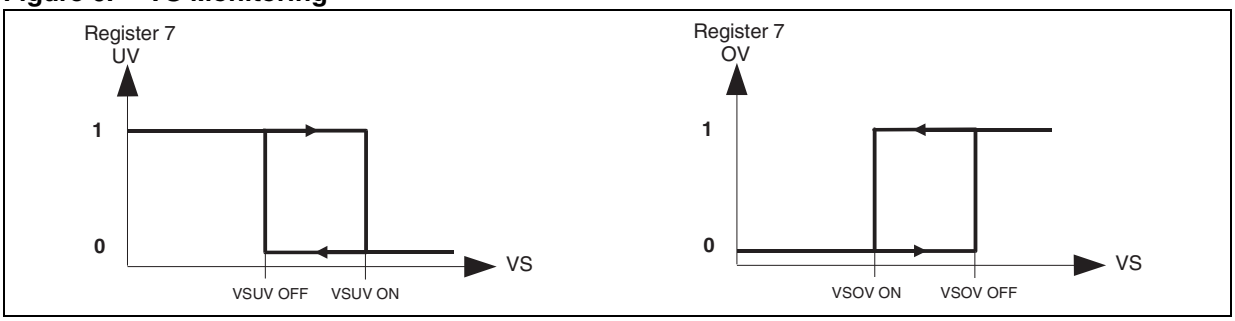
3.4.2 Over- and undervoltage detection

VS = 7 to 20 V, VCC = 3.0 to 5.3 V, EN=VCC, T_j = -40 to 150 °C, I_{REF} = -200 µA, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 8. Over- and undervoltage detection .

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{SUV\ ON}$	VS UV-threshold voltage	VS increasing			6.90	V
$V_{SUV\ OFF}$	VS UV-threshold voltage	VS decreasing	4.8			V
$V_{SUV\ hyst}$	VS UV-hysteresis	$V_{SUV\ ON}$ -$V_{SUV\ OFF}$		0.3		V
$V_{SOV\ OFF}$	VS OV-threshold voltage	VS increasing			25	V
$V_{SOV\ ON}$	VS OV-threshold voltage	VS decreasing	20			V
$V_{SOV\ hys}$t	VS OV-hysteresis	$V_{SOV\ OFF}$ -$V_{SOV\ ON}$		0.5		V
$V_{POR\ OFF}$	power-on-reset threshold	VCC increasing		2.6	2.9	V
$V_{POR\ ON}$	power-on-reset threshold	VCC decreasing	2.00	2.3		V
$V_{POR\ hyst}$	power-on-reset hysteresis	$V_{POR\ OFF}$ -$V_{POR\ ON}$		0.11		V

Figure 6. VS Monitoring



3.4.3 Reference Current Output

VS = 7 to 20 V, VCC = 3.0 to 5.3 V, EN=VCC, T_j = -40 to 150 °C, I_{REF} = -200 µA, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 9. Reference Current Output

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{REF}	reference voltage range	I_{REF} = -200 µA	1.05	1.25	1.45	V
$I_{REFshorted}$	reference current threshold shorted pin REF	register6 bit7 RERR = 1			-250	µA
$I_{REFopen}$	reference current threshold open pin REF	register6 bit7 RERR = 1	-150			µA

The device works properly without the external resistor at pin REF. In this case it doesn't have to fullfill all specified parameters.

3.4.4 Charge Pump Output

VS = 7 to 20 V, VCC = 3.0 to 5.3 V, EN=VCC, T_j = -40 to 150 °C, I_{REF} = -200 µA, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 10. Charge Pump Output

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
VCP	charge pump output voltage	VS=7V	I_{CP}= -100µA, all switches off at Qxn	11		20	V
		VS=13.5V		20		35	V
		VS=20V		30		40	V

The ripple of voltage at CP can suppressed using a capicity of e.g.100nF.

3.4.5 Outputs: Qxn (x=A;B n=1;2)

VS = 7 to 20 V, VCC = 3.0 to 5.3 V, EN=VCC, T_j = -40 to 150 °C, I_{REF} = -200 µA, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin

Table 11. Outputs: Qxn (x=A;B n=1;2)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{DSON\,HS}$	on-resistance Qxn to VS	VS = 13.5 V, T_j = 25 °C, I_{Qxn} = -1.0A		500	700	mΩ
		VS = 13.5 V, T_j = 125 °C, I_{Qxn} = -1.0 A		750	1000	mΩ
		VS = 7.0 V, T_j = 25 °C, I_{Qxn} = -1.0 A		550	750	mΩ
$R_{DSON\,LS}$	on-resistance Qxn to PGND	VS = 13.5 V, T_j = 25 °C, I_{Qxn} = + 1.0A		500	700	mΩ
		VS = 13.5 V, T_j = 125 °C, I_{Qxn} = + 1.0 A		750	1000	mΩ
		VS = 7.0 V, T_j = 25 °C, I_{Qxn} = + 1.0 A		550	750	mΩ
$\lvert I_{QxnOC} \rvert$	output overcurrent limitation to VS or PGND	testmode exclusive of filtertime 4us (*Chapter 2.10*)	1.6	2		A

3.4.6 Outputs: Qxn (x=A;B n=1;2)

The comparator, which is monitoring current image of HS, is working during ON cycle of PWM control. If load current is higher as set value then the signal ILIMIT is generated and after filter time the bridge is switched off. Test mode gets access to signal ILIMIT and threshold of current can be measured.

Table 12. Outputs: Qxn (x=A;B n=1;2)
VS = 7 to 20 V, VCC = 3.0 to 5.3 V, EN=VCC, T_j = -40 to 150 °C, I_{REF} = -200 µA, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{QxnFS_HS}	Value of output current to supply VS (so called full scale value)[1] sourcing from HS switch	Bits: DC2 DC1 DC0=000	60	95	130	mA
		Bits: DC2 DC1 DC0=001	100	140	180	
		Bits: DC2 DC1 DC0=010	180	230	280	
		Bits: DC2 DC1 DC0=011	300	360	420	
		Bits: DC2 DC1 DC0=100	485	550	615	
		Bits: DC2 DC1 DC0=101	720	810	900	
		Bits: DC2 DC1 DC0=110	1000	1150	1300	
		Bits: DC2 DC1 DC0=111	1200	1350	1500	
I_{QxnLIM_HS}	Accuracy of micro steps current limit		MIN[2]		MAX[2]	mA

Note: 1 Current profile has to pre set with I4 I3 I2 I1 I0 = 11111 and load to register 1 .

2 $MIN = 0.92 \cdot I_{QxnLIM} - 0.02 \cdot |I_{QxnFS_HS}|$, $MAX = 1.08 \cdot I_{QxnLIM} + 0.02 \cdot |I_{QxnFS_HS}|$

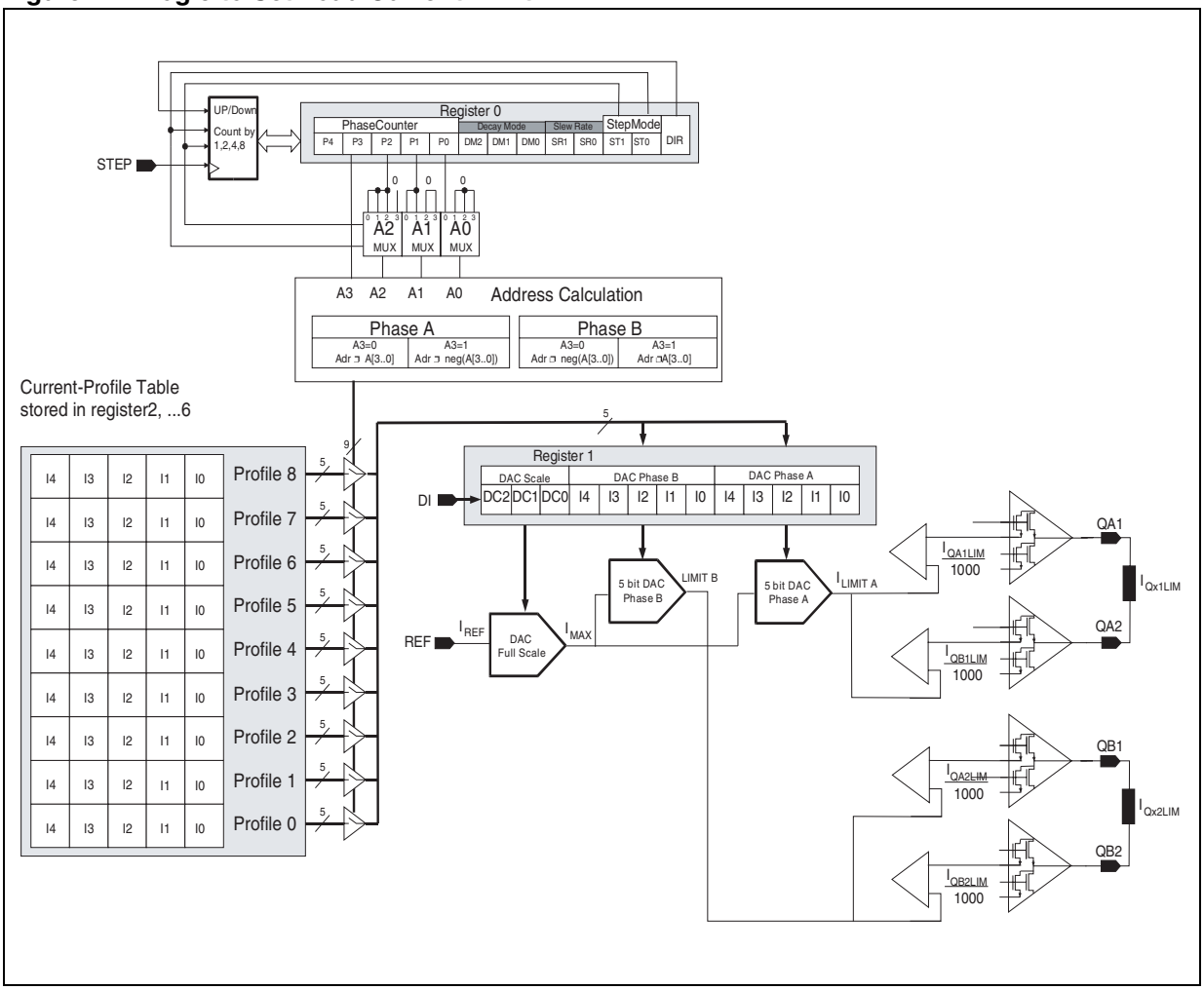
Output current limit IQxnLIM is product of full scale current IIQxnFS_ I (bits DC2 DC1 DC0) and value of DAC

PhaseA/B (bits I4 I3 I2 I1 I0) in register1.

Values of DAC Phase A and B can read out and depends on set up done before:

1. direction DIR , stepping mode ST1 ST0 and phase counter P4 P3 P2 P1 P0 in register 0 and
2. value of corresponding current profile (for address of current profile entry see also *Figure 3*).

Figure 7. Logic to Set Load Current Limit



3.4.7 PWM Control

VS = 7 to 20 V, VCC = 3.0 to 5.3 V, EN=VCC, T_j = -40 to 150 °C, I_{REF} = -200 µA, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 13. PWM Control (see *Figure 4* and *Figure 7*)

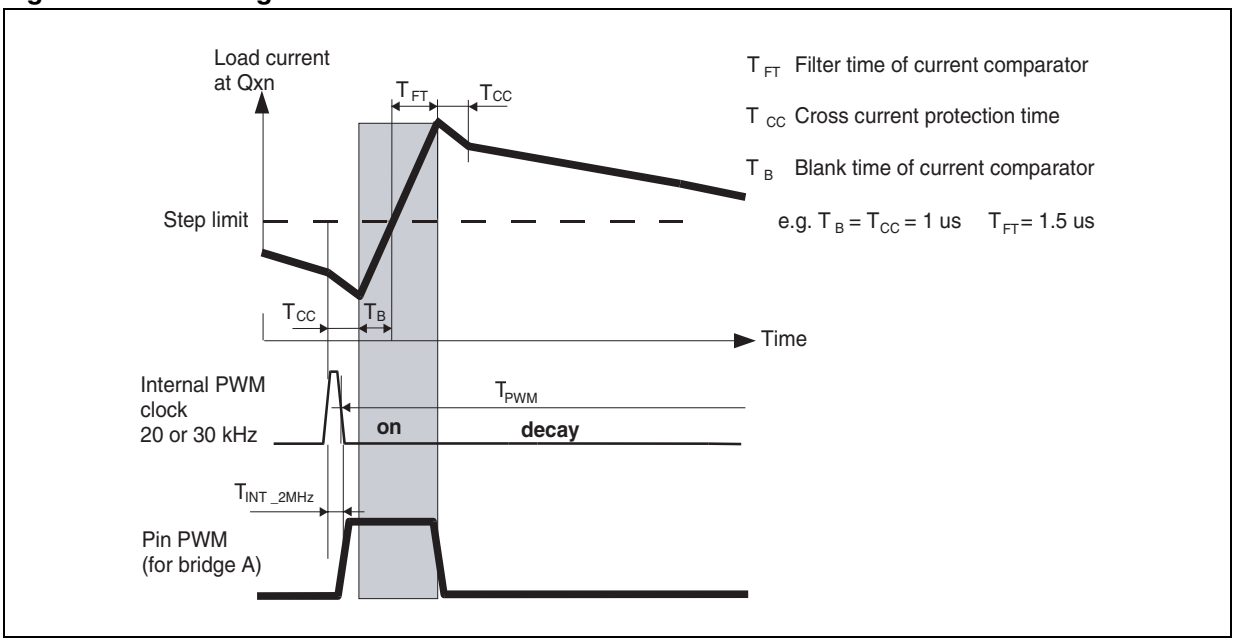
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{PWM} [1]	Frequency of PWM cycles	Bit: FRE= 1		20.8		kHz
		Bit: FRE= 0		31.3		kHz
T_{MD} [1]	Mixed decay switch off delay time	Bits: DM1 DM0= 0 1		4		us
		Bits: DM1 DM0= 1 0		8		us
T_{FT} [1]	Glitch filter delay time	Bit: FILTER= 0		1.5		us
		Bit: FILTER= 1		2.5		us

Table 13. PWM Control (see *Figure 4* and *Figure 7*) (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
T_{cc} [1] T_B [1]	Cross current protection time Blank time of comparator	Bits: SR1 SR0= 0 0		0.5		us
		Bits: SR1 SR0= 0 1		1		us
		Bits: SR1 SR0= 1 0		2		us
		Bits: SR1 SR0= 1 1		4		us
VSR	Slew rate (dV/dt 30%-70%) @HS switches on resistive load of 10Ω, VS=13.5V	Bits: SR1 SR0= 0 0		13		V/us
		Bits: SR1 SR0= 0 1		13		V/us
		Bits: SR1 SR0= 1 0		6		V/us
		Bits: SR1 SR0= 1 1		6		V/us

Note: 1 This parameter is guaranteed by design.
Time base is an internal trimmed oscillator of typical 2MHz and it has an accuracy of ±6% .

Figure 8. Switching on Minimum Time



4 Functional Description of the Logic with SPI

4.1 Motor Stepping Clock Input(STEP)

Rising edge of signal STEP is latched. It is synchronised by internal clock. At next start of a new PWM cycle the new values of output current limit are used to drive motor in next position. Before start new motor step this signal has to be low for at least two internal clock periods to reset latch.

4.2 PWM Output (PWM)

This output reflects the current duty cycle of the internal PWM controller of bridge A. High level indicates on state to increase current through load and low level is in off state so load current decreases depending on chosen decay mode.

4.3 Serial Peripheral Interface (SPI)

This device uses a standard 16 bit SPI to communicate with a microcontroller. The SPI can be driven by a microcontroller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0.

For this mode, input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin will reflect an internal Error Flag of the device which is a logical-or of all status bits in the Status Register (reg7) and in the Current Profile Register 4 (reg6). The microcontroller can poll the status of the device without the need of a full SPI-communication cycle.

4.4 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) will be in high impedance state. A low signal will activate the output driver and a serial communication can be started. The state when CSN is going low until the rising edge of CSN will be called a communication frame.

4.5 Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and latched into an internal 16 bit shift register. The first 3 bit are interpreted as address of the data register. At the rising edge of the CSN signal the contents of the shift register will be transferred to the selected data register. The writing to the register is only enabled if exactly 16 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

4.6 Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the status bit 0 (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

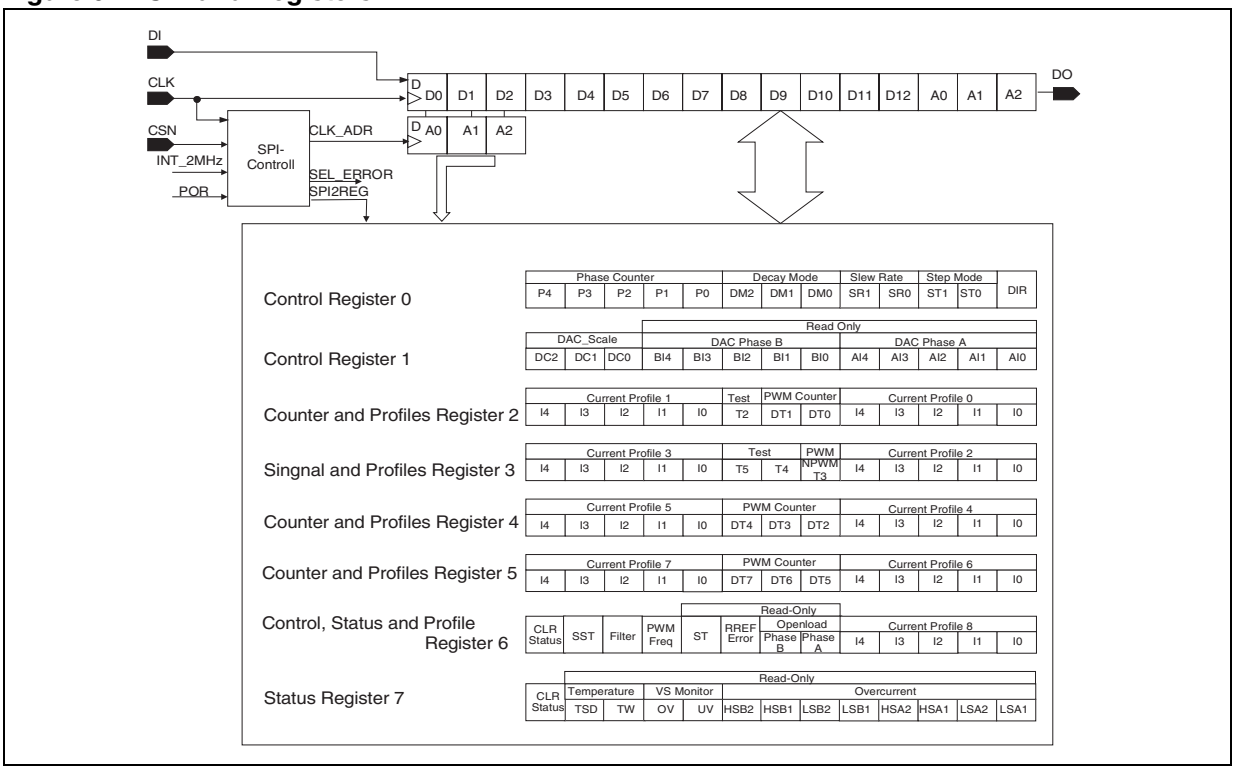
4.7 Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal.

4.8 Data Register

The device has eight data registers. The first three bits (bit0 ... bit2) at the DI-input are used to select one of the input registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register will be written to the selected Input Data Register only if a frame of exact 16 data bits are detected. The selected register will be transferred to DO during the current communication frame.

Figure 9. SPI and Registers



5 SPI - Control and Status Registers

5.1 Control Register 0

Bit	Phase Counter					Decay Mode			Slew Rate		Step Mode		DIR
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	P4	P3	P2	P1	P0	DM2	DM1	DM0	SR1	SR0	ST1	ST0	DIR

The meaning of the different bits is as follows:

DIR	This bit controls direction of motor movement. DIR=1 clockwise DIR=0 counter clockwise.

ST1 ST0	This bits controls step mode of motor movement (*Figure 3*).
00	Micro-stepping
01	Mini-stepping
10	Half-stepping
11	Full-stepping

SR1 SR0	This bit controls slew rate of bridge switches. See also parameter *Table 13*

DM2 DM1 DM0	This bits controls decay mode of output current (*Figure 3*).	
000	Slow decay	
001	Mixed decay, fast decay until T_{MD} > 4us	
010	Mixed decay, fast decay until T_{MD} > 8us	
011	Mixed decay, fast decay until current undershoot $T_{mc} = T_{FT} + T_{CC}$	
100	Auto decay, fast decay without delay time	Auto decay uses mixed decay automatically to reduce current for next step if required (see *Figure 3* down right).
101	Auto decay, fast decay until T_{MD} > 4us	
110	Auto decay, fast decay until T_{MD} > 8us	
111	Auto decay, fast decay until current undershoot T_{mc}	

P4 P3 P2 P1 P0	This bits control position of motor, e.g. 00000 step angle is 0°, 01111 step angle is 180°..

5.2 Control Register 1

Bit	DAC Scale			DAC Phase B					DAC Phase A				
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r	r	r	r	r	r	r	r	r	r
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	DC2	DC1	DC0	BI4	BI3	BI2	BI1	BI0	AI4	AI3	AI2	AI1	AI0

The meaning of the different bits is as follows:

AI4 AI3 AI2 AI1 AI0	These bits control DAC of bridge A.	Value depends on address and the value of corresponding current profile.
BI4 BI3 BI2 BI1 BI0	These bits control DAC of bridge B .	
DC2 DC1 DC0	These bits set full scale range of limit, e.g. 000 for 100 mA or 111for e.g. 1500mA	See also parameter *Table 12*.

5.3 Counter and Profiles Register 2

Bit	Current Profile 1					Not used			Current Profile 0				
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	I4	I3	I2	I1	I0	T2	T1	T0	I4	I3	I2	I1	I0

The meaning of the different bits is as follows:

I4 I3 I2 I1 I0	These bits are loaded in register1 DAC Phase A or B if needed.	See also parameter *Table 12*
T2 T1 T0	These bits are used in test mode only.	

5.4 Signal and Profile Register 3

Bit	Current Profile 3					PWM Counter		PWM	Current Profile 2				
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r
	w	w	w	w	w	w	w	w	w	w	w	w	w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	I4	I3	I2	I1	I0	D1 (T5)	D0 (T4)	NPWM(T3)	I4	I3	I2	I1	I0

The meaning of the different bits is as follows:

I4 I3 I2 I1 I0	These bits are loaded in register1 DAC Phase A or B if needed.	See also parameter *Table 12*
DT1 DT0	These bits are for threshold value in counter of active time during signal PWM.	
NPWM	This bit switches internal PWM signal of bridge A to pin PWM if it is set to 0, otherwise pin is in high resistance status.	
(T5 T4 T3)	These bits are used in test mode only.	

5.5 Counter and Profile (Register 4 and Register 5)

Bit	Current Profile 5 (7)					PWM Counter			Current Profile 4 (6)				
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w	r w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	I4	I3	I2	I1	I0	D4(7)	D3(6)	D2(5)	I4	I3	I2	I1	I0

The meaning of the different bits is as follows:

I4 I3 I2 I1 I0	These bits are loadedneeded. in register1 DAC Phase A or B if needed.	See also parameter *Table 12*
D4 D3 D2 (register4)	These bits are for threshold value in counter of active time during signal PWM. LSB and next value are set in register3 by D0 and D1.	
D7 D6 D5 (register5)		

5.6 Control, Status and Profile Register 6

	CLR	ST (PWM)	Filter	Freq	ST	REF ERR	Openload		Current Profile 8				
Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r w	r w	r w	r	r	r	r	r w	r w	r w	r w	r w
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	CLR6	SST	FT	FRE	ST	RERR	OB	OA	I4	I3	I2	I1	I0

The meaning of the different bits is as follows:

I4 I3 I2 I1 I0	These bits are loaded in register1 DAC Phase A or B if needed	See also parameter *Table 12*
OB OA	These bits indicate openload at bridges	
RERR	This bit indicates if reference current is OK (150uA $<I_{REF}<$ 250uA), then is RERR=0.	
ST	This bit indicates stall detection.	
FRE	This bit sets frequency of PWM cycle. FRE=1 frequency 20kHz, FRE=0 frequency 30kHz	

FT	This bit sets filter time in glitch filter. FT=0 T_F =1.5us, FT=1 T_F =2.5us
SST	This bit specifies output PWM to reflect same logical level like bit ST.
CLR6	This bit resets all bits to 0 in register 6.

5.7 Status Register7

Bit	CLR	Temperature		VS Monitor		Overcurrent							
	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r w	r	r	r	r	r	r	r	r	r	r	r	r
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	CLR7	TSD	TW	OV	UV	HSB2	HSB1	LSB2	LSB1	HSA2	HSA1	LSA2	LSA1

The meaning of the different bits is as follows:

bit7 ... bit0	These bits indicate overcurrent in each lowside or highside power transistor.
1	overcurrent failure I > 2A
OV UV	These bits indicates failure at VS (See also parameter *Table 8*)
01	Voltage at pin VS is too low.
10	Voltage at pin VS is too high.
TSD TW	These bits indicates temperature failure (See also parameter *Table 6*)
01	Only for information set at temperature warning threshold.
10	In case of thermal shutdown all bridges are switched off. It has to reset by bit CLR7.
CLR7	This bit resets all bits to 0 in register7.

5.8 Auxiliary logic blocks

5.8.1 Fault Condition

Logical level at pin D0 represents fault condition. It is valid from first high to low edge of signal CLK up to transfer of data bit D12. Fault bit is an logical OR of:

Control and Status Register 6 bit 5 and 6 for Open Load, bit7 reference current failure (RERR) and

Control and Status Register 7 bit 0 to bit 7 for Overcurrent, bit 8 and 9 failure at VS (UV,OV) and

bit 10 and bit 11 during high temperature (TW,TSD)

5.8.2 SPI communication monitoring

At the rising edge of the CSN signal the contents of the shift register will be transferred to the selected data register. A counter monitors proper SPI communication. It counts rising edges at pin CLK. The writing to the register is only enabled if exactly 16 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame. SPI communication can be checked by loading a command twice and then answer at pin DO must be same.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

5.8.3 PWM monitoring for stall detection

Control registers 4, 5, and 3 contain bits D0-D7, use for setting a stall detection threshold. The value in this set of bits determine the minimum time for current rise over one quadrant of motor driving. D7-D0 is compared with the sum of the rise times over one quadrant. When the sum is less than the value stored in D7-D0 the ST bit (register6 bit 8) is set to a logic “1”.

The PWM pin reflects the PWM control signal of the load current in bridge A. This is so after power on when the SST bit (register 6, bit11) is reset to a logic “0”. If this bit is set to a logical “1” then status of the ST bit 8 is mirrored to pin PWM. This provides stall detection without the need of reading register 6 through the SPI bus.

6 Logic with SPI - Electrical Characteristics

VS = 7 to 20 V, VCC = 3.0 to 5.3 V, EN=VCC, T_j = -40 to 150 °C, I_{REF} = -200 µA, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6.1 Inputs: CSN, CLK, STEP, EN and DI

Table 14. Inputs: CSN, CLK, STEP, EN and DI

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{in\ L}$	input low level	VCC = 5 V	1.5	2.0		V
$V_{in\ H}$	input high level	VCC = 5 V		3.0	3.5	V
$V_{in\ Hyst}$	input hysteresis	VCC = 5 V	0.5			V
$I_{CSN\ in}$	pull up current at input CSN	V_{CSN} = VCC-1.5 V,	-50	-25	-10	µA
$I_{CLK\ in}$	pull down current at input CLK	V_{CLK} = 1.5 V	10	25	50	µA
$I_{DI\ in}$	pull down current at input DI	V_{DI} = 1.5 V	10	25	50	µA
$I_{STEP\ in}$	pull down current at input STEP	V_{STEP} = 1.5 V	10	25	50	µA
$R_{EN\ in}$	resistance at input EN to GND	$V_{EN\ in}$ = VCC	110		510	kΩ
C_{in} (1)	input capacitance at input CSN, CLK, DI and PWM	0 V < VCC < 5.3 V		10	15	pF

(1) Parameter guaranteed by design.

6.2 DI timing

Table 15. DI timing (see *Figure 11* and *Figure 13*) (2)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{CLK}	clock period	VCC = 5 V	250			ns
t_{CLKH}	clock high time	VCC = 5 V	100			ns
t_{CLKL}	clock low time	VCC = 5 V	100			ns
$t_{set\ CSN}$	CSN set up time, CSN low before rising edge of CLK	VCC = 5 V	100			ns
$t_{set\ CLK}$	CLK set up time, CLK high before rising edge of CSN	VCC = 5 V	100			ns
$t_{set\ DI}$	DI set up time	VCC = 5 V	50			ns
$t_{hold\ DI}$	DI hold time	VCC = 5 V	50			ns
$t_{r\ in}$	rise time of input signal DI, CLK, CSN	VCC = 5 V			25	ns
$t_{f\ in}$	fall time of input signal DI, CLK, CSN	VCC = 5 V			25	ns

(2) DI timing parameters tested in production by a passed/failed test:
T_j=-40°C/+25°C: SPI communication @5MHz; T_j=+125°C: SPI communication @4.25MHz

6.3 Outputs: DO, PWM

Table 16. Outputs: DO, PWM

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DOoutL} / $V_{PWMoutL}$	output low level	VCC = 5 V, I_D = 2 mA		0.2	0.4	V
V_{DOoutH} / $V_{PWMoutH}$	output high level	VCC = 5 V, I_D = -2 mA	VCC - 0.4	VCC - 0.2		V
$I_{DOoutLK}$	tristate leakage current	V_{CSN} = VCC, 0 V < V_{DO} < VCC	-10		10	µA
$I_{PWMoutLK}$	tristate leakage current	Register3bit5=1 (NPWM) 0 V < V_{PWM} < VCC	-10		10	µA
C_{out} (1)	tristate input capacitance	V_{CSN} = VCC, 0 V < VCC < 5.3 V		10	15	pF

6.4 Output: DO timing

Table 17. Output: DO timing (see *Figure 12* and *Figure 13*)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$t_{r\ DO}$	DO rise time	C_L = 100 pF, I_{load} = -1 mA		50	100	ns
$t_{f\ DO}$	DO fall time	C_L = 100 pF, I_{load} = 1 mA		50	100	ns
$t_{en\ DO\ tri\ L}$	DO enable time from tristate to low level	C_L = 100 pF, I_{load} = 1 mA pull-up load to VCC		50	250	ns
$t_{dis\ DO\ L\ tri}$	DO disable time from low level to tristate	C_L = 100 pF, I_{load} = 4 mA pull-up load to VCC		50	250	ns
$t_{en\ DO\ tri\ H}$	DO enable time from tristate to high level	C_L = 100 pF, I_{load} = -1 mA pull-down load to GND		50	250	ns
$t_{dis\ DO\ H\ tri}$	DO disable time from high level to tristate	C_L = 100 pF, I_{load} = -4 mA pull-down load to GND		50	250	ns
$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 VCC, V_{DO} > 0.7 VCC, C_L = 100 pF		50	250	ns

6.5 CSN timing

Table 18. CSN timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$t_{CSN_HI,min}$ (1)	CSN high time, active mode	Transfer of SPI-command to Input Register	2			µs

6.6 STEP timing

Table 19. STEP timing

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$t_{STEPmin}$ (1)	STEP low or high time		2			µs

(1) Parameter guaranteed by design.

Figure 10. Transfer Timing Diagram

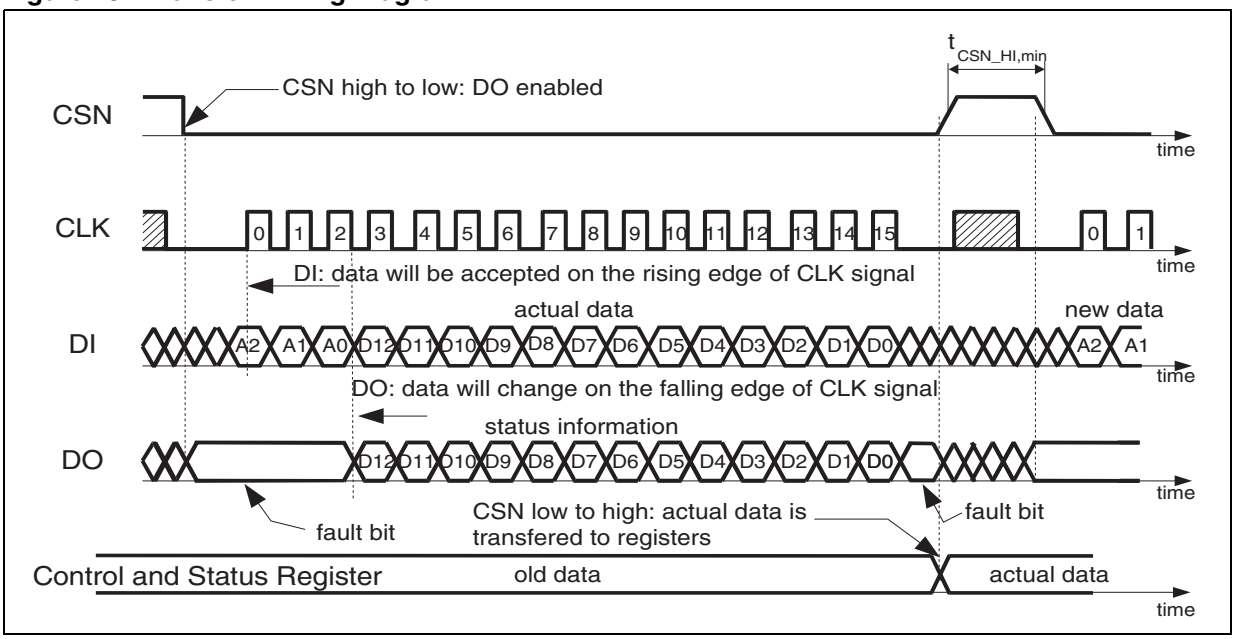


Figure 11. Input Timing

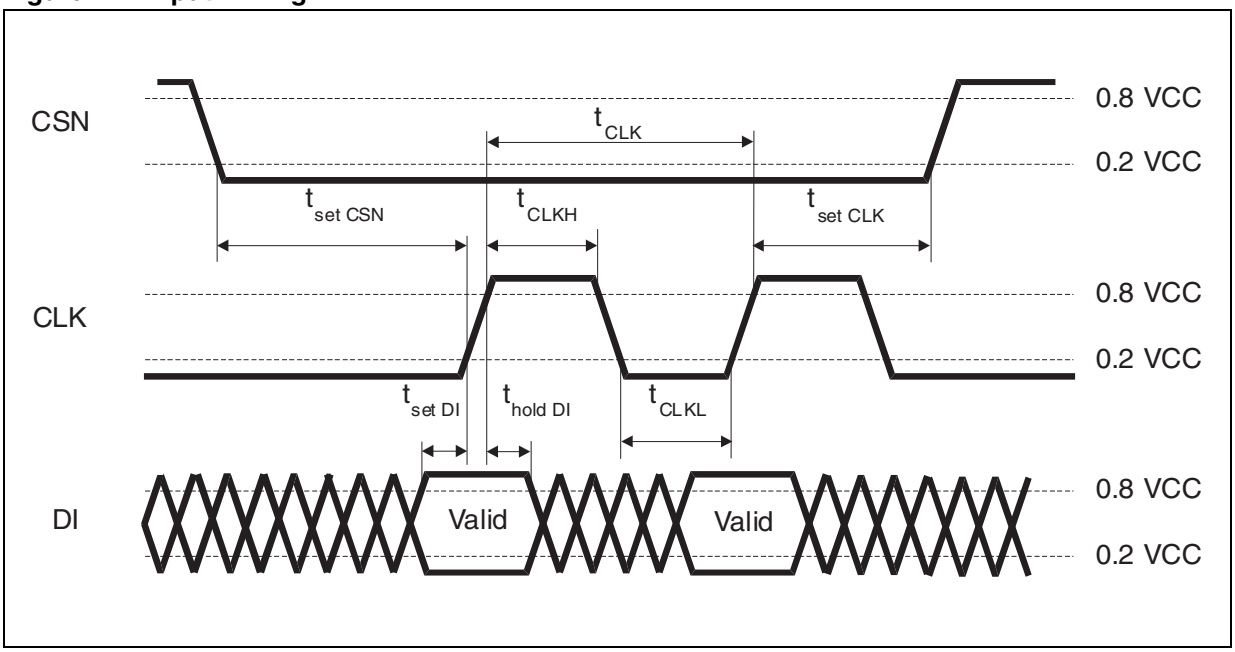


Figure 12. SPI - DO Valid Data Delay Time and Valid Time

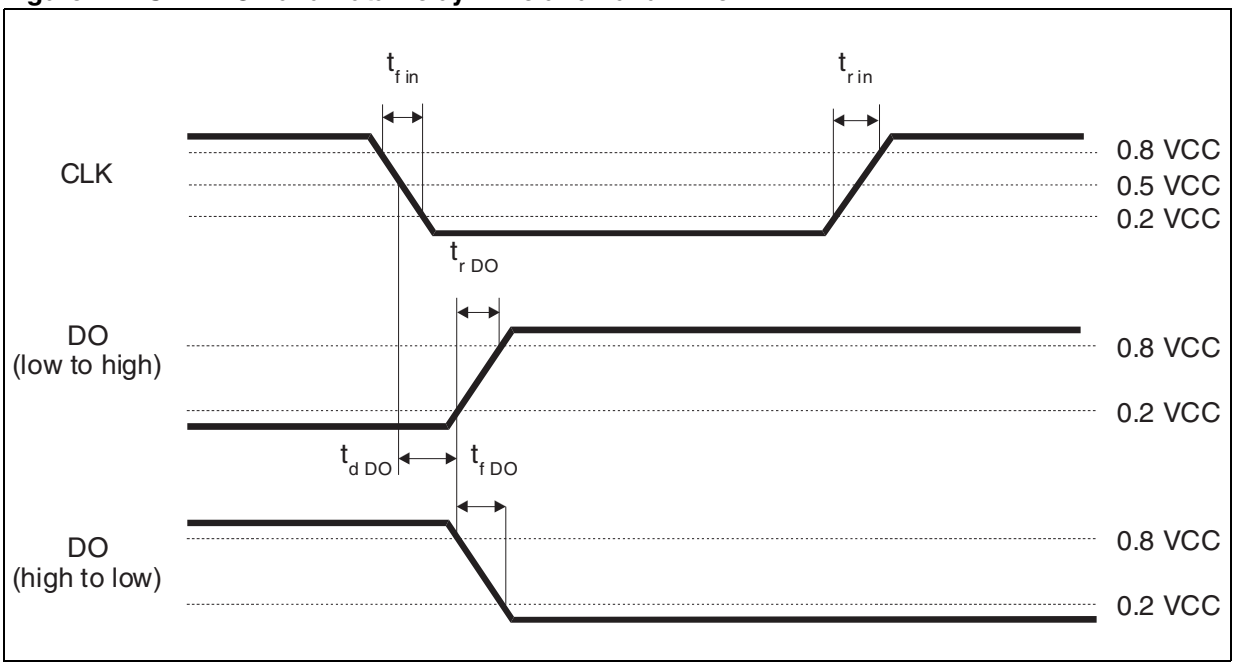


Figure 13. DO Enable and Disable Time

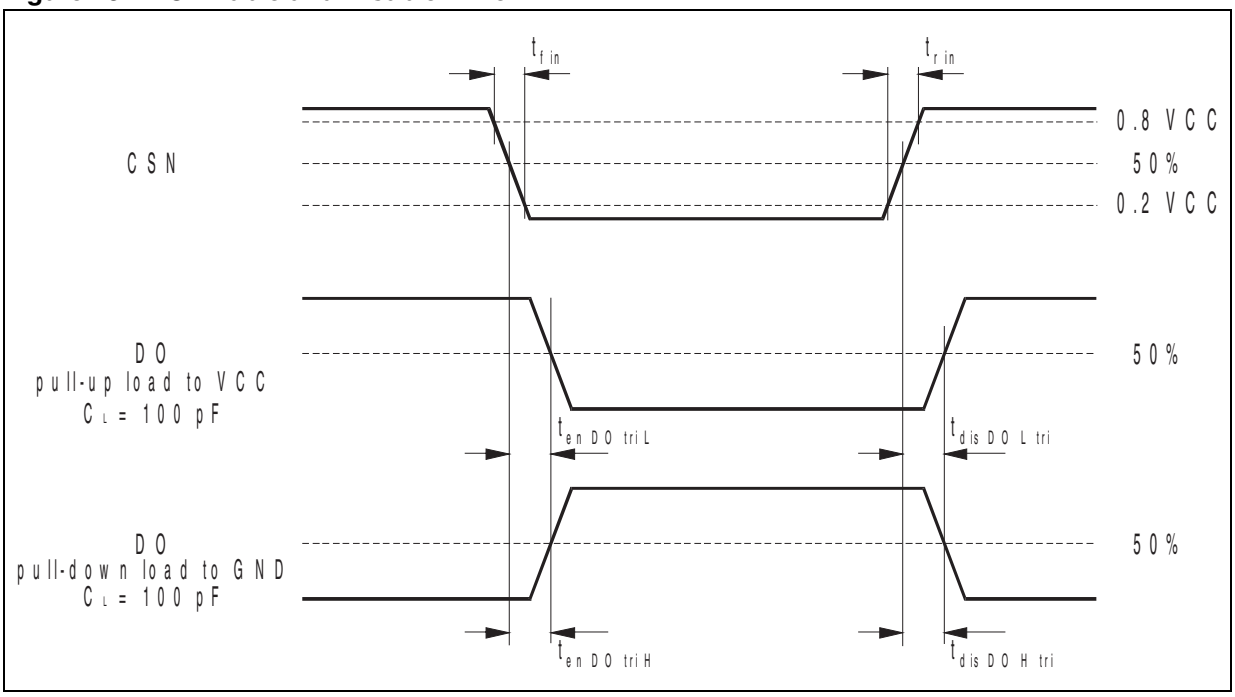
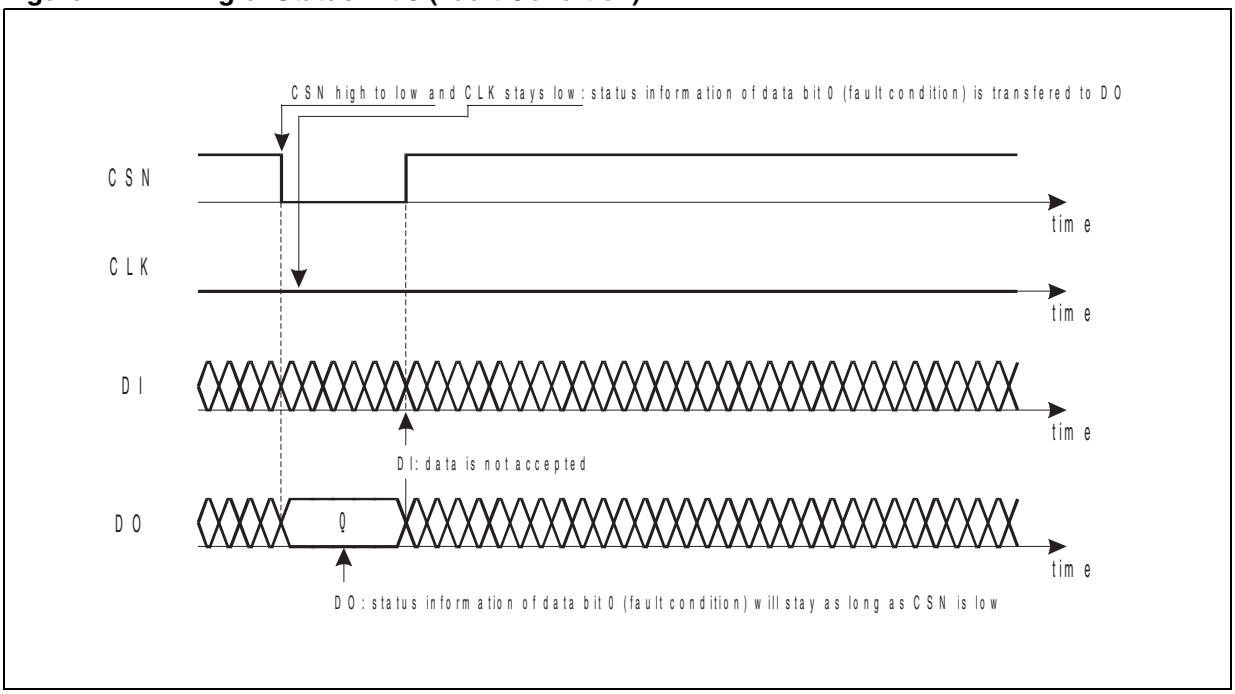


Figure 14. Timing of Status Bit 0 (Fault Condition)



7 Appendix

7.1 Stall Detection

The L9942 contains logic blocks designed to detect a motor stall caused by excessive mechanical load.

During a motor stall condition the load current rises much faster than during normal operation. The L9942 measures this time and compares it to a programmed value.

This is done by summing the PWM on times for one full quadrant. For a full wave stepping this is just one value (step 0). For microstepping this includes 8 separate values added together, one for each step. This measurement is only done on phase A during the quadrants where the current is increasing naturally (quadrants 1 and 3 of *Figure 15*); e.g. stall detection is active during phase counter values 1 to 8 and 17 to 24 for DIR=0. During the quadrants where the current is decreasing fast decay recirculation interferes with accurate measurement of this time.

If the sum of the PWM on time is less than a programmed threshold stored in D0-D7, stall is detected and indicated as a logic “1” in the stall (ST) bit found in register 6 bit 8 (*Figure 15* bottom). If bit 11 of register 6 is set to logical “1” then the ST bit is mirrored to the PWM pin providing detection externally.

The register values DT7-DT0 store the threshold value in 16us intervals. These bits can be found interstitially in register 3 (D0, D1), register4 (D2, D3, D4) and register5 (D5, D6, D7).

Care should be taken when deciding the threshold timing. Motor current slew rates are dependant on the driving voltage, the actual speed of the motor, the back EMF of the motor as well as the motor and the inductance. Be sure to set your threshold well away from what can be seen in normal operation at any temperature.

7.2 Load Current Control and Detection of Overcurrent (Shortages at Outputs)

The L9942 controls load current in the two full bridges by using a pulls with modulation (PWM) regulator. The mirrored output current of active HS switch is compared with a programmed reference current (e.g. in figure A2 HSA1 and HSB2). Bridge is switched off if current has exceeded the programmed limit value.

A second comparator of the related LS switch uses the mirrored load current to detect an overcurrent to ground during ON state of bridges (e.g. in *Figure 16* LSA2 and LSB1). The event of shortage from output to supply voltage VS is detectable, but short current between outputs is limited through PWM controller and so an overcurrent failure will not occur.

Load currents decrease more or less fast during OFF state of bridges depending on selected decay mode. Slow decay mode is realised by activating the HS switches of the bridge and current comparator has as new reference the overcurrent limit. A shortage to ground can be detected, but not between the outputs.

Is it recommended to use the different fast decay modes too, especially in period if the load current has to reduce from step to step. The duration of fast decay can set by fixed time ore that it depends on the comparator signal utilising the second current mirror at LS switch. There can be monitored the undershoot of bridge current during OFF state.

Fast decay can be seen as switching the bridge in opposite direction, if it is compared to ON state before. The load current control at HS switch is not used, but the comparator is still active. The reference value is changed to overcurrent limit and a shortage to ground or now between the outputs too will result in a signal. The internal filter time of at least 4 us will inhibit the signal in many applications. Then you can use the mode “auto decay without any delay time“ (On *Section 5.1 on page 21* mode 100). On page 34 you can find in the lower part of *Figure 3* the phase counter values, when fast decay as only part of mixed decay is used and the shortages can be detected during a longer time. After this it is signalised in register 7 as overcurrent in HS switch (e.g. in *Figure 17* HSA1).

Figure 15. Stall Detection

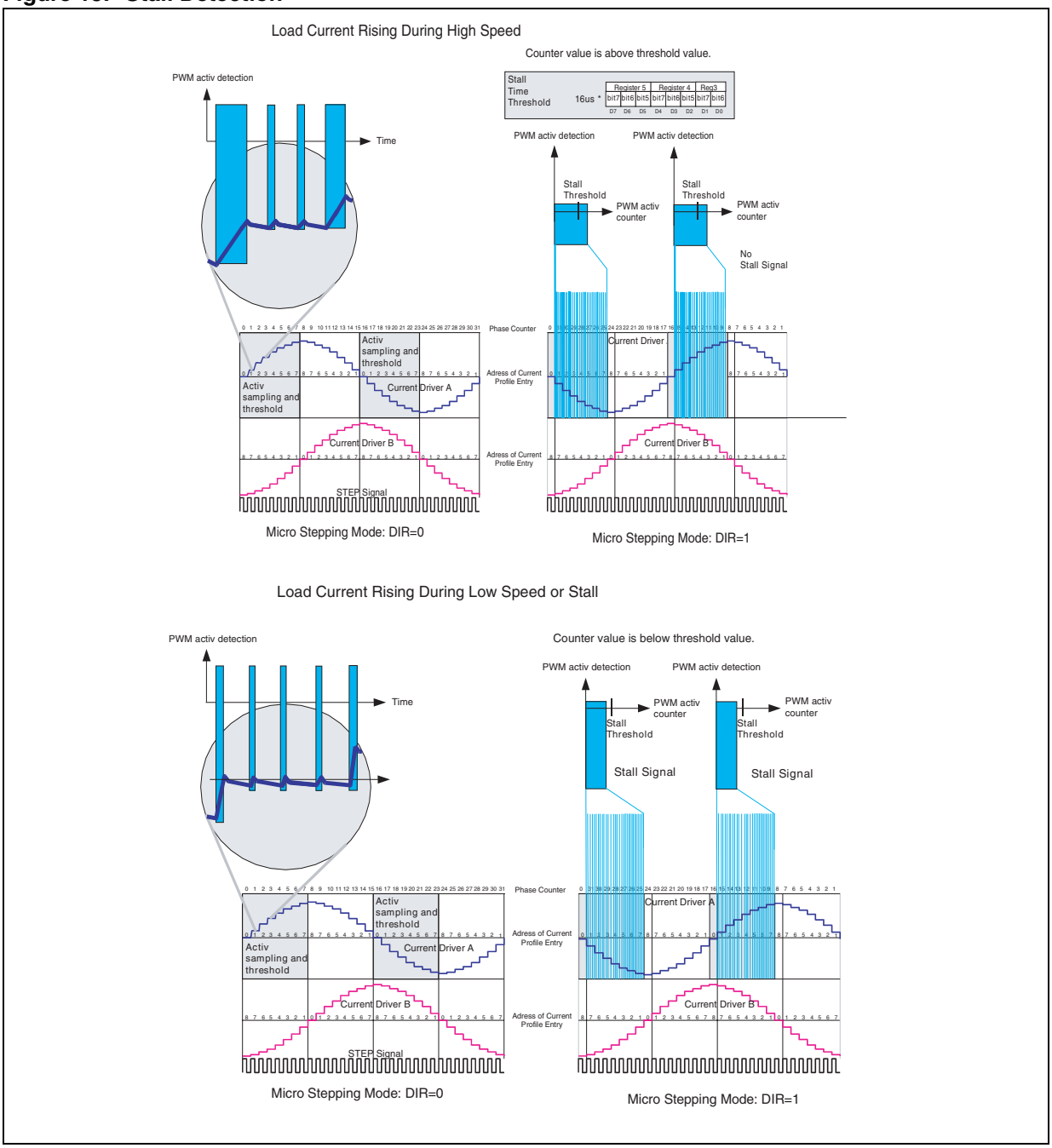


Figure 16. Reference Generation for PWM Control (Switch On)

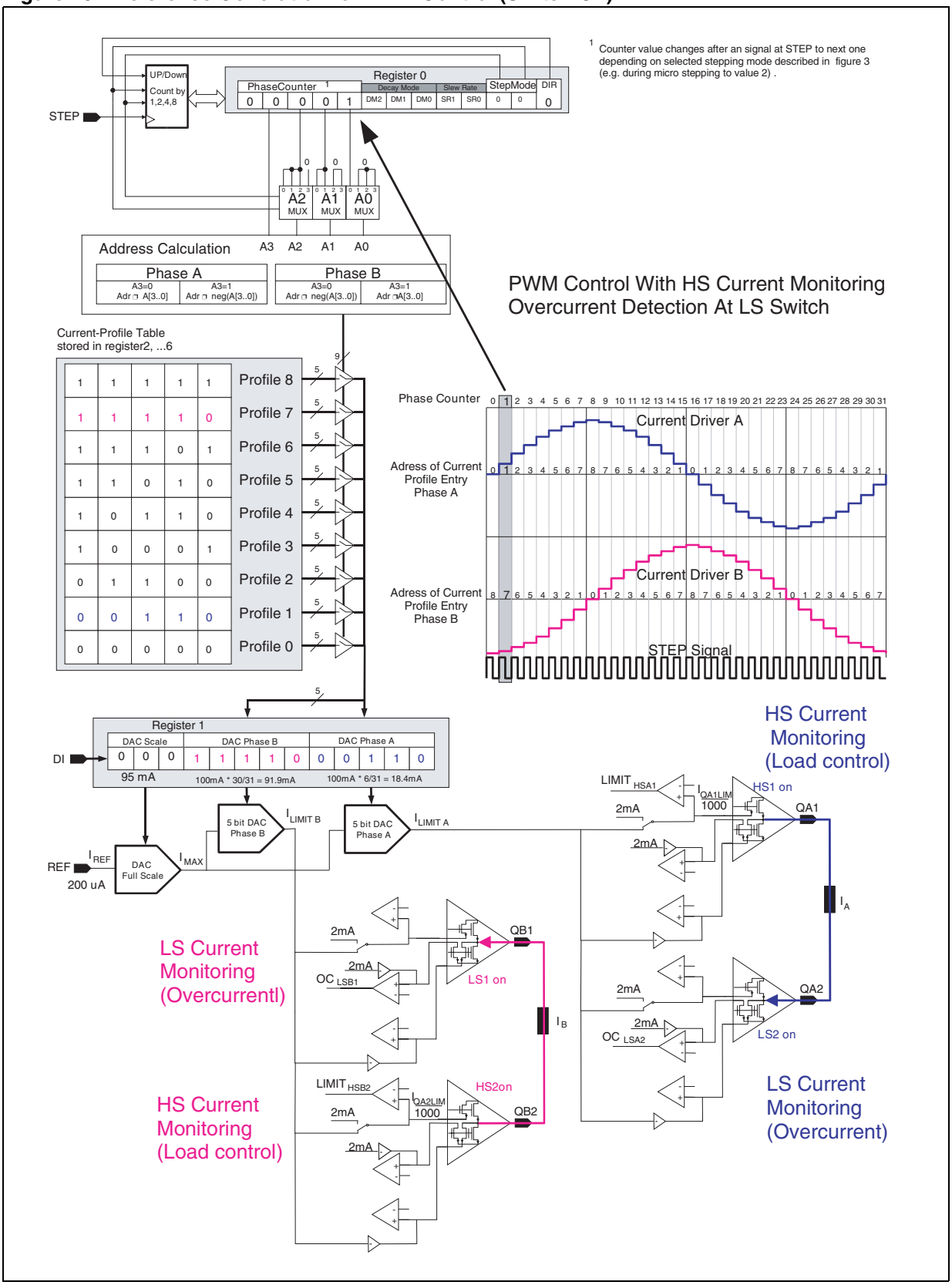
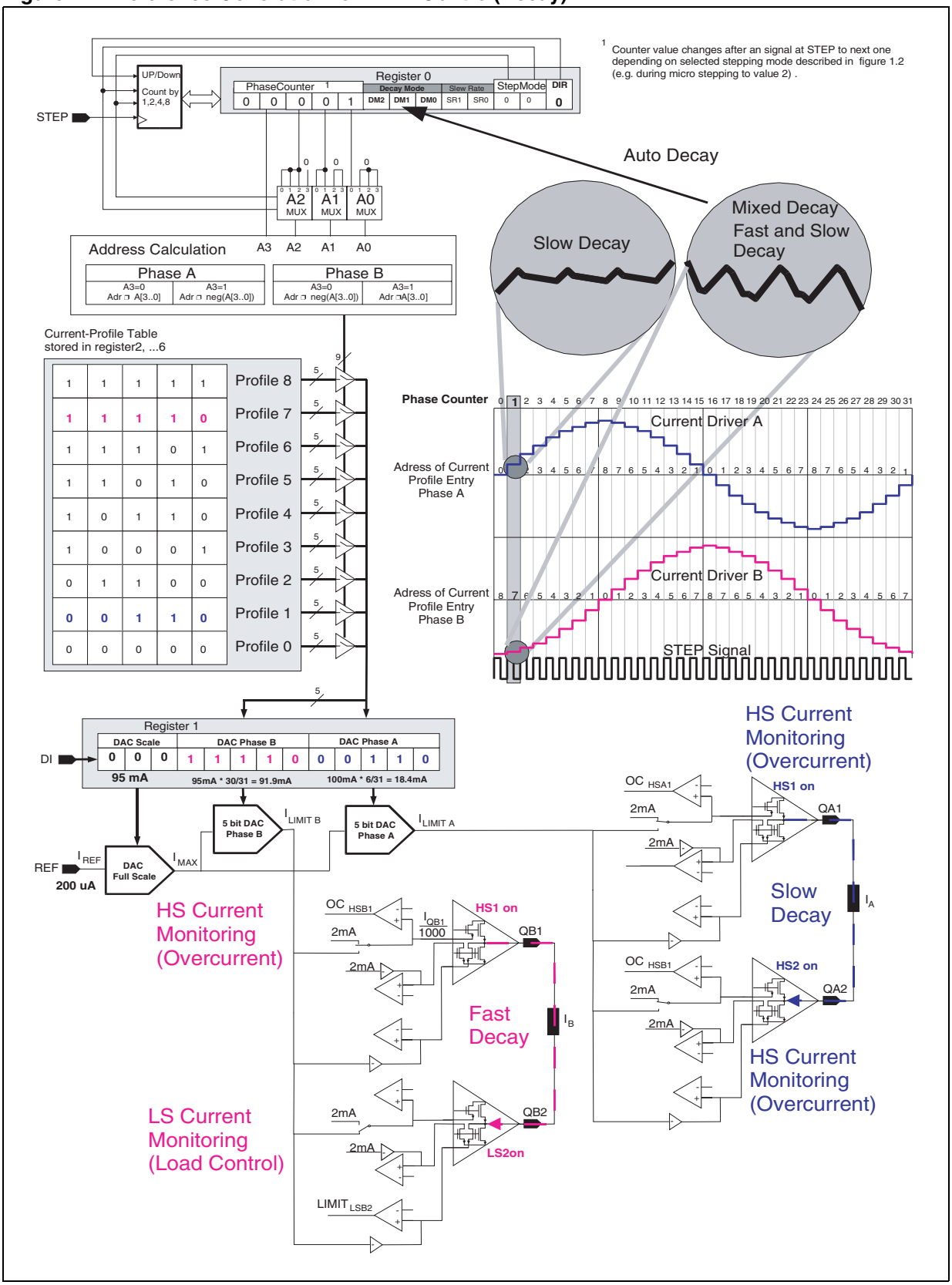


Figure 17. Reference Generation for PWM Contro (Decay)l



8 Package information

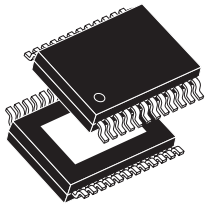
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

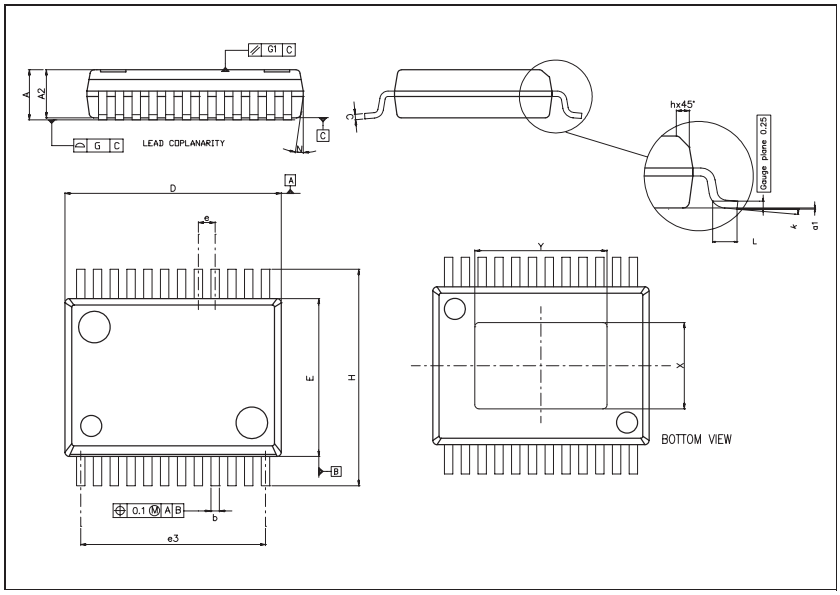
Figure 18. PowerSSO-24 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.15		2.47	0.085		0.097
A2	2.15		2.40	0.085		0.094
a1	0		0.075			0.003
b	0.33		0.51	0.013		0.02
c	0.23		0.32	0.009		0.012
D	10.10		10.50	0.398		0.413
E	7.4		7.6	0.291		0.299
e		0.8			0.031	
e3		8.8			0.346	
G			0.1			0.004
G1			0.06			0.002
H	10.1		10.5	0.398		0.413
k		5°			5°	
h			0.4			0.016
L	0.55		0.85	0.021		0.033
N			10°			10°
X	4.1		4.7	0.161		0.185
Y	6.5		7.1	0.256		0.279

OUTLINE AND MECHANICAL DATA



PowerSSO-24 (Exposed Pad)



9 Revision history

Date	Revision	Changes
7-Nov-2005	1	Initial release.

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