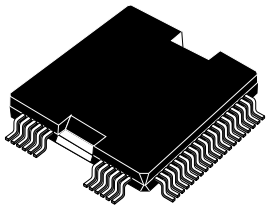
L9805

Super Smart Power Motor Driver with 8-BIT MCU, CAN Interface, 16K EPROM, 256Bytes RAM, 128 Bytes EEPROM, 10 Bit ADC, WDG, 2 Timers, 2 PWM Modules, Full H-Bridge Driver

PROUCT PREVIEW

- 6.4-18V Supply Operating Range
- 16 MHz Maximum Oscillator Frequency
- 8 MHz Maximum Internal Clock Frequency
- Oscillator Supervisor
- Fully Static operation
- -40°C to + 150°C Temperature Range
- User EPROM/OTP: 16 Kbytes
- Data RAM: 256 bytes
- Data EEPROM: 128 bytes
- 64 pin HiQUAD64 package
- 10 multifunctional bidirectional I/O lines
- Two 16-bit Timers, each featuring:
  - 2 Input Captures
  - 2 Output Compares
  - External Clock input (on Timer 1)
  - PWM and Pulse Generator modes
- Two Programmable 16-bit PWM generator modules.
- CAN peripheral including Bus line interface according 2A/B passive specifications
- 10-bit Analog-to-Digital Converter
- Software Watchdog for system integrity
- Master Reset, Power-On Reset, Low Voltage Reset



HiQUAD-64

ORDERING NUMBER: L9805

- 70mΩ DMOS H-bridge.
- 8-bit Data Manipulation
- 63 basic Instructions and 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on DOS/ WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)

This is preliminary information on a new product now in development. Details are subject to change without notice.

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1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The L9805 is a Super Smart Power device suited to drive resistive and inductive loads under software control. It includes a ST7 microcontroller and some pheripherals. The microcontroller can execute the software contained in the program EPROM/ROM and drive, through dedicated registers, the power bridge.

The internal voltage regulators rated to the automotive environment, PWM modules, CAN transceiver and controller, ISO 9141 transceiver, timers, temperature sensor and the AtoD converter allow the device to realize by itself a complete application, in line with the most common mechatronic requirements.

1.2 OTP, ROM AND EPROM DEVICES

For development purposes the device is available in plastic HiQuad package without window rating in the OTP class.

Mass production is supported by means of ROM devices.

Engineering samples could be assembled using window packages. These are generally referenced as “EPROM devices”.

EPROM devices are erased by exposure to high intensity UV light admitted through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current.

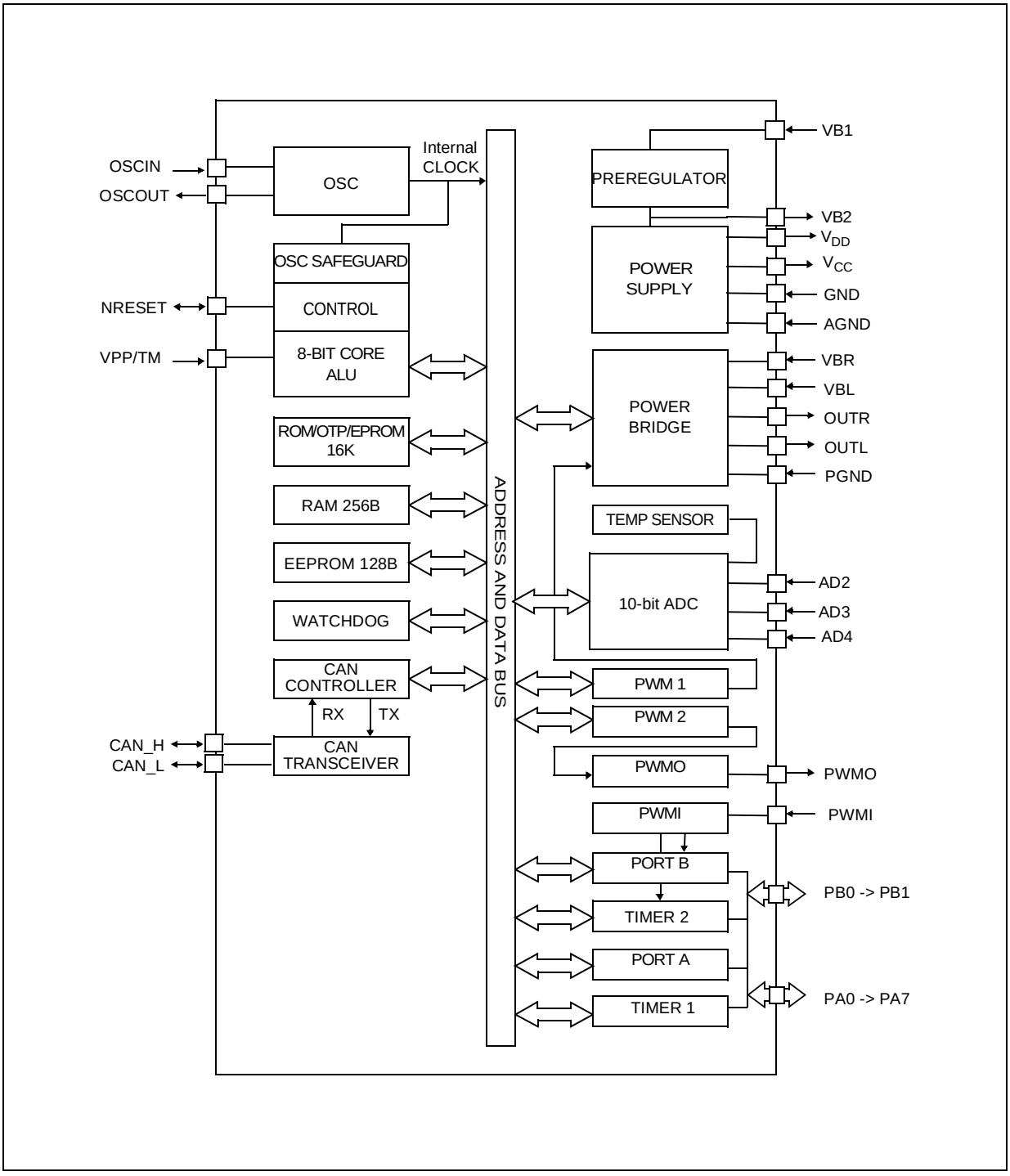
It is recommended to keep the L9805 device out of direct sunlight, since the UV content of sunlight can be sufficient to cause functional failure. Extended exposure to room level fluorescent lighting may also cause erasure.

An opaque coating (paint, tape, label, etc...) should be placed over the package window if the product is to be operated under these lighting conditions. Covering the window also reduces I_{DD} in power-saving modes due to photo-diode leakage currents.

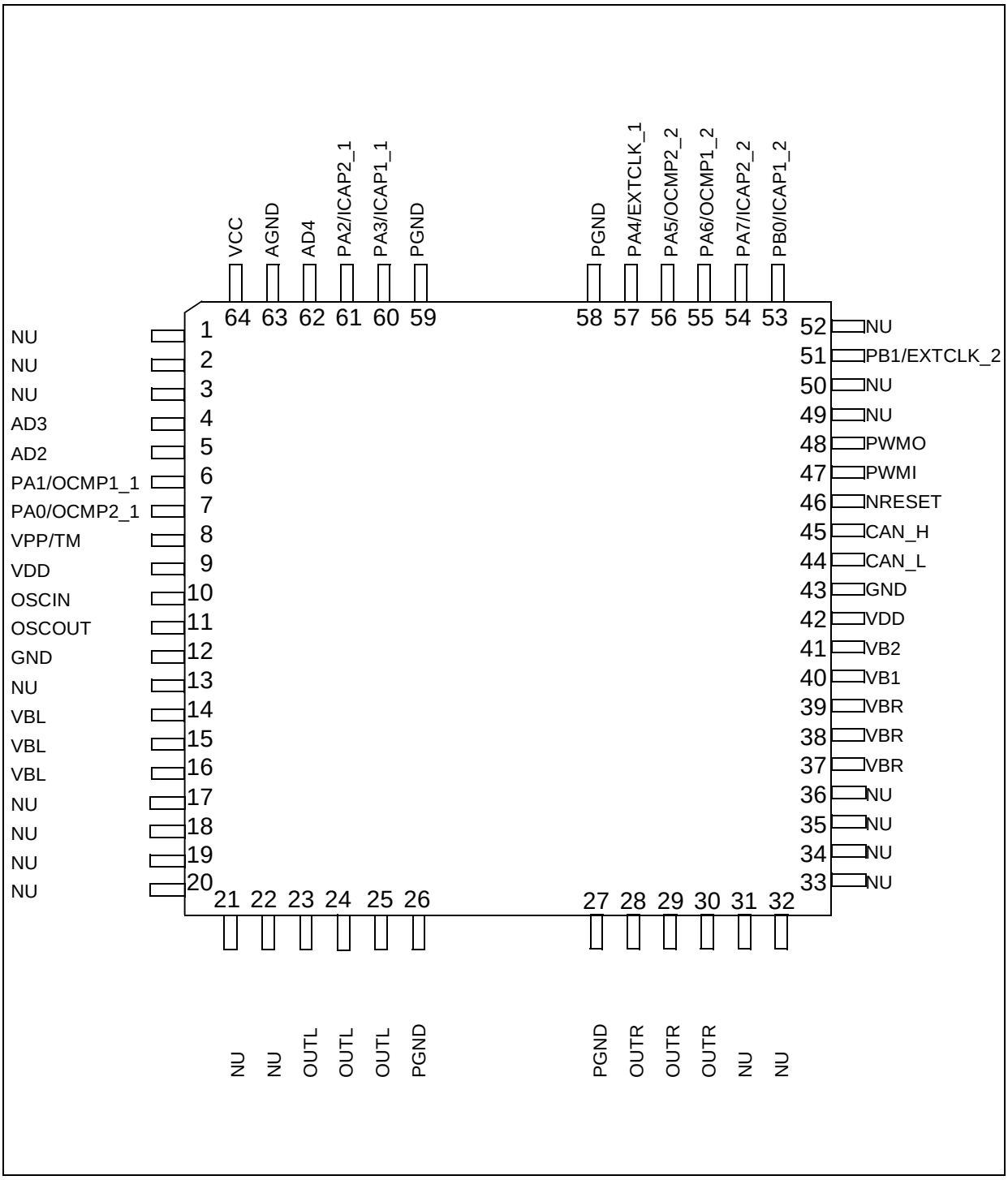
An Ultraviolet source of wave length 2537 Å yielding a total integrated dosage of 15 Watt-sec/cm^2 is required to erase the EPROM. The device will be erased in 40 to 45minutes if such a UV lamp with a 12mW/cm^2 power rating is placed 1 inch from the device window without any interposed filters.

OTP and EPROM devices can be programmed by a dedicated Eprom Programming Board and software that are part of the development tool-set.

Figure 1. L9805 Block Diagram



1.3 PIN OUT.


1 NU
2 NU
3 NU
4 AD3
5 AD2
6 PA1/OCMP1_1
7 PA0/OCMP2_1
8 VPP/TM
9 VDD
10 OSCIN
11 OSCOUT
12 GND
13 NU
14 VBL
15 VBL
16 VBL
17 NU
18 NU
19 NU
20 NU
21 NU
22 NU
23 OUTL
24 OUTL
25 OUTL
26 PGND
27 PGND
28 OUTR
29 OUTR
30 OUTR
31 NU
32 NU
33 NU
34 NU
35 NU
36 NU
37 VBR
38 VBR
39 VBR
40 VB1
41 VB2
42 VDD
43 GND
44 CAN_L
45 CAN_H
46 NRESET
47 PWMI
48 PWMO
49 NU
50 NU
51 PB1/EXTCLK_2
52 NU
53 PB0/ICAP1_2
54 PA7/ICAP2_2
55 PA6/OCMP1_2
56 PA5/OCMP2_2
57 PA4/EXTCLK_1
58 PGND
59 PGND
60 PA3/ICAP1_1
61 PA2/ICAP2_1
62 AD4
63 AGND
64 VCC

1.4 PIN DESCRIPTION

AD2-AD4: *Analog input to ADC.*

PA0/OCMP2_1-PA1/OCMP1_1: *I/Os or Output compares on Timer 1.* Alternate function software selectable (by setting OC2E or OC1E in CR2 register: bit 6 or 7 at 0031h). When used as an alternate function, this pin is a push-pull output as requested by Timer 1. Otherwise, this pin is a triggered floating input or a push-pull output.

PA2/ICAP2_1-PA3/ICAP1_1: I/*Os or Input captures on Timer 1.* Before using this I/O as alternate inputs, they must be configured by software in input mode (DDR=0). In this case, these pins are a triggered floating input. Otherwise (I/O function), these pin are triggered floating inputs or push-pull outputs.

PA4/EXTCLK_1: *PA4 I/O or External Clock on Timer 1*. Before using this I/O as alternate input, it must be configured by software in input mode (DDR=0). In this case, this pin is a triggered floating input. Otherwise (I/O function), this pin is a triggered floating input or a push-pull output.

PA5/OCMP2_2-PA6/OCMP1_2: *I/Os or Output Compares on Timer 2*. Alternate function software selectable (by setting OC2E or OC1E in CR2 register: bit 6 or 7 at 0041h). When used as alternate functions, these pins are push-pull outputs as requested by Timer 2. Otherwise, these pins are triggered floating inputs or push-pull outputs.

PA7/ICAP2_2-PB0/ICAP1_2: *I/Os or Input Captures on Timer 2*. Before using these I/Os as alternate inputs, they must be configured by software in input mode (DDR=0). In this case, these pins are triggered floating inputs. Otherwise (I/O function), these pins are triggered floating inputs or push-pull outputs.

PB1/EXTCLK_2: *PB1 I/O or External Clock on Timer 2*. Before using this I/O as alternate input, it must be configured by software in input mode (DDR=0). In this case, this pin is a triggered floating input. Otherwise (I/O function), this pin is a triggered floating input or a push-pull output.

VPP/TM: Input. This pin must be held low during normal operating modes.

VDD: Output. 5V Power supply for digital circuits, from internal voltage regulator.

OSCIN: Input Oscillator pin.

OSCOUT: Output Oscillator pin.

GND: Ground for digital circuits.

VBR: Power supply for Right half-bridge.

OUTR: Output of Left half-bridge.

PGND: Ground for power transistor.

OUTL: Output of Right half-bridge.

VBL: Power supply for Left half-bridge.

VB1: Power supply for voltage regulators.

VB2: Pre-regulated voltage for analog circuits.

CAN_L: Low side CAN bus output.

CAN_H: High side CAN bus input.

NRESET: Bidirectional. This active low signal forces the initialization of the MCU. This event is the top priority non maskable interrupt. It can be used to reset external peripherals.

PWMI: *PWM input.* Directly connected to Input Capture 2 on Timer 2.

PWMO: *PWM output.* Connected to the output of PWM2 module.

AGND: Ground for all analog circuitry (except power bridge)**.**

VCC: Output. 5V power supply for analog circuits, from internal voltage regulator.

1.5 REGISTER & MEMORY MAP

As shown in the Table 1, the MCU is capable of addressing 64K bytes of memories and I/O registers. In this MCU, 63742 of these bytes are user accessible.

The available memory locations consist of 128 bytes of I/O registers, 256 bytes of RAM, 128 bytes of EEPROM and 16Kbytes of user EPROM/ ROM. The RAM space includes 64bytes for the stack from 0140h to 017Fh.

The highest address bytes contain the user reset and interrupt vectors.

Table 1. Memory Map

Address	Block	Register Label	Register name	Reset Status	Remarks
0000h 0001h 0002h 0003h	Port A	PADR .. PADDR .. PAOR .. 	Data Register Data Direction Register Option Register Not Used	00h 00h 00h 	R/W R/W R/W Absent
0004h 0005h 0006h 0007h	Port B	PBDR .. PBDDR .. PBOR .. 	Data Register Data Direction Register Option Register Not Used	00h 00h 00h 	R/W R/W R/W Absent
0008h to 000Fh	RESERVED				
0010h 0011h 0012h 0013h 0014h 0015h 0016h	PWM1	P1CYRH .. P1CYRL .. P1DRH .. P1DRL .. P1CR .. P1CTH .. P1CTL ..	PWM1 Cycle Register High PWM1 Cycle Register Low PWM1 Duty Register High PWM1 Duty Register Low PWM1 Control Register PWM1 Counter Register High PWM1 Counter Register Low	00h 00h 00h 00h 00h 00h 00h	R/W R/W R/W R/W R/W Read Only Read Only
0017h	RESERVED				
0018h 0019h 001Ah 001Bh 001Ch 001Dh 001Eh	PWM2	P2CYRH .. P2CYRL .. P2DRH .. P2DRL .. P2CR .. P2CTH .. P2CTL ..	PWM2 Cycle Register High PWM2 Cycle Register Low PWM2 Duty Register High PWM2 Duty Register Low PWM2 Control Register PWM2 Counter Register High PWM2 Counter Register Low	00h 00h 00h 00h 00h 00h 00h	R/W R/W R/W R/W R/W Read Only Read Only
001Fh	RESERVED				
0020h		MISCR ..	Miscellaneous Register	00h	see Section 3.4
0021h	Power Bridge	PBCSR ..	Bridge Control Status Register	00h	R/W
0022h		DCSR ..	Dedicated Control Status Register	00h	R/W
0023h to 0029h	RESERVED				
002Ah 002Bh	WDG	WDGCR .. WDGSR ..	Watchdog Control Register Watchdog Status Register	7Fh 00h	R/W R/W
002Ch	EEPROM	EECR ..	EEPROM Control register	00h	R/W
002Dh 002Eh	EPROM	ECR1 ECR2	EPROM Control register 1 EPROM Control register 2		ST INTERNAL USE ONLY
002Fh 0030h	CRC	CRCL CRCH	CRCL Test Register CRCH Test Register		ST INTERNAL USE ONLY

Address	Block	Register Label	Register name	Reset Status	Remarks
0031h	TIM1	T1CR2 ..	Timer 1 Control Register2	00h	R/W
0032h		T1CR1 ..	Timer 1 Control Register1	00h	R/W
0033h		T1SR ..	Timer 1 Status Register	xxh	Read Only
0034h-0035h		T1IC1HR ..	Timer 1 Input Capture1 High Register	xxh	Read Only
		T1IC1LR ..	Timer 1 Input Capture1 Low Register	xxh	Read Only
0036h-0037h		T1OC1HR ..	Timer 1 Output Compare1 High Register	xxh	R/W
		T1OC1LR ..	Timer 1 Output Compare1 Low Register	xxh	R/W
0038h-0039h		T1CHR ..	Timer 1 Counter High Register	FFh	Read Only
		T1CLR ..	Timer 1 Counter Low Register	FCh	Read Only
003Ah-003Bh		T1ACHR ..	Timer 1 Alternate Counter High Register	FFh	Read Only
		T1ACLR ..	Timer 1 Alternate Counter Low RegisteR	FCh	Read Only
003Ch-003Dh		T1IC2HR ..	Timer 1 Input Capture2 High Register	xxh	Read Only
		T1IC2LR ..	Timer 1 Input Capture2 Low Register	xxh	Read Only
003Eh-003Fh		T1OC2HR ..	Timer 1 Output Compare2 High Register	xxh	R/W
		T1OC2LR ..	Timer 1 Output Compare2 Low Register	xxh	R/W
0040h	Reserved: Write Forbidden				
0041h	TIM2	T2CR2 ..	Timer 2 Control Register2	00h	R/W
0042h		T2CR1 ..	Timer 2 Control Register1	00h	R/W
0043h		T2SR ..	Timer 2 Status Register	xxh	Read Only
0044h-0045h		T2IC1HR ..	Timer 2 Input Capture1 High Register	xxh	Read Only
		T2IC1LR ..	Timer 2 Input Capture1 Low Register	xxh	Read Only
0046h-0047h		T2OC1HR ..	Timer 2 Output Compare1 High Register	xxh	R/W
		T2OC1LR ..	Timer 2 Output Compare1 Low Register	xxh	R/W
0048h-0049h		T2CHR ..	Timer 2 Counter High Register	FFh	Read Only
		T2CLR ..	Timer 2 Counter Low Register	FCh	Read Only
004Ah-004Bh		T2ACHR ..	Timer 2 Alternate Counter High Register	00h	Read Only
		T2ACLR ..	Timer 2 Alternate Counter Low Register	00h	Read Only
004Ch-004Dh		T2IC2HR ..	Timer 2 Input Capture2 High Register	xxh	Read Only
		T2IC2LR ..	Timer 2 Input Capture2 Low Register	xxh	Read Only
004Eh-004Fh		T2OC2HR ..	Timer 2 Output Compare2 High Register	xxh	R/W
		T2OC2LR ..	Timer 2 Output Compare2 Low Register	xxh	R/W
0050h to 0059h	RESERVED				
005Ah	CAN	CANISR ..	CAN Interrupt Status Register	00h	R/W
005Bh		CANICR ..	CAN Interrupt Control Register	00h	R/W
005Ch		CANCSR ..	CAN Control/Status Register	00h	R/W
005Dh		CANBRPR ..	CAN Baud Rate Prescaler	00h	R/W
005Eh		CANBTR ..	CAN Bit Timing Register	23h	R/W
005Fh		CANPSR ..	CAN Page Selection	00h	R/W
0060h to 006Fh			CAN First address to last address of PAGE X	--	see page mapping and register description
0070h	ADC	ADCDRH ..	ADC Data Register High	00h	Read Only
0071h		ADCDRL ..	ADC Data Register Low	00h	Read Only
0072h		ADCCSR ..	ADC Control/Status Register	20h	R/W

Address	Block	Description
0080h to 013Fh	RAM 256 Bytes including STACK 64 bytes (0140h to 017Fh)	User variables and subroutine nesting
0140h to 017Fh		
0180h to 0BFFh	RESERVED	
0C00h to 0C7Fh	EEPROM 128 bytes	including 4 bytes reserved for temperature sensor trimming (see Section 5.5.6) 0C7CH: T0H 0C7DH: T0L 0C7EH: VT0H 0C7FH: VT0L
0C80h to BFFFh	RESERVED	
C000 to FFDFh	EPROM 16K bytes (16384 bytes)	User application code and data
FFE0h to FFFFh		Interrupt and Reset Vectors

2 CENTRAL PROCESSING UNIT

2.1 INTRODUCTION

The CPU has a full 8-bit architecture. Six internal registers allow efficient 8-bit data manipulation. The CPU is capable of executing 63 basic instructions and features 17 main addressing modes.

2.2 CPU REGISTERS

The 6 CPU registers are shown in the programming model in Figure 2, on page 12. Following an interrupt, all registers except Y are pushed onto the stack in the order shown in Figure 3, on page 13. They are popped from stack in the reverse order.

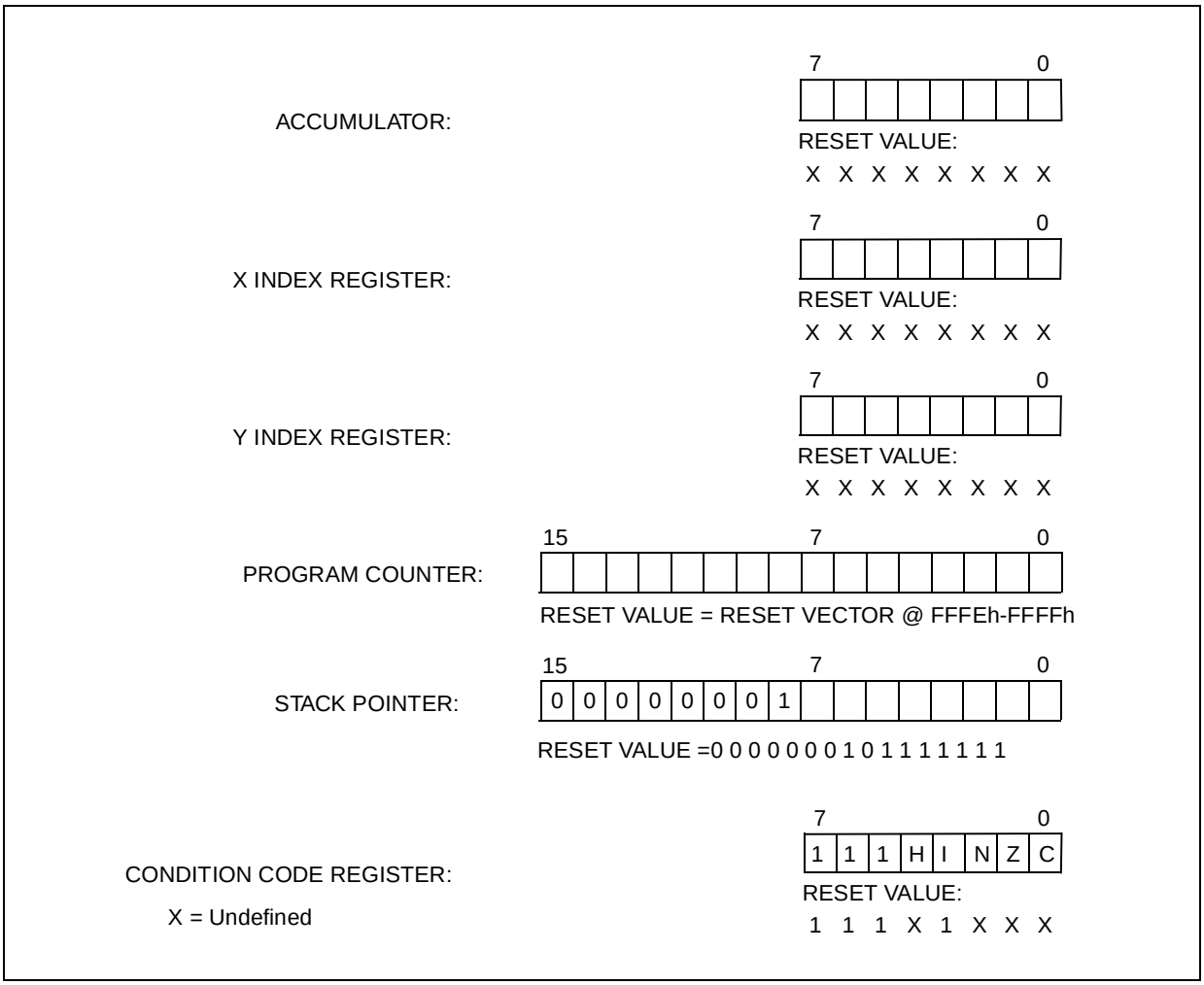
The Y register is not affected by these automatic procedures. The interrupt routine must therefore handle Y, if needed, through the PUSH and POP instructions.

Accumulator (A). The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations as well as data manipulations.

Index Registers (X and Y). These 8-bit registers are used to create effective addresses or as temporary storage areas for data manipulation. The Cross-Assembler generates a PRECEDE instruction (PRE) to indicate that the following instruction refers to the Y register.

Program Counter (PC). The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU.

Figure 2. Organization of Internal CPU Registers



CPU REGISTERS (Cont'd)

Stack Pointer (SP) The Stack Pointer is a 16-bit register. Since the stack is 64 bytes deep, the most significant bits are forced as indicated in Figure 2, on page 12 in order to address the stack as it is mapped in memory.

Following an MCU Reset, or after a Reset Stack Pointer instruction (RSP), the Stack Pointer is set to point to the next free location in the stack. It is then decremented after data has been pushed onto the stack and incremented before data is popped from the stack.

Note: When the lower limit is exceeded, the Stack Pointer wraps around to the stack upper limit, without indicating the stack overflow. The previously stored information is then overwritten and therefore lost.

The upper and lower limits of the stack area are shown in the Memory Map.

The stack is used to save the CPU context during subroutine calls or interrupts. The user may also directly manipulate the stack by means of the PUSH and POP instructions. In the case of an interrupt (refer to Figure 3), the PCL is stored at the first location pointed to by the SP. Then the other registers are stored in the next locations.

– When an interrupt is received, the SP is decremented and the context is pushed on the stack.
– On return from interrupt, the SP is incremented and the context is popped from the stack.

A subroutine call occupies two locations and an interrupt five locations in the stack area.

Condition Code Register (CC) The Condition Code register is a 5-bit register which indicates the result of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. The following paragraphs describe each bit of the CC register in turn.

Half carry bit (H) The H bit is set to 1 when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in BCD arithmetic subroutines.

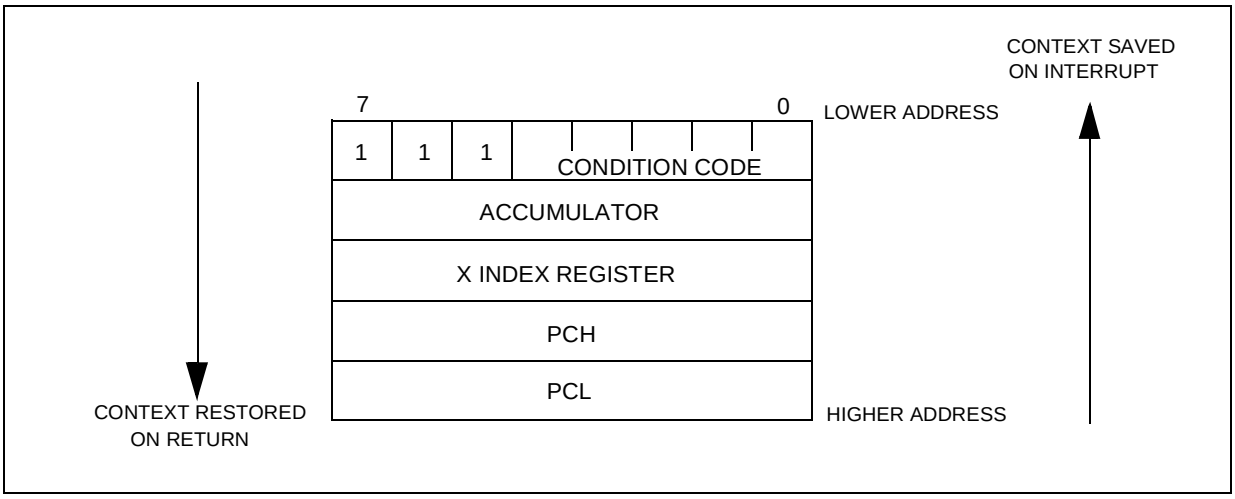
Interrupt mask (I) When the I bit is set to 1, all interrupts except the TRAP software interrupt are disabled. Clearing this bit enables interrupts to be passed to the processor core. Interrupts requested while I is set are latched and can be processed when I is cleared (only one interrupt request per interrupt enable flag can be latched).

Negative (N) When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is negative (i.e. the most significant bit is a logic 1).

Zero (Z) When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

Carry/Borrow (C) When set, C indicates that a carry or borrow out of the ALU occured during the last arithmetic operation. This bit is also affected during execution of bit test, branch, shift, rotate and store instructions.

Figure 3. Stack Manipulation on Interrupt



3 CLOCKS, RESET, INTERRUPTS & POWER SAVING MODES

3.1 CLOCK SYSTEM

3.1.1 General Description

The MCU accepts either a Crystal or Ceramic resonator, or an external clock signal to drive the internal oscillator. The internal clock (f_{CPU}) is derived from the external oscillator frequency (f_{OSC}). The external Oscillator clock is first divided by 2, and an additional division factor of 2, 4, 8, or 16 can be applied, in Slow Mode, to reduce the frequency of the f_{CPU}; this clock signal is also routed to the on-chip peripherals (except the CAN). The CPU clock signal consists of a square wave with a duty cycle of 50%.

The internal oscillator is designed to operate with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{osc}. The circuit shown in Figure 5 is recommended when using a crystal, and Table 2 lists the recommended capacitance and feedback resistance values. The crystal and associated components should be mounted as close as possible to the input pins in order to minimize output distortion and start-up stabilisation time.

Use of an external CMOS oscillator is recommended when crystals outside the specified frequency ranges are to be used.

Table 2. Recommended Values for 16 MHz Crystal Resonator

R_{SMAX}	40 Ω	60 Ω	150 Ω
C_{OSCIN}	56pF	47pF	22pF
C_{OSCOUT}	56pF	47pF	22pF
R_P	1-10 MΩ	1-10 MΩ	1-10 MΩ

Note: R_{SMAX} is the equivalent serial resistor of the crystal (see crystal specification).

C_{OSCIN},C_{OSCOUT}: Maximum total capacitances on pins OSCIN and OSCOUT (the value includes the external capacitance tied to the pin plus the parasitic capacitance of the board and of the device).

Rp: External shunt resistance. Recommended value for oscillator stability is 1MΩ.

Figure 4. External Clock Source Connections

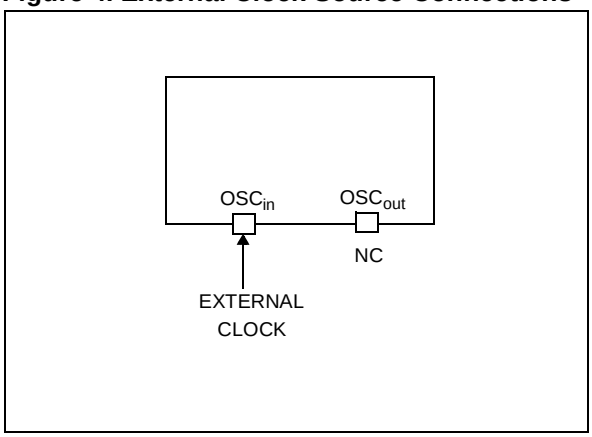


Figure 5. Crystal/Ceramic Resonator

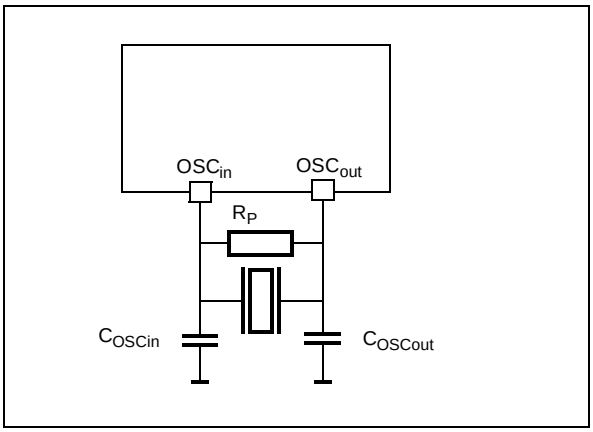
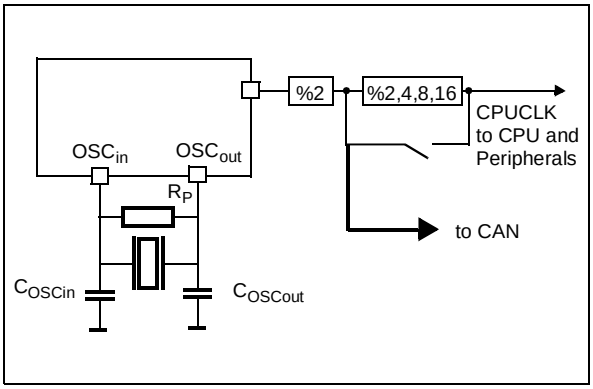


Figure 6. Clock Prescaler Block Diagram

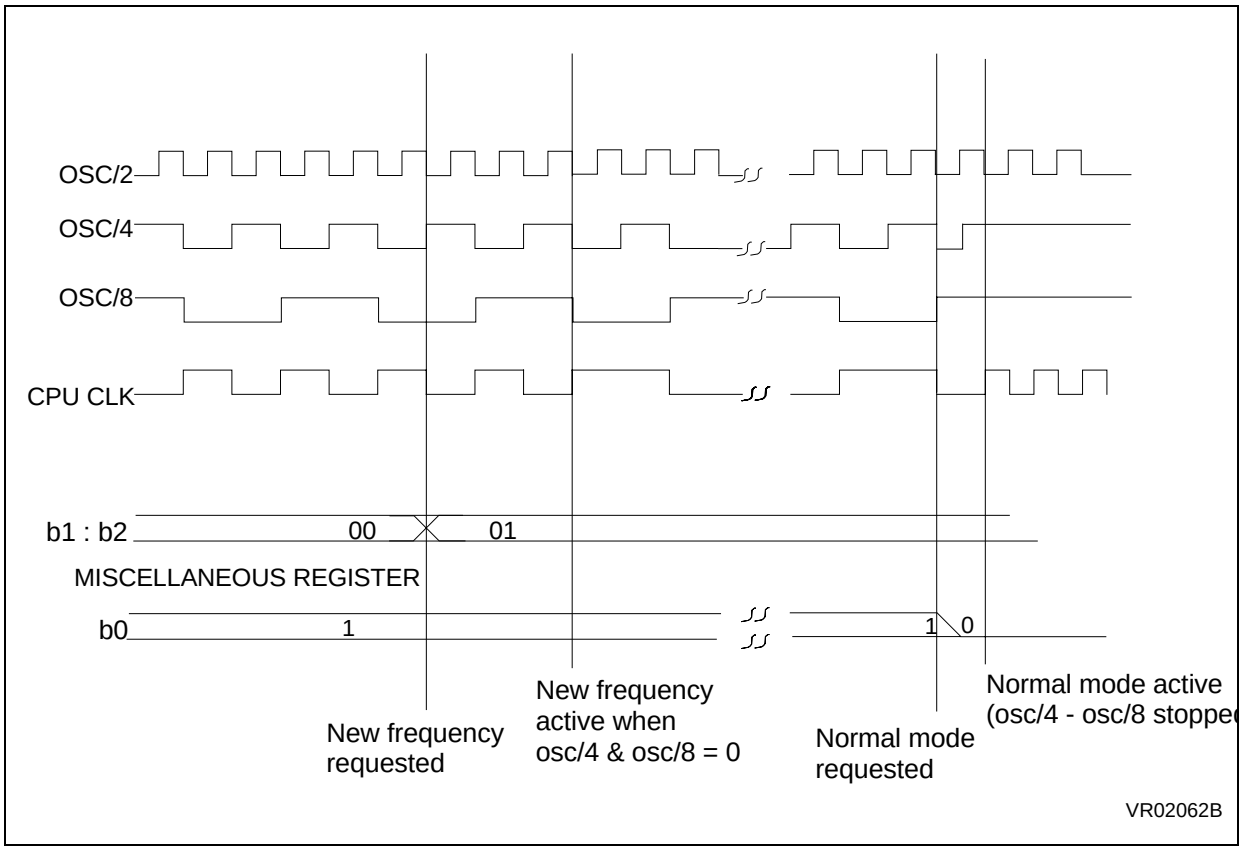


CLOCK SYSTEM (Cont'd)

3.1.2 External Clock

An external clock may be applied to the OSCIN input with the OSCOUT pin not connected, as shown on Figure 4. The t_{OXOV} specifications does not apply when using an external clock input. The equivalent specification of the external clock source should be used instead of t_{OXOV} (see).

Figure 7. Timing Diagram for Internal CPU Clock Frequency transitions



3.2 OSCILLATOR SAFEGUARD

The L9805 contains an oscillator safe guard function.

This function provides a real time check of the crystal oscillator generating a reset condition when the clock frequency has anomalous value.

If $f_{OSC}<f_{low}$, a reset is generated.

If $f_{OSC}>f_{high,}$ a reset is generated.

A flag in the Dedicated Control Status Register indicates if the last reset is a safeguard reset.

At the output of reset state the safeguard is disable. To activate the safeguard SFGEN bit must be set.

Notes: Following a reset, the safeguard is disabled. Once activated it cannot be disabled, except by a reset.

3.2.1 Dedicated Control Status Register

DCSR

Address 0022h - Read/Write

Reset Value:xx00 0000 (00h)

SGFL	SGFH	SFGEN	CANDS	b 3	b 2	b 1	PIEN

b6 = **SGFH:** Safeguard high flag. Set by an Oscillator Safeguard Reset generated for frequency too high, cleared by software (writing zero) or Power On / Low Voltage Reset. This flag is useful for distinguishing Safeguard Reset, Power On / Low Voltage Reset and Watchdog Reset.

b7 = **SGFL:** Safeguard low flag. Set by an Oscillator Safeguard Reset generated for frequency too low, cleared by software (writing zero) or Power On / Low Voltage Reset. This flag is useful for distinguishing Safeguard Reset, Power On / Low Voltage Reset and Watchdog Reset.

b5 = **SFGEN**: Safeguard enable when set. It's cleared only by hardware after a reset.

b4 = **CANDS**: CAN Transceiver disable. When this bit is set the CAN transceiver goes in Power Down Mode and does not work until this bit is reset. CANDS is 0 after reset so the standard condition is with the transceiver enabled. This bit can be used by application requiring low power consumption (see Section 5.7 for details).

b3,b2,b1 = **not used**

b0 = **PIEN**: PWMI input enable. When set, the PWMI input line is connected to Input Capture 2 of Timer 2. Otherwise, ICAP2_2 is the alternate function of PA7. See Figure 31 for the explanation of this function.

3.3 WATCHDOG SYSTEM (WDG)

3.3.1 Introduction

The Watchdog is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to give up its normal sequence. The Watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the counter's contents before it is decremented to zero.

3.3.2 Main Features

– Programmable Timer (64 increments of 12,288 CPU clock)

– Programmable Reset

– reset (if watchdog activated) after an HALT instruction or when bit timer MSB reaches zero

– Watchdog Reset indicated by status flag.

3.3.3 Functional Description

The counter value stored in the CR register (bits T6:T0), is decremented every 12,288 machine cycles, and the length of the timeout period can be programmed by the user in 64 increments.

If the watchdog is activated (the WDGA bit is set) and when the 7-bit timer (bits T6:T0) rolls over from 40h to 3Fh (T6 becomes cleared), it initiates a reset cycle pulling low the reset pin for typically 500ns.

The application program must write in the CR register at regular intervals during normal operation to prevent an MCU reset. The value to be stored in the CR register must be between FFh and C0h (see Table 1):

– The WDGA bit is set (watchdog enabled)

– The T6 bit is set to prevent generating an immediate reset

– The T5:T0 bit contain the number of increments which represents the time delay before the watchdog produces a reset.

Table 3. Watchdog Timing (f_{OSC} = 16 MHz)

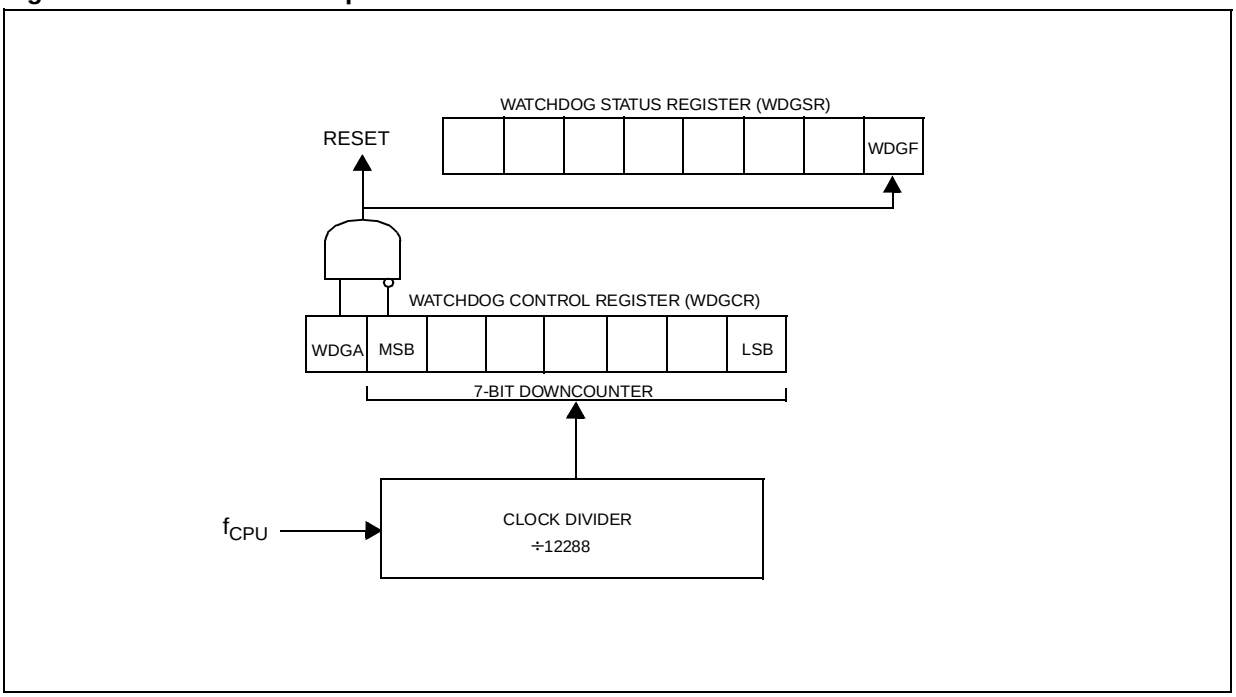
WDG Register initial value	WDG timeout period (ms)
7Fh	98.3
C0h	1.54

Notes: Following a reset, the watchdog is disabled. Once activated it cannot be disabled, except by a reset.

The T6 bit can be used to generate a software reset (the WDGA bit is set and the T6 bit is cleared).

If the watchdog is activated, the HALT instruction will generate a Reset.

Figure 8. Functional Description



WATCHDOG SYSTEM (Cont'd)

The Watchdog delay time is defined by bits 5-0 of the Watchdog register; bit 6 must always be set in order to avoid generating an immediate reset. Conversely, this can be used to generate a software reset (bit 7 = 1, bit 6 = 0).

The Watchdog must be reloaded before bit 6 is decremented to "0" to avoid a Reset. Following a Reset, the Watchdog register will contain 7Fh (bits 0-7).

If the circuit is not used as a Watchdog (i.e. bit 7 is never set), bits 6 to 0 may be used as a simple 7-bit timer, for instance as a real time clock. Since no reset will be generated under these conditions, the Watchdog control register must be monitored by software.

A flag in the watchdog status register indicates if the last reset is a watchdog reset or not, before clearing by a write of this register.

3.3.4 Register Description

3.3.4.1 Watchdog Control Register (WDGCR)

Register Address: 002Ah — Read/Write

Reset Value: 0111 1111 (7Fh)

7							0
WDGA	T6	T5	T4	T3	T2	T1	T0

b7 = **WDGA:** Activation bit.

This bit is set by software and only cleared by hardware after a reset. When WDGA = 1, the watchdog can generate a reset.

0: Watchdog disabled

1: Watchdog enabled.

b6-0 =**T6-T0**: 7 bit timer (Msb to Lsb)

These bits contain the decremented value. A reset is produced when it rolls over from 40h to 3Fh (T6 become cleared).

3.3.4.2 Watchdog Status Register (WDGSR)

Register Address: 002Bh — Read/Write

Reset Value(*): 0000 0000 (00h)

7							0
-	-	-	-	-	-	-	WDGF

b7-1 = **not used**

b0 = **WDGF:** Watchdog flag. Set by a Watchdog Reset, cleared by software (writing zero) or Power On / Low Voltage Reset. This flag is useful for distinguishing Power On / Low Voltage Reset and Watchdog Reset.

(*): Except in the case of Watchdog Reset.

3.4 MISCELLANEOUS REGISTER

(MISCR)

The Miscellaneous register allows the user to select the Slow operating mode and to set the clock division prescaler factor. Bits 3, 4 determine the signal conditions which will trigger an interrupt request on I/O pins having interrupt capability.

Register Address: 0020h — Read/Write

Reset Value:0000 0000 (00h)

b7	b6	b5	b4	b3	b2	b1	b0

b0 - *Slow Mode Select*

0- Normal mode - Oscillator frequency / 2 (Reset state)

1- Slow mode (Bits b1 and b2 define the prescaler factor)

b1, b2 - *CPU clock prescaler for Slow Mode*

b2	b1	Option
0	0	Oscillator frequency / 4
1	0	Oscillator frequency / 8
0	1	Oscillator frequency / 16
1	1	Oscillator frequency / 32

b4	b3	Option
0	0	Falling edge and low level (Reset state)
1	0	Falling edge only
0	1	Rising edge only
1	1	Rising and Falling edge

The selection issued from b3/b4 combination is applied to PA[0]..PA[7],PB0,PB1 external interrupt. The selection can be made only if I bit in CC register is reset (interrupt enabled).

b3, b4 can be written only when the Interrupt Mask (I) of the CC (Condition Code) register is set to 1.

b5,b6,b7 = **not used**

3.5 RESET

3.5.1 Introduction

There are four sources of Reset:

– NRESET pin (external source)

– Power-On Reset / Low Voltage Detection (Internal source)

– WATCHDOG (Internal Source)

– SAFEGUARD (Internal source)

The Reset Service Routine vector is located at address FFFEh-FFFFh.

3.5.2 External Reset

The NRESET pin is both an input and an open-drain output with integrated pull-up resistor. When one of the internal Reset sources is active, the Reset pin is driven low to reset the whole application.

3.5.3 Reset Operation

The duration of the Reset condition, which is also reflected on the output pin, is fixed at 4096 internal CPU Clock cycles. A Reset signal originating from an external source must have a duration of at least 1.5 internal CPU Clock cycles in order to be recognised. At the end of the Power-On Reset cycle, the MCU may be held in the Reset condition by an External Reset signal. The NRESET pin may thus be used to ensure V_{DD} has risen to a point where the MCU can operate correctly before the user program is run. Following a Power-On Reset event, or after exiting Halt mode, a 4096 CPU Clock cycle delay period is initiated in order to allow the oscillator to stabilise and to ensure that recovery has taken place from the Reset state.

During the Reset cycle, the device Reset pin acts as an output that is pulsed low. In its high state, an internal pull-up resistor of about 300KΩ is connected to the Reset pin. This resistor can be pulled low by external circuitry to reset the device.

3.5.4 Power-on Reset - Low Voltage Detection

The POR/LVD function generates a static reset when the supply voltage is below a reference value. In this way, the Power-On Reset and Low Voltage Reset function are provided, in order to keep the system in safe condition when the voltage is too low.

The Power-Up and Power-Down thresholds are different, in order to avoid spurious reset when the MCU starts running and sinks current from the supply.

The LVD reset circuitry generates a reset when V_{DD} is below:

– $V_{ResetON}$ when V_{DD} is rising

– $V_{ResetOFF}$ when V_{DD} is falling

The POR/LVD function is explained in Figure 9.

Power-On Reset activates the reset pull up transistor performing a complete chip reset. In the same way a reset can be triggered by the watchdog, by the safeguard or by external low level at NRESET pin. An external capacitor connected between NRESET and ground can extend the power on reset period if required.

Figure 9. Power Up/Down behaviour

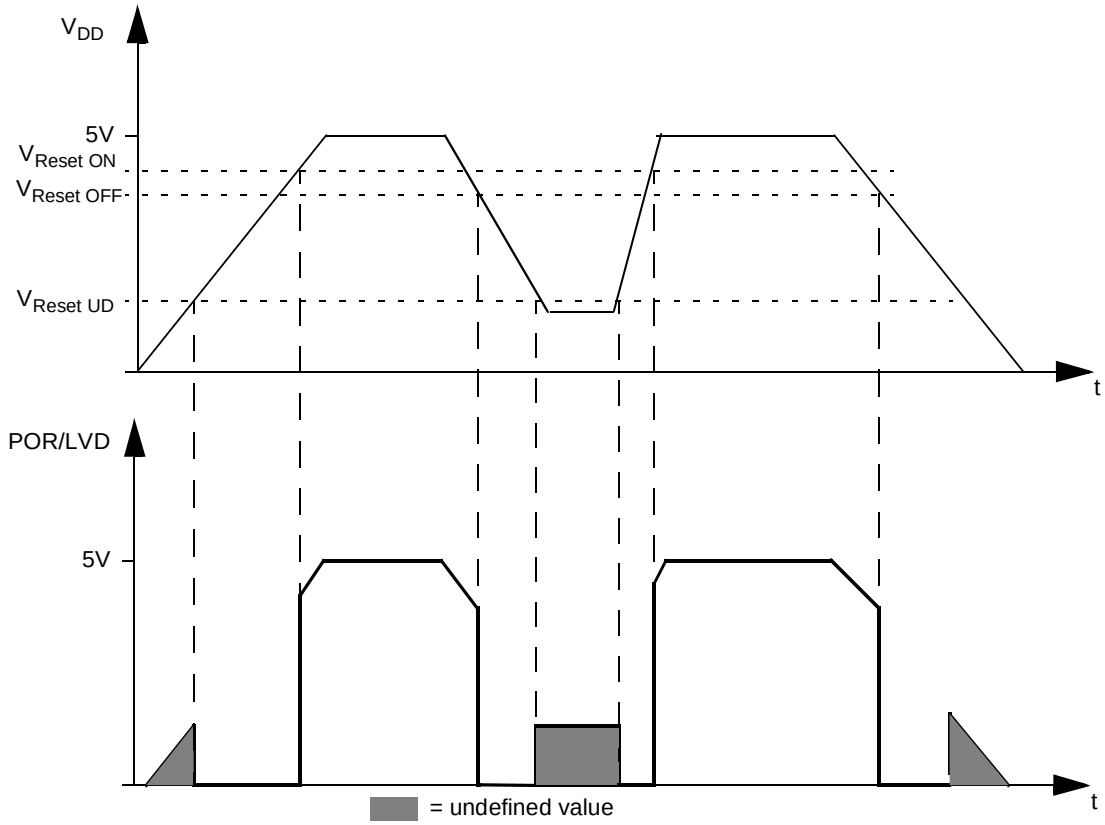
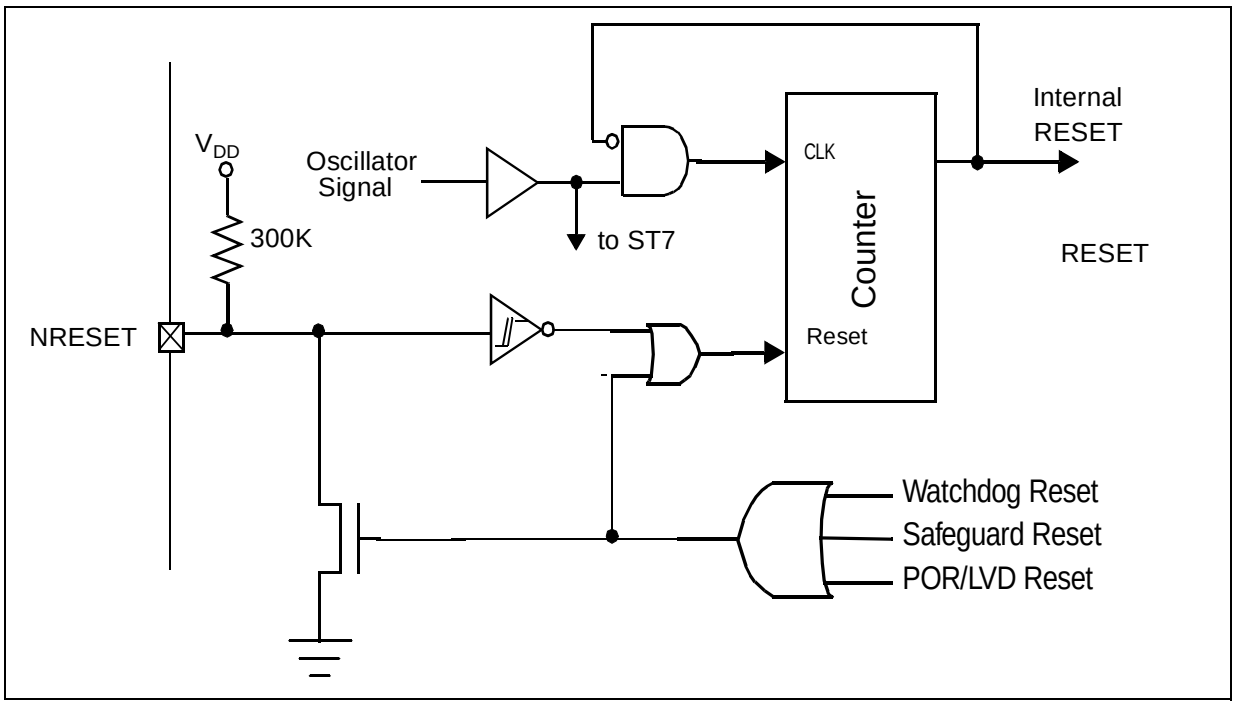


Figure 10. Reset Block Diagram



3.6 INTERRUPTS

A list of interrupt sources is given in Table 4 below, together with relevant details for each source. Interrupts are serviced according to their order of priority, starting with I0, which has the highest priority, and so to I12, which has the lowest priority.

The following list describes the origins for each interrupt level:

– I0 connected to Ports PA0-PA7, PB0-PB1
– I1 connected to CAN
– I2 connected to Power Diagnostics
– I3 connected to Output Compare of Timer 1
– I4 connected to Input Capture of TImer 1
– I5 connected to Timer 1 Overflow
– I6 connected to Output Compare of Timer 2
– I7 connected to Input Capture of TImer 2
– I8 connected to Timer 2 Overflow
– I9 connected to ADC End Of Conversion
– I10 connected to PWM 1 Overflow
– I11 connected to PWM 2 Overflow
– I12 connected to EEPROM

Exit from Halt mode may only be triggered by an External Interrupt on one of the following ports: PA0-PA7 (I0), PB0-PB1 (I0), or by an Internal Interrupt coming from CAN peripheral (I1).

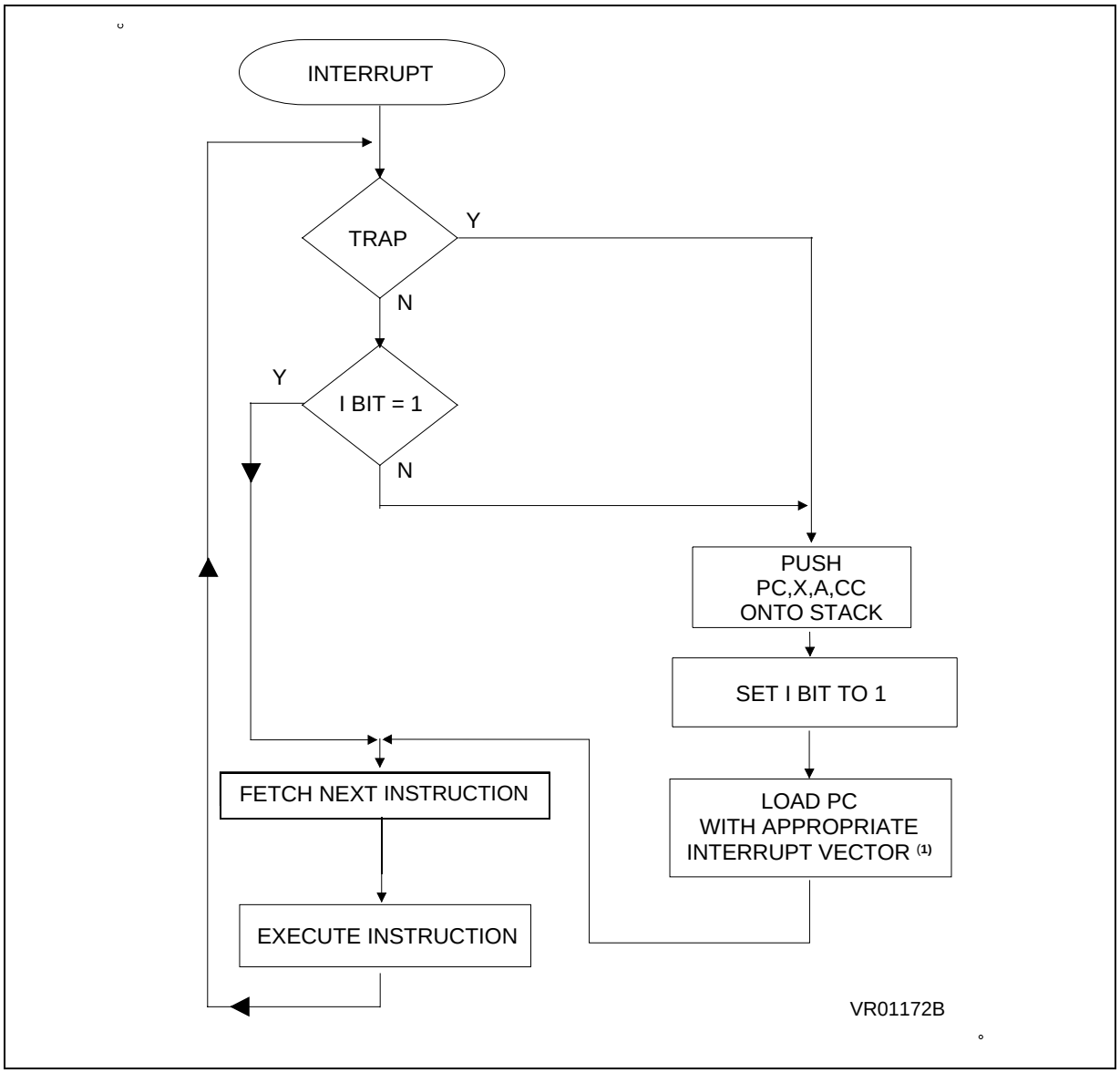
If more than one input pin of a group connected to the same interrupt line are selected simultaneously, the OR of this signals generates the interrupt.

Table 4. Interrupt Mapping

Interrupts	Register	Flag name	Interrupt source	Vector Address
Reset	N/A	N/A	-	FFFEh-FFFFh
Software	N/A	N/A	-	FFFCh-FFFDh
Ext. Interrupt (Ports PA0-PA7, PB0-PB1)	N/A	N/A	I0	FFFAh-FFFBh
Receive Interrupt Flag	CAN Status	RXIFi	I1	FFF8h-FFF9h
Transmit Interrupt Flag		TXIF		
Error Interrupt Pending		EPND		
Power Bridge Short Circuit	Bridge Control Status	SC	I2	FFF6h-FFF7h
Overtemperature		OVT		
Output Compare 1	Timer 1 Status	OCF1_1	I3	FFF4h-FFF5h
Output Compare 2		OCF2_1		
Input Capture 1	Timer 1 Status	ICF1_1	I4	FFF2h-FFF3h
Input Capture 2		ICF2_1		
Timer Overflow	Timer 1 Status	TOF_1	I5	FFF0h-FFF1h
Output Compare 1	Timer 2 Status	OCF1_2	I6	FFEEh-FFEFh
Output Compare 2		OCF2_2		
Input Capture 1	Timer 2 Status	ICF1_2	I7	FFECh-FFEDh
Input Capture 2		ICF2_2		
Timer Overflow	Timer 2 Status	TOF_2	I8	FFEAh-FFEBh
ADC End Of Conversion	ADC Control	EOC	I9	FFE8h-FFE9h
PWM 1 Overflow	N/A	N/A	I10	FFE6h-FFE7h
PWM 2 Overflow	N/A	N/A	I11	FFE4h-FFE5h
EEPROM Programming	EEPROM Control	E2ITE	I12	FFE2h-FFE3h

INTERRUPTS (Cont'd)

Figure 11. Interrupt Processing Flowchart



Note 1. See Table 4

3.7 POWER SAVING MODES

3.7.1 Introduction

There are three Power Saving modes. The Slow Mode may be selected by setting the relevant bits in the Miscellaneous register as detailed in Section 3.4. Wait and Halt modes may be entered using the WFI and HALT instructions.

3.7.2 Slow Mode

In Slow mode, the oscillator frequency can be divided by 4, 8, 16 or 32 rather than by 2. The CPU and peripherals (except CAN, see Note) are clocked at this lower frequency. Slow mode is used to reduce power consumption.

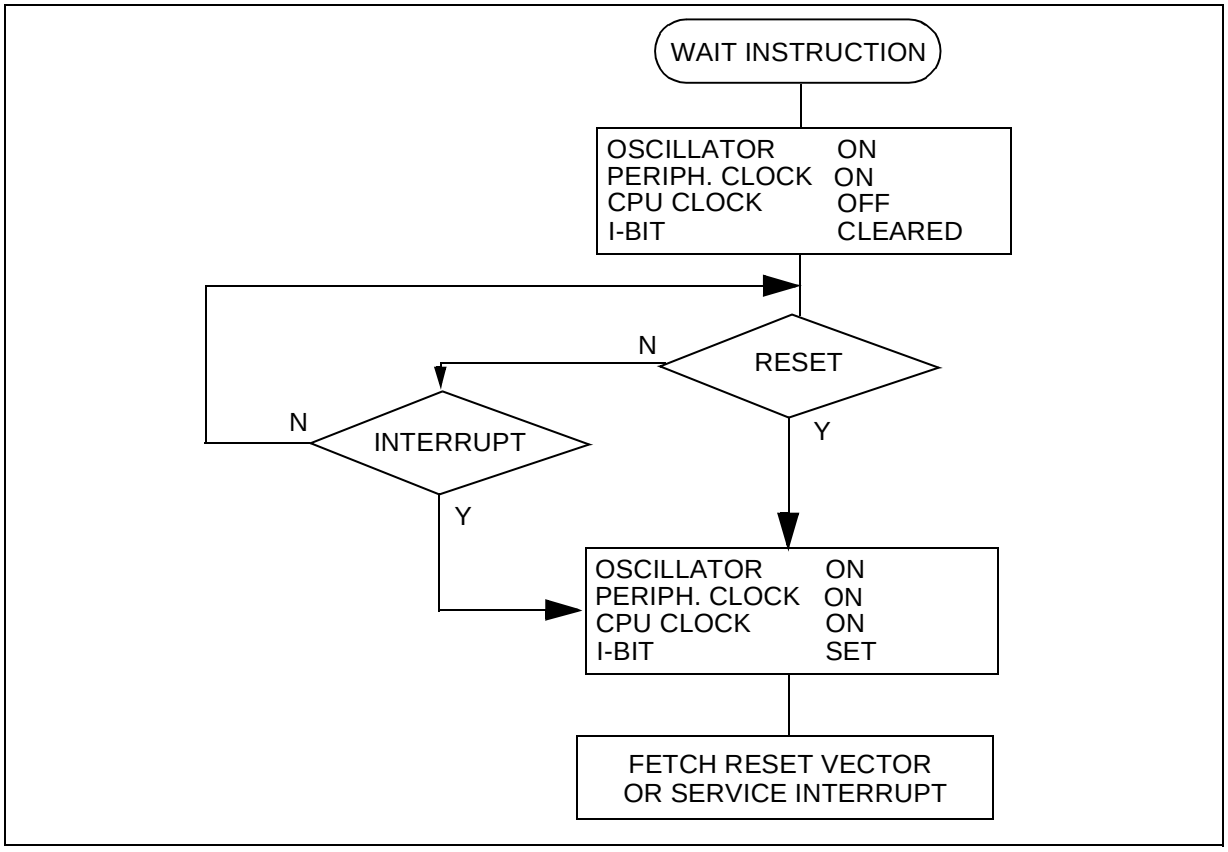
Note: Before entering Slow mode and to guarantee low power operations, the CAN Controller must be placed by software in STANDBY mode.

3.7.3 Wait Mode

Wait mode places the MCU in a low power consumption mode by stopping the CPU. All peripherals remain active. During Wait mode, the I bit (CC Register) is cleared, so as to enable all interrupts. All other registers and memory remain unchanged. The MCU will remain in Wait mode until an Interrupt or Reset occurs, whereupon the Program Counter branches to the starting address of the Interrupt or Reset Service Routine.
The MCU will remain in Wait mode until a Reset or an Interrupt (coming from CAN, Timers 1 & 2, EEPROM, ADC, PWM 1 & 2, I/O ports peripherals and Power Bridge) occurs, causing its wake-up.

Refer to Figure 12 below.

Figure 12. Wait Mode Flow Chart



POWER SAVING MODES (Cont'd)

3.7.4 Halt Mode

The Halt mode is the MCU lowest power consumption mode. The Halt mode is entered by executing the HALT instruction. The internal oscillator is then turned off, causing all internal processing to be stopped, including the operation of the on-chip peripherals.

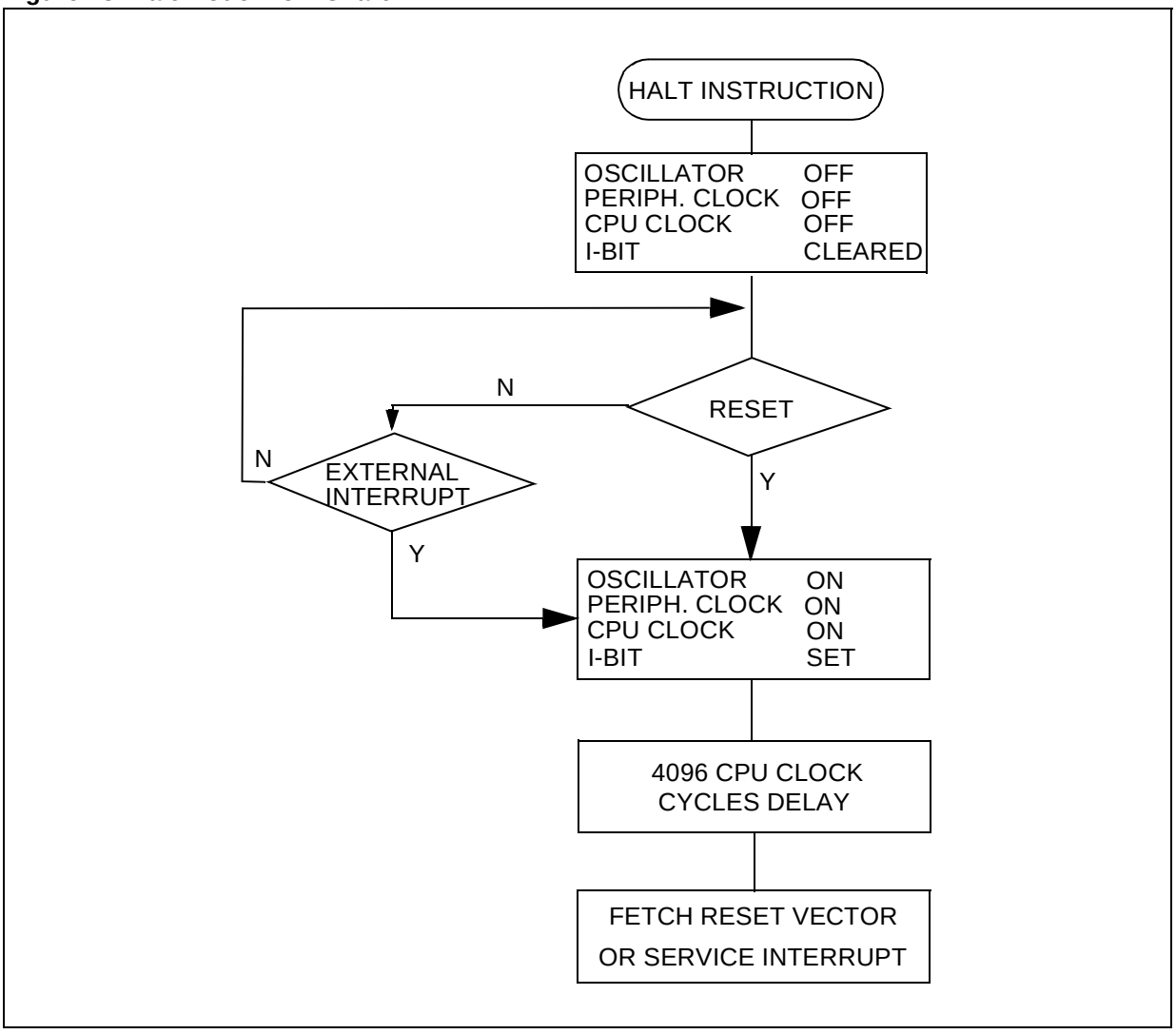
When entering Halt mode, the I bit in the CC Register is cleared so as to enable External Interrupts. If an interrupt occurs, the CPU becomes active.

The MCU can exit the Halt mode upon reception of either an external interrupt (I0), a internal interrupt coming from the CAN peripheral (I1) or a reset. The oscillator is then turned on and a stabilisation time is provided before releasing CPU operation. The stabilisation time is 4096 CPU clock cycles.
After the start up delay, the CPU continues operation by servicing the interrupt which wakes it up or by fetching the reset vector if a reset wakes it up.

Note The Halt mode cannot be used when the watchdog or the Safeguard are enabled, if the HALT instruction is executed while the watchdog or safeguard system are enabled, a reset is automatically generated thus resetting the entire MCU.

Note Halt Mode affects only the digital section of the device. All the analog circuit remain in their status, including ADC, voltage regulators, bus transceivers and power bridge.

Figure 13. Halt Mode Flow Chart



4 VOLTAGE REGULATOR

4.1 Introduction

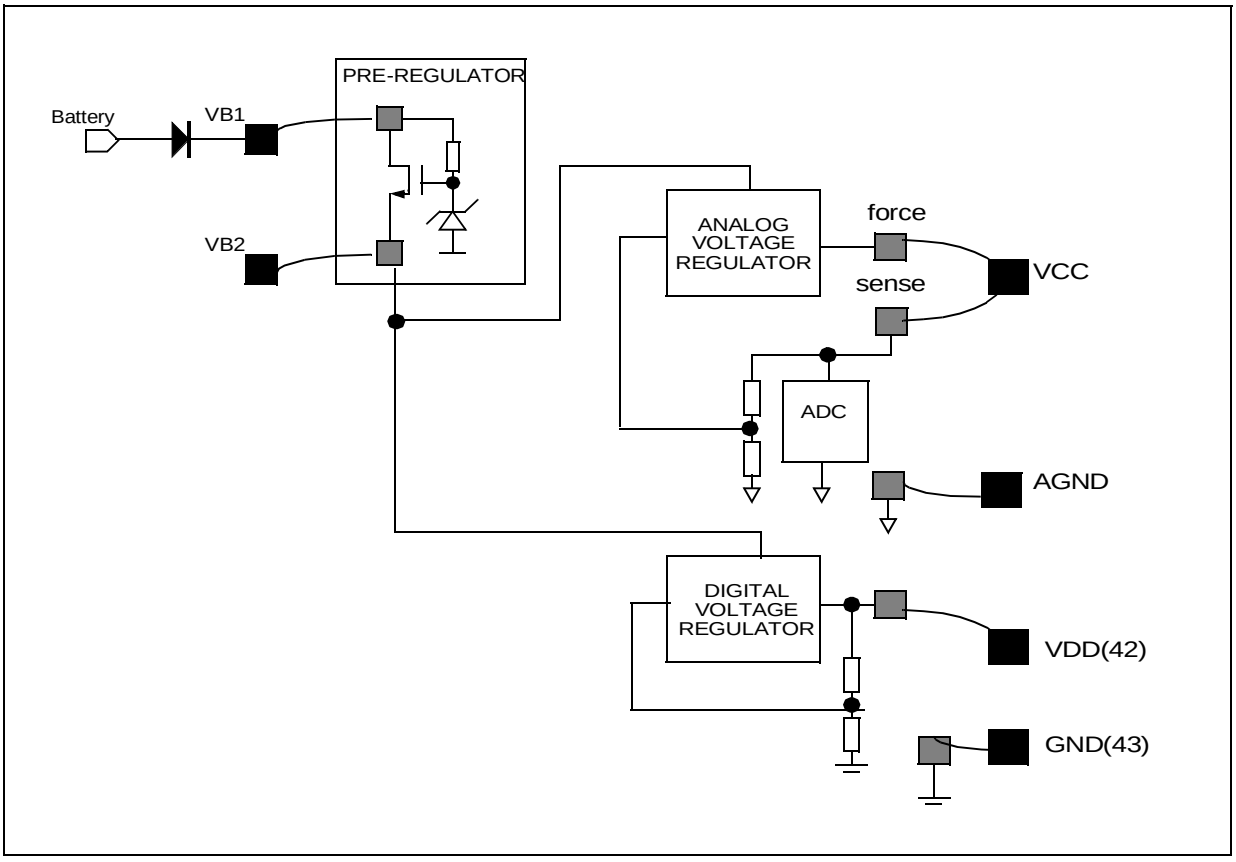
The on chip voltage regulator provides two regulated voltage, nominally 5V both. VCC supplies ADC and the analog periphery and VDD supplies the microcontroller and logic parts. These voltage are available at pins VDD and VCC to supply external components and connects a capacitors to optimize EMI performance. A pre-regulator circuit allows to connect external tantalum capacitors to a lower (10V) voltage (VB2 pin).

4.1.1 Functional Description

The main supply voltage is taken from VB1 pin. A voltage pre-regulator provides the regulated voltage on pin VB2. VB2 is the supply for the digital and analog regulators. The block diagram shows the connections between the regulators and the external pins.

In order to prevent negative spikes on the battery line to propagate on the internal supply generating spurious reset, a series diode supply VB1 pin is recommended.

Figure 14. Voltage regulation block diagram



4.2 Digital Section Power Supply

The digital supply voltage VDD is available at pin number 42 and 9. The digital ground GND is available at pin number 43 and 12.

Pin 42 and 43 are the actual voltage regulator output and external loads must be supply by these pin. The 100nF compensation capacitor should be connected as close as possible to pin 42 and 43.

Pin number 9 and 12 provide an external access to the internal oscillator supply. Resonator's capacitors should be grounded on pin 12.

The application board can improve noise reduction in the chip connecting directly pin 42 to pin 9 and pin 43 to pin 12 using traces as short as possible. An additional capacitor mounted close to pin 9 and 12 can lead additional improvement.

4.2.1 VDD Short Circuit Protection

The output current of the digital voltage regulator is controlled by a circuit that limits it to a maximum value (I_{MAXVDD}). When the output current exceeds this value the VDD voltage starts falling down. External loads must be chosen taking in account this maximum current capability of the regulator.

4.3 Analog Section Power Supply

The analog supply voltage is available on VCC pin. The external 100nF compensation capacitor should be placed as close as possible to this pin and AGND pin.

VCC is the reference voltage for the AD conversion and must be used to supply ratiometric sensors feeding AD inputs. Any voltage drop between VCC pin and the sensor supply pin on the application board, will cause the ADC to be inaccurate when reading the sensor's output.

4.3.1 VCC Short Circuit Protection

The output current of the analog voltage regulator is controlled by a circuit that limits it to a maximum value (I_{MAXVCC}). When the output current exceeds this value the VCC voltage starts falling down. External loads must be chosen taking in account this maximum current capability of the regulator.

WARNING: The pin VB2 is not short circuit protected so a short circuit on this pin will destroy the device.

5 ON-CHIP PERIPHERALS

5.1 I/O PORTS

5.1.1 Introduction

The internal I/O ports allow the transfer of data through digital inputs and outputs, the interrupt generation coming from an I/O and for specific pins, the input/output of alternate signals for the on-chip peripherals (TIMERS...).

Each pin can be programmed independently as digital input (with or without interrupt generation) or digital output.

5.1.2 Functional Description

Each I/O pin may be programmed independently as a digital input or a digital output, using the corresponding register bits.

Each port pin of the I/O Ports can be individually configured under software control as either input or output.

Each bit of a Data Direction Register (DDR) corresponds to an I/O pin of the associated port. This corresponding bit must be set to configure its associated pin as output and must be cleared to configure its associated pin as input. The Data Direction Registers can be read and written.

5.1.2.1 Input Mode

When DDR=0, the corresponding I/O is configured in Input mode.
In this case, the output buffer is switched off, the state of the I/O is readable through the Data Register address, but the I/O state comes directly from the Schmitt-Trigger output and not from the Data Register output.

5.1.2.2 Interrupt function

When an I/O is configured in Input with Interrupt generation mode (DDR=0 and OR=1), a low level or any transition on this I/O (according to the Miscellaneous register configuration - see Section 3.4, “b3, b4 External Interrupt Option”) will generate an Interrupt request to the CPU.

Each pin can independently generate an Interrupt request. When at least one of the interrupt inputs is tied low, the port’s common interrupt will activate a CPU interrupt input according to the external interrupt option in the Miscellaneous Register.

5.1.2.3 Output Mode

When DDR=1, the corresponding I/O is configured in Output mode. In this mode, the interrupt function is disabled.

The output buffers can be individually configured as Open Drain or Push-Pull by means of the Option Register.
The output buffer is activated according to the Data Register’s content.
A read operation is directly performed from the Data Register output.

5.1.2.4 Alternate function

A signal coming from a on-chip peripheral can be output on the I/O.
In this case, the I/O is automatically configured in output mode (without pull-up).
This must be controlled directly by the peripheral with a signal coming from the peripheral which enables the alternate signal to be output.

The I/O’s state is readable as in normal mode by addressing the corresponding I/O Data Register.

A signal coming from an I/O can be input in a on-chip peripheral.
Before using an I/O as Alternate Input, it must be configured in Input without interrupt mode (DDR=0 and OR=0). So, both Alternate Input configuration (with or without pull-up) and I/O input configuration (with or without pull-up) are the same.

The signal to be input in the peripheral is taken after the Schmitt-trigger. The I/O’s state is readable as in normal mode by addressing the corresponding I/O Data Register.

I/O PORTS (Cont'd)

5.1.2.5 I/O Port Implementation

The I/O port register configurations are resumed as following.

Port PA(7:0), Port PB(2:0)

DDR	OR	MODE
0	0	input no interrupt (pull-up enabled)
0	1	input interrupt (pull-up enabled)
1	0	Open-Drain output
1	1	Push-Pull output

RESET status: DR=0, DDR=0 and OR=0 (Input mode, no interrupt).

These ports offer interrupt capabilities.

5.1.2.6 Dedicated Configurations

Table 5. Port A Configuration

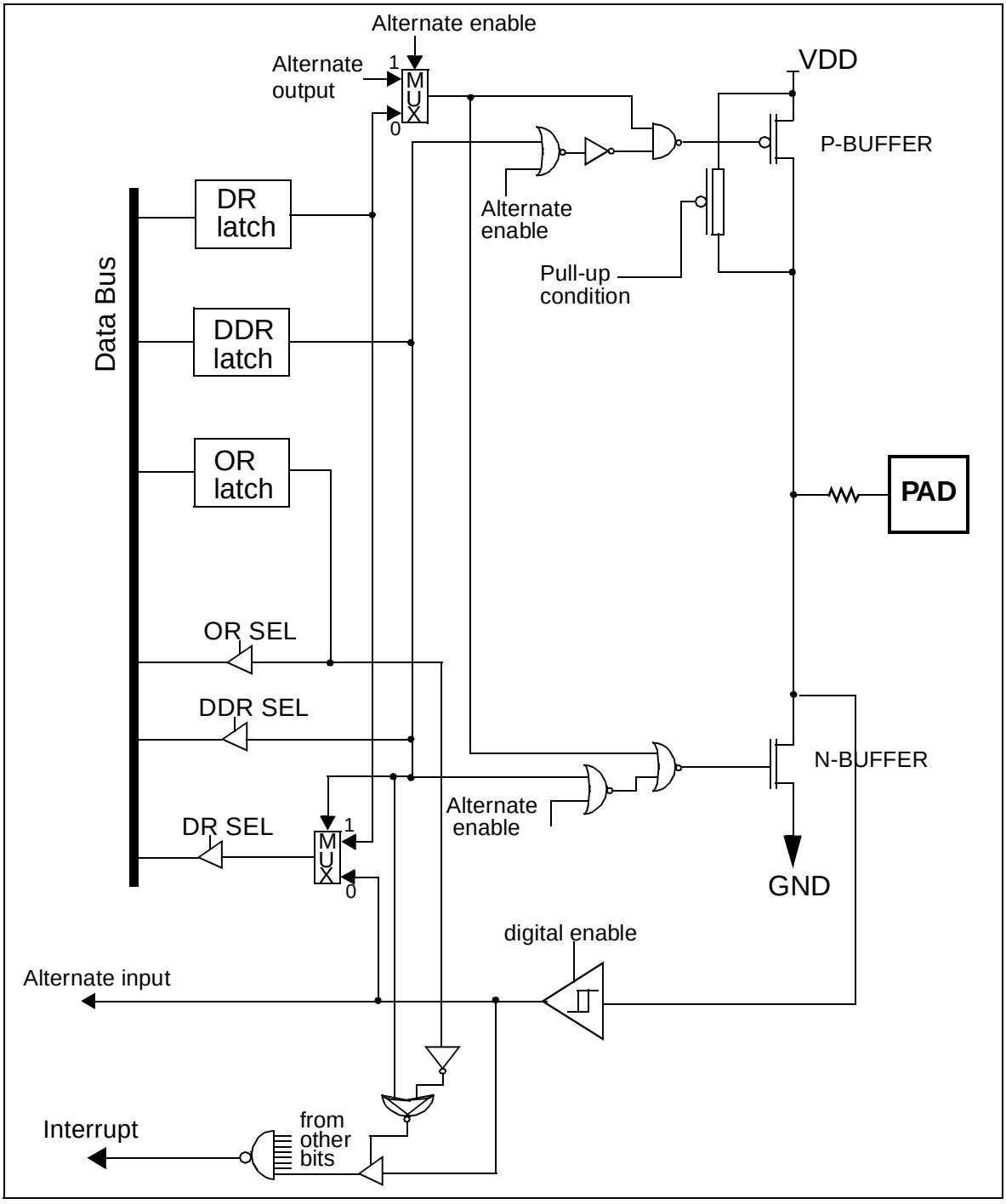
PORT A	I / O		Function	
	Input	Output	Alternate	Interrupt
PA0	triggered with pull-up	push-pull/open drain	OCMP2_1: Output Compare #2 Timer 1	wake-up interrupt (I0)
PA1	triggered with pull-up	push-pull/open drain	OCMP1_1: Output Compare #1 Timer 1	wake-up interrupt (I0)
PA2	triggered with pull-up	push-pull/open drain	ICAP2_1: Input Capture #2 Timer 1	wake-up interrupt (I0)
PA3	triggered with pull-up	push-pull/open drain	ICAP1_1: Input Capture #1 Timer 1	wake-up interrupt (I0)
PA4	triggered with pull-up	push-pull/open drain	EXTCLK_1: External Clock Timer 1	wake-up interrupt (I0)
PA5	triggered with pull-up	push-pull/open drain	OCMP2_2: Output Compare #2 Timer 2	wake-up interrupt (I0)
PA6	triggered with pull-up	push-pull/open drain	OCMP1_2: Output Compare #1 Timer 2	wake-up interrupt (I0)
PA7	triggered with pull-up	push-pull/open drain	ICAP2_2: Input Capture #2 Timer 2	wake-up interrupt (I0)

Table 6. Port B Configuration

PORT B	I / O		Function	
	Input	Output	Alternate	Interrupt
PB0	triggered with pull-up	push-pull/open drain	ICAP1_2: Input Capture #1 Timer 2	wake-up interrupt (I0)
PB1	triggered with pull-up	push-pull/open drain	EXTCLK_2: External Clock Timer 2	wake-up interrupt (I0)
PB2[1)]	Not connected to pad	Not connected to pad	PWMI: PWM input	

Note 1. The PB2 bit is not connected to the external. It must be configured as an Input without interrupt, to be used only as an alternate function.

I/O PORTS (Cont'd)
Figure 15. **Ports PA0-PA7, PB0-PB1**



I

I/O PORTS (Cont'd)

5.1.3 Register Description

5.1.3.1 Data registers

(PADR)

Port A: 0000h

Read/Write
Reset Value: 0000 0000 (00h)

7							0
MSB							LSB

(PBDR)

Port B: 0004h

Read/Write
Reset Value: 0000 0000 (00h)

7							0
MSB	0	0	0	0			LSB

5.1.3.2 Data direction registers

(PADDR)

Port A: 0001h

Read/Write
Reset Value: 0000 0000 (00h) (input mode)

7							0
MSB							LSB

(PBDDR)

Port B: 0005h

Read/Write
Reset Value: 0000 0000 (00h) (input mode)

7							0
MSB	0	0	0	0			LSB

5.1.3.3 Option registers

(PAOR)

Port A: 0002h

Read/Write
Reset Value: 0000 0000 (00h) (no interrupt)

7							0
MSB							LSB

(PBOR)

Port B: 0006h

Read/Write
Reset Value: 0000 0000 (00h) (no interrupt)

7							0
MSB	0	0	0	0			LSB

5.2 16-BIT TIMER

5.2.1 Introduction

The timer consists of a 16-bit free-running counter driven by a programmable prescaler.

It may be used for a variety of purposes, including pulse length measurement of up to two input signals (*input capture*) or generation of up to two output waveforms (*output compare* and *PWM*).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the CPU clock prescaler.

5.2.2 Main Features

- Programmable prescaler: f_{cpu} divided by 2, 4 or 8.
- Overflow status flag and maskable interrupt
- External clock input (must be at least 4 times slower than the CPU clock speed) with the choice of active edge
- Output compare functions with
  - 2 dedicated 16-bit registers
  - 2 dedicated programmable signals
  - 2 dedicated status flags
  - 1 dedicated maskable interrupt
- Input capture functions with
  - 2 dedicated 16-bit registers
  - 2 dedicated active edge selection signals
  - 2 dedicated status flags
  - 1 dedicated maskable interrupt
- Pulse width modulation mode (PWM)
- One pulse mode
- 5 alternate functions on I/O ports

The Block Diagram is shown in Figure 16, on page 33.

Note: Some external pins are not available on all devices. Refer to the device pin out description.

5.2.3 Functional Description

5.2.3.1 Counter

The principal block of the Programmable Timer is a 16-bit free running counter and its associated 16-bit registers:

Counter Registers

- Counter High Register (CHR) is the most significant byte (MSB).
- Counter Low Register (CLR) is the least significant byte (LSB).

Alternate Counter Registers

- Alternate Counter High Register (ACHR) is the most significant byte (MSB).
- Alternate Counter Low Register (ACLR) is the least significant byte (LSB).

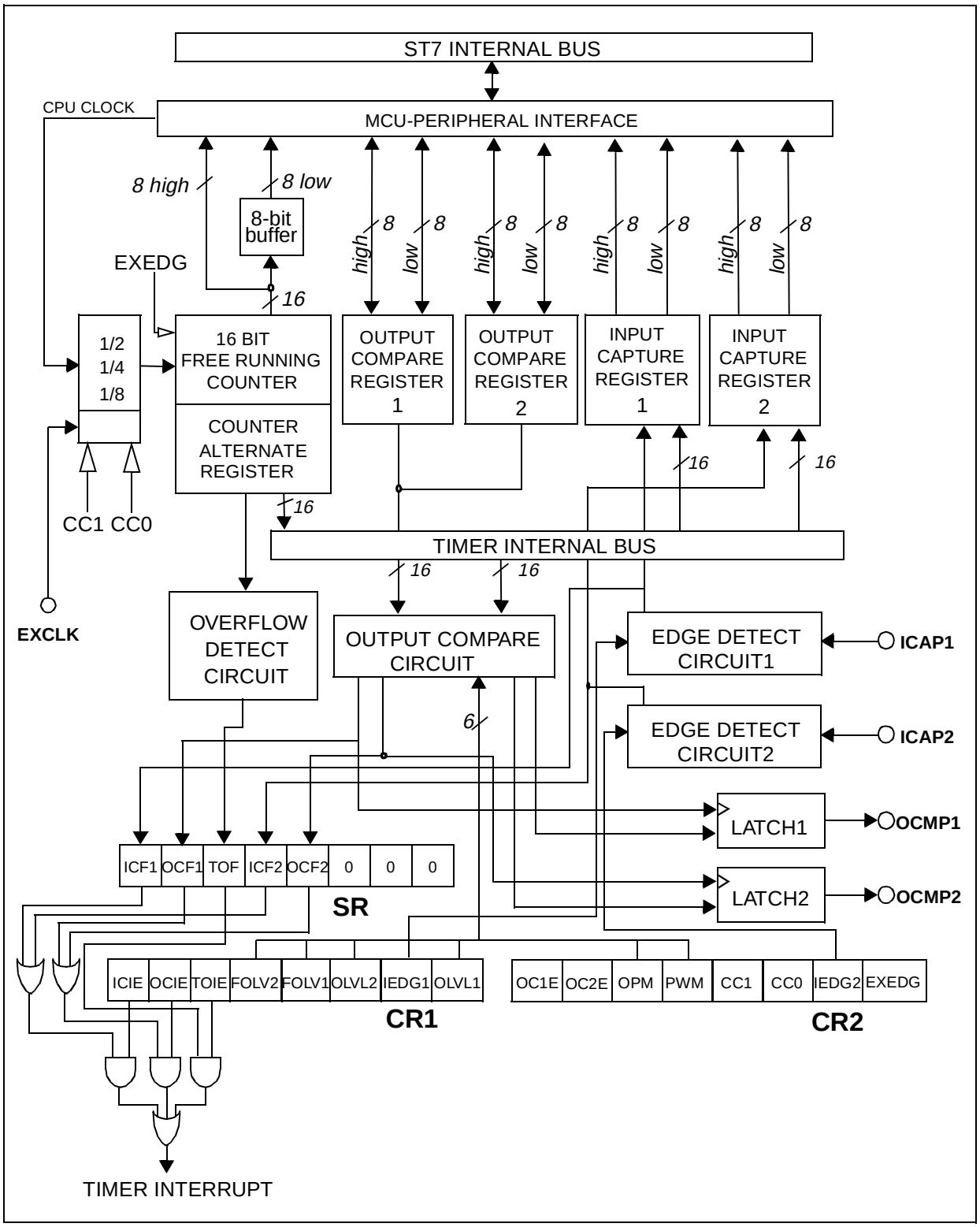
These two read-only 16-bit registers contain the same value but with the difference that reading the ACLR register does not clear the TOF bit (overflow flag), (see note page 3).

Writing in the CLR register or ACLR register resets the free running counter to the FFFCh value.

The timer clock depends on the clock control bits of the CR2 register, as illustrated in Table 7 Clock Control Bits. The value in the counter register repeats every 131.072, 262.144 or 524.288 internal processor clock cycles depending on the CC1 and CC0 bits.

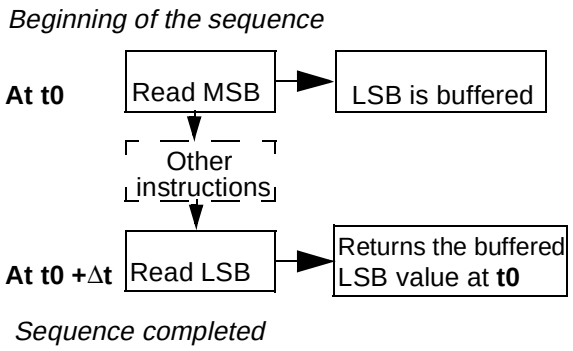
16-BIT TIMER (Cont'd)

Figure 16. Timer Block Diagram



16-BIT TIMER (Cont'd)

16-bit read sequence: (from either the Counter Register or the Alternate Counter Register).



The user must read the MSB first, then the LSB value is buffered automatically.

This buffered value remains unchanged until the 16-bit read sequence is completed, even if the user reads the MSB several times.

After a complete reading sequence, if only the CLR register or ACLR register are read, they return the LSB of the count value at the time of the read.

An overflow occurs when the counter rolls over from FFFFh to 0000h then:

– The TOF bit of the SR register is set.

– A timer interrupt is generated if:

  – TOIE bit of the CR1register is set and

  – I bit of the CCR register is cleared.

If one of these conditions is false, the interrupt remains pending to be issued as soon as they are both true.

Clearing the overflow interrupt request is done by:

1. Reading the SR register while the TOF bit is set.
2. An access (read or write) to the CLR register.

Notes: The TOF bit is not cleared by accesses to ACLR register. This feature allows simultaneous use of the overflow function and reads of the free running counter at random times (for example, to measure elapsed time) without the risk of clearing the TOF bit erroneously.

The timer is not affected by WAIT mode.

In HALT mode, the counter stops counting until the mode is exited. Counting then resumes from the previous count (MCU awakened by an interrupt) or from the reset count (MCU awakened by a Reset).

5.2.3.2 External Clock

The external clock (where available) is selected if CC0=1 and CC1=1 in CR2 register.

The status of the EXEDG bit determines the type of level transition on the external clock pin EXCLK that will trigger the free running counter.

The counter is synchronised with the falling edge of the internal CPU clock.

At least four falling edges of the CPU clock must occur between two consecutive active edges of the external clock; thus the external clock frequency must be less than a quarter of the CPU clock frequency.

16-BIT TIMER (Cont'd)

Figure 17. Counter Timing Diagram, internal clock divided by 2

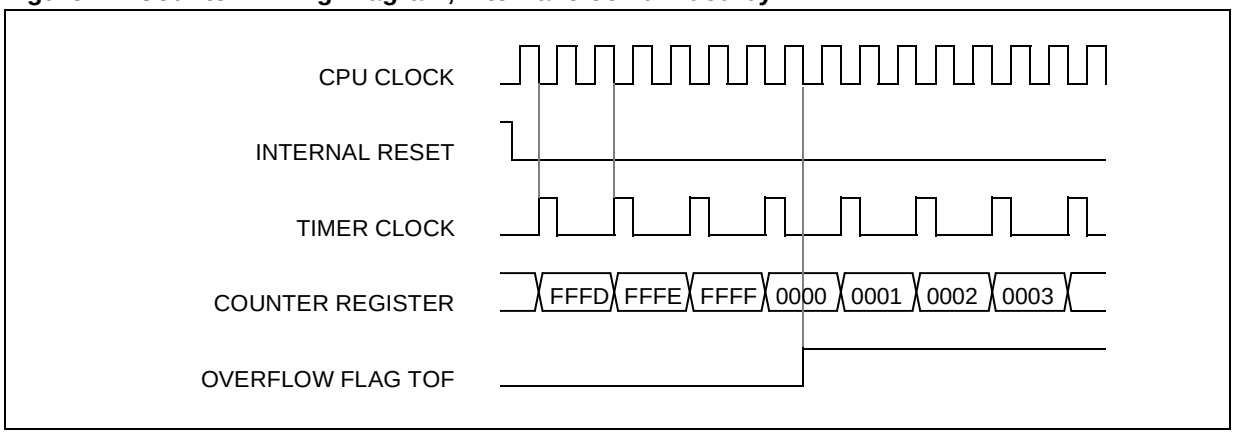


Figure 18. Counter Timing Diagram, internal clock divided by 4

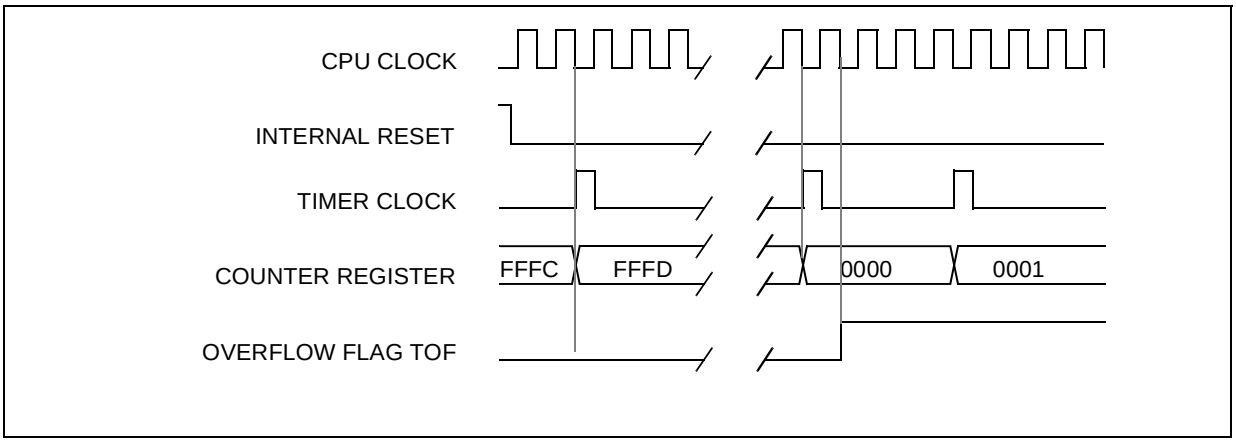
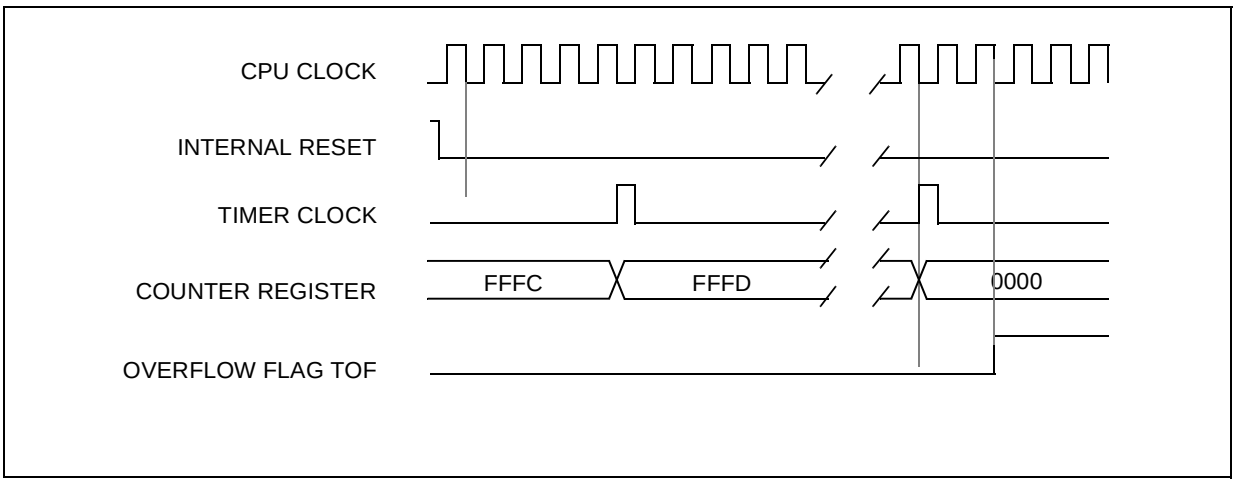


Figure 19. Counter Timing Diagram, internal clock divided by 8



16-BIT TIMER (Cont'd)

5.2.3.3 Input Capture

In this section, the index, *i*, may be 1 or 2

The two input capture 16-bit registers (ICR1 and ICR2) are used to latch the value of the free running counter after a transition detected by the ICAP*i* pin (see figure 5).

	MS Byte	LS Byte
ICR*i*	**ICHR*i***	**ICLR*i***

ICR*i* register is a read-only register.

The active transition is software programmable through the IEDG*i* bit of the Control Register (CR*i*).

Timing resolution is one count of the free running counter: ($f_{CPU/(CC1.CC0)}$).

Procedure

To use the input capture function select the following in the CR2 register:

– Select the timer clock (CC1-CC0) (see Table 7 Clock Control Bits).

– Select the edge of the active transition on the ICAP2 pin with the IEDG2 bit.

And select the following in the CR1 register:

– Set the ICIE bit to generate an interrupt after an input capture.

– Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit.

When an input capture occurs:

– ICF*i* bit is set.

– The ICR*i* register contains the value of the free running counter on the active transition on the ICAP*i* pin (see Figure 21).

– A timer interrupt is generated if the ICIE bit is set and the I bit is cleared in the CCR register. Otherwise, the interrupt remains pending until both conditions become true.

Clearing the Input Capture interrupt request is done by:

1. Reading the SR register while the ICF*i* bit is set.

2. An access (read or write) to the ICLR*i* register.

Note: After reading the ICHR*i* register, transfer of input capture data is inhibited until the ICLR*i* register is also read.

The ICR*i* register always contains the free running counter value which corresponds to the most recent input capture.

During HALT mode, if at least one valid input capture edge occurs on the ICAP*i* pin, the input capture detection circuitry is armed. This does not set any timer flags, and does not "wake-up" the MCU. If the MCU is awoken by an interrupt, the input capture flag will become active, and data corresponding to the first valid edge during HALT mode will be present.

16-BIT TIMER (Cont'd)

Figure 20. Input Capture Block Diagram

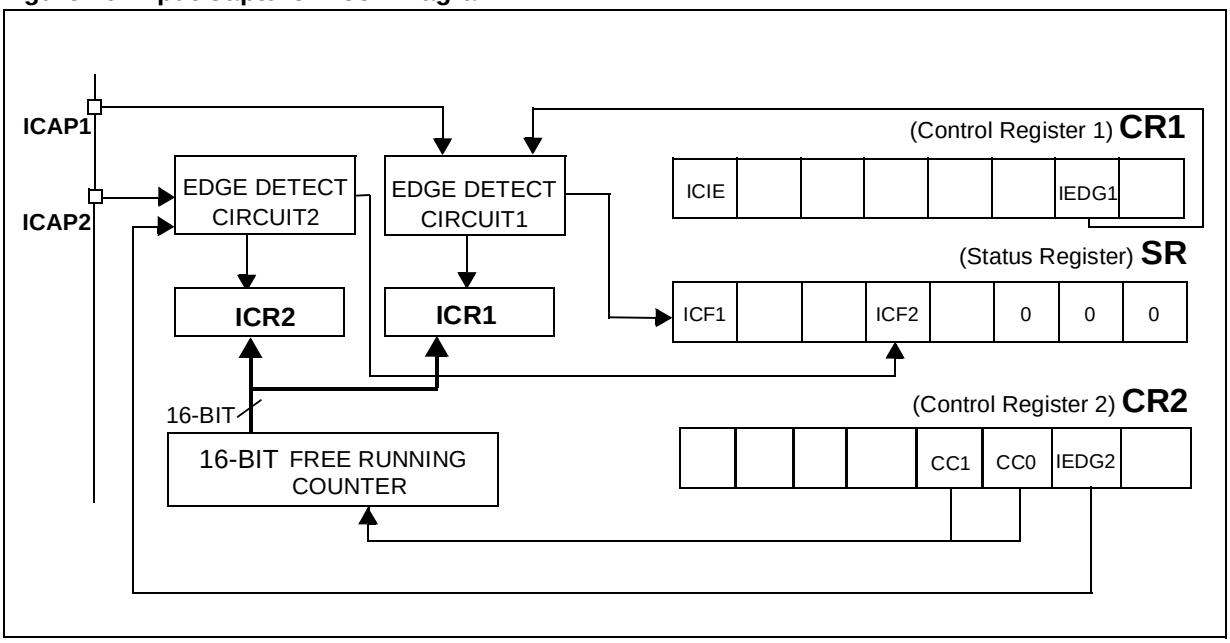
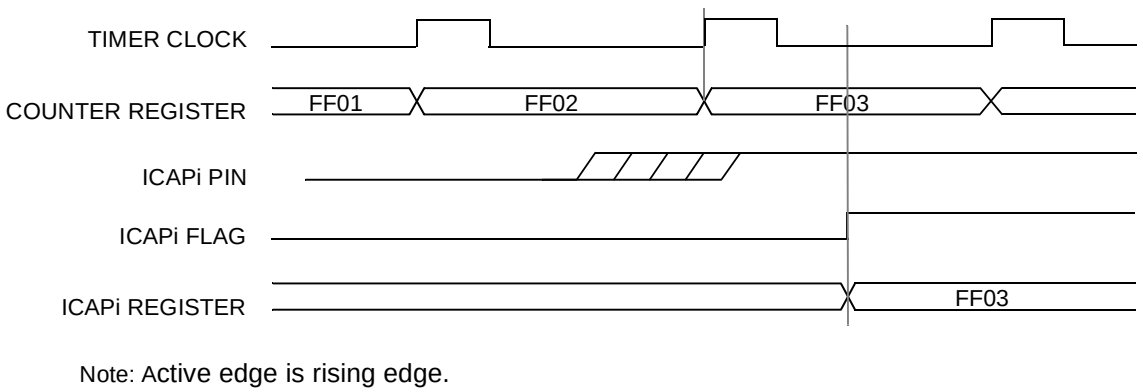


Figure 21. Input Capture Timing Diagram



Note: Active edge is rising edge.

16-BIT TIMER (Cont'd)

5.2.3.4 Output Compare

In this section, the index, *i*, may be 1 or 2.

This function can be used to control an output waveform or indicating when a period of time has elapsed.

When a match is found between the Output Compare register and the free running counter, the output compare function:

- Assigns pins with a programmable value if the OCIE bit is set
- Sets a flag in the status register
- Generates an interrupt if enabled

Two 16-bit registers Output Compare Register 1 (OCR1) and Output Compare Register 2 (OCR2) contain the value to be compared to the free running counter each timer clock cycle.

	MS Byte	LS Byte
OCR*i*	OCHR*i*	OCLR*i*

These registers are readable and writable and are not affected by the timer hardware. A reset event changes the OCRi value to 8000h.

Timing resolution is one count of the free running counter: ($f_{CPU/(CC1.CC0)}$).

Procedure

To use the output compare function, select the following in the CR2 register:

– Set the OC*i*E bit if an output is needed then the OCMP*i* pin is dedicated to the output compare *i* function.

– Select the timer clock (CC1-CC0) (see Table 7 Clock Control Bits).

And select the following in the CR1 register:

– Select the OLVL*i* bit to applied to the OCMP*i* pins after the match occurs.

– Set the OCIE bit to generate an interrupt if it is needed.

When match is found:

– OCF*i* bit is set.

– The OCMP*i* pin takes OLVL*i* bit value (OCMP*i* pin latch is forced low during reset and stays low until valid compares change it to a high level).

– A timer interrupt is generated if the OCIE bit is set in the CR2 register and the I bit is cleared in the CCR register (CCR).

Clearing the output compare interrupt request is done by:

3. Reading the SR register while the OCF*i* bit is set.
4. An access (read or write) to the OCLR*i* register.

Note: After a processor write cycle to the OCHR*i* register, the output compare function is inhibited until the OCLR*i* register is also written.

If the OC*i*E bit is not set, the OCMP*i* pin is a general I/O port and the OLVL*i* bit will not appear when match is found but an interrupt could be generated if the OCIE bit is set.

The value in the 16-bit OCR*i* register and the OLV*i* bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

The OCR*i* register value required for a specific timing application can be calculated using the following formula:

$$\Delta \text{ OCR}i \text{ register Value} = \frac{t * f_{CPU}}{(CC1.CC0)}$$

Where:

t = Desired output compare period (in seconds calculated from the current counter)

f_{CPU} = Internal clock frequency (see Miscellaneous register)

CC1-CC0 = Timer clock prescaler

The following procedure is recommended to prevent the OCF*i* bit from being set between the time it is read and the write to the OCR*i* register:

– Write to the OCHR*i* register (further compares are inhibited).

– Read the SR register (first step of the clearance of the OCF*i* bit, which may be already set).

– Write to the OCLR*i* register (enables the output compare function and clears the OCF*i* bit).

16-BIT TIMER (Cont'd)

Figure 22. Output Compare Block Diagram

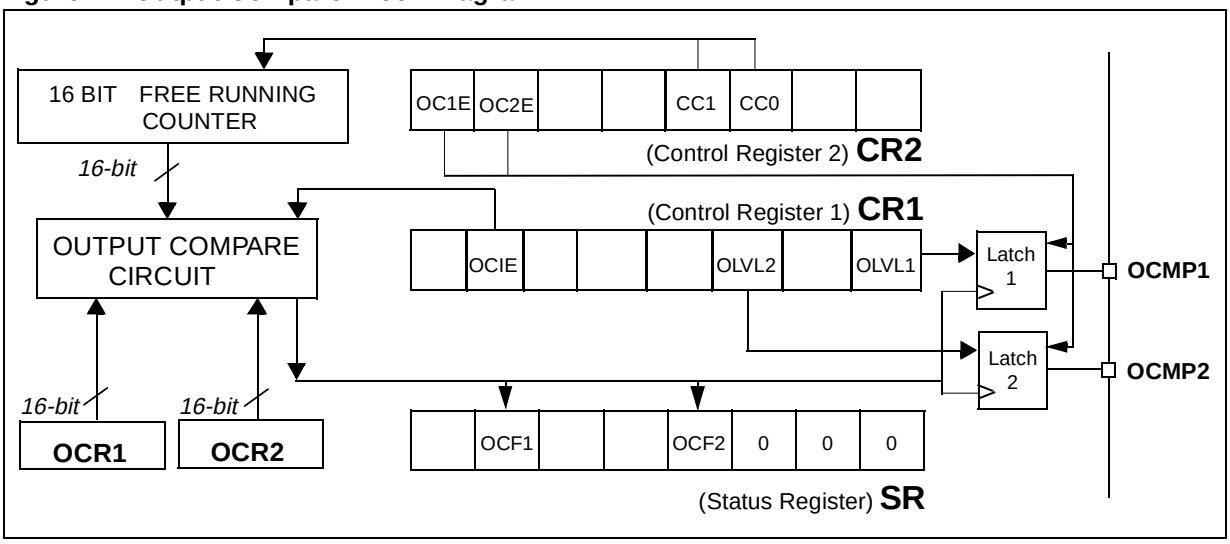
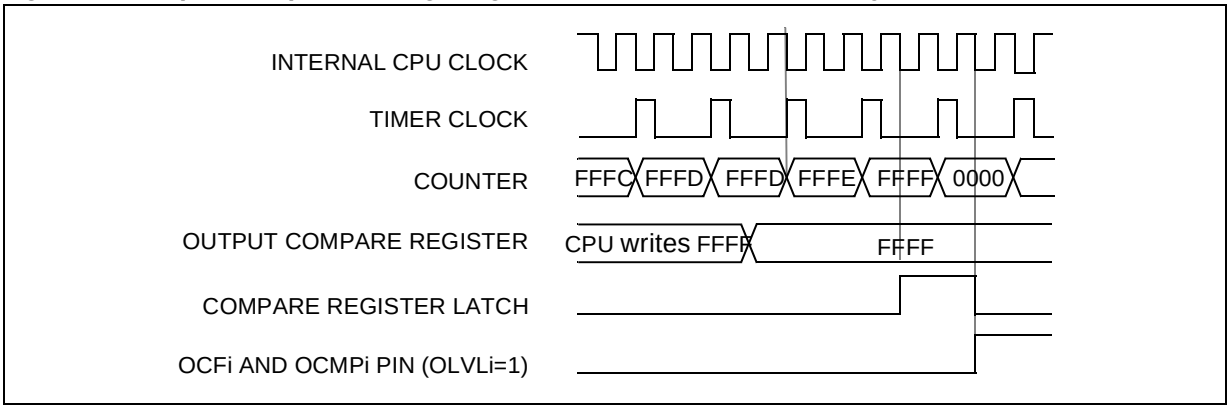


Figure 23. Output Compare Timing Diagram, Internal Clock Divided by 2



16-BIT TIMER (Cont'd)

5.2.3.5 Forced Compare Mode

In this section *i* may represent 1 or 2.

The main purpose of the Forced Compare mode is to easily generate a fixed frequency.

The following bits of the CR1 register are used:

			FOLV 2	FOLV 1	OLVL 2		OLVL 1

When the FOLV*i* bit is set, the OLVL*i* bit is copied to the OCMP*i* pin.

To provide this capability, internal logic allows a single instruction to change the OLVL*i* bit and causes a forced compare with the new value of the OLVL*i* bit.

The OCF*i* bit is not set, and thus no interrupt request is generated.

5.2.3.6 One Pulse Mode

One Pulse mode enables the generation of a pulse when an external event occurs. This mode is selected via the OPM bit in the CR2 register.

The one pulse mode uses the Input Capture1 function and the Output Compare1 function.

Procedure

To use one pulse mode, select the following in the CR1 register:

– Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after the pulse.

– Using the OLVL2 bit, select the level to be applied to the OCMP1 pin during the pulse.

– Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit.

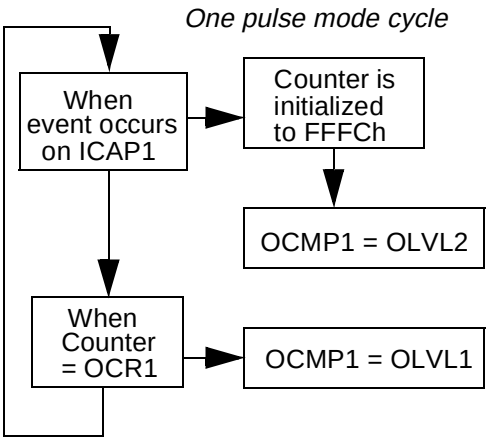
– Set OC1E pin, the OCMP1 pin is then dedicated to the Output Compare 1 function.

And select the following in the CR2 register:

– Set the OPM bit.

– Select the timer clock CC1-CC0 (see Table 7 Clock Control Bits).

Load the OCR1 register with the value corresponding to the length of the pulse (see the formula in Section 5.2.3.7).



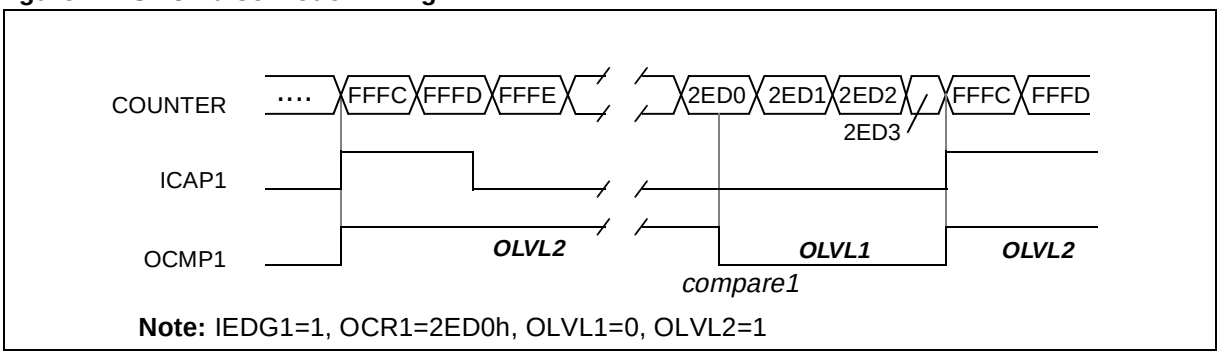
Then, on a valid event on the ICAP1 pin, the counter is initialized to FFFCh and OLVL2 bit is loaded on the OCMP1 pin. When the value of the counter is equal to the value of the contents of the OCR1 register, the OLVL1 bit is output on the OCMP1 pin, (See Figure 24).

Note: The OCF1 bit cannot be set by hardware in one pulse mode but the OCF2 bit can generate an Output Compare interrupt.

The ICF1 bit is set when an active edge occurs and can generate an interrupt if the ICIE bit is set.

When the Pulse Width Modulation (PWM) and One Pulse Mode (OPM) bits are both set, the PWM mode is the only active one.

Figure 24. One Pulse Mode Timing



Note: IEDG1=1, OCR1=2ED0h, OLVL1=0, OLVL2=1

16-BIT TIMER (Cont'd)

5.2.3.7 Pulse Width Modulation Mode

Pulse Width Modulation mode enables the generation of a signal with a frequency and pulse length determined by the value of the OCR1 and OCR2 registers.

The pulse width modulation mode uses the complete Output Compare 1 function plus the OCR2 register.

Procedure

To use pulse width modulation mode select the following in the CR1 register:

– Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after a successful comparison with OCR1 register.

– Using the OLVL2 bit, select the level to be applied to the OCMP1 pin after a successful comparison with OCR2 register.

– Set OC1E bit: the OCMP1 pin is then dedicated to the output compare 1 function.

And select the following in the CR2 register:

– Set the PWM bit.

– Select the timer clock (CC1-CC0) (see Table 7 Clock Control Bits).

Load the OCR2 register with the value corresponding to the period of the signal.

Load the OCR1 register with the value corresponding to the length of the pulse if (OLVL1=0 and OLVL2=1).

If OLVL1=1 and OLVL2=0 the length of the pulse is the difference between the OCR2 and OCR1 registers.

The OCR*i* register value required for a specific timing application can be calculated using the following formula:

$$\text{OCR}i\ \text{Value} = \frac{t * f_{CPU}}{(CC1.CC0)} - 5$$

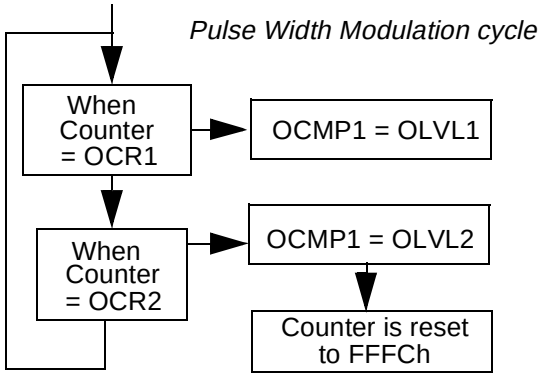
Where:

– t = Desired output compare period (seconds)

– f_{CPU} = Internal clock frequency (see Miscellaneous register)

– CC1-CC0 = Timer clock prescaler

The Output Compare 2 event causes the counter to be initialized to FFFCh (See Figure 25, on page 42).

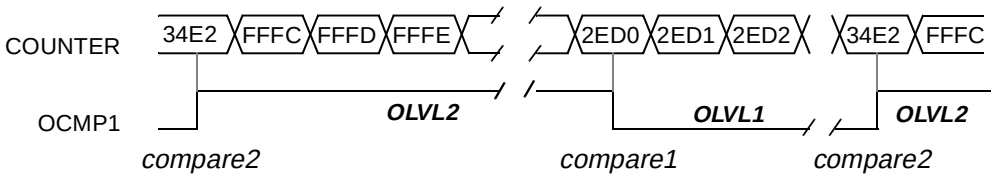


Note: After a write instruction to the OCHR*i* register, the output compare function is inhibited until the OCLR*i* register is also written.

The OCF1 and OCF2 bits cannot be set by hardware in PWM mode therefore the Output Compare interrupt is inhibited. The Input Capture interrupt is available.

When the Pulse Width Modulation (PWM) and One Pulse Mode (OPM) bits are both set, the PWM mode is the only active one.

Figure 25. Pulse Width Modulation Mode Timing



Note: OCR1=2ED0h, OCR2=34E2, OLVL1=0, OLVL2= 1

16-BIT TIMER (Cont'd)

5.2.4 Register Description

Each Timer is associated with three control and status registers, and with six pairs of data registers (16-bit values) relating to the two input captures, the two output compares, the counter and the alternate counter.

CONTROL REGISTER 1 (CR1)

Timer1 Register Address: 0032h

Timer2 Register Address: 0042h

Read/Write

Reset Value: 0000 0000 (00h)

7							0
ICIE	OCIE	TOIE	FOLV 2	FOLV 1	OLVL 2	IEDG 1	OLVL 1

Bit 7 = **ICIE** *Input Capture Interrupt Enable.*
0: Interrupt is inhibited.
1: A timer interrupt is generated whenever the ICF1 or ICF2 bits of the SR register are set

Bit 6 = **OCIE** *Output Compare Interrupt Enable.*
0: Interrupt is inhibited.
1: A timer interrupt is generated whenever the OCF1 or OCF2 bits of the SR register are set

Bit 5 = **TOIE** *Timer Overflow Interrupt Enable.*
0: Interrupt is inhibited.
1: A timer interrupt is enabled whenever the TOF bit of the SR register is set.

Bit 4 = **FOLV2** *Forced Output Compare 2.*
0: No effect.
1: Forces the OLVL2 bit to be copied to the OCMP2 pin.

Bit 3 = **FOLV1** *Forced Output Compare 1.*
0: No effect.
1: Forces OLVL1 to be copied to the OCMP1 pin.

Bit 2 = **OLVL2** *Output Level 2.*
This bit is copied to the OCMP2 pin whenever a successful comparison occurs with the OCR2 register. This value is copied to the OCMP1 pin in One Pulse Mode and Pulse Width Modulation mode.

Bit 1 = **IEDG1** *Input Edge 1.*
This bit determines which type of level transition on the ICAP1 pin will trigger the capture.
0: A falling edge triggers the capture.
1: A rising edge triggers the capture.

Bit 0 = **OLVL1** *Output Level 1.*
The OLVL1 bit is copied to the OCMP1 pin whenever a successful comparison occurs with the OCR1 register.

16-BIT TIMER (Cont'd)

CONTROL REGISTER 2 (CR2)

Timer1 Register Address: 0031h

Timer2 Register Address: 0041h

Read/Write

Reset Value: 0000 0000 (00h)

7							0
OC1E	OC2E	OPM	PWM	CC1	CC0	IEDG2	EXEDG

Bit 7 = **OC1E** *Output Compare 1 Enable.*
0: Output Compare 1 function is enabled, but the OCMP1 pin is a general I/O.
1: Output Compare 1 function is enabled, the OCMP1 pin is dedicated to the Output Compare 1 capability of the timer.

Bit 6 = **OC2E** *Output Compare 2 Enable.*
0: Output Compare 2 function is enabled, but the OCMP2 pin is a general I/O.
1: Output Compare 2 function is enabled, the OCMP2 pin is dedicated to the Output Compare 2 capability of the timer.

Bit 5 = **OPM** *One Pulse Mode.*
0: One Pulse Mode is not active.
1: One Pulse Mode is active, the ICAP1 pin can be used to trigger one pulse on the OCMP1 pin; the active transition is given by the IEDG1 bit. The length of the generated pulse depends on the contents of the OCR1 register.

Bit 4 = **PWM** *Pulse Width Modulation.*
0: PWM mode is not active.
1: PWM mode is active, the OCMP1 pin outputs a programmable cyclic signal; the length of the pulse depends on the value of OCR1 register; the period depends on the value of OCR2 register.

Bit 3, 2 = **CC1-CC0** *Clock Control.*
The value of the timer clock depends on these bits:

Table 7. Clock Control Bits

CC1	CC0	Timer Clock
0	0	f_{CPU} / 4
0	1	f_{CPU} / 2
1	0	f_{CPU} / 8
1	1	External Clock (where available)

Bit 1 = **IEDG2** *Input Edge 2.*
This bit determines which type of level transition on the ICAP2 pin will trigger the capture
0: A falling edge triggers the capture.
1: A rising edge triggers the capture.

Bit 0 = **EXEDG** *External Clock Edge.*
This bit determines which type of level transition on the external clock pin EXCLK will trigger the free running counter.
0: A falling edge triggers the free running counter.
1: A rising edge triggers the free running counter.

16-BIT TIMER (Cont'd)

STATUS REGISTER (SR)

Timer1 Register Address: 0033h

Timer2 Register Address: 0043h

Read Only

Reset Value: 0000 0000 (00h)

The three least significant bits are not used.

7							0
ICF1	OCF1	TOF	ICF2	OCF2			

Bit 7 = **ICF1** *Input Capture Flag 1.*
0: No input capture (reset value)
1: An input capture has occurred. To clear this bit, first read the SR register, then read or write the low byte of the ICR1 (ICLR1) register.

Bit 6 = **OCF1** *Output Compare Flag 1.*
0: No match (reset value)
1: The content of the free running counter has matched the content of the OCR1 register. To clear this bit, first read the SR register, then read or write the low byte of the OCR1 (OCLR1) register.

Bit 5 = **TOF** *Timer Overflow.*
0: No timer overflow (reset value)
1: The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register.

Note: Reading or writing the ACLR register do not clear TOF.

Bit 4 = **ICF2** *Input Capture Flag 2.*
0: No input capture (reset value)
1: An input capture has occurred.To clear this bit, first read the SR register, then read or write the low byte of the ICR2 (ICLR2) register.

Bit 3 = **OCF2** *Output Compare Flag 2.*
0: No match (reset value)
1: The content of the free running counter has matched the content of the OCR2 register. To clear this bit, first read the SR register, then read or write the low byte of the OCR2 (OCLR2) register.

Bit 2-0 = Unused.

16-BIT TIMER (Cont'd)

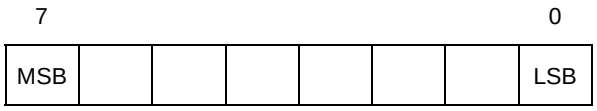
INPUT CAPTURE 1 HIGH REGISTER (ICHR1)

Timer1 Register Address: 0034h

Timer2 Register Address: 0044h

Read Only
Reset Value: Undefined

This is an 8-bit read only register that contains the high part of the counter value (transferred by the input capture 1 event).



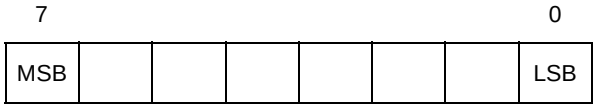
INPUT CAPTURE 1 LOW REGISTER (ICLR1)

Timer1 Register Address: 0035h

Timer2 Register Address: 0045h

Read Only
Reset Value: Undefined

This is an 8-bit read only register that contains the low part of the counter value (transferred by the input capture 1 event).



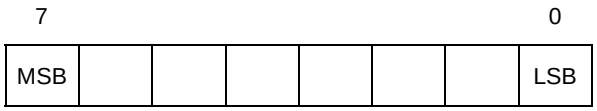
OUTPUT COMPARE 1 HIGH REGISTER (OCHR1)

Timer1 Register Address: 0036h

Timer2 Register Address: 0046h

Read/Write
Reset Value: 1000 0000 (80h)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.



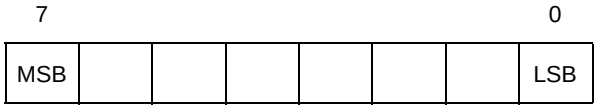
OUTPUT COMPARE 1 LOW REGISTER (OCLR1)

Timer1 Register Address: 0037h

Timer2 Register Address: 0047h

Read/Write
Reset Value: 0000 0000 (00h)

This is an 8-bit register that contains the low part of



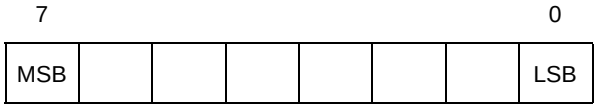
OUTPUT COMPARE 2 HIGH REGISTER (OCHR2)

Timer1 Register Address: 003Eh

Timer2 Register Address: 004Eh

Read/Write
Reset Value: 1000 0000 (80h)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.



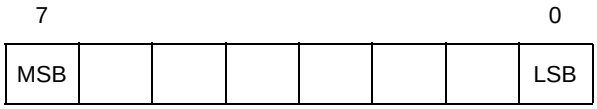
OUTPUT COMPARE 2 LOW REGISTER (OCLR2)

Timer1 Register Address: 003Fh

Timer2 Register Address: 004Fh

Read/Write
Reset Value: 0000 0000 (00h)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.



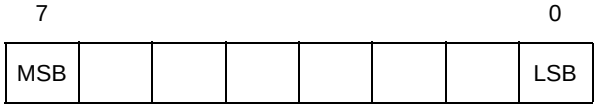
COUNTER HIGH REGISTER (CHR)

Timer1 Register Address: 0038h

Timer2 Register Address: 0048h

Read Only
Reset Value: 1111 1111 (FFh)

This is an 8-bit register that contains the high part of the counter value.



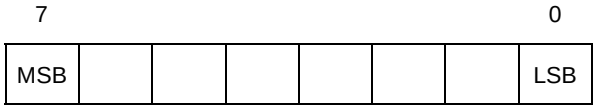
COUNTER LOW REGISTER (CLR)

Timer1 Register Address: 0039h

Timer2 Register Address: 0049h

Read/Write
Reset Value: 1111 1100 (FCh)

This is an 8-bit register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after accessing the SR register clears the TOF bit.16-BIT



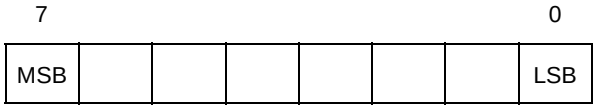
ALTERNATE COUNTER HIGH REGISTER (ACHR)

Timer1 Register Address: 003Ah

Timer2 Register Address: 004Ah

Read Only
Reset Value: 1111 1111 (FFh)

This is an 8-bit register that contains the high part of the counter value.



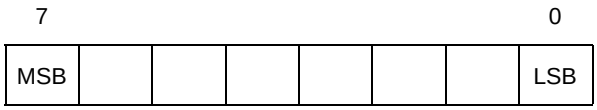
ALTERNATE COUNTER LOW REGISTER (ACLR)

Timer1 Register Address: 003Bh

Timer2 Register Address: 004Bh

Read/Write
Reset Value: 1111 1100 (FCh)

This is an 8-bit register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after an access to SR register does not clear the TOF bit in SR register.



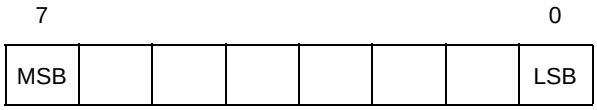
INPUT CAPTURE 2 HIGH REGISTER (ICHR2)

Timer1 Register Address: 003Ch

Timer2 Register Address: 004Ch

Read Only
Reset Value: Undefined

This is an 8-bit read only register that contains the high part of the counter value (transferred by the Input Capture 2 event).



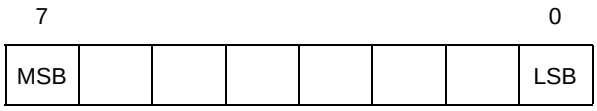
INPUT CAPTURE 2 LOW REGISTER (ICLR2)

Timer1 Register Address: 003Dh

Timer2 Register Address: 004Dh

Read Only
Reset Value: Undefined

This is an 8-bit read only register that contains the low part of the counter value (transferred by the Input Capture 2 event).



16-BIT TIMER (Cont'd)

Table 8. 16-Bit Timer Register Map and Reset Values

Address (Hex.)	Register Name	7	6	5	4	3	2	1	0
Timer1: 32 Timer2: 42	**CR1** Reset Value	ICIE 0	OCIE 0	TOIE 0	FOLV2 0	FOLV1 0	OLVL2 0	IEDG1 0	OLVL1 0
Timer1: 31 Timer2: 41	**CR2** Reset Value	OC1E 0	OC2E 0	OPM 0	PWM 0	CC1 0	CC0 0	IEDG2 0	EXEDG 0
Timer1: 33 Timer2: 43	**SR** Reset Value	ICF1 0	OCF1 0	TOF 0	ICF2 0	OCF2 0	- 0	- 0	- 0
Timer1: 34 Timer2: 44	**ICHR1** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer1: 35 Timer2: 45	**ICLR1** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer1: 36 Timer2: 46	**OCHR1** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer1: 37 Timer2: 47	**OCLR1** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer1: 3E Timer2: 4E	**OCHR2** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer1: 3F Timer2: 4F	**OCLR2** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer1: 38 Timer2: 48	**CHR** Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
Timer1: 39 Timer2: 49	**CLR** Reset Value	MSB 1	1	1	1	1	1	0	LSB 0
Timer1: 3A Timer2: 4A	**ACHR** Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
Timer1: 3B Timer2: 4B	**ACLR** Reset Value	MSB 1	1	1	1	1	1	0	LSB 0
Timer1: 3C Timer2: 4C	**ICHR2** Reset Value	MSB -	-	-	-	-	-	-	LSB -
Timer1: 3D Timer2: 4D	**ICLR2** Reset Value	MSB -	-	-	-	-	-	-	LSB -

5.3 PWM GENERATOR

5.3.1 Introduction

This PWM peripheral includes a 16-bit Pulse Width Modulator (PWM) and a programmable prescaler able to generate an internal clock with period as long as $128*T_{CPU}$.

The repetition rate of the 16-Bit PWM output can be defined by a dedicated register (f_{CPU}/CYREG); its resolution is defined by the internal clock as per the prescaler programming.

Main Features

-Programmable prescaler: f_{CPU} divided by 2, 4, 8, 16, 32, 64 or 128.

-1 control register

-2 dedicated 16-bit registers for cycle and duty control

-1 dedicated maskable interrupt

Procedure

To use the pulse width modulation peripheral, the EN_PWM bit in CONREG register must be set.

Load PS(2:0) in CONREG register to define the programmable prescaler.

Load the CYREG register with the value defining the cycle length (in internal clock periods). The 16 bits of this register are separated in two registers: CYREGH and CYREGL.

Load the DUTYREG register with the value corresponding to the pulse length (in internal cycle periods). The 16 bits of this register are separated in two registers: DUTYREGH and DUTYREGL.

The counter is reset to zero when EN_PWM bit is reset.

Writing the DUTYREG and CYREG registers has no effect on the current PWM cycle. The cycle or duty cycle change take place only after the first overflow of the counter.

The suggested procedures to change the PWM parameters are the following:

Duty Cycle control:

- Write the low and high DUTYREG registers.

A writing only on one DUTYREG register has no effect until both registers are written.

The current PWM cycle will be completed. The new duty cycle will be effective at the following PWM cycle, with respect to the last DUTYREG writing.

Cycle control:

- Write the low and high CYREG register

A writing only on one CYREG register has no effect until both registers are written.

The current PWM cycle will be completed. The new cycle will be effective at the following PWM cycle, with respect to the last CYREG writing.

Another possible procedure is:

- Reset the EN_PWM bit.

- Write the wanted configuration in CYREG and DUTYREG..

- Set the EN_PWM bit.

If the EN_PWM bit is set after being reset, the current values of DUTYREG and CYREG are determining the output waveform, no matter if only the low or the high part, or both were written.

The first time EN_PWM is set, if CYREG and DUTYREG were not previously written, the output is permanently low, because the default value of the registers is 00h.

Changing the Prescaler ratio writing PS(2:0) in CONREG has immediate effect on the waveform frequency.

5.3.2 Functional Description

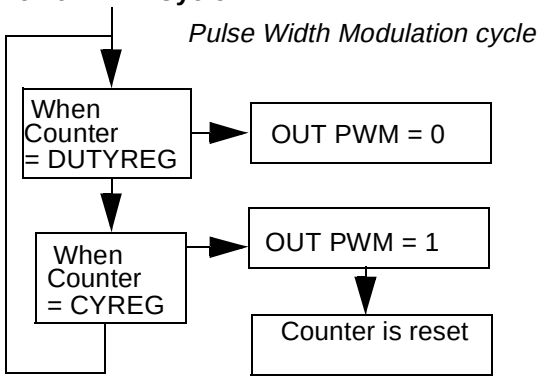
The PWM module consists of a 16-bit counter, a comparator and the cycle generation logic.

PWM Generation

The counter increments continuously, clocked at internal clock generated by prescaler. Whenever the 16 bits of the counter (defined as the PWM counter) overflow, the output level is set. The overflow value is defined by CYREG register.

The state of the PWM counter is continuously compared to the PWM binary weight, as defined in DUTYREG register, and when a match occurs the output level is reset.

Figure 26. PWM Cycle



Note: If the CYREG value is minor or equal than DUTYREG value, PWM output remains set. With a

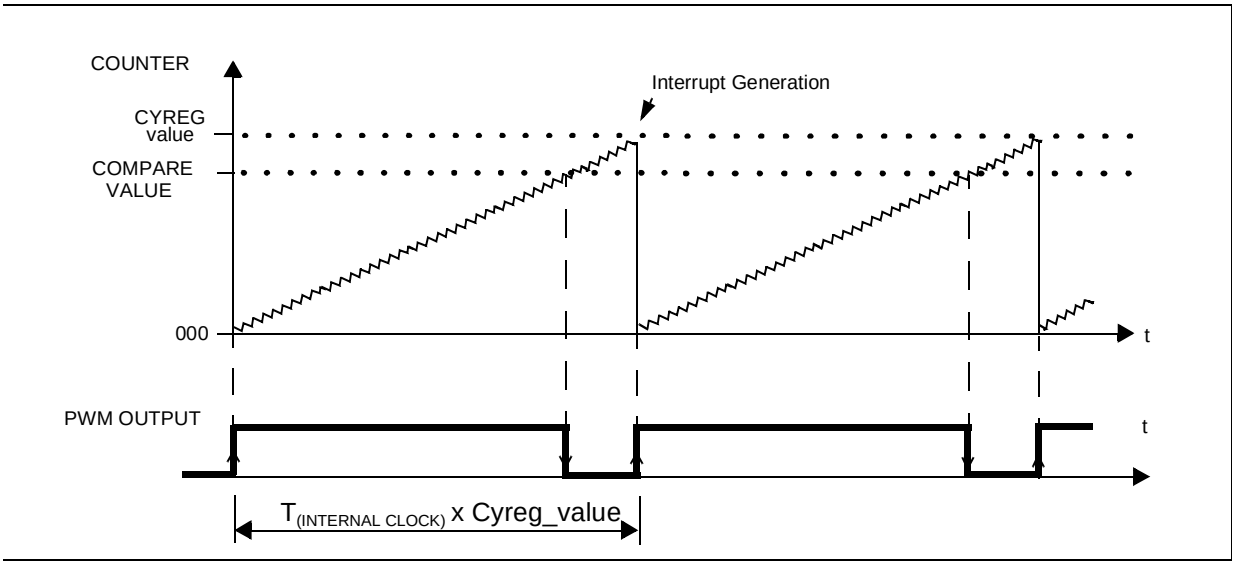
DUTYREG value of 0000h, the PWM output is permanently at low level, no matter of the value of CYREG. With a DUTYREG value of FFFFh, the PWM output is permanently at high level.

Interrupt Request

The EN_INT bit in CONREG register must be set to enable the interrupt generation. When the 16 bits of the counter roll-over CYCLEREG value, interrupt request is set.

The interrupt request is cleared when any of the PWM registers is written.

Figure 27. PWM Generation



5.3.3 Register Description

The PWM is associated with a 8-bit control registers, and with two 16-bit data registers, each split in two 8-bit registers.

PWM CYCLE REGISTER LOW (CYREGL)

PWM1 Register Address: 0011h

PWM2 Register Address: 0019h

Read/Write
Reset Value: 0000 0000 (00h)

This is an 8-bit register that contains the low part of the value to be multiplied by internal clock period.

7							0
MSB							LSB

PWM CYCLE REGISTER HIGH (CYREGH)

PWM1 Register Address: 0010h

PWM2 Register Address: 0018h

Read/Write
Reset Value: 0000 0000 (00h)

This is an 8-bit register that contains the high part of the value to be multiplied by internal clock period.

7							0
MSB							LSB

PWM DUTYCYCLE REGISTER LOW (DUTYREGL)

PWM1 Register Address: 0013h

PWM2 Register Address: 001Bh

Read/Write
Reset Value: 0000 0000 (00h)

This is an 8-bit register that contains the low part of the value corresponding to the binary weight of the PWM pulse.

7							0
MSB							LSB

PWM DUTYCYCLE REGISTER HIGH (DUTYREGH)

PWM1 Register Address: 0012h

PWM2 Register Address: 001Ah

Read/Write
Reset Value: 0000 0000 (00h)

This is an 8-bit register that contains the high part of the value corresponding to the binary weight of the PWM pulse**.**

7							0
MSB							LSB

PWM CONTROL REGISTER (CONREG)

PWM1 Register Address: 0014h

PWM2 Register Address: 001Ch

Read/Write
Reset Value: 0000 0000 (00h)

7			4	3	2	1	0
0	0	0	PS2	PS1	PS0	EN_ INT	EN_ PWM

Bit 0= **EN _PWM**: 1 = enables the PWM output, 0 = disables PWM output.

Bit 1= **EN _INT**: 1 = enables interrupt request, 0 disables interrupt request.

Bit 4, 3, 2= **PS2**,**PS1**,**PS0**: prescaler bits

The value of the PWM internal clock depends on these bits.

PS2	PS1	PS0	PWM internal clock
0	0	0	f_{CPU}
0	0	1	f_{CPU} / 2
0	1	0	f_{CPU} / 4
0	1	1	f_{CPU} / 8
1	0	0	f_{CPU} / 16
1	0	1	f_{CPU} / 32
1	1	0	f_{CPU} / 64
1	1	1	f_{CPU} / 128

Bit 5, 6, 7= not used.

PWM COUNTER REGISTER LOW (CTL)

PWM1 Register Address: 0016h

PWM2 Register Address: 001Eh

Read Only
Reset Value: 0000 0000 (00h)

This is an 8-bit register that contains the low part of the PWM counter value.

7							0
MSB							LSB

PWM COUNTER REGISTER HIGH(CTH)

PWM1 Register Address: 0015h

PWM2 Register Address: 001Dh

Read Only
Reset Value: 0000 0000 (00h)

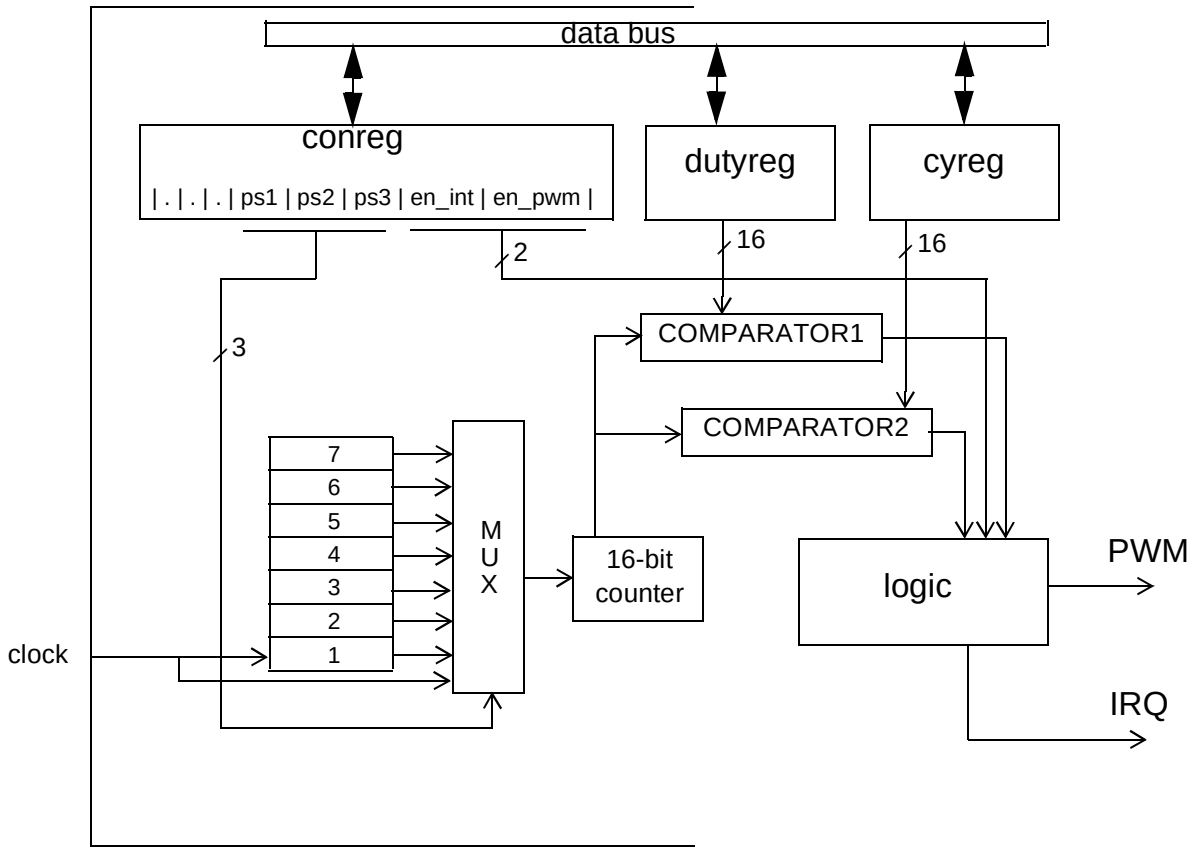
This is an 8-bit register that contains the high part of the PWM counter value.

7							0
MSB							LSB

Table 9. PWM Timing (f_{CPU} = 8MHz)

Prescaler (PS)	$T_{internal\ clock}$	CYREG @16 bit Resolution	PWM $_{cycle}$ @ f_{in}=8MHz
0	$1/f_{in} * 2^{ps}$	$1/f_{in} * 2^{ps} * 1$.....$1/f_{in} * 2^{ps} * 65535$	0.125 µs..... ~8192 µs
1	$1/f_{in} * 2^{ps}$	$1/f_{in} * 2^{ps} * 1$.....$1/f_{in} * 2^{ps} * 65535$	0.25 µs..... ~16384 µs
2	$1/f_{in} * 2^{ps}$	$1/f_{in} * 2^{ps} * 1$.....$1/f_{in} * 2^{ps} * 65535$	0.5 µs..... ~32768 µs
3	$1/f_{in} * 2^{ps}$	$1/f_{in} * 2^{ps} * 1$.....$1/f_{in} * 2^{ps} * 65535$	1 µs..... 65535 µs
4	$1/f_{in} * 2^{ps}$	$1/f_{in} * 2^{ps} * 1$.....$1/f_{in} * 2^{ps} * 65535$	2 µs..... 131070 µs
5	$1/f_{in} * 2^{ps}$	$1/f_{in} * 2^{ps} * 1$.....$1/f_{in} * 2^{ps} * 65535$	4 µs..... 262140 µs
6	$1/f_{in} * 2^{ps}$	$1/f_{in} * 2^{ps} * 1$.....$1/f_{in} * 2^{ps} * 65535$	8 µs..... 524280 µs
7	$1/f_{in} * 2^{ps}$	$1/f_{in} * 2^{ps} * 1$.....$1/f_{in} * 2^{ps} * 65535$	16 µs..... 1048560 µs

Figure 28. PWM Block Diagram



5.4 PWM I/O

5.4.1 Introduction

The PWM I/O interface is a circuit able to connect internal logic circuits with external high voltage lines.

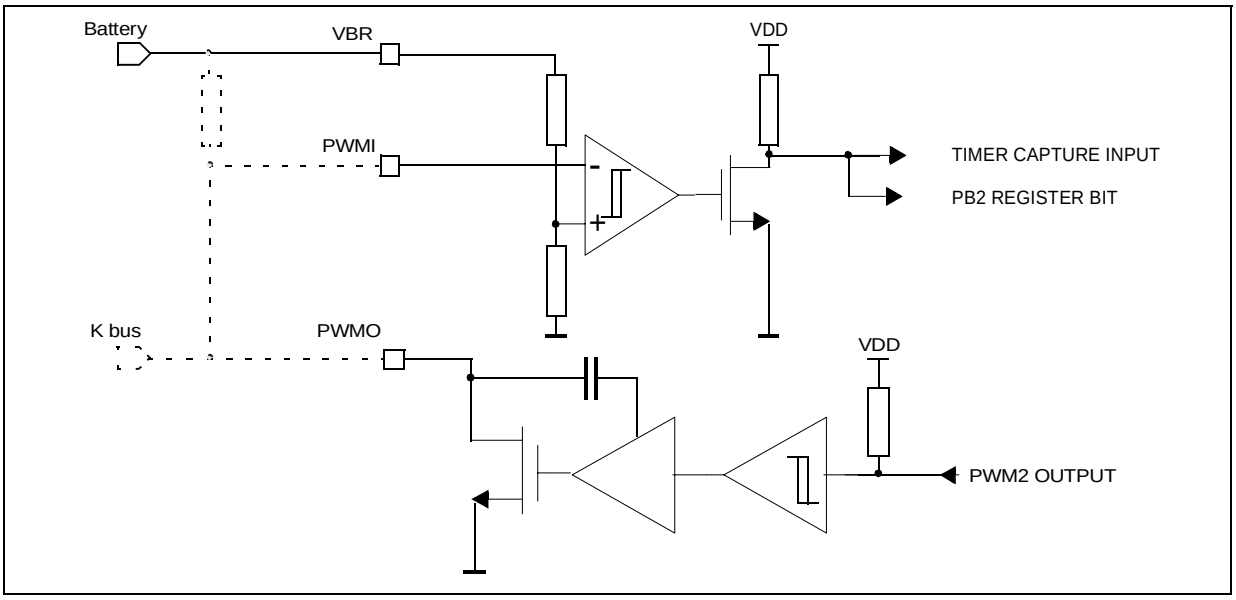
The two interfaces represent respectively the receiver and the transmitter section of a standard IS0 9141 transceiver.

Connecting PWMO and PWMI together a standard K bus (ISO 9141) can be realized.

Voltage thresholds are referred to the battery voltage connected to VBR pin. This pin must be used as reference for the K bus. Voltage drops between this pin and the battery line can cause thresholds mismatch between the L9805 ISO trasceiver and the counterpart trasceiver(s) connected to the same bus line.

See Figure 29 for a block diagram description of the two interfaces.

Figure 29. PWM I/O Block Diagram



5.4.2 PWMO

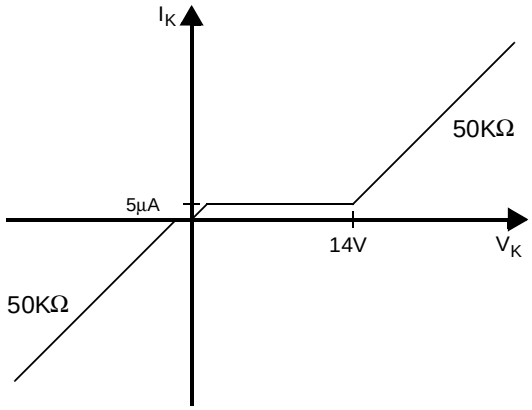
PWMO is an output line, directly driven by the PWM2 output signal. The circuit translates the logic levels of PWM2 output to voltage levels referred to the VB supply (see Figure 29). When PWM2=0 the open drain is switched off, in the other case the PWMO line is pulled down by the open drain driver.

PWMO is protected against short circuit to battery by a dedicated circuit that limits the current sunk by the output transistor. When the limiter is activated the voltage on PWMO pin rises up. If the limiter remains active for more than 25µs the driver is switched off.

If the battery or ground connection are lost, the PWMO line shows a controlled impedance characteristic (see Figure 30).

PWM0 is high at NRESET is asserted.

Figure 30. Impedance at PWMO/I pin



5.4.3 PWMI

PWMI is an input line, directly connected to PB2 bit. The circuit translates the voltage levels referred to VB voltage supply to the internal logic levels (see Figure 29). When the voltage on PWMI

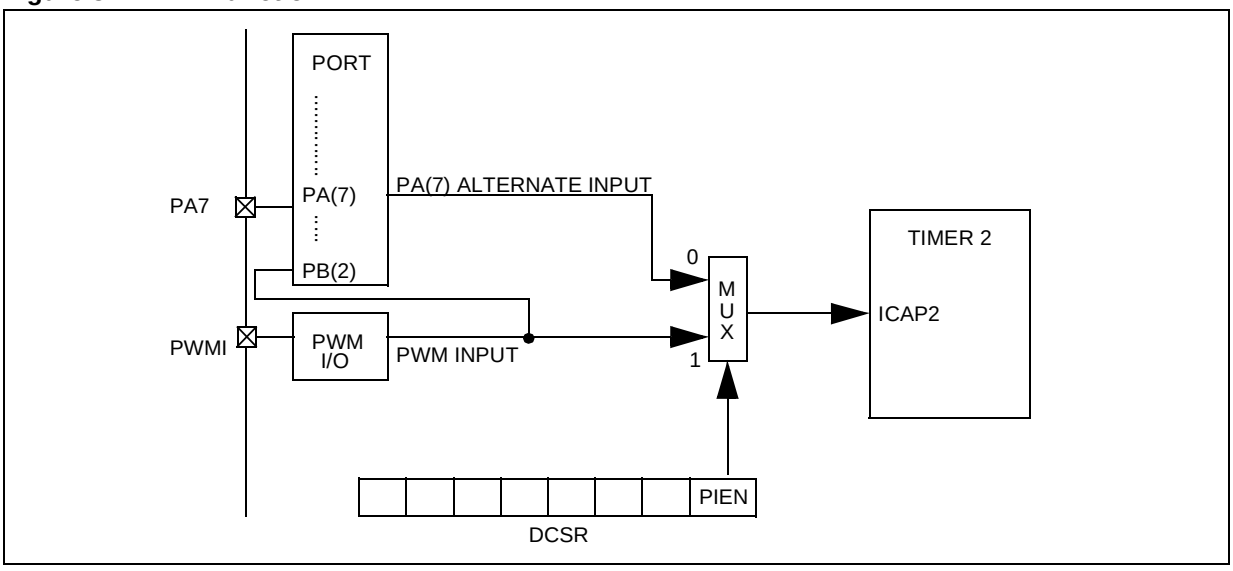
pin is higher than VB/2 PB2 reads an high logic level.

If the bit PWMI in DCSR register is set (see Section 3.2.1), PWMI is directly connected with the Input Capture 2 on Timer 2, which is otherwise connected in alternate function to PA7 (see Figure 31).

An internal pull down current generator (5uA) allows to detect the Open Bus condition (external pull up missing).

If the battery or ground connection are lost, the PWMI line shows a controlled impedance characteristic (see Figure 30)..

Figure 31. PWMI function



5.5 10-BIT A/D CONVERTER (AD10)

5.5.1 Introduction

The Analog to Digital converter is a single 10-bit successive approximation converter with 4 input channels. Analog voltage from external sources are input to the converter through AD2,AD3 and AD4 pins. Channel 1 (AD1) is connected to the internal temperature sensor (see Section 5.5.5).

Note The anti aliasing filtering must be accomplished using an external RC filter. The internal AD1 channel is filtered by an RC network with approx. 1us time constant.

5.5.2 Functional Description

The result of the conversion is stored in 2 registers: the Data Register High (ADCDRH) and the Data Register Low (ADCDRL).

The A/D converter is enabled by setting the ADST bit in ADCCSR Register. Bits CH1 and CH0 of ADCCSR Register select the channel to be converted. The high and low reference voltage are connected to pins VCC and AGND.

When enabled, the A/D converter performs a complete conversion in 14us (with system clock f_{CPU}=8Mhz). The total conversion time includes multiplex, sampling of the input voltage, 10-bit conversion and writing DRH and DRL registers.

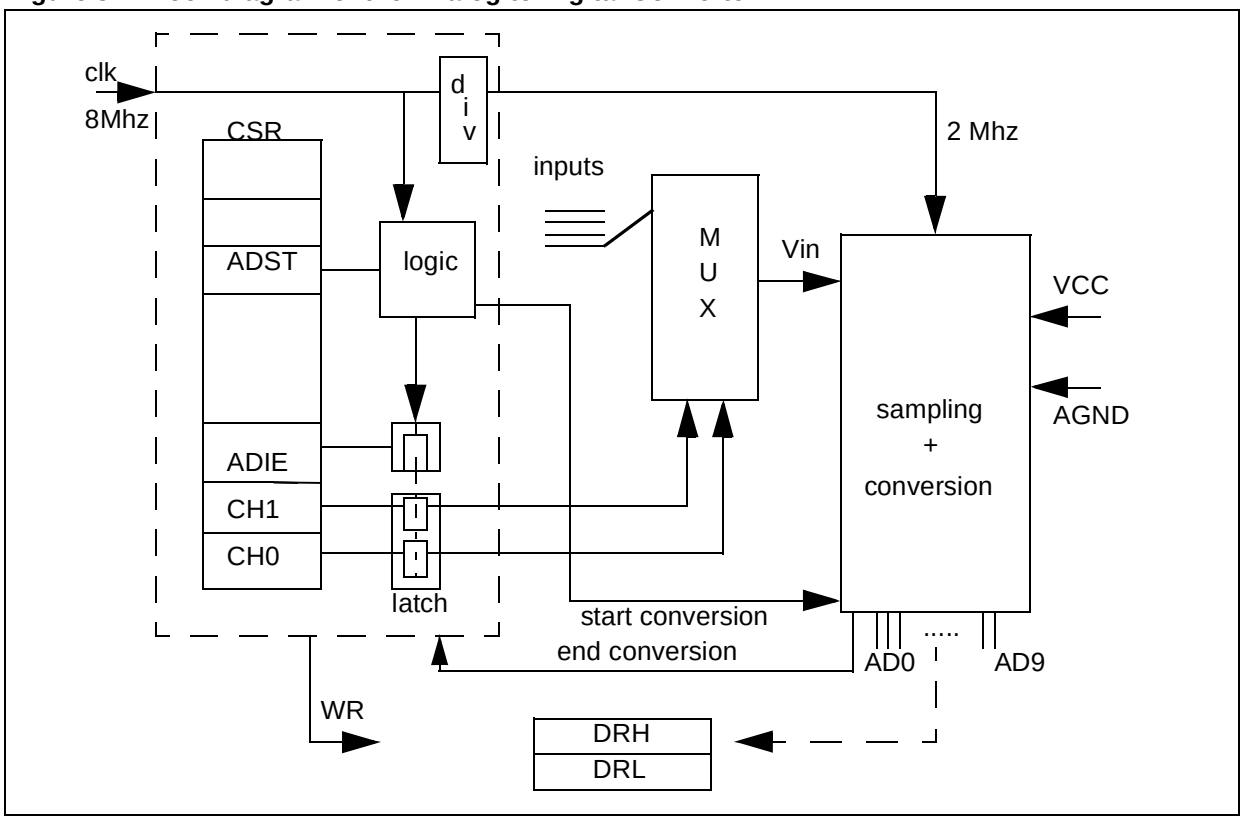
When the conversion is completed COCO bit (COnversion COmpleted) is set in ADCCSR.

A conversion starts from the moment ADST bit is set. When a conversion is running it is possible to write the ADCCSR without stopping the ADC operations, because all the data in ADCCSR are latched when ADST is set. This property allows to select a different channel to be processed during the next conversion or to manage the interrupt enable bit. The new setting will have effect on the next conversion (including interrupt generation)

At the end of the conversion ADST is reset and COCO bit is set.

Note To start a new conversion the ADST must be set after the completion of the current one. Any writing to ADST when a conversion is running (COCO=0) has no effect since ADST bit is automatically reset by the end of conversion event.

Figure 32. Block diagram of the Analog to Digital Converter



5.5.3 Input Selections and Sampling

The input section of the ADC includes the analog multiplexer and a buffer. The input of the buffer is permanently connected to the multiplexer output. The buffer output is fed to the sample and hold circuit.

The multiplexer is driven with CH1 and CH0 bit only after ADST is set. Starting from this event, the sampler follows the selected input signal for 2.5us and then holds it for the remaining conversion time (i.e. when the conversion is actually running).

5.5.4 Interrupt Management

If ADIE bit is set in register ADCCSR, an interrupt is generated when a conversion is completed (i.e. when COCO is set).

The interrupt request is cleared when any of the ADC registers is access (either read or write).

Enabling/disabling the interrupt generation while the conversion is running has no effect on the current conversion. ADIE value is latched when ADST is set and this internal value holds all the conversion time long.

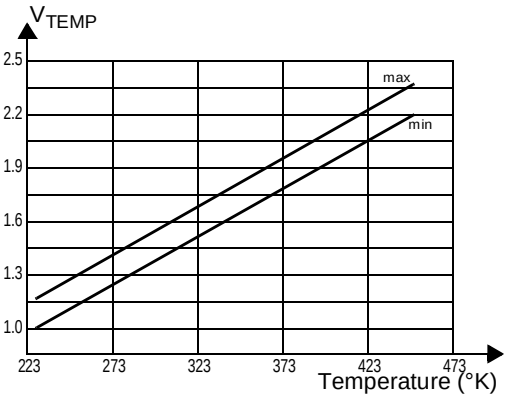
5.5.5 Temperature Sensing

The AD1 input is internally connected to the output of a temperature sensing circuit.

The sensor generates a voltage proportional to the absolute temperature of the die. It works over the whole temperature range, with a minimum resolution of 1LSB/°K (5mV/°K) (Figure 33 shows the indicative voltage output of the sensor).

Note The voltage output of the sensor is only related to the absolute temperature of the silicon junctions. Junction temperature and ambient temperature must be related taking in account the power dissipated by the device and the thermal resistance Rth_{je} between the silicon and the environment around the application board.

Figure 33. Temperature Sensor output



The output of the sensor is not ratiometric with the voltage reference for the ADC conversion (VCC). When calculating the ADC reading error of this signal the variation of VCC must be accounted. Additional errors are due to the intrinsic spread of the sensor characteristic.

5.5.6 Precise Temperature Measurement

To allow a more precise measurement of the temperature a trimming procedure can be adopted (on request).

The temperature is measured in EWS and two values are stored in four EEPROM bytes (see memory map):

T0L,T0H: temperature of the trimming measurement (in Kelvin).

VT0L,VT0H: output value of the ADC corresponding to T0 (in number of LSBs).

The corrected measurement of the temperature **in Kelvin** must be accomplished in the following way:

TEMP (in °K) = VTEMP * T0 / VT0

where VTEMP is the output code in LSB of the ADC corresponding to the measurement.

Example:

If the value stored in EEPROM are:

0C7Ch: 01h ->T0H

0C7Dh: 43h ->T0L

0C7Eh: 01h -> VT0H

0C7Fh: 5Ch -> VT0L

T0 = 0143h = 323K (50 Celsius)

VTo = 015Ch = 348 LSB (conversion of 1.7V, sensor output)

and the sensor output is 2V, converted by the ADC in code 0110011001 = 019Ah = 410LSB, the temperature of the chip is

TEMP = 019Ah * 0143h / 015Ch = 017Ch

equivalent to:

TEMP = 410 * 323 / 348 = 380 K = 107 °C

Note The sensor circuit may have two kind of error: one translating its output characteristic up and down and the other changing its slope. The described trimming recovers only the translation errors but can not recover slope error. After trimming, being T_{TRIM} the trimming temperature, the specified precision can be achieved in the range T_{TRIM}-80, max[T_{TRIM}+80, 150°C]. Precision is related to the read temperature in Kelvin.

5.5.7 Register Description

CONTROL/STATUS REGISTER (ADCCSR)

Address: 0072h — Read/Write

Reset Value: 0010 0000 (20h)

7							0
0	0	COCO	ADIE	0	ADST	CH1	CH0

Bit 7,6 = **Reserved**

Bit 5 =**COCO** *(Read Only) Conversion Complete*

COCO is set (by the ADC) as soon as a conversion is completed (results can be read). COCO is cleared by setting ADST=1 (start of new conversion). If COCO=0 a conversion is running, if COCO=1 no conversion is running.

Bit 4 = **ADIE** *A/D Interrupt Enable*

This bit is used to enable / disable the interrupt function:
0: interrupt disabled
1: interrupt enabled

Bit 3= **Reserved**

Bit 2= **ADST** *Start Conversion*

When this bit is set a new conversion starts. ADST is automatically reset when the conversion is completed (COCO=1).

Bits 1-0 = **CH1-CH0** *Channel Selection*

These bits select the analog input to convert. See Table 10 for reference.

Table 10. ADC Channel Selection Table

CH1	CH0	Channel
0	0	AD1, Temperature Sensor
0	1	AD2, external input
1	0	AD3, external input
1	1	AD4, external input

DATA REGISTER HIGH (ADCDRH)

Address: 0070h — Read Only

Reset Value: 00000 0000 (00h)

7							0
0	0	0	0	0	0	AD9	AD8

Bit 1:0 = **AD9-AD8** *Analog Converted Value*

This register contains the high part of the converted analog value

DATA REGISTER LOW (ADCDRL)

Address: 0071h — Read Only

Reset Value: 00000 0000 (00h)

7							0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Bit 7:0 = **AD7-AD0** *Analog Converted Value*

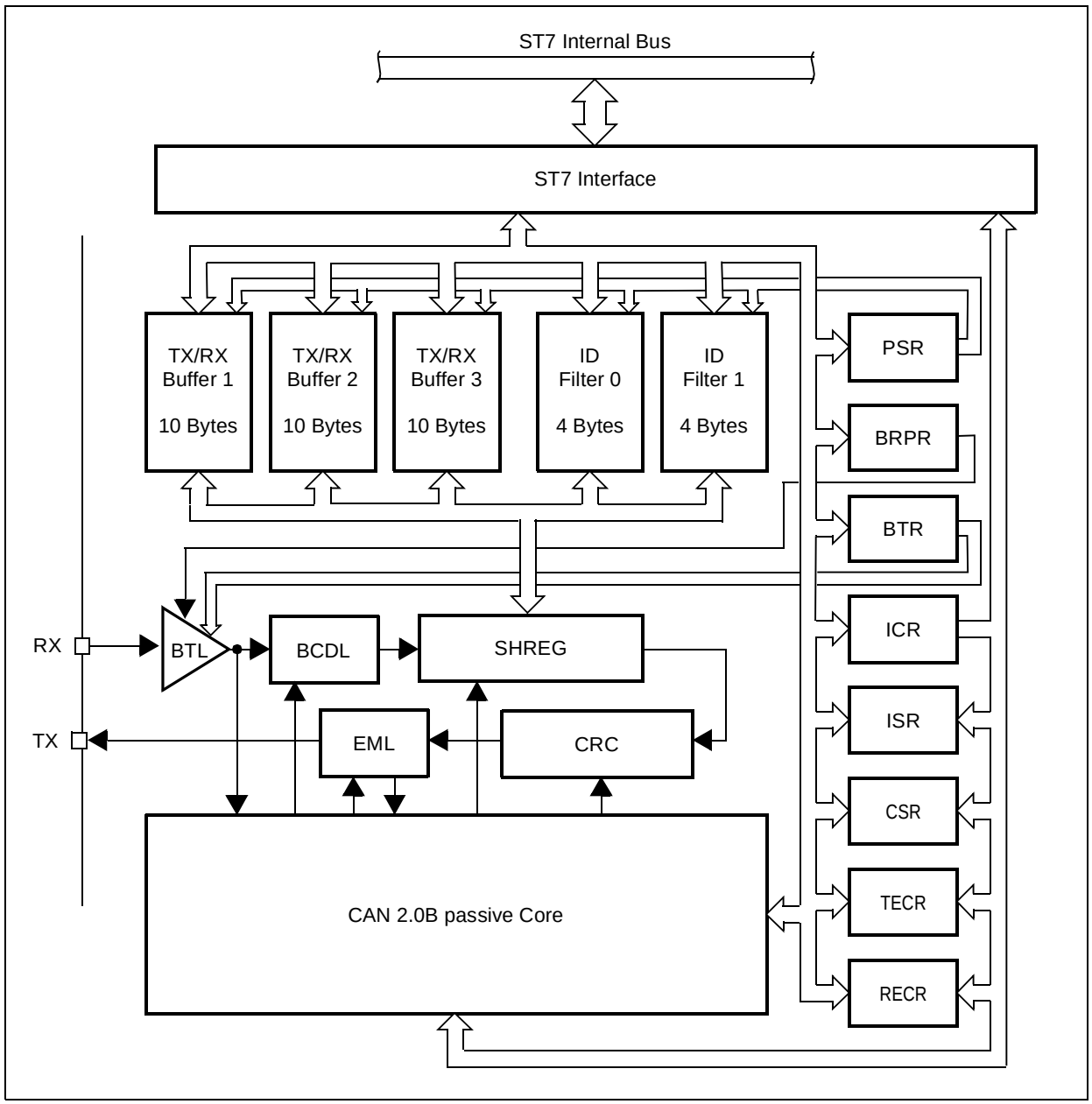
This register contains the low part of the converted analog value

5.6 CONTROLLER AREA NETWORK (CAN)

5.6.1 Introduction

This peripheral is designed to support serial data exchanges using a multi-master contention based priority scheme as described in CAN specification Rev. 2.0 part A. It can also be connected to a 2.0 B network without problems, since extended frames are checked for correctness and acknowledged accordingly although such frames cannot be transmitted nor received. The same applies to overload frames which are recognized but never initiated.

Figure 34. CAN Block Diagram



CONTROLLER AREA NETWORK (Cont'd)

5.6.2 Main Features

– Support of CAN specification 2.0A and 2.0B passive
– Three prioritized 10-byte Transmit/Receive message buffers
– Two programmable global 12-bit message acceptance filters
– Programmable baud rates up to 1 MBit/s
– Buffer flip-flopping capability in transmission
– Maskable interrupts for transmit, receive (one per buffer), error and wake-up
– Automatic low-power mode after 20 recessive bits or on demand (stand-by mode)
– Interrupt-driven wake-up from stand-by mode upon reception of dominant pulse
– Optional dominant pulse transmission on leaving stand-by mode
– Automatic message queuing for transmission upon writing of data byte 7
– Programmable loop-back mode for self-test operation
– Advanced error detection and diagnosis functions
– Software-efficient buffer mapping at a unique address space
– Scalable architecture.

5.6.3 Functional Description

5.6.3.1 Frame Formats

A summary of all the CAN frame formats is given in Figure 35 for reference. It covers only the standard frame format since the extended one is only acknowledged.

A message begins with a start bit called Start Of Frame (SOF). This bit is followed by the arbitration field which contains the 11-bit identifier (ID) and the Remote Transmission Request bit (RTR). The RTR bit indicates whether it is a data frame or a remote request frame. A remote request frame does not have any data byte.

The control field contains the Identifier Extension bit (IDE), which indicates standard or extended format, a reserved bit (ro) and, in the last four bits, a count of the data bytes (DLC). The data field ranges from zero to eight bytes and is followed by the Cyclic Redundancy Check (CRC) used as a frame integrity check for detecting bit errors.

The acknowledgement (ACK) field comprises the ACK slot and the ACK delimiter. The bit in the ACK slot is placed on the bus by the transmitter as a recessive bit (logical 1). It is overwritten as a dominant bit (logical 0) by those receivers which have at this time received the data correctly. In this way, the transmitting node can be assured that at least one receiver has correctly received its message. Note that messages are acknowledged by the receivers regardless of the outcome of the acceptance test.

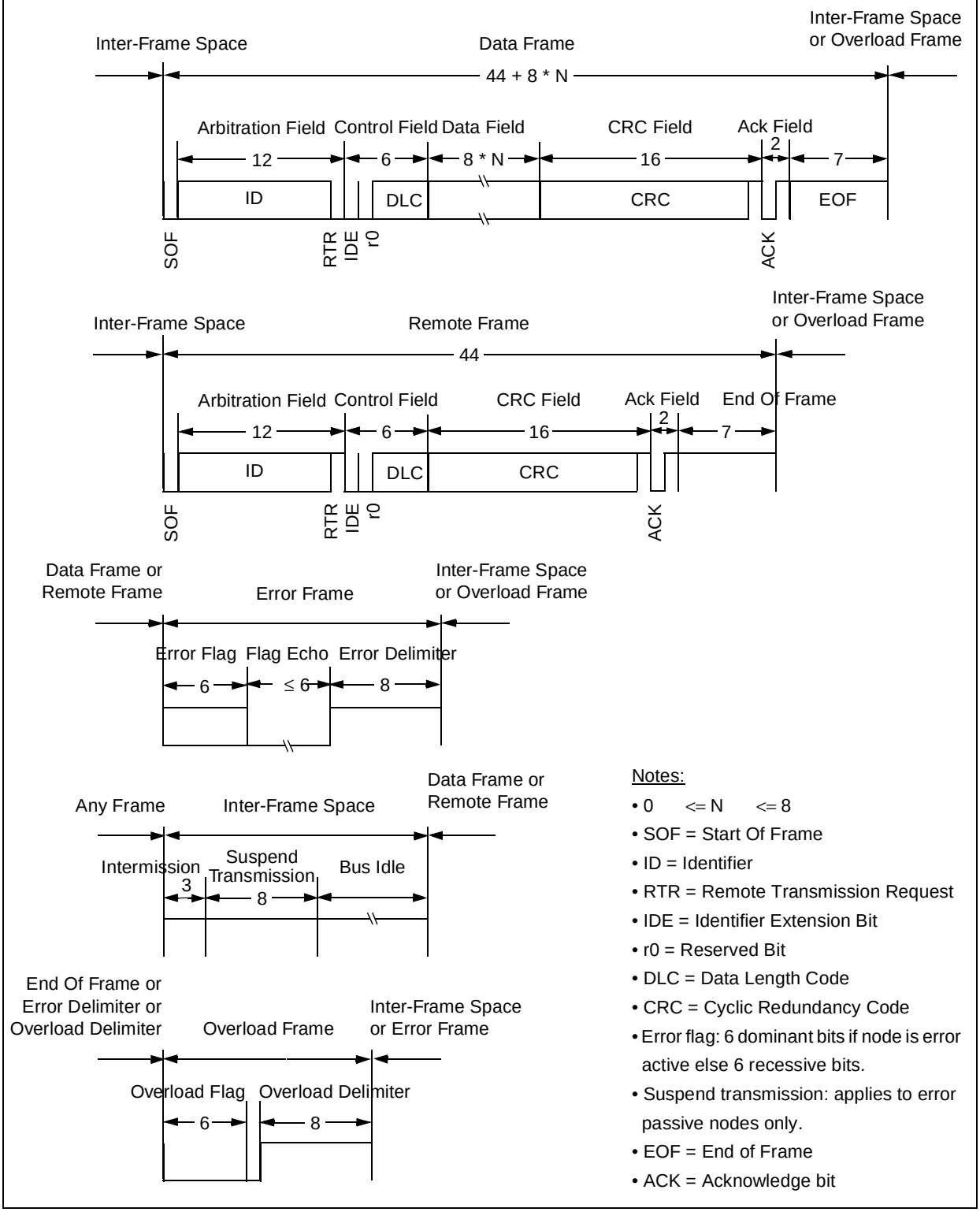
The end of the message is indicated by the End Of Frame (EOF). The intermission field defines the minimum number of bit periods separating consecutive messages. If there is no subsequent bus access by any station, the bus remains idle.

5.6.3.2 Hardware Blocks

The CAN controller contains the following functional blocks (refer to Figure 34):

– ST7 Interface: buffering of the ST7 internal bus and address decoding of the CAN registers.
– TX/RX Buffers: three 10-byte buffers for transmission and reception of maximum length messages.
– ID Filters: two 12-bit compare and don't care masks for message acceptance filtering.
– PSR: page selection register (see memory map).
– BRPR: clock divider for different data rates.
– BTR: bit timing register.
– ICR: interrupt control register.
– ISR: interrupt status register.
– CSR: general purpose control/status register.
– TECR: transmit error counter register.
– RECR: receive error counter register.
– BTL: bit timing logic providing programmable bit sampling and bit clock generation for synchronization of the controller.
– BCDL: bit coding logic generating a NRZ-coded data-stream with stuff bits.
– SHREG: 8-bit shift register for serialization of data to be transmitted and parallelisation of received data.
– CRC: 15-bit CRC calculator and checker.
– EML: error detection and management logic.
– CAN Core: CAN 2.0B passive protocol controller.

Figure 35. CAN Frames



Notes:

- 0 <= N <= 8
- SOF = Start Of Frame
- ID = Identifier
- RTR = Remote Transmission Request
- IDE = Identifier Extension Bit
- r0 = Reserved Bit
- DLC = Data Length Code
- CRC = Cyclic Redundancy Code
- Error flag: 6 dominant bits if node is error active else 6 recessive bits.
- Suspend transmission: applies to error passive nodes only.
- EOF = End of Frame
- ACK = Acknowledge bit

CONTROLLER AREA NETWORK (Cont'd)

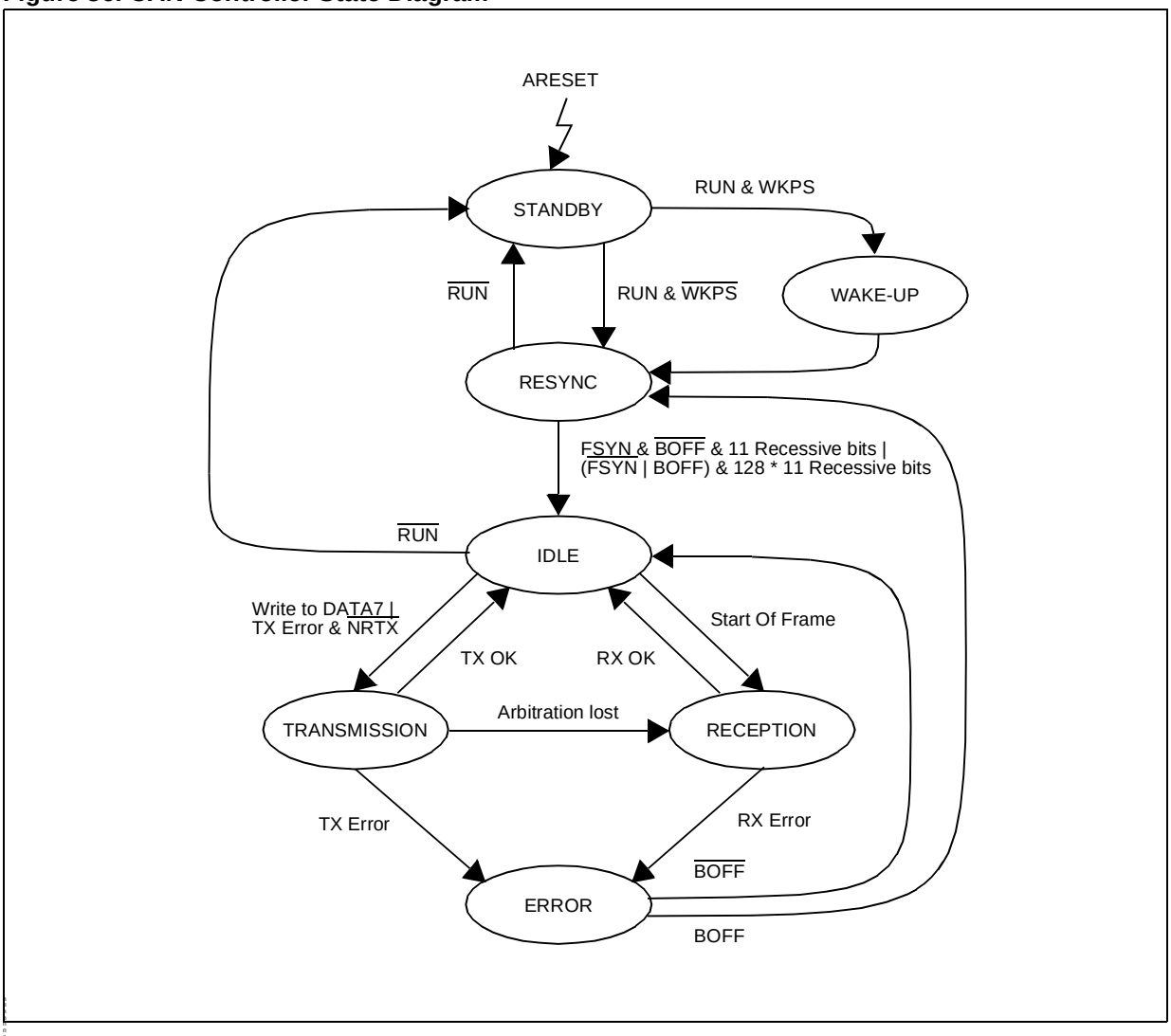
5.6.3.3 Modes of Operation

The CAN Core unit assumes one of the seven states described below:

– **STANDBY**. Stand-by mode is entered either on a chip reset or on resetting the RUN bit in the Control/Status Register (CSR). Any on-going transmission or reception operation is not interrupted and completes normally before the Bit Time Logic and the clock prescaler are turned off for minimum power consumption. This state is signalled by the RUN bit being read-back as 0. Once in stand-by, the only event monitored is the reception of a dominant bit which causes a wake-up interrupt if the SCIE bit of the Interrupt Control Register (ICR) is set.
The STANDBY mode is left by setting the RUN bit. If the WKPS bit is set in the CSR register, then the controller passes through WAKE-UP otherwise it enters RESYNC directly.
It is important to note that the wake-up mechanism is software-driven and therefore carries a significant time overhead. All messages received after the wake-up bit and before the controller is set to run and has completed synchronization are ignored.

– **WAKE-UP**. The CAN bus line is forced to dominant for one bit time signalling the wake-up condition to all other bus members.

Figure 36. CAN Controller State Diagram



CONTROLLER AREA NETWORK (Cont'd)

– **RESYNC**. The re-synchronization mode is used to find the correct entry point for starting transmission or reception after the node has gone asynchronous either by going into the STANDBY or bus-off states.
Re-synchronization is achieved when 128 sequences of 11 recessive bits have been monitored unless the node is not bus-off and the FSYN bit in the CSR register is set in which case a single sequence of 11 recessive bits needs to be monitored.

– **IDLE**. The CAN controller looks for one of the following events: the RUN bit is reset, a Start Of Frame appears on the CAN bus or the DATA7 register of the currently active page is written to.

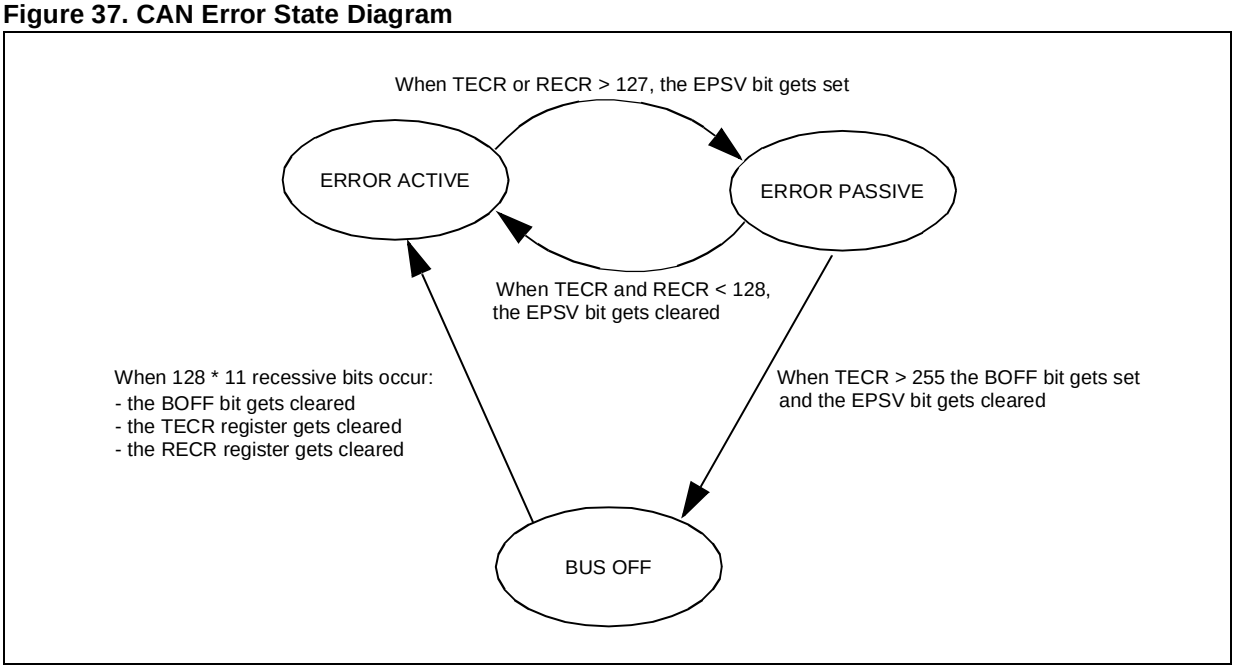
– **TRANSMISSION**. Once the LOCK bit of a Buffer Control/Status Register (BCSRx) has been set and read back as such, a transmit job can be submitted by writing to the DATA7 register. The message with the highest priority will be transmitted as soon as the CAN bus becomes idle. Among those messages with a pending transmission request, the highest priority is given to Buffer 3 then 2 and 1. If the transmission fails due to a lost arbitration or to an error while the NRTX bit of the CSR register is reset, then a new transmission attempt is performed. This goes on until the transmission ends successfully or until the job is cancelled by unlocking the buffer, by setting the NRTX bit or if the node ever enters bus-off or if a higher priority message becomes pending. The RDY bit in the BCSRx register, which was set since the job was submitted, gets reset. When a transmission is in progress, the BUSY bit in the BCSRx register is set. If it ends successfully then the TXIF bit in the Interrupt Status Register (ISR) is set, else the TEIF bit is set. An interrupt is generated in either case provided the TXIE and TEIE bits of the ICR register are set. The ETX bit in the same register is used to get an early transmit interrupt and to automatically unlock the transmitting buffer upon successful completion of its job. This enables the CPU to get a new transmit job pending by the end of the current transmission while always leaving two buffers available for reception. An uninterrupted stream of messages may be transmitted in this way at no overrun risk.
Note: Setting the SRTE bit of the CSR register allows transmitted messages to be simultaneously received when they pass the acceptance filtering. This is particularly useful for checking the integrity of the communication path.

– **RECEPTION**. Once the CAN controller has synchronized itself onto the bus activity, it is ready for reception of new messages. Every incoming message gets its identifier compared to the acceptance filters. If the bit-wise comparison of the selected bits ends up with a match for at least one of the filters then that message is elected for reception and a target buffer is searched for. This buffer will be the first one - order is 1 to 3 - that has the LOCK and RDY bits of its BCSRx register reset.
  – When no such buffer exists then an overrun interrupt is generated if the ORIE bit of the ICR register has been set. In this case the identifier of the last message is made available in the Last Identifier Register (LIDHR and LIDLR) at least until it gets overwritten by a new identifier picked-up from the bus.
  – When a buffer does exist, the accepted message gets written into it, the ACC bit in the BCSRx register gets the number of the matching filter, the RDY and RXIF bits get set and an interrupt is generated if the RXIE bit in the ISR register is set.

  Up to three messages can be automatically received without intervention from the CPU because each buffer has its own set of status bits, greatly reducing the reactiveness requirements in the processing of the receive interrupts.

– **ERROR**. The error management as described in the CAN protocol is completely handled by hardware using 2 error counters which get incremented or decremented according to the error condition. Both of them may be read by the application to determine the stability of the network. Moreover, as one of the node status bits (EPSV or BOFF of the CSR register) changes, an interrupt is generated if the SCIE bit is set in the ICR Register. Refer to Figure 37.

Figure 37. CAN Error State Diagram



CONTROLLER AREA NETWORK (Cont'd)

5.6.3.4 Bit Timing Logic

The bit timing logic monitors the serial bus-line and performs sampling and adjustment of the sample point by synchronizing on the start-bit edge and resynchronization on following edges.

Its operation may be explained simply when the nominal bit time is divided into three segments as follows:

– **Synchronisation segment (SYNC_SEG)**: a bit change is expected to lie within this time segment. It has a fixed length of one time quanta (1 x t_{CAN}).

– **Bit segment 1 (BS1)**: defines the location of the sample point. It includes the PROP_SEG and PHASE_SEG1 of the CAN standard. Its duration is programmable between 1 and 16 time quanta but may be automatically lengthened to compensate for positive phase drifts due to differences in the frequency of the various nodes of the network.

– **Bit segment 2 (BS2)**: defines the location of the transmit point. It represents the PHASE_SEG2 of the CAN standard. Its duration is programmable between 1 and 8 time quanta but may also be automatically shortened to compensate for negative phase drifts.

The resynchronization jump width (RJW) defines an upper bound to the amount of lengthening or shortening of the bit segments. It is programmable between 1 and 4 time quanta.

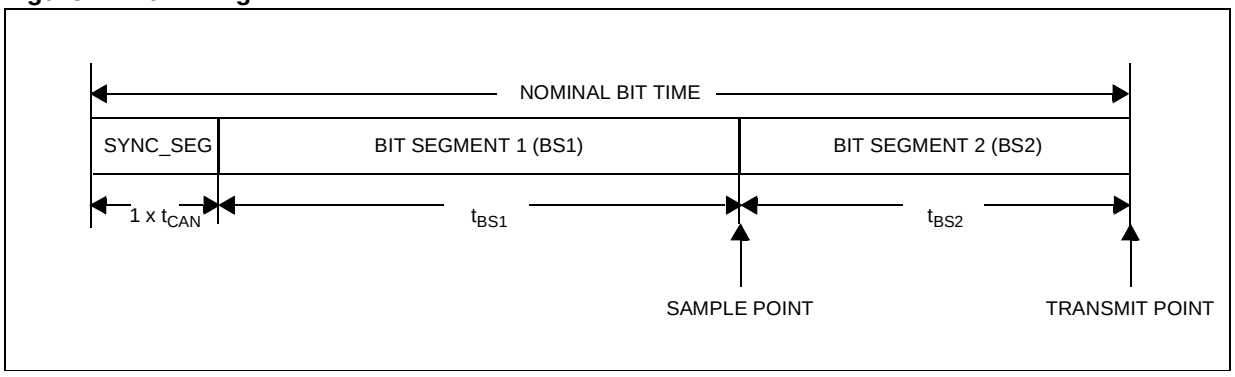
A valid edge is defined as the first transition in a bit time from dominant to recessive bus level provided the controller itself does not send a recessive bit.

If a valid edge is detected in BS1 instead of SYNC_SEG, BS1 is extended by up to RJW so that the sample point is delayed.

Conversely, if a valid edge is detected in BS2 instead of SYNC_SEG, BS2 is shortened by up to RJW so that the transmit point is moved earlier.

As a safeguard against programming errors, the configuration of the Bit Timing Register (BTR) is only possible while the device is in STANDBY mode.

Figure 1. Bit Timing



CONTROLLER AREA NETWORK (Cont'd)

5.6.4 Register Description

The CAN registers are organized as 6 general purpose registers plus 5 pages of 16 registers spanning the same address space and primarily used for message and filter storage. The page actually selected is defined by the content of the Page Selection Register. Refer to Figure 38.

5.6.4.1 General Purpose Registers

INTERRUPT STATUS REGISTER (ISR)

Address: 005Ah - Read/Write

Reset Value: 00h

7							0
RXIF3	RXIF2	RXIF1	TXIF	SCIF	ORIF	TEIF	EPND

Bit 7 = **RXIF3** *Receive Interrupt Flag for Buffer 3*
— Read/Clear
Set by hardware to signal that a new error-free message is available in buffer 3.
Cleared by software to release buffer 3.
Also cleared by resetting bit RDY of BCSR3.

Bit 6 = **RXIF2** *Receive Interrupt Flag for Buffer 2*
— Read/Clear
Set by hardware to signal that a new error-free message is available in buffer 2.
Cleared by software to release buffer 2.
Also cleared by resetting bit RDY of BCSR2.

Bit 5 = **RXIF1** *Receive Interrupt Flag for Buffer 1*
— Read/Clear
Set by hardware to signal that a new error-free message is available in buffer 1.
Cleared by software to release buffer 1.
Also cleared by resetting bit RDY of BCSR1.

Bit 4 = **TXIF** *Transmit Interrupt Flag*
— Read/Clear
Set by hardware to signal that the highest priority message queued for transmission has been successfully transmitted (ETX = 0) or that it has passed successfully the arbitration (ETX = 1).
Cleared by software.

Bit 3 = **SCIF** *Status Change Interrupt Flag*
— Read/Clear
Set by hardware to signal the reception of a dominant bit while in standby or a change from error active to error passive and bus-off while in run. Also signals any receive error when ESCI = 1.
Cleared by software.

Bit 2 = **ORIF** *Overrun Interrupt Flag*
— Read/Clear
Set by hardware to signal that a message could not be stored because no receive buffer was available.
Cleared by software.

Bit 1 = **TEIF** *Transmit Error Interrupt Flag*
— Read/Clear
Set by hardware to signal that an error occurred during the transmission of the highest priority message queued for transmission.
Cleared by software.

Bit 0 = **EPND** *Error Interrupt Pending*
— Read Only
Set by hardware when at least one of the three error interrupt flags SCIF, ORIF or TEIF is set.
Reset by hardware when all error interrupt flags have been cleared.

Caution;

Interrupt flags are reset by writing a "0" to the corresponding bit position. The appropriate way consists in writing an immediate mask or the one's complement of the register content initially read by the interrupt handler. Bit manipulation instruction BRES should never be used due to its read-modify-write nature.

CONTROLLER AREA NETWORK (Cont'd)

INTERRUPT CONTROL REGISTER (ICR)

Address: 005Bh - Read/Write

Reset Value: 00h

7							0
0	ESCI	RXIE	TXIE	SCIE	ORIE	TEIE	ETX

Bit 6 = **ESCI** *Extended Status Change Interrupt*
— Read/Set/Clear
Set by software to specify that SCIF is to be set on receive errors also.
Cleared by software to set SCIF only on status changes and wake-up but not on all receive errors.

Bit 5 = **RXIE** *Receive Interrupt Enable*
— Read/Set/Clear
Set by software to enable an interrupt request whenever a message has been received free of errors.
Cleared by software to disable receive interrupt requests.

Bit 4 = **TXIE** *Transmit Interrupt Enable*
— Read/Set/Clear
Set by software to enable an interrupt request whenever a message has been successfully transmitted.
Cleared by software to disable transmit interrupt requests.

Bit 3 = **SCIE** *Status Change Interrupt Enable*
— Read/Set/Clear
Set by software to enable an interrupt request whenever the node's status changes in run mode or whenever a dominant pulse is received in standby mode.
Cleared by software to disable status change interrupt requests.

Bit 2 = **ORIE** *Overrun Interrupt Enable*
— Read/Set/Clear
Set by software to enable an interrupt request whenever a message should be stored and no receive buffer is avalaible.
Cleared by software to disable overrun interrupt requests.

Bit 1 = **TEIE** *Transmit Error Interrupt Enable*
— Read/Set/Clear
Set by software to enable an interrupt whenever an error has been detected during transmission of a message.
Cleared by software to disable transmit error interrupts.

Bit 0 = **ETX** *Early Transmit Interrupt*
— Read/Set/Clear
Set by software to request the transmit interrupt to occur as soon as the arbitration phase has been passed successfully.
Cleared by software to request the transmit interrupt to occur at the completion of the transfer.

CONTROLLER AREA NETWORK (Cont'd)

CONTROL/STATUS REGISTER (CSR)

Address: 005Ch - Read/Write

Reset Value: 00h

7							0
0	BOFF	EPSV	SRTE	NRTX	FSYN	WKPS	RUN

Bit 6 = **BOFF** *Bus-Off State*
— Read Only
Set by hardware to indicate that the node is in bus-off state, i.e. the Transmit Error Counter exceeds 255.
Reset by hardware to indicate that the node is involved in bus activities.

Bit 5 = **EPSV** *Error Passive State*
— Read Only
Set by hardware to indicate that the node is error passive.
Reset by hardware to indicate that the node is either error active (BOFF = 0) or bus-off.

Bit 4 = **SRTE** *Simultaneous Receive/Transmit Enable* — Read/Set/Clear
Set by software to enable simultaneous transmission and reception of a message passing the acceptance filtering. Allows to check the integrity of the communication path.
Reset by software to discard all messages transmitted by the node. Allows remote and data frames to share the same identifier.

Bit 3 = **NRTX** *No Retransmission*
— Read/Set/Clear
Set by software to disable the retransmission of unsuccessful messages.
Cleared by software to enable retransmission of messages until success is met.

Bit 2 = **FSYN** *Fast Synchronization*
— Read/Set/Clear
Set by software to enable a fast resynchronization when leaving standby mode, i.e. wait for only 11 recessive bits in a row.
Cleared by software to enable the standard resynchronization when leaving standby mode, i.e. wait for 128 sequences of 11 recessive bits.

Bit 1 = **WKPS** *Wake-up Pulse*
— Read/Set/Clear
Set by software to generate a dominant pulse when leaving standby mode.
Cleared by software for no dominant wake-up pulse.

Bit 0 = **RUN** *CAN Enable*
— Read/Set/Clear

Set by software to leave stand-by mode after 128 sequences of 11 recessive bits or just 11 recessive bits if FSYN is set.
Cleared by software to request a switch to the stand-by or low-power mode as soon as any on-going transfer is complete. Read-back as 1 in the meantime to enable proper signalling of the stand-by state. The CPU clock may therefore be safely switched OFF whenever RUN is read as 0.

CONTROLLER AREA NETWORK (Cont'd)

BAUD RATE PRESCALER REGISTER (BRPR)

Address: 005Dh - Read/Write in Stand-by mode

Reset Value: 00h

7							0
RJW1	RJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0

RJW[1:0] determine the maximum number of time quanta by which a bit period may be shortened or lengthened to achieve resynchronization.
$t_{RJW} = t_{CAN} * (RJW + 1)$

BRP[5:0] determine the CAN system clock cycle time or time quanta which is used to build up the individual bit timing.
$t_{CAN} = t_{CPU} * (BRP + 1)$

Where t_{CPU} = time period of the CPU clock.
The resulting baud rate can be computed by the formula:

$$BR = \frac{1}{t_{CPU} \times (BRP + 1) \times (BS1 + BS2 + 3)}$$

Note: Writing to this register is allowed only in Stand-by mode to prevent any accidental CAN protocol violation through programming errors.

BIT TIMING REGISTER (BTR)

Address: 005Eh - Read/Write in Stand-by mode

Reset Value: 23h

BS2[2:0] determine the length of Bit Segment 2.
$t_{BS2} = t_{CAN} * (BS2 + 1)$

7							0
0	BS22	BS21	BS20	BS13	BS12	BS11	BS10

BS1[3:0] determine the length of Bit Segment 1.
$t_{BS1} = t_{CAN} * (BS1 + 1)$

Note: Writing to this register is allowed only in Stand-by mode to prevent any accidental CAN protocol violation through programming errors.

PAGE SELECTION REGISTER (PSR)

Address: 005Fh - Read/Write

Reset Value: 00h

7							0
0	0	0	0	0	PAGE2	PAGE1	PAGE0

PAGE[2:0] determine which buffer or filter page is mapped at addresses 0060h to 006Fh.

PAGE2	PAGE1	PAGE0	Page Title
0	0	0	Diagnosis
0	0	1	Buffer 1
0	1	0	Buffer 2
0	1	1	Buffer 3
1	0	0	Filters
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

CONTROLLER AREA NETWORK (Cont'd)

5.6.4.2 Paged Registers

LAST IDENTIFIER HIGH REGISTER (LIDHR)

Read/Write

Reset Value: Undefined

7							0
LID10	LID9	LID8	LID7	LID6	LID5	LID4	LID3

LID[10:3] are the most significant 8 bits of the last Identifier read on the CAN bus.

LAST IDENTIFIER LOW REGISTER (LIDLR)

Read/Write

Reset Value: Undefined

7							0
LID2	LID1	LID0	LRTR	LDLC3	LDLC2	LDLC1	LDLC0

LID[2:0] are the least significant 3 bits of the last Identifier read on the CAN bus.

LRTR is the last Remote Transmission Request bit read on the CAN bus.

LDLC[3:0] is the last Data Length Code read on the CAN bus.

TRANSMIT ERROR COUNTER REG. (TECR)

Read Only

Reset Value: 00h

7							0
TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0

TEC[7:0] is the least significant byte of the 9-bit Transmit Error Counter implementing part of the fault confinement mechanism of the CAN protocol. In case of an error during transmission, this counter is incremented by 8. It is decremented by 1 after every successful transmission. When the counter value exceeds 127, the CAN controller enters the error passive state. When a value of 256 is reached, the CAN controller is disconnected from the bus.

RECEIVE ERROR COUNTER REG. (RECR)

Page: 00h — Read Only

Reset Value: 00h

7							0
REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0

REC[7:0] is the Receive Error Counter implementing part of the fault confinement mechanism of the CAN protocol. In case of an error during reception, this counter is incremented by 1 or by 8 depending on the error condition as defined by the CAN standard. After every successful reception the counter is decremented by 1 or reset to 120 if its value was higher than 128. When the counter value exceeds 127, the CAN controller enters the error passive state.

IDENTIFIER HIGH REGISTERS (IDHRx)

Read/Write

Reset Value: Undefined

7							0
ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3

ID[10:3] are the most significant 8 bits of the 11-bit message identifier.The identifier acts as the message's name, used for bus access arbitration and acceptance filtering.

CONTROLLER AREA NETWORK (Cont'd)

IDENTIFIER LOW REGISTERS (IDLRx)

Read/Write

Reset Value: Undefined

7							0
ID2	ID1	ID0	RTR	DLC3	DLC2	DLC1	DLC0

ID[2:0] are the least significant 3 bits of the 11-bit message identifier.

RTR is the Remote Transmission Request bit. It is set to indicate a remote frame and reset to indicate a data frame.

DLC[3:0] is the Data Length Code. It gives the number of bytes in the data field of the message.The valid range is 0 to 8.

DATA REGISTERS (DATA0-7x)

Read/Write

Reset Value: Undefined

7							0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

DATA[7:0] is a message data byte. Up to eight such bytes may be part of a message. Writing to byte DATA7 initiates a transmit request and should always be done even when DATA7 is not part of the message.

BUFFER CONTROL/STATUS REGs. (BCSRx)

Read/Write

Reset Value: 00h

7							0
0	0	0	0	ACC	RDY	BUSY	LOCK

Bit 3 = **ACC** *Acceptance Code*
— Read Only
Set by hardware with the id of the highest priority filter which accepted the message stored in the buffer.
ACC = 0: Match for Filter/Mask0. Possible match for Filter/Mask1.
ACC = 1: No match for Filter/Mask0 and match for Filter/Mask1.

Reset by hardware when either RDY or RXIF gets reset.

Bit 2 = **RDY** *Message Ready*
— Read/Clear
Set by hardware to signal that a new error-free message is available (LOCK = 0) or that a transmission request is pending (LOCK = 1).
Cleared by software when LOCK = 0 to release the buffer and to clear the corresponding RXIF bit in the Interrupt Status Register.
Cleared by hardware when LOCK = 1 to indicate that the transmission request has been serviced or cancelled.

Bit 1 = **BUSY** *Busy Buffer*
— Read Only
Set by hardware when the buffer is being filled (LOCK = 0) or emptied (LOCK = 1).
Reset by hardware when the buffer is not accessed by the CAN core for transmission nor reception purposes.

Bit 0 = **LOCK** *Lock Buffer*
— Read/Set/Clear
Set by software to lock a buffer. No more message can be received into the buffer thus preserving its content and making it available for transmission.
Cleared by software to make the buffer available for reception. Cancels any pending transmission request.
Cleared by hardware once a message has been successfully transmitted provided the early transmit interrupt mode is on. Left untouched otherwise.

Note that in order to prevent any message corruption or loss of context, LOCK cannot be set nor reset while BUSY is set. Trying to do so will result in LOCK not changing state.

CONTROLLER AREA NETWORK (Cont'd)

FILTER HIGH REGISTERS (FHRx)

Read/Write

Reset Value: Undefined

7							0
FIL11	FIL10	FIL9	FIL8	FIL7	FIL6	FIL5	FIL4

FIL[11:3] are the most significant 8 bits of a 12-bit message filter. The acceptance filter is compared bit by bit with the identifier and the RTR bit of the incoming message. If there is a match for the set of bits specified by the acceptance mask then the message is stored in a receive buffer.

FILTER LOW REGISTERS (FLRx)

Read/Write

Reset Value: Undefined

7							0
FIL3	FIL2	FIL1	FIL0	0	0	0	0

FIL[3:0] are the least significant 4 bits of a 12-bit message filter.

MASK HIGH REGISTERS (MHRx)

Read/Write

Reset Value: Undefined

7							0
MSK11	MSK10	MSK9	MSK8	MSK7	MSK6	MSK5	MSK4

MSK[11:3] are the most significant 8 bits of a 12-bit message mask. The acceptance mask defines which bits of the acceptance filter should match the identifier and the RTR bit of the incoming message.
MSK_i = 0: don't care.
MSK_i = 1: match required.

MASK LOW REGISTERS (MLRx)

Read/Write

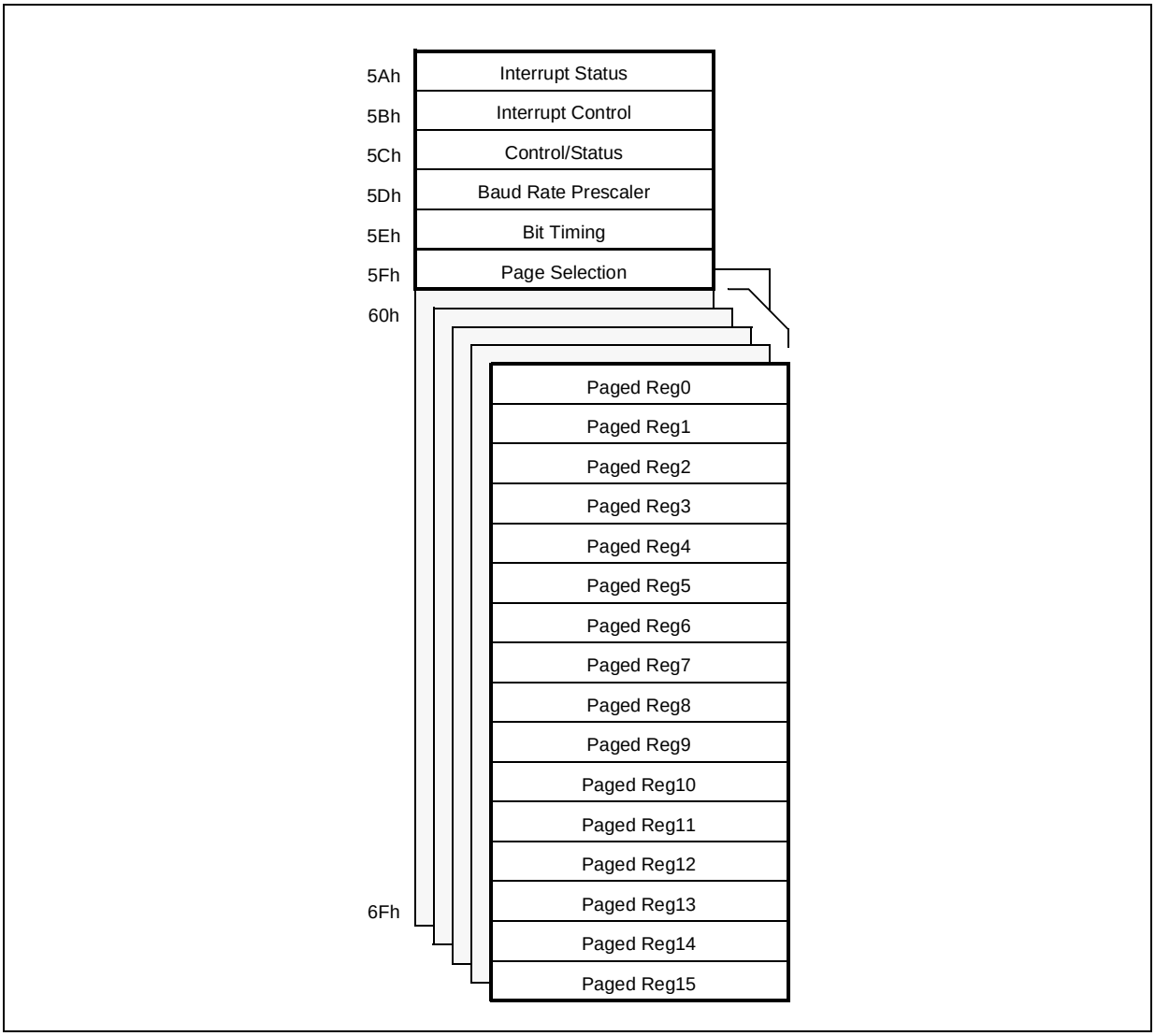
Reset Value: Undefined

7							0
MSK3	MSK2	MSK1	MSK0	0	0	0	0

MSK[3:0] are the least significant 4 bits of a 12-bit message mask.

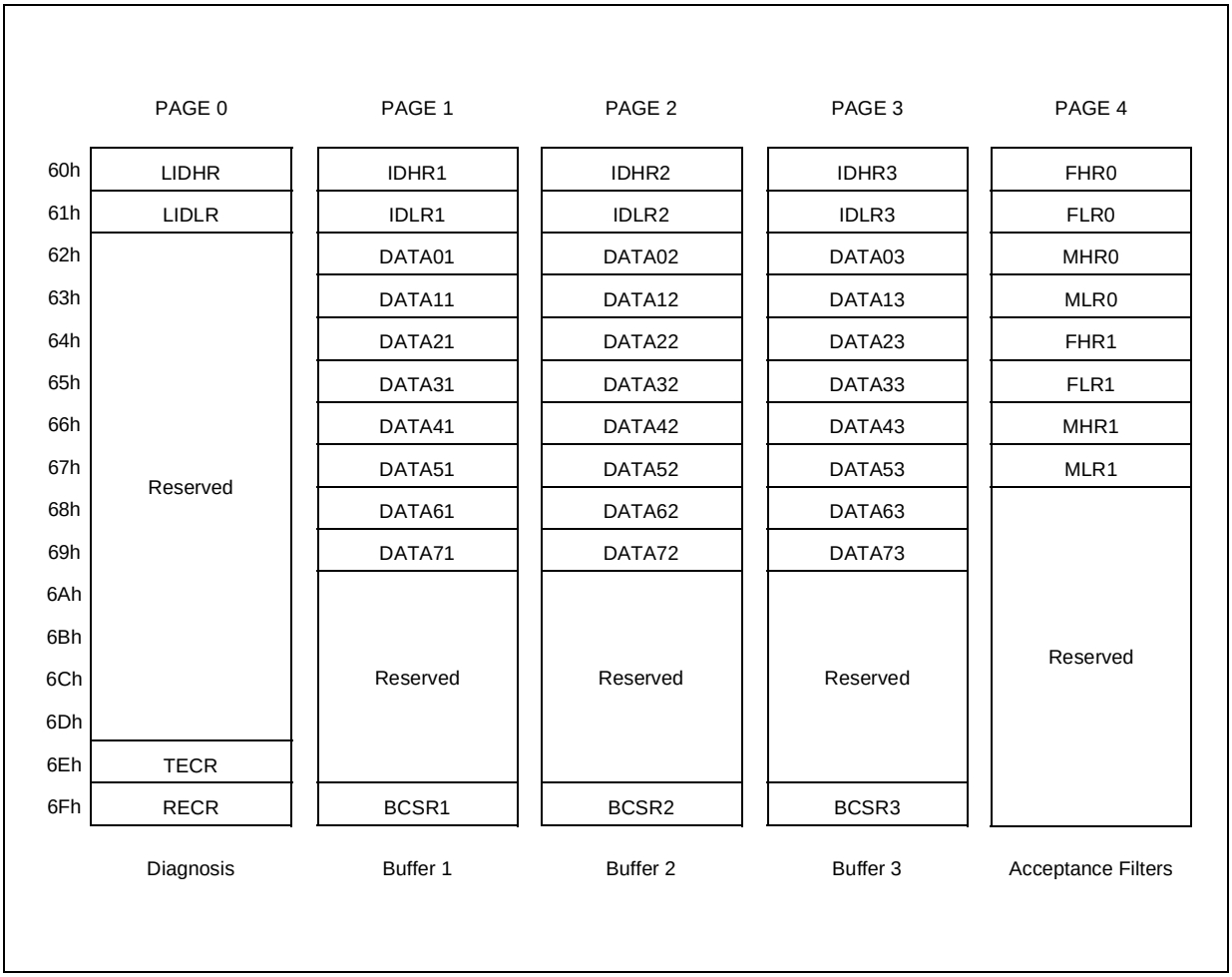
CONTROLLER AREA NETWORK (Cont'd)

Figure 38. CAN Register Map



CONTROLLER AREA NETWORK (Cont'd)

Figure 39. Page Maps



CONTROLLER AREA NETWORK (Cont'd)

Table 11. CAN Register Map and Reset Values

Address (Hex.)	Page	Register Name	7	6	5	4	3	2	1	0
5Ah		**ISR**	RXIF3	RXIF2	RXIF1	TXIF	SCIF	ORIF	TEIF	EPND
		Reset Value	0	0	0	0	0	0	0	0
5Bh		**ICR**	0	ESCI	RXIE	TXIE	SCIE	ORIE	TEIE	ETX
		Reset Value	0	0	0	0	0	0	0	0
5Ch		**CSR**	0	BOFF	EPSV	SRTE	NRTX	FSYN	WKPS	RUN
		Reset Value	0	0	0	0	0	0	0	0
5Dh		**BRPR**	RJW1	RJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		Reset Value	0	0	0	0	0	0	0	0
5Eh		**BTR**	0	BS22	BS21	BS20	BS13	BS12	BS11	BS10
		Reset Value	0	0	1	0	0	0	1	1
5Fh		**PSR**	0	0	0	0	0	PAGE2	PAGE1	PAGE0
		Reset Value	0	0	0	0	0	0	0	0
60h	00h	**LIDHR**	LID10	LID9	LID8	LID7	LID6	LID5	LID4	LID3
		Reset Value	x	x	x	x	x	x	x	x
	01h-03h	**IDHRx**	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
		Reset Value	x	x	x	x	x	x	x	x
60h/64h	04h	**FHRx**	FIL11	FIL10	FIL9	FIL8	FIL7	FIL6	FIL5	FIL4
		Reset Value	x	x	x	x	x	x	x	x
61h	00h	**LIDLR**	LID2	LID1	LID0	LRTR	LDLC3	LDLC2	LDLC1	LDLC0
		Reset Value	x	x	x	x	x	x	x	x
	01h-03h	**IDLRx**	ID2	ID1	ID0	RTR	DLC3	DLC2	DLC1	DLC0
		Reset Value	x	x	x	x	x	x	x	x
61h/65h	04h	**FLRx**	FIL3	FIL2	FIL1	FIL0	0	0	0	0
		Reset Value	x	x	x	x	0	0	0	0
62h-69h	01h-03h	**DATA0-7x**	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
		Reset Value	x	x	x	x	x	x	x	x
62h/66h	04h	**MHRx**	MSK11	MSK10	MSK9	MSK8	MSK7	MSK6	MSK5	MSK4
		Reset Value	x	x	x	x	x	x	x	x
63h/67h	04h	**MLRx**	MSK3	MSK2	MSK1	MSK0	0	0	0	0
		Reset Value	x	x	x	x	0	0	0	0
6Eh	00h	**TECR**	TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0
		Reset Value	0	0	0	0	0	0	0	0
6Fh	00h	**RECR**	REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0
		Reset Value	0	0	0	0	0	0	0	0
	01h-03h	**BCSRx**	0	0	0	0	ACC	RDY	BUSY	LOCK
		Reset Value	0	0	0	0	0	0	0	0

5.7 CAN BUS TRANSCEIVER

5.7.1 Introduction

The CAN bus transceiver allows the connection of the microcontroller, with CAN controller unit, to a CAN bus. The transmitter section drives the CAN bus while the receiver section senses the data on the bus.

The CAN transceiver meets ISO/DIS 11898 up to 1 MBaud.

5.7.2 Main Features

TRANSMITTER:

– Generation of differential Output signals

– Short Circuit protection from transients in automotive environment

– Slope control to reduce RFI and EMI

– High speed (up to 1Mbaud)

– If un-powered, L9805 CAN node does not disturb the bus lines (the transceiver is in recessive state).

RECEIVER:

– Differential input with high interference suppression

– Common mode input voltage range (V_{COM}) from -5 to 12V

5.7.3 Functional Description

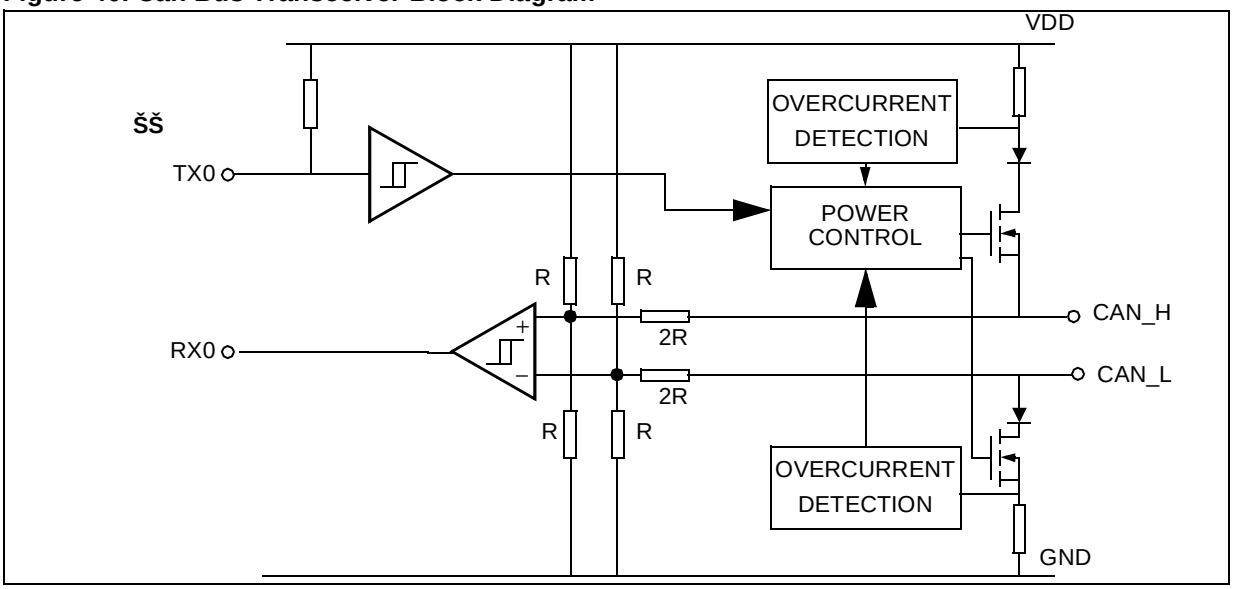
The Can Bus Transceiver is used as an interface between a CAN controller and the physical bus. The device provides transmitting capability to the CAN controller. The transceiver has one logic input pin (TX), one logic output pin (RX) and two Input/Output pins for the electrical connections to the two bus wires (CAN_L and CAN_H). The microcontroller sends data to the TX pin and it receives data from the RX pin. The transmission slew-rates of CAN_H and CAN_L voltage are controlled to reduce RFI and EMI. The transceiver is protected against short circuit or overcurrent: If I_{CANH} and/or I_{CANL} exceeds a current thresholds I_{SC}, then the CAN_H and CAN_L power transistors are switched off and the transmission is disabled for T_D=25µs typical.

5.7.4 CAN Transceiver Disabling function

The transceiver can be disabled and forced to move in a low power consumption mode, setting CANDS bit in DCSR register (see Section 3.2.1). When the transceiver is in this mode it can not receive nor transmit any information to the bus. The only way to have again on board the CAN capabilities is reset CANDS bit. The CAN protocol handler can not disable nor enable the transceiver and there is no way to communicate to the controller the transceiver is down. The disabling function has the only purpose to allow the reduction of the current consumption of the device in application not using the CAN at all or using it for particular functions (such like debugging). Current consumption reduction, when disabling the trasceiver, can be as high as 15mA.

Note When the CAN capabilities of L9805 are not needed additional consumption reduction can be achieved putting the CAN controller in Stand-by Mode (see Section 5.6.3.3).

Figure 40. Can Bus Transceiver Block Diagram



5.8 POWER BRIDGE

5.8.1 Introduction

The power part of the device consists of two identical independent DMOS half bridges. It is suited to drive resistive and inductive loads.

5.8.2 Main Features

The Rdson of each of the 4 DMOS transistors is 60 mΩ at 25°C.

The nominal current is 2A.

The maximum current is 5A.

The low-side switch is a n-channel DMOS transistor while the high-side switch is a p-channel DMOS transistor. Therefore no charge pump is needed.

An anti-crossconduction circuit is included: the low side DMOS is switched on only when the high side is switched off and vice versa. This function avoid the two DMOS are switched on together firing the high current path from battery to ground. The function is obtained by sensing the gate voltage and therefore the delay between command and effective switch on of the DMOS doesn't have a fixed length.

The MCU controls all operations of the power stage through the BCSR dedicated register. Short circuit and overtemperature conditions are reported to the CPU using dedicated error flags.

Overtemperature and short circuit conditions switch off the bridge immediately without CPU intervention. The function of the flags is independent of the operation mode of the bridge (sink, source, Z).

In addition both the PWM modules can be directly connected to the power bridge. The power bridge offers then many driving mode alternatives:

Direct Mode: the two half bridges are directly driven by IN1 and IN2 control bit in BCSR.

PWM1 Up/Down Brake Mode: the output of PWM1 drives one side of the bridge while the other side is maintained in a fixed status.

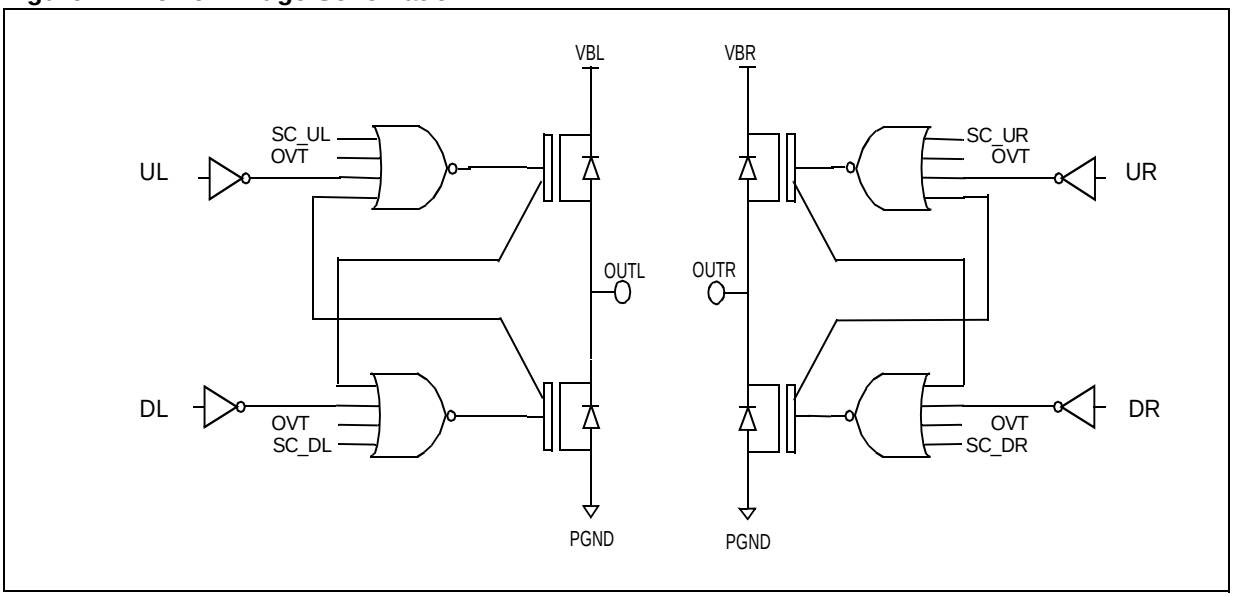
PWM1 Symmetrical Driving Mode: PWM1 line drives directly and symmetrically both side of the bridge.

PWM1/PWM2 Mode: PWM1 drives one side while PWM2 drives the other (two independent half bridges).

5.8.3 Functional Description

A schematic description of the Power Bridge circuit is depicted in Figure 41. In this schematic the transistors must be considered in ON condition when they gate is high (set).

Figure 41. Power Bridge Schematic



EN bit in BCSR is the main enable signal, active high. If EN = 0, all the bridge transistors are switched off (UL, UR, DL and DR are reset) and the outputs OUTL and OUTR are in high impedance state.

Being '0' the status after reset of EN, the bridge is in safe condition (OUTL=OUTR=Z). Therefore the

safe condition is guaranteed in undervoltage condition (LVD reset) and in case of main clock (Safeguard reset) or software (Watchdog reset) failures.

Each power DMOS has its own over current detector circuit generating SC_xx signals (see Figure 41). SC_xx signals are ORed together to generate SC flag in BCSR register.

SC flag is then set by hardware as soon as one of the two outputs (or both) are short to battery, ground or if the two outputs are short together (load short). This read only bit is reset only by clearing the EN bit. The rising edge of SC causes an interrupt request if the PIE bit is set in BCSR register.

When the current monitored in any of the four DMOS of the bridge exceeds limit threshold (I_{SC}), the SC bit is set and the corresponding DMOS is switched off after t_{SCPI} time. This function is dominant over any write from data bus by software (i. e. as long as SC is set, the bridge cannot be switched on).

To switch the bridge on again the EN bit must be cleared by software. This resets the SC bit. Setting again EN, the bridge is switched on. If the overcurrent condition is still present, SC is set again (and a interrupt is generated when enabled).

An internal thermal protection circuit monitors continuously the temperature of the device and drives the OVT bit in BCSR register and, in turn, the OVT signal in Figure 41.

The OVT flag is set as soon as the temperature of the chip exceeds Thw and all the transistor of the bridge are switched off. This rising edge causes an interrupt request if the PIE bit is set. This read only bit is reset only by clearing the EN bit. This function is dominant over any write from data bus by software (i. e. as long as OVT is set the bridge cannot be switched on).

To switch the bridge on again the EN bit must be cleared by software. This resets the OVT bit. Setting again EN, the bridge is switched on. If the overtemperature condition is still present, OVT is set again (and a interrupt is generated when enabled).

5.8.4 Interrupt generation

Interrupt generation is controlled by PDIE bit in BCSR register. When this bit is set Overtemperature and Short-circuit conditions generate an interrupt as described in Section 5.8.3.

Setting PDIE when SC and/or OVT flag are set, immediately generates an interrupt request.

The interrupt request of the power bridge is cleared when the EN bit is cleared by software.

5.8.5 Operating Modes

The status of the OUTL and OUTR power outputs is controlled by IN1, IN2, EN, PWM_EN and DIR bit in BCSR register, plus the PWM1 and PWM2 line, according to the Functional Description Table (Table 12).

Note The functional description table (Table 12) uses symbols UL,R (Up Left or Right) and DR,L (Down Left or Right) to indicate the driving signal of the four DMOS. Conventionally a transistor is in the on status when its driving signal is set (‘1’) while it is in off status when the driving signal is reset (‘0’).

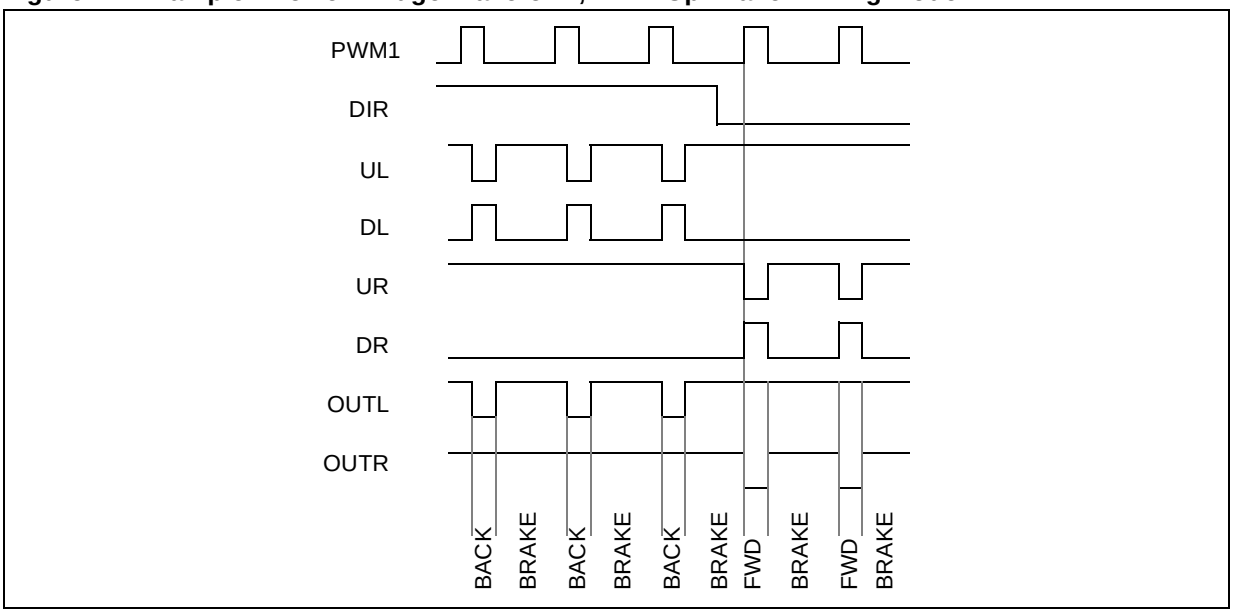
Table 12. Functional Description Table

Drive	EN	PWM_EN	DIR	PWM1	IN1	IN2	UL	DL	UR	DR		Operation	Configuration
	0	X	X	X	X	X	0	0	0	0		INHIBIT	
Direct Mode	1	0	X	X	0	0	0	1	0	1		BRAKE	Full or Two Half Bridges
	1	0	X	X	0	1	0	1	1	0		BACK	Full or Two Half Bridges
	1	0	X	X	1	0	1	0	0	1		FORWARD	Full or Two Half Bridges
	1	0	X	X	1	1	1	0	1	0		BRAKE	Full or Two Half Bridges
PWM1 Up Brake Mode	1	1	0	0	0	0	1	0	1	0		BRAKE	Full Bridge
	1	1	0	1	0	0	1	0	0	1		FORWARD	Full Bridge
	1	1	1	0	0	0	1	0	1	0		BRAKE	Full Bridge
	1	1	1	1	0	0	0	1	1	0		BACK	Full Bridge

Drive	EN	PWM_EN	DIR	PWM1	IN1	IN2	UL	DL	UR	DR		Operation	Configuration
PWM1 Down Brake Mode	1	1	0	0	0	1	0	1	0	1		BRAKE	Full Bridge
	1	1	0	1	0	1	1	0	0	1		FORWARD	Full Bridge
	1	1	1	0	0	1	0	1	0	1		BRAKE	Full Bridge
	1	1	1	1	0	1	0	1	1	0		BACK	Full Bridge
PWM1 Symmetrical Driving Mode	1	1	0	0	1	0	0	1	1	0		BACK	Full Bridge
	1	1	0	1	1	0	1	0	0	1		FORWARD	Full Bridge
	1	1	1	0	1	0	1	0	0	1		FORWARD	Full Bridge
	1	1	1	1	1	0	0	1	1	0		BACK	Full Bridge
PWM1/PWM2 Mode	1	1	0		1	1	pwm1	$\overline{\text{pwm1}}$	pwm2	$\overline{\text{pwm2}}$		PWM1 ->left PWM2->right	Two Half Bridges
	1	1	1		1	1	$\overline{\text{pwm1}}$	pwm1	$\overline{\text{pwm2}}$	pwm2		$\overline{\text{PWM1}}$ ->left $\overline{\text{PWM2}}$->right	Two Half Bridges

Note The DIR signal is internally synchronized with the PWM1 and PWM2 signals according to the selected Driving Mode. After writing the DIR bit in BCSR register, the direction changes in correspondence with the first rising edge of PWM1. The same procedure is used in the case of PWM2. This allows the proper control of the direction changes. When the PWM signal is 0% or 100%, being no edges available, the DIR bit can't be latched and the direction does not change until a PWM edge occurs.

Figure 42. Example - Power Bridge Waveform, PWM Up Brake Driving Mode



5.8.6 Register Description

The power section is controlled by the microcontroller through the following register:

POWER BRIDGE CONTROL STATUS REGISTER (PBCSR)

Address: 0021h - Read/Write

Reset Value: 00000000

7							0
PIE	OVT	SC	DIR	IN2	IN1	PWM_ EN	EN

Bit 0 **= EN:** Power Bridge enable. When reset the bridge is disabled and OUTL and OUTR are in high impedance condition.

Bit 1**= PWM_EN**: PWM driving enable. When reset the bridge is driven directly by IN1 and IN2 bit (Direct Mode). When set the driving is made by PWM1 and/or PWM2 bit according to the Operation Mode selected by IN1 and IN2 bit.

Bit 2**= IN1**: Left Half Bridge control bit if PWM_EN=0, driving mode selection bit if PWM_EN=1.

Bit 3**= IN2**: Right Half Bridge control bit if PWM_EN=0, driving mode selection bit if PWM_EN=1.

The following table summarizes the driving mode selection made by PWM_EN, IN1 and IN2 bit

PWM_EN	IN1	IN2	Driving Mode
0	X	X	Direct
1	0	0	PWM1 Up Braking
1	0	1	PWM1 Down Braking
1	1	0	PWM1 Symmetrical
1	1	1	PWM1/PWM2

Bit 4**= DIR**: Direction bit. This bit is meaningless when PWM_EN=0. When PWM_EN is set the DIR bit controls the “driving direction” of the bridge. In order to implement a precise control of the direction changes, DIR value is latched by the rising edge of the pwm signal driving the bridge. When the signal does not have edges (i.e. pwm = 0% or 100%) the DIR bit can not be latched and the driving direction does not change even changing DIR bit in BCSR.

Bit 5**= SC**: Short Circuit flag (read only)

Bit 6**= OVT**: Overtemperature flag (read only)

Bit 7**= PIE**: Power section interrupt enable.

5.9 EEPROM (EEP)

5.9.1 Introduction

The Electrically Erasable Programmable Read Only Memory is used to store data that need a non volatile back-up. The use of the EEPROM requires a basic protocol described in this chapter.

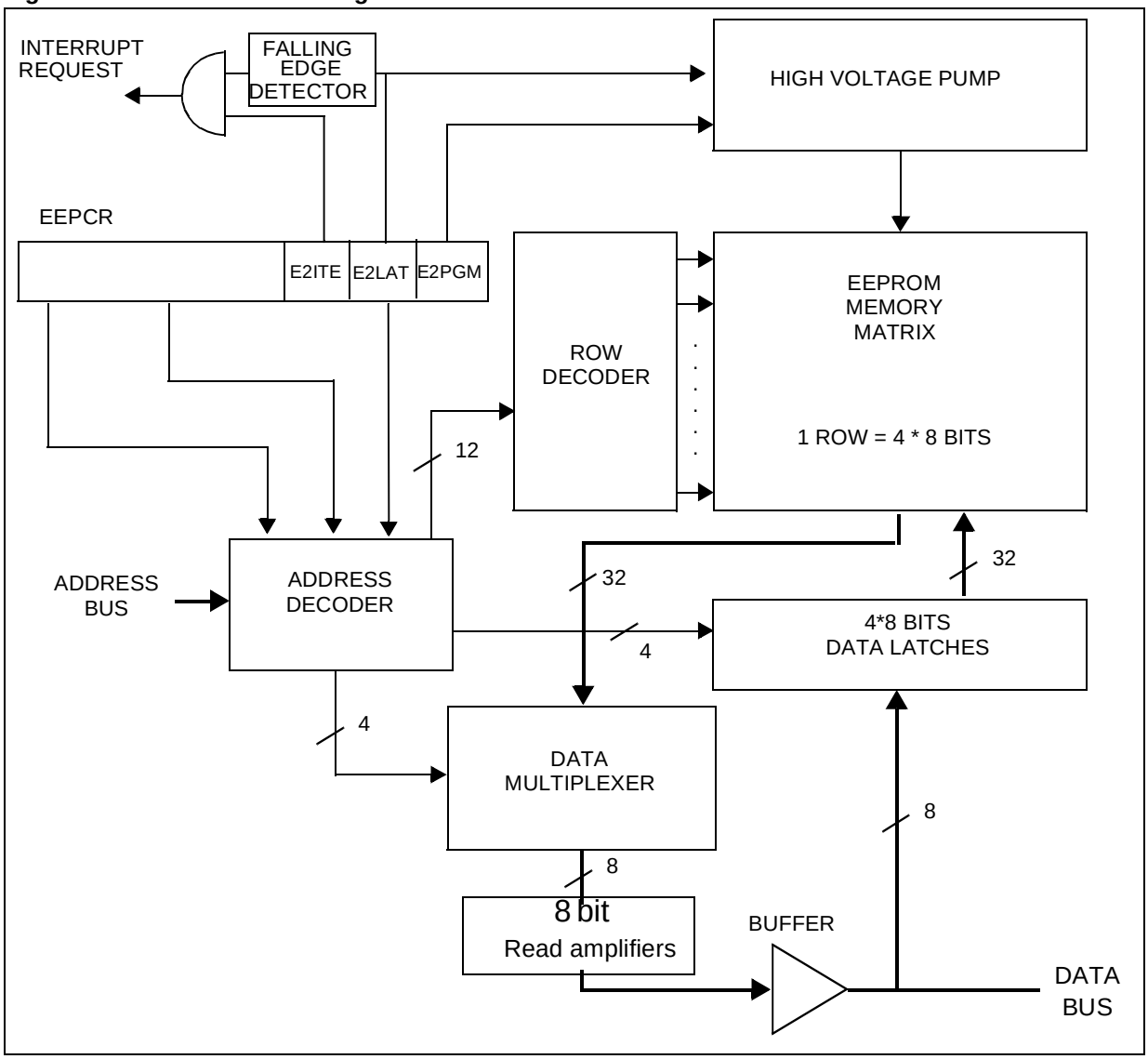
Software or hardware reset and halt modes are managed immediately, stopping the action in progress. Wait mode does not affect the programming of the EEPROM.

The Read operation of this memory is the same of a Read-Only-Memory or RAM. The erase and programming cycles are controlled by an EEPROM control register.

The user can program 1 to 4 bytes at the same programming cycle providing that the high part of the address is the same for the bytes to be written (only address bits A1 and A0 can change).

The EEPROM is mono-voltage. A charge pump generates the high voltage internally to enable the erase and programming cycles. The erase and programming cycles are chained automatically. The global programming cycle duration is controlled by an internal circuit.

Figure 43. EEPROM Block Diagram



5.9.2 Functional description

5.9.2.1 Read operation (E2LAT=0)

The EEPROM can be read as a normal ROM/RAM location when the E2LAT bit of the CR register is cleared. The address decoder selects the desired byte. The 8 sense amplifiers evaluate the stored byte which is put on the data bus.

5.9.2.2 Write operation (E2LAT=1)

The EEPROM programming flowchart is shown in Figure 45.

To access the write mode, E2LAT bit must be set. Then when a write access to the EEPROM occurs, the value on the data bus is latched on the 8 data latches depending on the address. To program the memory, the E2PGM bit must be set, so the programming cycle starts. At the end of the cycle, the E2PGM bit and E2LAT bit are cleared, and an interrupt could be generated id E2ITE is set.

5.9.2.3 Wait mode

The EEPROM can enter the wait mode by executing the wait instruction of the micro-controller. The EEPROM will effectively enter this mode if there is no programming in progress, in such a case the EEPROM will finish the cycle and then enter this low consumption mode.

5.9.2.4 Halt mode

The EEPROM enters the halt mode if the micro-controller did execute the halt instruction. The EEPROM will stop the function in progress, and will enter in this low consumption mode.

Figure 44. EEPROM Programming Cycle

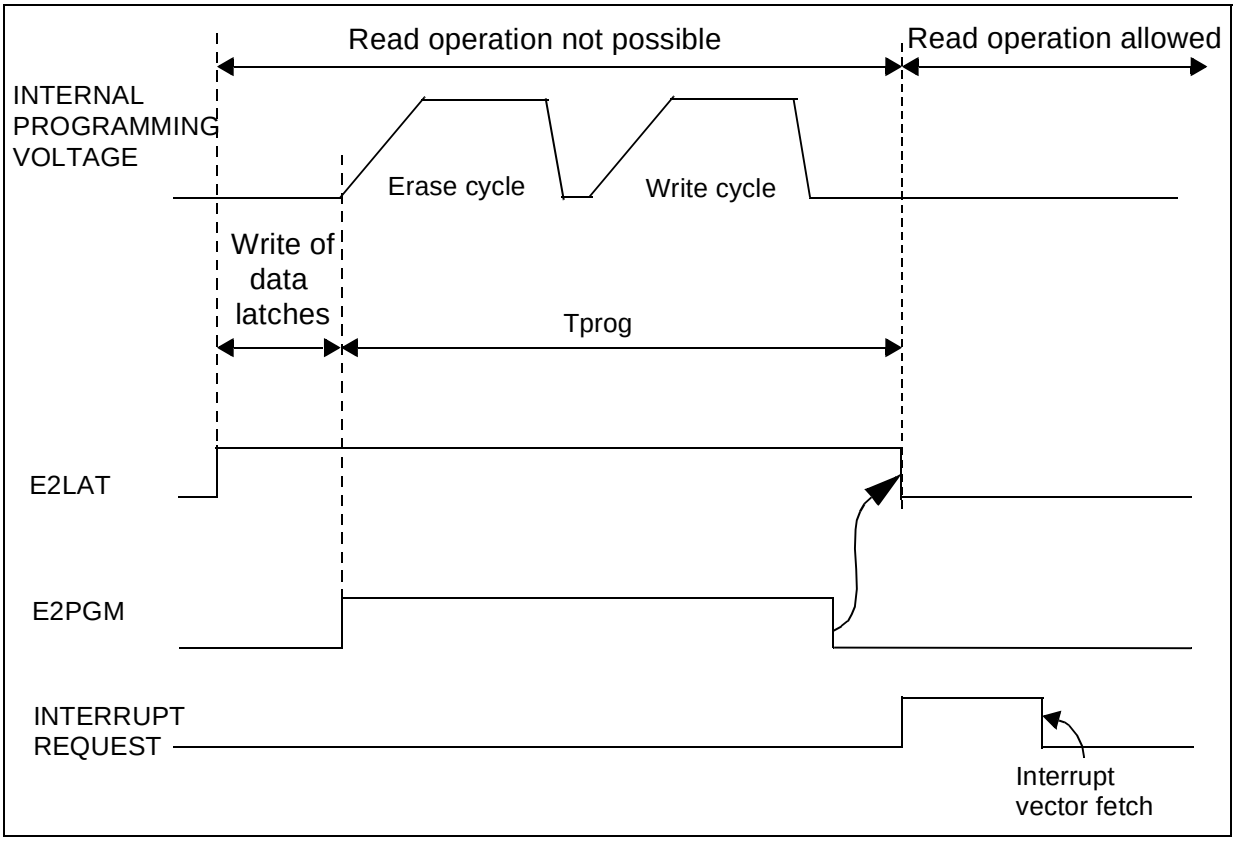
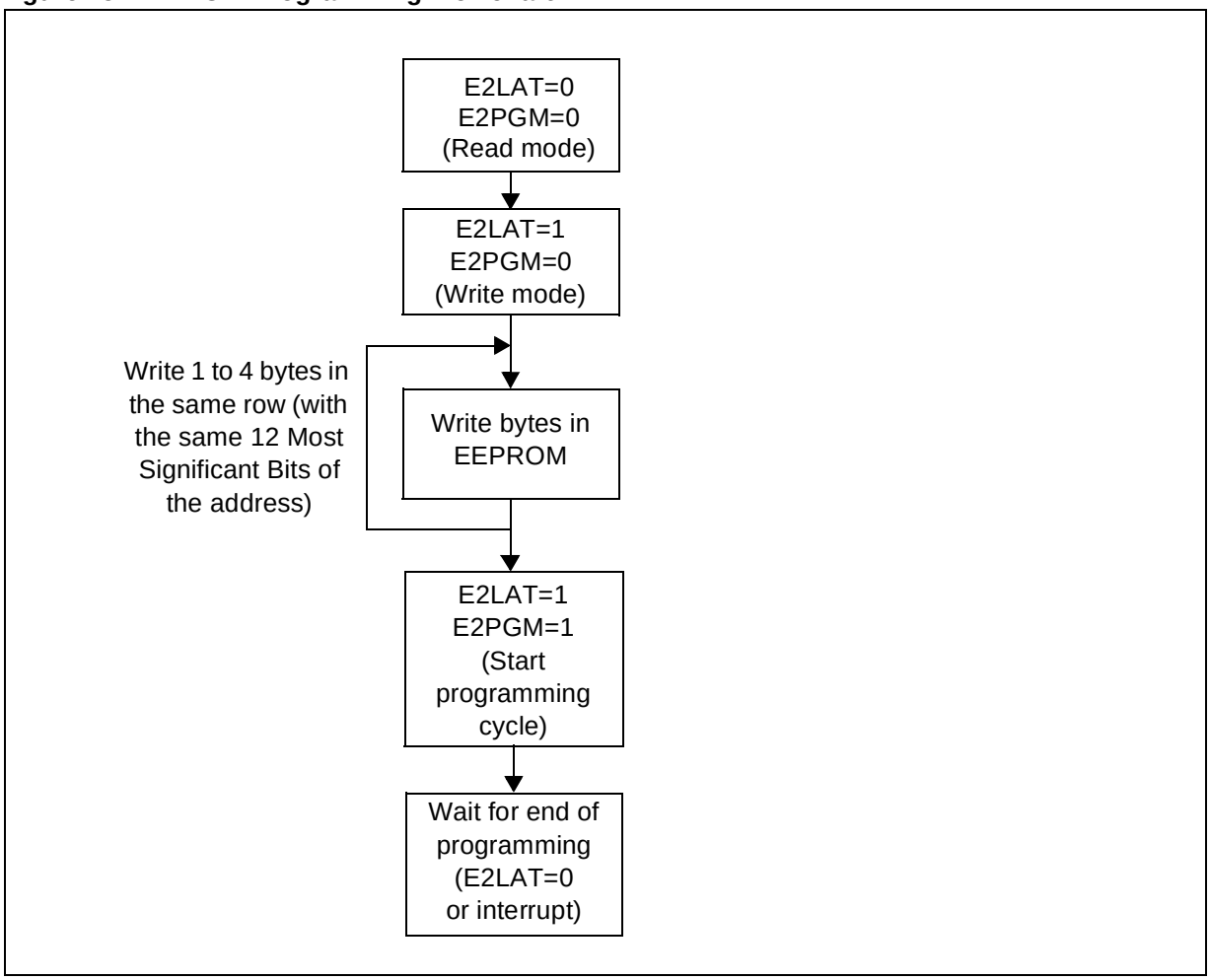


Figure 45. EEPROM Programming Flowchart



5.9.3 Register Description

EEPROM CONTROL REGISTER (EECR)

Address: 002Ch - Read/Write
Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	0	E2ITE	E2LAT	E2PGM

Bit 7:3 = Reserved, forced by hardware to 0.

Bit 2 = **E2ITE**: *Interrupt enable.*
This bit is set and cleared by software.
0: Interrupt disabled
1: Interrupt enabled

When the programming cycle is finished (E2PGM toggle from 1 to 0), an interrupt is generated only if E2ITE is high. The interrupt is automatically cleared when the micro-controller enters the EEPROM interrupt routine.

Bit 1 = **E2LAT**: *Read/Write mode.*
This bit is set by software. It is cleared by hardware at the end of the programming cycle. It can be cleared by software only if E2PGM=0.
0: Read mode
1: Write mode

When E2LAT=1, if the E2PGM bit is low and the micro-controller is in write mode, the 8 bit data bus is stored in one of the four groups of 8 bit data latches, selected by the address. This happens every time the device executes an EEPROM Write instruction. If E2PGM remains low, the content of the 8 bit data latches is not transferred into the matrix, because the High Voltage charge-pump does not start. The 8 data latches are selected by the lower part of the address (A<1:0> bits). If 4 consecutive write instructions are executed, by sweeping from A<1:0>=0h to A<1:0>=3h, with the

same higher part of the address, all the 4 groups of data latches will be written, and they will be ready to write a whole row of the EEPROM matrix, as soon as E2PGM goes high and the charge-pump starts. If only one write instruction is executed before E2PGM goes high, only one group of data latches will be selected and only one byte of the matrix will be written. At the end of the programming cycle, E2LAT bit is automatically cleared, and the data latches are cleared.

Bit 0 = **E2PGM**: *Programming Control.*
This bit is set by software to begin the programming cycle. At the end of the programming cycle, this bit is cleared by hardware and an interrupt is generated if the E2ITE bit is set.
0: Programming finished or not started
1: Programming cycle is in progress

Note: if the E2PGM bit is cleared during the programming cycle, the memory data is not guaranteed.

Note: Care should be taken during the programming cycle. Writing to the same memory location will over-program the memory (logical AND between the two write access data result) because the data latches are only cleared at the end of the programming cycle and by the falling edge of E2LAT bit.
It is not possible to read the latched data.

Special management of wrong EEPROM access:

If a read happens while E2LAT=1, then the data bus will not be driven.

If a write access happens while E2LAT=0, then the data on the bus will not be latched.

The data latches are cleared when the user sets E2LAT bit.

6 INSTRUCTION SET

6.1 ST7 ADDRESSING MODES

The ST7 Core features 17 different addressing modes which can be classified in 7 main groups:

Addressing Mode	Example
Inherent	nop
Immediate	ld A,#$55
Direct	ld A,$55
Indexed	ld A,($55,X)
Indirect	ld A,([$55],X)
Relative	jrne loop
Bit operation	bset byte,#5

The ST7 Instruction set is designed to minimize the number of bytes required per instruction: To do so, most of the addressing modes may be subdivided in two sub-modes called long and short:

– Long addressing mode is more powerful because it can use the full 64Kbyte address space, however it uses more bytes and more CPU cycles.

– Short addressing mode is less powerful because it can generally only access page zero (0000 - 00FFh range), but the instruction size is more compact, and faster. All memory to memory instructions use short addressing modes only (CLR, CPL, NEG, BSET, BRES, BTJT, BTJF, INC, DEC, RLC, RRC, SLL, SRL, SRA, SWAP)

The ST7 Assembler optimize the use of long and short addressing modes.

Table 13. ST7 Addressing Mode Overview:

Mode			Syntax	Destination	Pointer Address (Hex.)	Pointer Size (Hex.)	Length (Bytes)
Inherent			nop				+ 0
Immediate			ld A,#$55				+ 1
Short	Direct		ld A,$10	00..FF			+ 1
Long	Direct		ld A,$1000	0000..FFFF			+ 2
No Offset	Direct	Indexed	ld A,(X)	00..FF			+ 0
Short	Direct	Indexed	ld A,($10,X)	00..1FE			+ 1
Long	Direct	Indexed	ld A,($1000,X)	0000..FFFF			+ 2
Short	Indirect		ld A,[$10]	00..FF	00..FF	byte	+ 2
Long	Indirect		ld A,[$10.w]	0000..FFFF	00..FF	word	+ 2
Short	Indirect	Indexed	ld A,([$10],X)	00..1FE	00..FF	byte	+ 2
Long	Indirect	Indexed	ld A,([$10.w],X)	0000..FFFF	00..FF	word	+ 2
Relative	Direct		jrne loop	PC+/-127			+ 1
Relative	Indirect		jrne [$10]	PC+/-127	00..FF	byte	+ 2
Bit	Direct		bset $10,#7	00..FF			+ 1
Bit	Indirect		bset [$10],#7	00..FF	00..FF	byte	+ 2
Bit	Direct	Relative	btjt $10,#7,skip	00..FF			+ 2
Bit	Indirect	Relative	btjt [$10],#7,skip	00..FF	00..FF	byte	+ 3

INSTRUCTION SET OVERVIEW (Cont'd)

Inherent:

All Inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Inherent Instruction	Function
NOP	No operation
TRAP	S/W Interrupt
WFI	Wait For Interrupt (Low Power Mode)
HALT	Halt Oscillator (Lowest Power Mode)
RET	Sub-routine Return
IRET	Interrupt Sub-routine Return
SIM	Set Interrupt Mask
RIM	Reset Interrupt Mask
SCF	Set Carry Flag
RCF	Reset Carry Flag
RSP	Reset Stack Pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
MUL	Byte Multiplication
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles

Immediate:

Immediate instructions have two bytes, the first byte contains the opcode, the second byte contains the operand value..

Immediate Instruction	Function
LD	Load
CP	Compare
BCP	Bit Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Operations

Direct (Short, Long):

In Direct instructions, the operands are referenced by their memory address, which follows the opcode.

Available Long and Short Direct Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substructions operations
BCP	Bit Compare

Short Direct Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The direct addressing mode consists of two submodes:

Direct (short):

The address is a byte, thus requires only one byte after the opcode, but only allows 00 - FF addressing space.

Direct (long):

The address is a word, thus allowing 64Kb addressing space, but requires 2 bytes after the opcode.

INSTRUCTION SET OVERVIEW (Cont'd)

Indexed (No Offset, Short, Long)

In this mode, the operand is referenced by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset which follows the opcode.

No Offset, Long and Short Indexed Instruction	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substructions operations
BCP	Bit Compare

No Offset and Short Indexed Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2's Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The indirect addressing mode consists of three sub-modes:

Indexed (No Offset)

There is no offset, (no extra byte after the opcode), and allows 00 - FF addressing space.

Indexed (Short)

The offset is a byte, thus requires only one byte after the opcode and allows 00 - 1FE addressing space.

Indexed (long):

The offset is a word, thus allowing 64Kb addressing space and requires 2 bytes after the opcode.

Indirect (Short, Long):

The required data byte to do the operation is found by its memory address, located in memory (pointer).

Available Long and Short Indirect Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substructions operations
BCP	Bit Compare

Short Indirect Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2's Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The pointer address follows the opcode. The indirect addressing mode consists of two sub-modes:

Indirect (short):

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - FF addressing space, and requires 1 byte after the opcode.

Indirect (long):

The pointer address is a byte, the pointer size is a word, thus allowing 64Kb addressing space, and

INSTRUCTION SET OVERVIEW (Cont'd)

Indirect Indexed (short, long):

This is a combination of indirect and short indexed addressing modes. The operand is referenced by its memory address, which is defined by the unsigned addition of an index register value (X or Y) with a pointer value located in memory. The pointer address follows the opcode.

Long and Short Indirect Indexed Instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Additions/Substructions operations
BCP	Bit Compare

Short Indirect Indexed Instructions Only	Function
CLR	Clear
INC, DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
BSET, BRES	Bit Operations
BTJT, BTJF	Bit Test and Jump Operations
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles
CALL, JP	Call or Jump subroutine

The indirect indexed addressing mode consists of two sub-modes:

Indirect Indexed (short):

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - 1FE addressing space, and requires 1 byte after the opcode.

Indirect Indexed (long):

The pointer address is a byte, the pointer size is a word, thus allowing 64Kb addressing space, and requires 1 byte after the opcode.

Relative mode (direct, indirect):

This addressing mode is used to modify the PC register value, by adding an 8 bit signed offset to it.

Available Relative Direct/Indirect Instructions	Function
JRxx	Conditional Jump
CALLR	Call Relative

The relative addressing mode consists of two sub-modes:

Relative (direct):

The offset is following the opcode.

Relative (indirect):

The offset is defined in memory, which address follows the opcode.

INSTRUCTION SET OVERVIEW (Cont'd)

6.2 INSTRUCTION GROUPS

The ST7 family devices use an Instruction Set consisting of 63 instructions. The instructions may be subdivided into 13 main groups as illustrated in the following table:

Load and Transfer	LD	CLR						
Stack operation	PUSH	POP	RSP					
Increment/Decrement	INC	DEC						
Compare and Tests	CP	TNZ	BCP					
Logical operations	AND	OR	XOR	CPL	NEG			
Bit Operation	BSET	BRES						
Conditional Bit Test and Branch	BTJT	BTJF						
Arithmetic operations	ADC	ADD	SUB	SBC	MUL			
Shift and Rotates	SLL	SRL	SRA	RLC	RRC	SWAP	SLA	
Unconditional Jump or Call	JRA	JRT	JRF	JP	CALL	CALLR	NOP	RET
Conditional Branch	JRxx							
Interruption management	TRAP	WFI	HALT	IRET				
Code Condition Flag modification	SIM	RIM	SCF	RCF				

Using a pre-byte

The instructions are described with one to four opcodes.

In order to extend the number of available opcodes for an 8-bit CPU (256 opcodes), three different probate pockets are defined. These prebytes modify the meaning of the instruction they precede.

The whole instruction becomes:

PC-2 End of previous instruction

PC-1 Prebyte

PC opcode

PC+1 Additional word (0 to 2) according to the number of bytes required to compute the effective address

These prebytes enable instruction in Y as well as indirect addressing modes to be implemented. They precede the opcode of the instruction in X or the instruction using direct addressing mode. The prebytes are:

PDY 90 Replace an X based instruction using immediate, direct, indexed, or inherent addressing mode by a Y one.

PIX 92 Replace an instruction using direct, direct bit, or direct relative addressing mode to an instruction using the corresponding indirect addressing mode.
It also changes an instruction using X indexed addressing mode to an instruction using indirect X indexed addressing mode.

PIY 91 Replace an instruction using X indirect indexed addressing mode by a Y one.

INSTRUCTION SET OVERVIEW (Cont'd)

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
ADC	Add with Carry	A = A + M + C	A	M	H		N	Z	C
ADD	Addition	A = A + M	A	M	H		N	Z	C
AND	Logical And	A = A . M	A	M			N	Z	
BCP	Bit compare A, Memory	tst (A . M)	A	M			N	Z	
BRES	Bit Reset	bres Byte, #3	M						
BSET	Bit Set	bset Byte, #3	M						
BTJF	Jump if bit is false (0)	btjf Byte, #3, Jmp1	M						C
BTJT	Jump if bit is true (1)	btjt Byte, #3, Jmp1	M						C
CALL	Call subroutine								
CALLR	Call subroutine relative								
CLR	Clear		reg, M				0	1	
CP	Arithmetic Compare	tst(Reg - M)	reg	M			N	Z	C
CPL	One Complement	A = FFH-A	reg, M				N	Z	1
DEC	Decrement	dec Y	reg, M				N	Z	
HALT	Halt					0			
IRET	Interrupt routine return	Pop CC, A, X, PC			H	I	N	Z	C
INC	Increment	inc X	reg, M				N	Z	
JP	Absolute Jump	jp [TBL.w]							
JRA	Jump relative always								
JRT	Jump relative								
JRF	Never jump	jrf *							
JRIH	Jump if Port A INT pin = 1	(no Port A Interrupts)							
JRIL	Jump if Port A INT pin = 0	(Port A interrupt)							
JRH	Jump if H = 1	H = 1 ?							
JRNH	Jump if H = 0	H = 0 ?							
JRM	Jump if I = 1	I = 1 ?							
JRNM	Jump if I = 0	I = 0 ?							
JRMI	Jump if N = 1 (minus)	N = 1 ?							
JRPL	Jump if N = 0 (plus)	N = 0 ?							
JREQ	Jump if Z = 1 (equal)	Z = 1 ?							
JRNE	Jump if Z = 0 (not equal)	Z = 0 ?							
JRC	Jump if C = 1	C = 1 ?							
JRNC	Jump if C = 0	C = 0 ?							
JRULT	Jump if C = 1	Unsigned <							
JRUGE	Jump if C = 0	Jmp if unsigned >=							
JRUGT	Jump if (C + Z = 0)	Unsigned >							

INSTRUCTION SET OVERVIEW (Cont'd)

JRULE	Jump if (C + Z = 1)	Unsigned <=							
LD	Load	dst <= src	reg, M	M, reg			N	Z	
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A	0				0
NEG	Negate (2's compl)	neg $10	reg, M				N	Z	C
NOP	No Operation								
OR	OR operation	A = A + M	A	M			N	Z	
POP	Pop from the Stack	pop reg pop CC	reg CC	M M	H	I	N	Z	C
PUSH	Push onto the Stack	push Y	M	reg, CC					
RCF	Reset carry flag	C = 0							0
RET	Subroutine Return								
RIM	Enable Interrupts	I = 0				0			
RLC	Rotate left true C	C <= A <= C	reg, M				N	Z	C
RRC	Rotate right true C	C => A => C	reg, M				N	Z	C
RSP	Reset Stack Pointer	S = Max allowed							
SBC	Substract with Carry	A = A - M - C	A	M			N	Z	C
SCF	Set carry flag	C = 1							1
SIM	Disable Interrupts	I = 1				1			
SLA	Shift left Arithmetic	C <= A <= 0	reg, M				N	Z	C
SLL	Shift left Logic	C <= A <= 0	reg, M				N	Z	C
SRL	Shift right Logic	0 => A => C	reg, M				0	Z	C
SRA	Shift right Arithmetic	A7 => A => C	reg, M				N	Z	C
SUB	Substraction	A = A - M	A	M			N	Z	C
SWAP	SWAP nibbles	A7-A4 <=> A3-A0	reg, M				N	Z	
TNZ	Test for Neg & Zero	tnz lbl1					N	Z	
TRAP	S/W trap	S/W interrupt				1			
WFI	Wait for Interrupt					0			
XOR	Exclusive OR	A = A XOR M	A	M			N	Z	

7 ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields. Nevertheless, it is recommended that normal precautions be observed in order to avoid subjecting this high-impedance circuit to voltage above those quoted in the Absolute Maximum Ratings. For proper operation, it is recommended that the input voltage V_{IN}, on the digital pins, be constrained within the range:

$$(GND - 0.3V) \leq V_{IN} \leq (V_{DD} + 0.3V)$$

To enhance reliability of operation, it is recommended to configure unused I/Os as inputs and to connect them to an appropriate logic voltage level such as GND or V_{DD}.

All the voltage in the following tables are referenced to GND.

Table 14. Absolute Maximum Ratings (Voltage Referenced to GND)

Symbol	Ratings	Value	Unit
VBR VBL = VB VB1	Supply Voltage t = 10m ISO transients t = 400ms[1)]	0 to 18 0 to 24 0 to 40	V
|AGND - GND|	Max. variations (Ground Line)	50	mV
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_J	Junction Temperature	150	°C
ESD	ESD susceptibility	2000	V
V_{LV}	Input Voltage, low voltage pins	GND - 0.3 to V_{DD} + 0.3	V
V_{PWM}	Pin Voltage, PWMI, PWMO pins	GND - 18 to VB	V
V_{CAN}	Pin Voltage, CAN_H, CAN_L pins	GND - 18 to VB	V
I_{IN}	Input Current (low voltage pins)	-25.....+25	mA

Note 1. ISO transient must not reset the device

7.2 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)^*$$

Where:

– T_A is the Ambient Temperature in °C,

– θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,

– P_D is the sum of P_{INT} and $P_{I/O}$,

– P_{INT} is the product of I_1 and VB, plus the power dissipated by the power bridge, expressed in Watts. This is the Chip Internal Power

– $P_{I/O}$ represents the Power Dissipation on Input and Output Pins; User Determined.

For most applications $P_{I/O} << P_{INT}$ and may be neglected. $P_{I/O}$ may be significant if the device is configured to drive Darlington bases or sink LED Loads.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Therefore:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times P_D^2 \quad (3)$$

Where:

– K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 15. Thermal Characteristics (VB=18V, T_J = 150°C, I_{LOAD} = 2A)

Symbol	Description	Value	Unit
P_D	Dissipated Power	3	W

(*): Maximum chip dissipation can directly be obtained from T_j (max), θ_{JA} and T_A parameters.

Figure 46. Hiquad-64: θ_{JA}

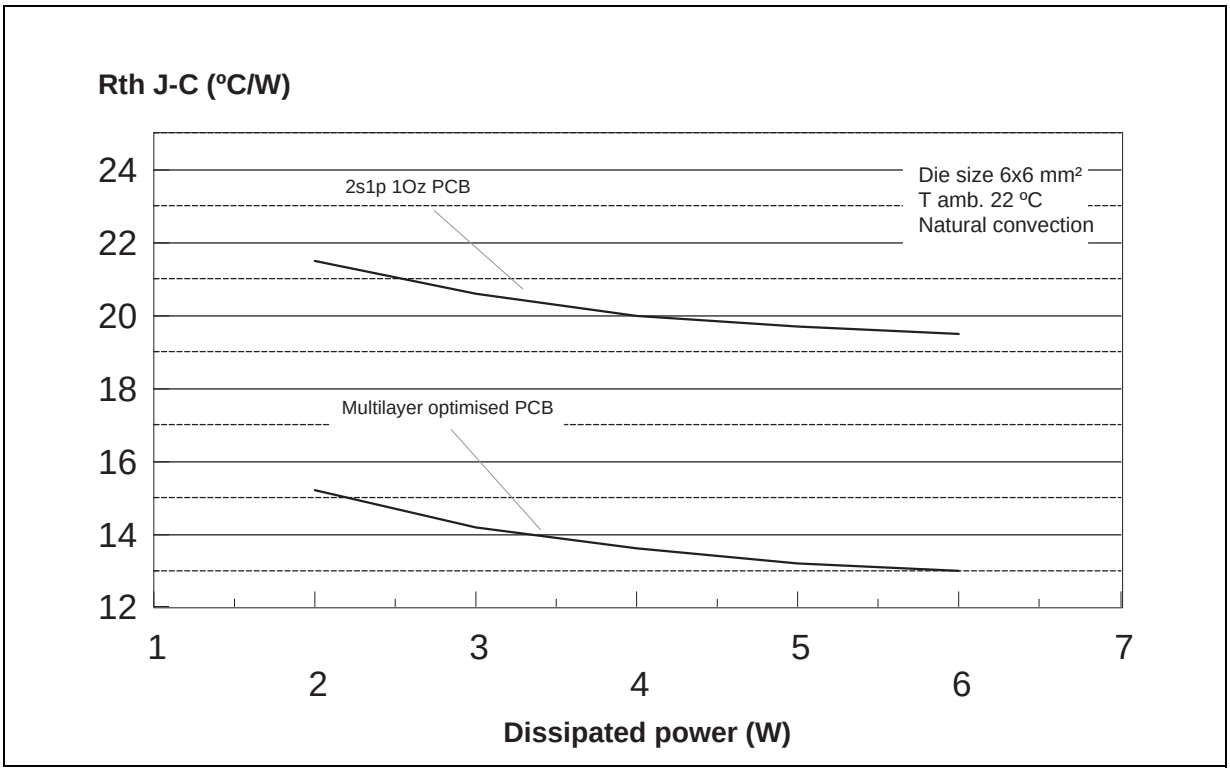
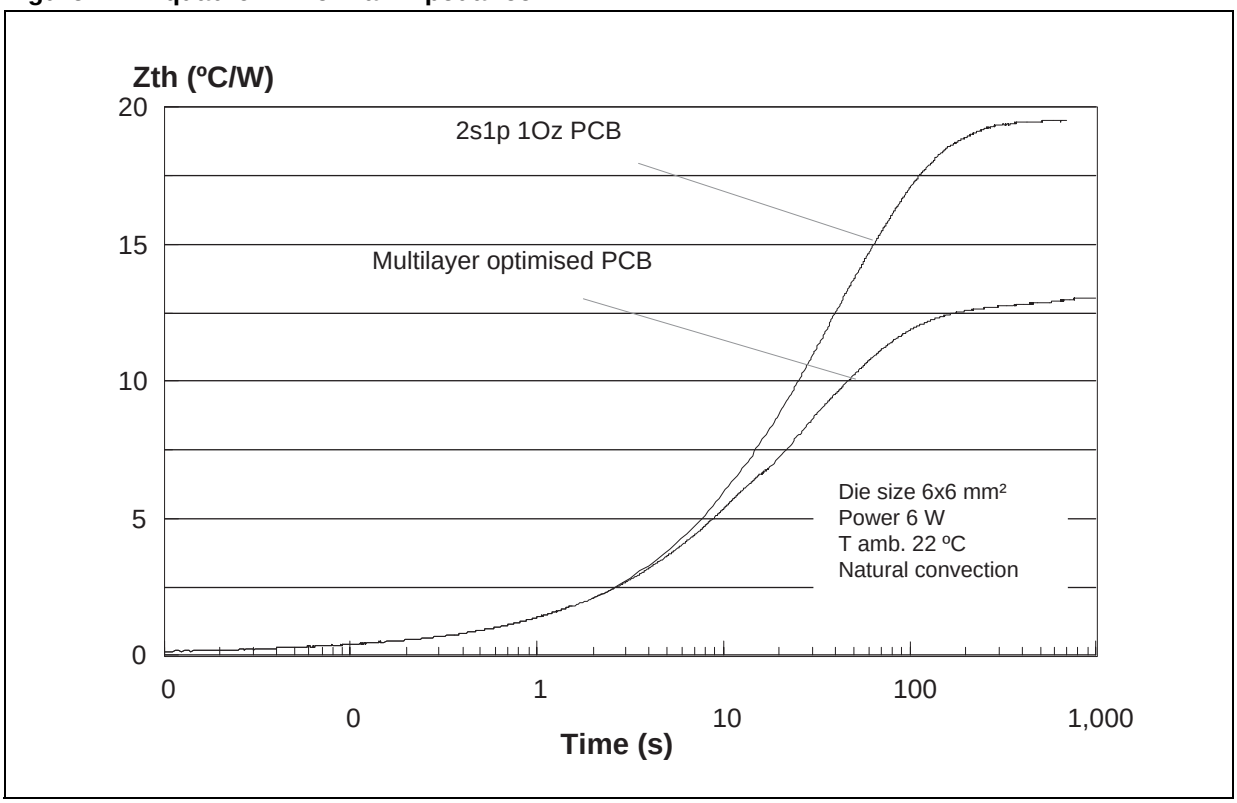


Figure 47. Hiquad-64: Thermal impedance

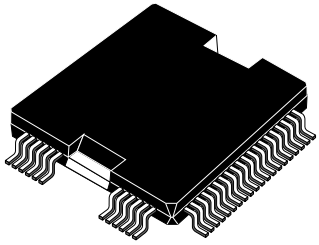


7.3 PACKAGE MECHANICAL DATA

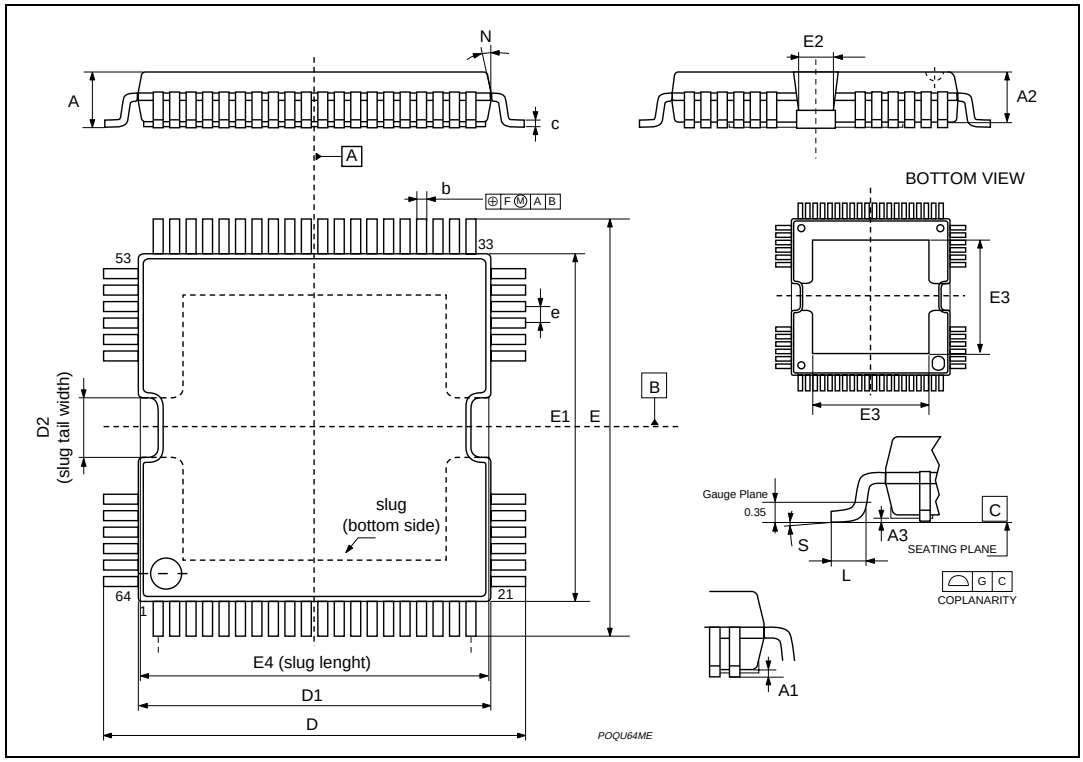
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.15			0.124
A1	0		0.25	0		0.010
A2	2.50		2.90	0.10		0.114
A3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	17.00		17.40	0.669		0.685
D1 (1)	13.90	14.00	14.10	0.547	0.551	0.555
D2	2.65	2.80	2.95	0.104	0.110	0.116
E	17.00		17.40	0.669		0.685
E1 (1)	13.90	14.00	14.10	0.547	0.551	0.555
e		0.65			0.025	
E2	2.35		2.65	0.092		0.104
E3	9.30	9.50	9.70	0.366	0.374	0.382
E4	13.30	13.50	13.70	0.523	0.531	0.539
F		0.10			0.004	
G		0.12			0.005	
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	0°(min.), 7°(max.)					

(1): "D1" and "E1" do not include mold flash or protusions
- Mold flash or protusions shall not exceed 0.15mm(0.006inch) per side

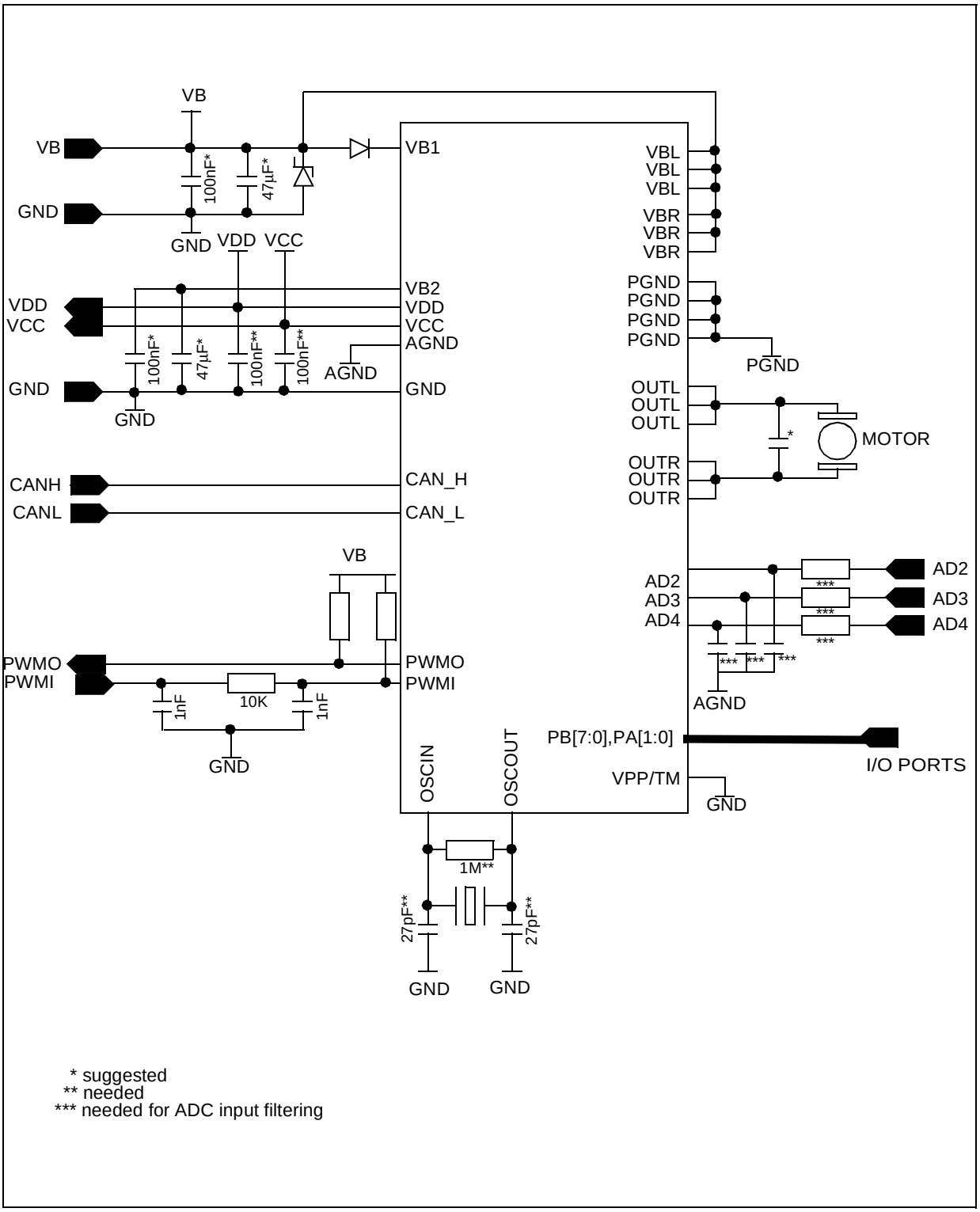
OUTLINE AND MECHANICAL DATA



HiQUAD-64



7.4 APPLICATION DIAGRAM EXAMPLE



7.5 DC ELECTRICAL CHARACTERISTICS

(T_J = -40 to +150°C, VB=12V unless otherwise specified)

GENERAL						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max**	**Unit**
VB1	Supply Voltage	f_{OSC} = 16 MHz	6.4	12	18	V
VBR, VBL = VB	Power Supply Voltage	f_{OSC} = 16 MHz	7.1	12	18	V
I1	Supply Current from VB1	No external loads RUN mode WAIT mode Halt mode[1)]		 24 21 16		 mA mA mA
I_{IN}	Input Current	Low voltage pins[2)]	-5		5	mA

Note 1. Halt mode is not allowed if Watchdog or Safeguard are enabled

Note 2. A current of 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device.

POWER SUPPLY						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
VB2	Pre-regulated Voltage	VB1 = 12V	8	10	12	V
VDD	Regulated Voltage	VB1 = 12V	4.75	5	5.25	V
VDD	Regulated Voltage	VB1 = 3.. 6.4V	VB1 - 1.1			V
ΔVDD	Line Regulation	VB1 = 6.4..18V			50	mV
ΔVDD	Load Regulation	I_{VDD}=0..50mA			50	mV
VCC	Regulated Voltage		4.75	5	5.25	V
VCC	Regulated Voltage	VB1 = 3.. 6.4V	VB1 - 1.1			V
ΔVCC	Line Regulation	VB1 = 6.4..18V			50	mV
ΔVCC	Load Regulation	I_{VCC}=0..15mA			50	mV
I_{VDD}	Current sunk from VDD pin				50	mA
I_{VCC}	Current sunk from VCC pin				15	mA
I_{MAXVDD}	Current limit from VDD		200		350	mA
I_{MAXVCC}	Current limit from VCC		50		160	mA
C_{VDD}	External capacitor to be connected to VDD pin			100		nF
C_{VCC}	External capacitor to be connected to VCC pin			100		nF

STANDARD I/O PORT PINS						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
V_{IL}	Input Low Level Voltage		-	-	$0.3xV_{DD}$	V
V_{IH}	Input High Level Voltage		$0.7xV_{DD}$	-	-	V

STANDARD I/O PORT PINS						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
V_{OL}	Output Low Level Voltage	I=-5mA	-	-	1.0	V
	"	I=-1.6mA	-	-	0.4	V
V_{OH}	Output High Level Voltage	I=5mA	3.1	-	-	V
	"	I=1.6mA	3.4	-	-	V
I_L	Input Leakage Current	$GND<V_{PIN}<V_{DD}$	-10	-	10	µA
I_{RPU}	Pull-up Equivalent Resistance	V_{IN}=GND	40	-	250	KΩ
T_{ohl}	Output H-L Fall Time	C_l=50pF	-	30	-	ns
T_{olh}	Output L-H Rise Time	C_l=50pF	-	30	-	ns

Note: All voltage are referred to GND unless otherwise specified.

7.6 CONTROL TIMING

(Operating conditions T_j = -40 to +150°C, VB=12V unless otherwise specified)

Symbol	**Parameter**	**Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max**	
f_{OSC}	Oscillator Frequency		0[1)]		16	MHz
f_{CPU}	Operating Frequency		0[2)]		8	MHz
t_{RL}	External RESET Input pulse Width		1.5			t_{CPU}
t_{PORL}	Internal Power Reset Duration		4096			t_{CPU}
T_{DOGL}	Watchdog or Safeguard RESET Output Pulse Width			500		ns
t_{DOG}	Watchdog Time-out	f_{cpu} = 8 MHz	12,288 1.54		786,432 98.3	t_{CPU} ms
t_{OXOV}	Crystal Oscillator Start-up Time				50	ms
t_{DDR}	Power up rise time				100	ms

Note 1. With Safeguard disabled, A/D operations and Oscillator start-up are not garanteed below 1Mhz

Note 2. With Safeguard disabled, A/D operations and Oscillator start-up are not garanteed below 1Mhz

7.7 OPERATING BLOCK ELECTRICAL CHARACTERISTICS

These device-specific values take precedence over any generic values given elsewhere in the document. (T_j = -40... +150°C, V_{DD} - GND = 5 V unless otherwise specified).

A/D Converter						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
V_{AL}	Resolution			10		bit
AE	Absolute Error		-2		2	LSB
FSC	Full Scale Error		-1		1	LSB
ZOE	Zero Offset Error		-1		1	LSB
NLE	Non Linearity Error		-2		2	LSB
DNLE	Differential Non Linearity Error		-1/2		1/2	LSB
tc	Conversion Time	f_{cpu} = 8MHz			20	µs
IL	Leakage current		-0.5		0.5	µA
Vin	Input Voltage		0		VCC	V
T_{SENS}	Temperature sensing range		-40		150	°C
T_{SENSR}	Temperature sensor resolution		1			LSB/°K
T_{SENSE}	Temperature sensor error (T in °K)				±2[1)]	%

Note 1. After trimming, being T_{TRIM} the trimming temperature, the specified precision can be achieved in the range T_{TRIM}-80, max[T_{TRIM}+80, 150°C]. Precision is related to the read temperature in Kelvin.

POWER BRIDGE						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
RdsON	Output Resistance	Measured on OUTL and OUTR.			150	mΩ
RdsON @ 25°C	Output Resistance	Measured on OUTL and OUTR.		70		mΩ
I_{SC}	Short circuit current	Short to VBL,VBR, GND: load short	6	8	10	A
t_{SCPI}	Short circuit protection intervention time			12		µs
T_{hw}	Thermal shutdown threshold		165	175	185	°C
T_{hwh}	Thermal shutdown threshold hysteresis			20		°C
t_{rp}	OUTL, OUTR rise time	measured from 10% to 90%		1		µs

EEPROM			
Parameter	**Min.**	**Max**	**Unit**
Write time		4.0	ms
Write Erase Cycles	50000		Cycles
Data Retention	10		Years

PWM OUTPUT						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
V_{OH}	Output Voltage High	RL = 500Ω to VB	VB-0.2		VB	V
V_{SL}	Saturation Voltage Low	IO = 20mA	0		0.5	V

PWM OUTPUT						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
I_{IO}	Input Current	VB = 12V	0		25	µA
I_{PSC}	Short circuit current		30	60	100	mA

PWM INPUT						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
V_{TL}	Input state low	VB=VBR	-1		0.45*VB	V
V_{TH}	Input state high	VB=VBR	0.55VB		VB	V
V_H	Hysteresis	VB=VBR		0.025*VB	0.8	V
I_{II}	Input Current	VB = 12V	0.5		8	µA

OSCILLATOR SAFEGUARD						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
f_{low}	reset low frequency		0.6	1.1	1.7	MHz
f_{high}	reset high frequency		17	24	31	MHz

CAN TRANSCEIVER

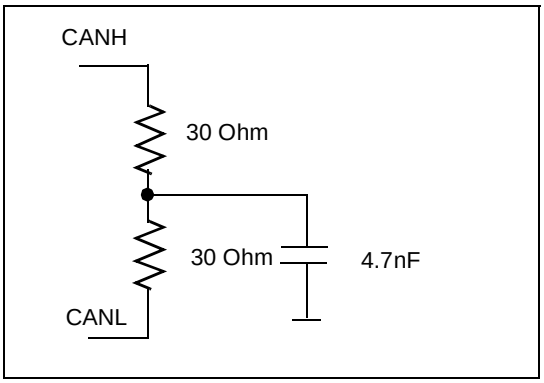
Rl = 60 Ohm, see note 1, unless otherwise specified.

Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
V_{CANHL_R}	Recessive State CAN_H, CAN_L Output Voltage	TX=High Level V_{DD} = 5V $I_{CANH} = I_{CANL} = 0$	2.0	2.5	3.0	V
V_{DIFF_R}	Recessive State Differential Output Voltage ($V_{DIFF} = V_{CANH} - V_{CANL}$)	TX=High Level $I_{CANH} = I_{CANL} = 0$	-500	0	50	mV
V_{CANH_D}	Dominant State CAN_H Output Voltage	TX = Low Level; VDD = 5V	2.75	3.5	4.5	V
V_{CANL_D}	Dominant State CAN_L Output Voltage	TX = Low Level; VDD = 5V	0.5	1.5	2.25	V
V_{DIFF_D}	Dominant State Differential Output Voltage ($V_{DIFF} = V_{CANH} - V_{CANL}$)	TX = Low Level; VDD = 5V	1.5	2.0	3.0	V
I_{SC}	CAN_H, CAN_L Short Circuit Threshold Current		90		200	mA
V_{REC}	Differential Input Voltage for Recessive State ($V_{DIFF} = V_{CANH} - V_{CANL}$)	V_{CANL} = -2V; TX = High Level V_{CANH} = 6.5V: TX = High Level			500	mV
V_{DOM}	Differential Input Voltage for Dominant State ($V_{DIFF} = V_{CANH} - V_{CANL}$)	V_{CANL} = -2V; TX = High Level V_{CANH} = 6.1V: TX = High Level	900			mV
V_{DIFF_HYS}	Differential Input Voltage Hysteresis			150		mV
t_{TD}	Delay Time from TX to $V_{DIFF} = V_{CANH} - V_{CANL}$				50	ns

CAN TRANSCEIVER Rl = 60 Ohm, see note 1, unless otherwise specified.						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
t_{DR}	Delay Time from V_{DIFF} to RX $V_{DIFF} = V_{CANH} - V_{CANL}$				150	ns
t_D	Disabled Transmission Time for Overcurrent Protection		1	5	10	us
SR_H	VCANH Slew Rate Between 20% and 80%		30		80	V/µs
SR_L	VCANL Slew Rate Between 20% and 80%		30		80	V/µs
t_{TR}	Delay Time from TX to RX				200	ns
$1/t_{bit}$	Transmission speed	non return to zero			1	Mb/s

POWER ON / LOW VOLTAGE RESET						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ**	**Max**	**Unit**
$V_{Reset\ L}$	Input low level voltage	NRESET pin			0.3VDD	V
$V_{Reset\ H}$	Input high level voltage	NRESET pin	0.7VDD			V
$I_{Reset\ L,\ H}$	Input current	NRESET pin VDD = 5V Leakage current Internal reset by watch-dog or POR Pull up current source	 30		 1 1 70	 µA mA µA
$V_{Reset\ UD}$	VDD for RESET undefined	Below this voltage RE-SET is not defined			2	V
$V_{Reset\ ON}$	VDD low threshold for RESET on		3.4			V
$V_{Reset\ OFF}$	VDD high threshold for RESET off				3.9	V

Note 1:



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