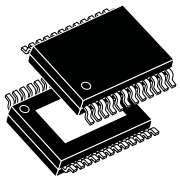
L9001

Automotive power supply IC with multiple voltage regulators

Datasheet - production data



PowerSSO-24 (exposed pad down)

GADG3003171630PS

Features



- AEC-Q100 qualified
- Flexible, configurable voltage regulator for multiple power supply schemes
  - First stage asynchronous switch mode regulator (VDD1), supplying second stage regulator (VDD2), peripherals or µC [3.3 V/5.0 V/6.0 V/1 A]; optionally disabled
  - Second regulator (VDD2), configurable as BUCK converter or LDO regulator, supplying peripherals, µC or µC-core [0.8 V to 5.0 V/1 A BUCK and 300 mA for LDO]; optionally disabled
  - ADC LDO [3.3 V/5 V/100 mA] for ADC µC supply
- Supervision and diagnosis
  - VS monitoring
  - Over temperature detection
  - Output supply supervision
  - Output overcurrent protection
- Fail-safe functionality
  - Output under or over voltage reset generation
  - Configurable Watchdog
  - Over temperature shutdown
- Low power mode

Description

L9001 SPS (Simple Power Supply) device is a multiple power regulator for Automotive applications with one buck regulator, one configurable buck or linear regulator and one linear regulator. Its output voltages are configurable via discrete pins.

On top of the regulators, this device integrates a watchdog functional block, and a diagnosis functional block (under/over voltage, output current and temperature).

Device is capable of low power operation mode with main regulators still active and reduced power consumption from battery.

Table 1. Device summary

Order code	Package	Packing
L9001	PowerSSO-24 (exposed pad down(1))	Tube
L9001-TR		Tape and reel

1. The exposed pad dimensions for this device is showed in *Table 19: PowerSSO-24 (exposed pad) package mechanical data* (VARIATIONS - Option A, “D1 and E2”).

This is information on a product in full production.

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1 General description

The L9001 is a power management device targeting various automotive applications. The device contains three voltage regulators: VDD1, VDD2 and ADCLDO.

1.1 VDD1 regulator

VDD1 is an asynchronous switch mode power supply with integrated FET and can be used as pre-regulator for VDD2 and/or to supply external devices such as µC, transceivers, or sensors. The regulated voltage can be configured to 3.3 V / 5 V or 6 V by a proper connection of CONF3 input pin. Current capability is up to 1A, and the device provides an internal peak current limitation as protection. In addition VDD1 output voltage is monitored through VR1 pin and if the voltage goes outside the specified range, RSTN1 output is asserted low; when the fault disappears the output is released after the specified hold time.

If the application does not require it, VDD1 regulator can be also disabled without the need to insert additional external components.

1.2 VDD2 regulator

VDD2 is a configurable power supply with integrated FET that can be used as BUCK regulator (also referenced as BUCK2 in this case) or as LDO regulator (also referenced as LDO2 in this case) to supply µC or µC core. In fact the regulated voltage is highly configurable and can be adjusted between 0.8 V and 5 V by proper sizing of external divider on FB2 input pin. The choice between BUCK and LDO is done by setting the proper connection of CONF2 input pin. Current capability is up to 1 A in BUCK mode and 300 mA in LDO mode and the device provides an internal limitation according to the chosen option (BUCK / LDO). In addition VDD2 output voltage is monitored through FB2 input pin and if the voltage goes outside the specified range, RSTN2 output is asserted low; when the fault disappears the output is released after the specified hold time.

The input voltage of VDD2 regulator can be connected to:

- VS supply voltage, in a configuration in which VDD2 is directly supplied from battery
- VDD1 output, in a configuration where VDD2 is supplied by VDD1 pre regulator

The connection to VS battery will automatically disable VDD1 as the device does not allow the independent operation of VDD1 and VDD2 both supplied from battery.

If the application does not require it, VDD2 regulator can be disabled without the need to insert additional external components.

1.3 ADCLDO regulator

ADCLDO is a LDO power supply with integrated FET which can be used for external loads with low current demand. The regulated voltage VADC can be configured to 3.3 V / 5 V by a proper connection of CONF1 input pin. Current capability is up to 100 mA, and the device provides an internal current limitation as protection. In addition VADC output voltage is monitored internally and if the voltage goes outside the specified range, ADCMON output is asserted low; when the fault disappears the output is released after the specified hold time.

1.4 Supervision and diagnosis

In addition to the described protection features of current limitation and output voltage monitor, the device provides additional supervision and diagnosis functions: VS UV/OV, over temperature, watchdog and latch mode.

VS input voltage is monitored and if an undervoltage or overvoltage is detected with respect to the specified thresholds, the device enters a so called safe state in which output voltages are switched off.

The device internal temperature is also monitored: when temperature increases over the specified threshold, the TWN output is asserted low and, if the temperature increases above a shutdown threshold, the device enters safe state.

The device also has a charge pump block which is used to ensure proper regulators functionality inside spec limits; undervoltage on CP also triggers device safe state.

The device integrates a watchdog functional block which constantly monitors the status of the microcontroller's oscillator. This is done by checking the synchronization of the microcontroller with an internal time signal whose period is configured by applying a specific capacitor at the input pin WDT. If the microcontroller signal, which is transmitted to the watchdog via the pin WDI, is not serving the watchdog correctly, the output pin WDO is asserted low for the specified time.

L9001 provides a feature, called latch state, that disables the system in case a systematic fault is repetitively detected on the charge pump structure, watchdog or in case of repetitive thermal events. The separated fail counters and detection mechanism are explained in the dedicated sections of this document.

1.5 Low power mode

For low power applications L9001 provides a Low Power mode feature which drastically reduces the device power consumption while the attached loads are still supplied via bypass LDOs. This mode can be entered with STBY input pin to high level as described in the dedicated section of this document. Load current is monitored in this mode and main regulators are automatically reenabled if needed.

2 Block and application diagrams

Figure 1. Block diagram

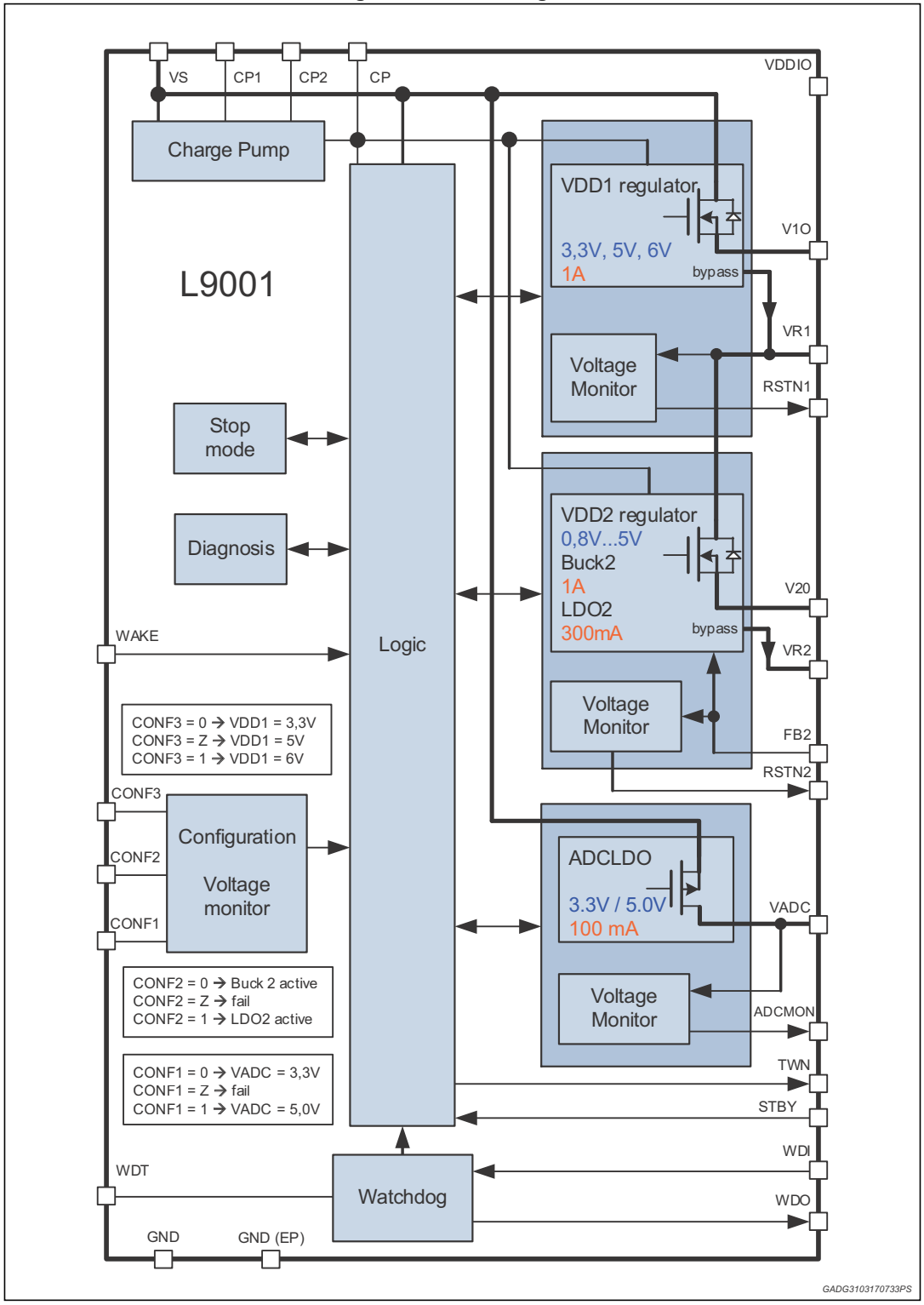
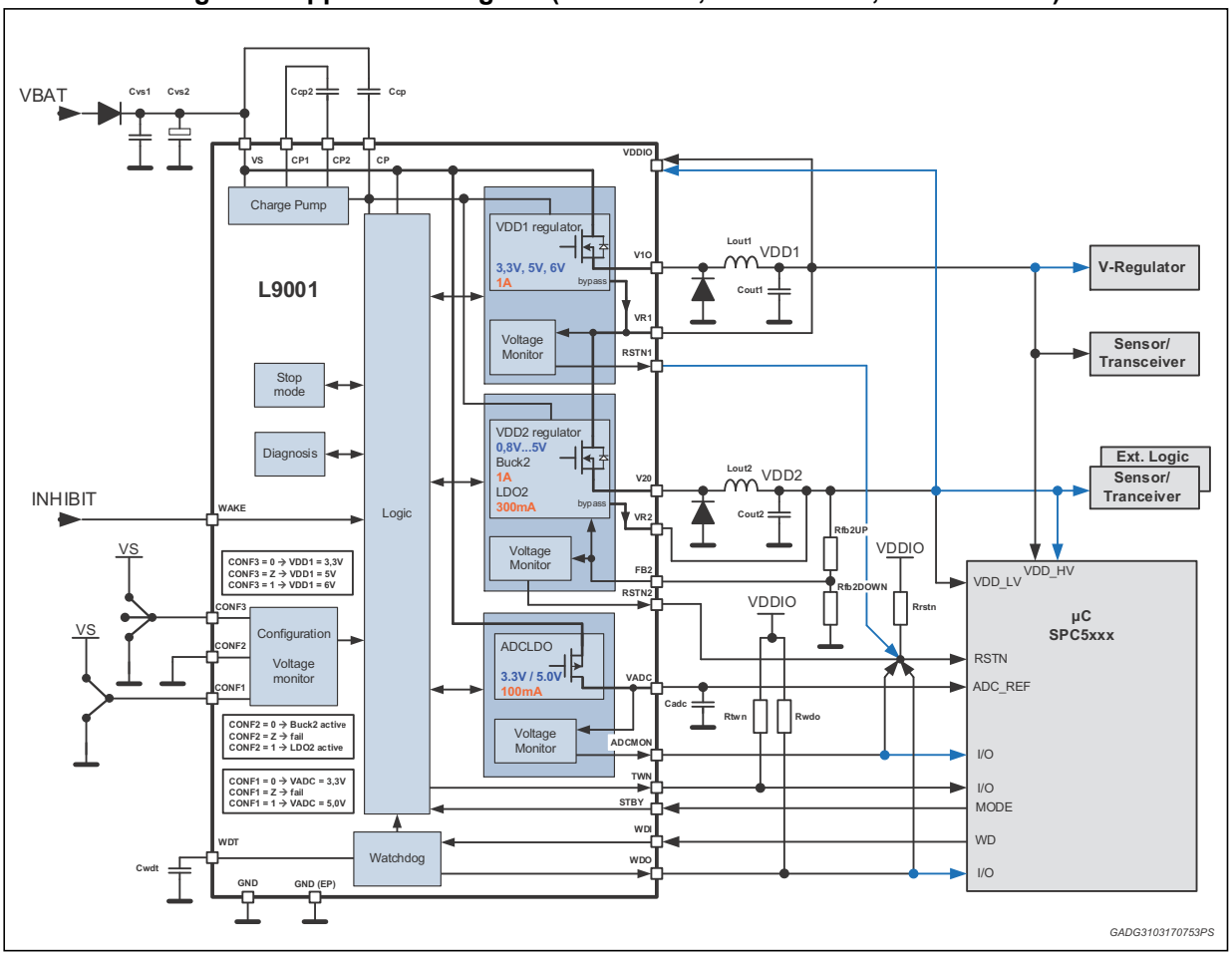


Figure 2. Application diagram (VDD1 = 5 V, BUCK2 = 1.2, VADC = 3.3 V)



3 Pin description

Figure 3. Pin connection diagram (top view)

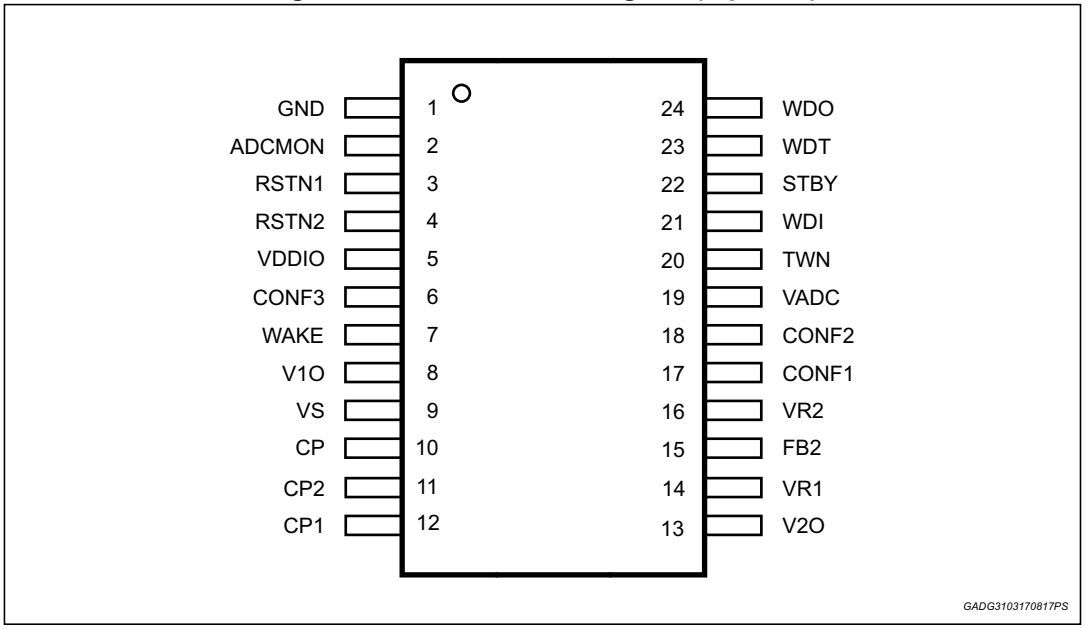


Table 2. Pin out description

Pin	Symbol	Function	Type	
EP	GND	Exposed pad: connected to GND	supply	Global
1	GND	Power ground	supply	Global
2	ADCMON	ADCLDO monitor (reset)	O	Local
3	RSTN1	VDD1 monitor (reset)	O	Local
4	RSTN2	VDD2 monitor (reset)	O	Local
5	VDDIO	Input/Output voltage reference	supply	Local
6	CONF3	Configuration input 3	I	Local
7	WAKE	Wake-up input	I	Local
8	V1O	VDD1 switching pin	supply	Local
9	VS	Battery supply voltage	supply	Global
10	CP	Charge pump output	supply	Local
11	CP2	Charge pump capacitor pin 2	supply	Local
12	CP1	Charge pump capacitor pin 1	supply	Local
13	V2O	BUCK2 switching pin / LDO2 output voltage	supply	Local
14	VR1	VDD1 BYP output voltage / VDD2 supply pin	supply	Global
15	FB2	VDD2 feedback voltage pin	I	Local
16	VR2	VDD2 BYP output voltage	supply	Local

Table 2. Pin out description (continued)

Pin	Symbol	Function	Type	
17	CONF1	Configuration input 1	I	Local
18	CONF2	Configuration input 2	I	Local
19	VADC	ADCLDO output voltage	supply	Local
20	TWN	Thermal warning output flag	O	Local
21	WDI	Watchdog input	I	Local
22	STBY	Stand-by input	I	Local
23	WDT	Watchdog timer input	I/O	Local
24	WDO	Watchdog error output flag	O	Local

4 Electrical specifications

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Pin Name	Test Condition	Min	Max	Unit
VS	-	-0.3	40	V
WAKE	-	-0.3	40	V
CP	Note: (1)	-0.3	45	V
CP1	Note: (2)	-0.3	40	V
CP2	Note: (3)	-0.3	45	V
VR1	-	-0.3	40	V
V1O,V2O	-	-0.5	40	V
VR2,FB2	-	-0.3	40	V
VADC	-	-0.3	19	V
VDDIO	-	-0.3	19	V
RSTN1, RSTN2, ADCMON	-	-0.3	19	V
STBY,WDI	-	-0.3	19	V
TWN,WDO	-	-0.3	19	V
WDT	-	-0.3	40	V
RSTN1, RSTN2, ADCMON, TWN, WDO	-	-	10	mA
CONF1,CONF2,CONF3	-	-0.3	40	V

1. CP-VS<6V, VS-CP<0.3V.
2. CP1-VS<0.3V.
3. CP2-VS<6V VS-CP2<0.3V

4.2 ESD protection

Table 4. ESD protection values

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
ESD HBM Global	HBM global pins	ESD according to the Human Body Model (HBM), Q100-002 for global pins; (100 pF/1.5 kΩ)	-4000	-	4000	V	9, 14
ESD HBM	HBM local pins	ESD according to the Human Body Model (HBM), Q100-002 for all pins; (100 pF/1.5 kΩ)	-2000	-	2000	V	ALL
ESD CDM Corner	CDM corner pins	ESD according to the Charged Device Model (CDM), Q100-011 Corner pins	-750	-	750	V	Corner
ESD CDM	CDM all pins	ESD according to the Charged Device Model (CDM), Q100-011 All pins	-500	-	500	V	ALL

4.3 Operating range

Table 5. Supply voltage range

Symbol	Parameter	Min.	Max.	Unit
V_S	Supply voltage	5.5 (1)	18	V

1. If VS<6.5V, VDD1 output degradation can occur depending on device settings (see VDD1 regulator section for details)

4.4 Thermal data

Table 6. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{amb}	Ambient temperature	-40	-	125	°C
T_j	Junction temperature	-40	-	175	°C
$R_{Th(j\text{-}amb)}$	Thermal resistance junction-to-ambient (2s2p thermally enhanced PCB)	-	-	24	°C/W
$R_{Th(j\text{-}case)}$	Thermal Resistance junction-to-case	-	-	2	°C/W

4.5 General operating conditions

As described in this chapter, all electrical characteristics contained within this document are valid for the following conditions unless otherwise noted:

$$-40\ °C < T_j < 175\ °C,\ 5.5\ V < V_S < 18\ V.$$

Moreover all electrical parameters related to time/frequency have a spread of ±30% unless otherwise stated.

5 Power supply

5.1 Configuration

The device regulators must be configured by proper connection of CONFx input pins.

VDD1 regulator output voltage level must be configured through pin CONF3.

The pin has a tri-state configuration: LOW, MID and HIGH. The output of the regulator corresponding to each configuration is summarized in the table below:

Table 7. CONF3 configuration

-	Low config	MID config	HIgh config
CONF3	VDD1 = 3.3 V	VDD1 = 5 V	VDD1 = 6 V

VDD2 regulator mode must be configured in either Buck regulator or LDO through pin CONF2.

ADCLDO output voltage must be configured by proper configuration on pin CONF1.

CONF1 and CONF2 pin have a LOW/HIGH configuration. The regulator configurations corresponding to each option are summarized in the table below.

Table 8. CONF2 and CONF1 configuration

-	Low config	High config
CONF1	VADC = 3.3 V	VADC = 5 V
CONF2	VDD2 as Buck	VDD2 as Linear

In order to have the described configuration, pin CONFx must be connected as follows:

- LOW configuration: pin CONFx must be connected to ground;
- HIGH configuration: pin CONFx must be connected to VS supply;
- MID configuration (only for CONF3): pin CONF3 must be left open.

Voltage levels at CONF1, CONF2 and CONF3 pins are latched at power-up; in addition, CONF1 and CONF2 have an open load check. In case of disconnected pins all output voltages are disabled, the device stays in OFF state and a new power-up sequence would be needed to refresh the signal values on the input pins.

5.2 VDD1 regulator

VDD1 is an asynchronous switch mode power supply with integrated FET. The input voltage of VDD1 regulator is VS pin; the output voltage generated by the buck can be configured as 3.3 V / 5 V / 6 V as described in *Section 5.1*.

The output voltage can be directly used by external loads and must be connected also to pin VR1. In fact VR1 is the output of a LDO bypass regulator which is used to keep regulation active when the output current demand goes below a specified threshold ILIM_BP1. In this bypass mode, the output voltage is regulated according to the VR1_byp parameter. Such mode is used for example when the system needs to reduce the overall consumption by entering the Low Power mode (see dedicated *Section 8.2.4* for details)

The connection of VDD1 output voltage to VR1 also allows the usage of VDD1 as pre-regulator for VDD2 in case VDD2 regulator is not disabled (see *Section 5.3* for details).

To guarantee full flexibility in the system power supply architecture, VDD1 regulator can also be disabled, if the application does not require it. This can be configured by shorting the VR1 output pin to VS supply and CONF3 to ground.

Table 9. VDD1 regulator parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VR1	Output voltage	CONF3 LOW 1 A > I_{load1} > I_{LIM_BP1}	3.2	3.3	3.4	V
		CONF3 MID 1 A > I_{load1} > I_{LIM_BP1}	4.85	5	5.15	V
		CONF3 HIGH 1 A > I_{load1} > I_{LIM_BP1} , VS > 6 .5 V	5.82	6	6.18	V
I_{load1}	Output current	-	0	-	1	A
dVSR1_ac	Line transient response(1)	Not tested, guaranteed by design, SR < 1 V/µs	-8	-	8	%
dVLR1_ac	Load transient response(1)	Not tested, guaranteed by design, I_{load1} > I_{LIM_BP1}, dt = 10 µs	-8	-	8	%
VR1_byp	Output voltage in bypass mode	CONF3 LOW I_{load1} < I_{LIM_BP1}	3.25	3.25	3.45	V
		CONF3 MID I_{load1} < I_{LIM_BP1}	4.93	5.08	5.23	V
		CONF3 HIGH I_{load1} < I_{LIM_BP1}	5.91	6.09	6.27	V
I_{lim1}	Current limitation	-	2.2	2.8	4	A
SwFreq1	Switching frequency	-	-	465	-	kHz
RDSon1	High side RDSon	-	-	-	0.5	Ω
SS1	Soft start control	CONF3 LOW (20%-80%)	-	-	15.5	V/ms
		CONF3 MID (20%-80%)	-	-	21	V/ms
		CONF3 HIGH (20%-80%)	-	-	24.5	V/ms
I_{CMP1_l}	LPM current low threshold	-	3	-	-	mA
I_{CMP1_h}	LPM current high threshold	-	-	-	28	mA
I_{LIM_BP1}	Bypass LDO current limitation	-	22	30	45	mA
C_{out1}	Capacitor at VR1	Application info	-	22	-	µF

Table 9. VDD1 regulator parameters (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
L_{out1}	Inductor at VR1	Application info	-	22	-	µH
ESR_C_{out1}	Eq. series resistance for C_{out1}	Application info	-	-	50	mΩ
C_{vs1}	V_S bypass capacitor	Application info	-	100	-	nF
C_{vs2}			-	4.7	-	µF

1. For further load/line transient details, please refer to AN5163.

5.3 VDD2 regulator

The device integrates a second configurable BUCK/LDO regulator VDD2, whose output voltage can be adjusted between 0.8 V and 5 V and so it can be adapted to supply uC core voltage.

The BUCK/LDO mode can be selected through CONF2 pin as described in *Section 5.1*; the current capability depends on the chosen option and is specified in *Table 10*.

The output voltage can be adjusted by adequately sizing the external divider in order to have the specified feedback reference voltage on the FB2 input pin.

The input voltage of VDD2 regulator is VR1 and this input can be connected to:

- VS supply voltage, in a configuration in which VDD2 is directly supplied from battery;
- VDD1 output, in a configuration in which VDD2 is supplied by VDD1 pre regulator.

The connection of VR1 to VS battery will automatically disable VDD1 (as explained in the previous section) as the device does not allow the independent operation of VDD1 and VDD2 both supplied from battery. As a consequence, when both regulators are operating, the external load applicable on VDD1 is 1 A reduced by the input current of VDD2 regulator.

When VDD2 regulator input is connected to VS supply, the output voltage in buck mode cannot reach voltages lower than 2.5 V, whereas there are no limitations in LDO mode.

The output voltage of VDD2 regulator (which is generated by the buck or directly V20 in case of LDO mode) can be directly used by external loads and must be connected also to pin VR2. In fact VR2 is the output of a LDO bypass regulator which is used to keep regulation active when output current demand decreases below a specified threshold ILIM_BP2 (bypass mode). In this bypass mode, the reference feedback voltage FB2 is regulated according to the FB2_byp parameter. Such mode is used for example when the system needs to reduce the overall consumption by entering the Low Power mode (see dedicated *Section 8.2.4* for details)

To guarantee full flexibility in the system power supply architecture, VDD2 regulator can also be disabled, if application does not require it. This can be done by shorting the FB2 output pin to VS.

Table 10. VDD2 regulator parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VR2	Nominal output voltage	-	0.8	-	5	V
I_{load2}	Output current	Application info, Buck	0	-	1	A
I_{load2_lin}		Application info, LDO	0	-	0.3	A
dVSR2_ac	Line transient response(1)	Not tested, guaranteed by design, Buck, SR < 1 V/µs	-8	-	8	%
dVSR2_ac_lin		Not tested, guaranteed by design, LDO, SR < 1 V/µs	-5	-	5	%
dVLR2_ac	Load transient response(1)	Not tested, guaranteed by design, Buck , VR2 < 2.5 V, 0.4 A > I_{load2} > ILIM_BP2, dt = 10 µs	-8	-	8	%
		Not tested, guaranteed by design, Buck, VR2 ≥ 2.5 V, I_{load2} > I_{LIM_BP2}, dt = 10 µs	-8	-	8	%
dVLR2_ac_lin		Not tested, guaranteed by design, LDO, I_{load2} > I_{LIM_BP2}, dt = 10 µs	-8	-	8	%
I_{lim2}	Current limitation	-	2.2	2.8	4	A
I_{lim2_lin}		-	0.3	-	-	A
FB2	Feedback reference voltage	1 A > I_{load2} Buck > ILIM_BP2	0.776	0.8	0.824	V
		0.3 A > I_{load2} LDO > ILIM_BP2	0.776	0.8	0.824	V
Rfb2UP	Feedback resistor	Application info	10	-	100	kΩ
FB2_byp	Feedback reference voltage in bypass mode	I_{load2} < ILIM_BP2	0.788	0.812	0.836	V
SwFreq2	Switching frequency	-	-	465	-	KHz
RDSon2	High side RDSon	-	-	-	0.5	Ω
SS2	Soft start control	Buck (20%-80% of VR2)	-	-	21	V/ms
		LDO (20%-80% of VR2)	-	-	10.5	V/ms
I_{CMP2_l}	LPM current-low threshold	-	3	-	-	mA
I_{CMP2_h}	LPM current-high threshold	-	-	-	28	mA
I_{LIM_BP2}	Bypass LDO current limitation	-	18	30	45	mA
C_{out2}	Capacitor at VR2	Buck, VR2 < 2.5 V, Application info	-	47	-	µF
		Buck, VR2 ≥ 2.5 V, Application info	-	22	-	µF
		LDO, Application info	7	-	-	µF
L_{out2}	Inductor at VR2	VR2 < 2.5 V	-	10	-	µH
		VR2 ≥ 2.5 V	-	22	-	µH

Table 10. VDD2 regulator parameters (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ESR_C_{out2}	Eq. series resistance for C_{out2}	Application info	-	-	50	mΩ
Cin1_vdd2	Bypass capacitor at VR1 pin	Application info	-	100	-	nF
Cin2_vdd2			-	4.7	-	µF

1. For further load/line transient details, please refer to AN5163.

5.4 ADCLDO Regulator

ADCLDO is a LDO power supply with integrated FET. The input voltage is VS pin; the output voltage is VADC which can be selected as either 3.3 V or 5.0 V as described in *Section 5.1*.

Table 11. ADCLDO regulator parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VADC	Output voltage	CONF1 LOW	3.23	3.3	3.37	V
VADC		CONF1 HIGH	4.9	5	5.1	V
$I_{loadADC}$	Output current	Application info	0	-	100	mA
dVSRADC_ac	Line transient response	Not tested, guaranteed by design, SR < 1 V/µs	-5	-	5	%
dVLRADC_ac	Load transient response	Not tested, guaranteed by design	-5	-	5	%
I_{limADC}	Current limitation	-	100	-	-	mA
RDSonADC	High side RDSon	-	-	-	4	Ω
-SSADC	Soft start control	CONF1 LOW (20%-80% of VADC)	-	-	12	V/ms
		CONF1 HIGH (20%-80% of VADC)	-	-	17	V/ms
Cadc	Capacitor at VADC	Application info	0.7	-	-	µF

5.5 Power up and power down sequences

As soon as the battery level on VS in greater than 5.5 V and the pin WAKE reaches a value greater than WAKE_Hth (see *Table 12*) for a minimum time of WPH, the internal regulators are activated.

A dedicated design approach is used to mitigate emissions and soft start control is used to define the start-up behavior.

When internal regulators are ready, at first VDD1 regulator is activated with soft start functionality. When the under-voltage threshold is reached, the other regulators (VDD2 and ADCLDO) are activated with soft start functionality. In case the VDD1 regulator is not used, the VDD2 and ADCLDO regulators will start right after internal regulators are ready.

In the power down sequence, as soon as WAKE goes below WAKE_Lth (see *Table 12*) for a minimum time of WPL, the internal regulators and all output pins are deactivated.

Figure 4. Power up and Power down sequences

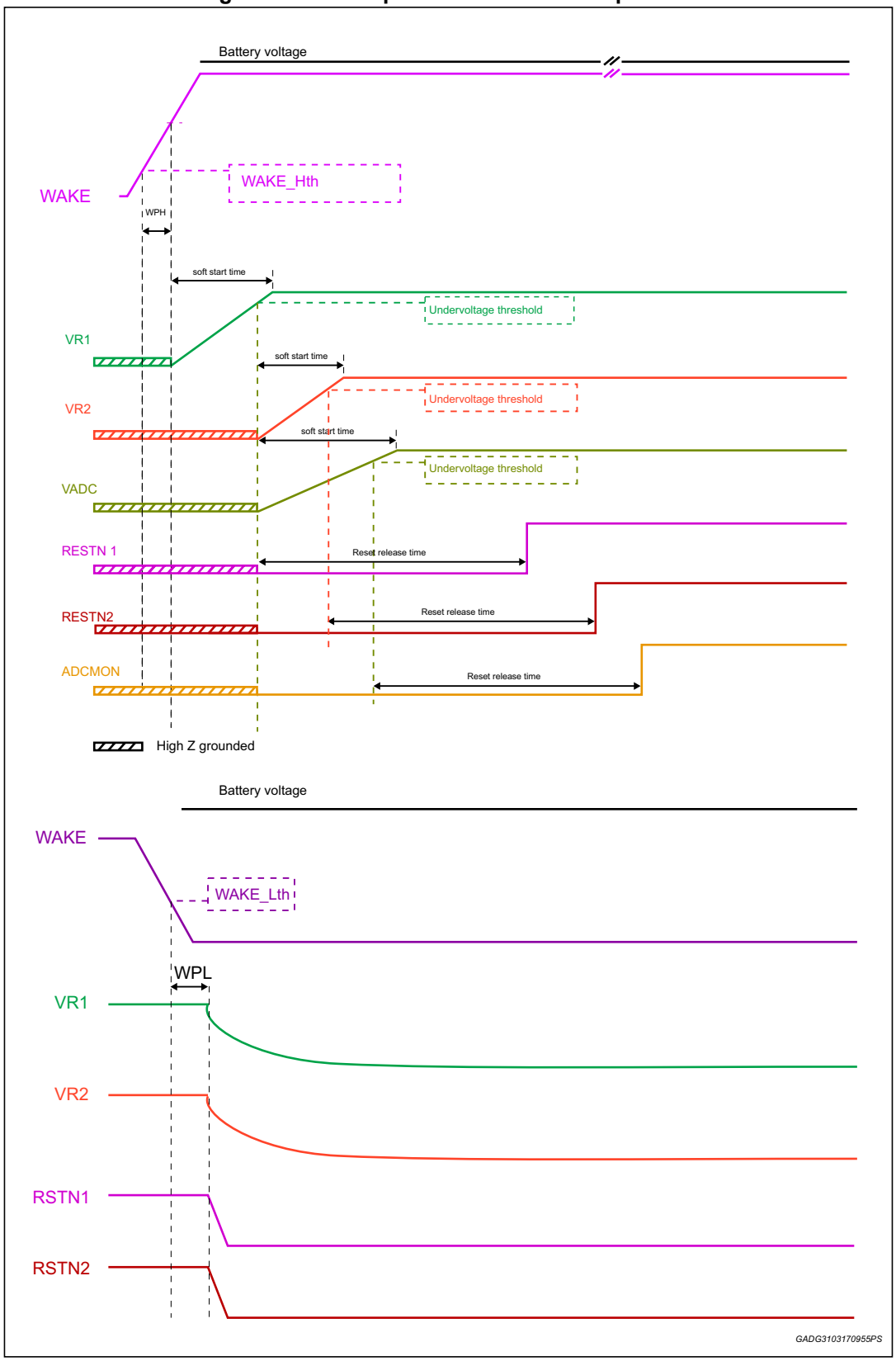


Table 12. Wake parameters

Symbol	Parameter	Description	Min.	Typ.	Max.	Unit
WPL	Wake power latch low	Time delay before a WAKE = L change is taken in account	-	1	-	ms
WPH	Wake power latch high	Time delay before a WAKE = H change is taken in account	-	150	-	µs
WAKE_Hth	WAKE pin threshold to exit OFF mode (WAKE = H)	-	3.1	3.25	3.5	V
WAKE_Lth	WAKE pin threshold to enter OFF mode (WAKE = L)	-	2.1	2.27	2.5	V
WAKE_RPD	WAKE pin pull-down internal resistance	-	4	-	9	MΩ

6 Diagnosis

Each power supply line generated by the device is monitored against over voltage, under voltage and provides an internal current limitation circuit; besides the device provides additional diagnosis functions: watchdog, over temperature, VS UV/OV and latch mode.

VDD1 regulator output is monitored through VR1 pin and if the voltage goes below (above) the specified threshold VR1_uv (VR1_ov) for more than $t_{FILT_uv_VR1}$ ($t_{FILT_ov_VR1}$) filter time, RSTN1 is driven low; when the fault disappears, RSTN1 is released after the specified time t_{RSTN1_act}.

VDD2 regulator output is monitored through FB2 pin and if the voltage goes below (above) the specified threshold VR2_uv (VR2_ov) for more than $t_{FILT_uv_VR2}$ ($t_{FILT_ov_VR2}$) filter time, RSTN2 is driven low; when the fault disappears, RSTN2 is released after the specified time t_{RSTN2_act}.

ADCLDO regulator output is monitored through VADC pin and if the voltage goes below (above) the specified threshold VADC_uv (VADC_ov) for more than $t_{FILT_uv_VADC}$ ($t_{FILT_ov_VADC}$) filter time, ADCMON is driven low; when the fault disappears, ADCMON is released after the specified time t_{ADCMON_act}.

As supervision watchdog function, the WDI input is monitored and WDO output is driven low in case of faults (see *Section 7* for details)

Internal junction temperature is monitored and when Tj > TW_H, TWN output is driven low and it is released when Tj < TW_L (hysteresis implemented); when T_j > TSD, L9001 shut down regulators entering a protection mode called SAFE state (see *Section 8.2.5* for details). L9001 goes back to ACTIVE mode when Tj < TW_L.

TWN and WDO are open drain. RSTN1, RSTN2 and ADCMON all have an internal resistive pull-up R_INT_RPU to VDDIO. RSTN1, RSTN2 and ADCMON are driven low level at power-up when WAKE is greater than WAKE_Hth after WPH filter time and are released after their relative output voltages (VR1, VR2 and VADC) have risen above their under voltage thresholds.

VS input pin is monitored and in case one of the following conditions applies the device goes in a protection mode called SAFE state:

- VS > VS_ov_h for a period longer than $t_{FILT_VS_ov}$,
  - L9001 goes back to ACTIVE mode if VS < VS_ov_l for a period longer than $t_{FILT_VS_ov}$
- VS < VS_uv_l for a period longer than $t_{FILT_VS_uv}$,
  - L9001 goes back to ACTIVE mode if VS > VS_uv_h for a period longer than $t_{FILT_VS_uv}$

Internal CP voltage is monitored as well and when CP<CP_uv for a period longer than tFILT_CP_uv L9001 shuts down regulators and enters SAFE state; it goes back to ACTIVE mode if CP>CP_uv for a period longer than tFILT_CP_uv.

L9001 provides a feature, called latch state, that disables the system in case a systematic fault is repetitively detected on CP_uv, watchdog or thermal shutdown events. For detailed description see LATCH mode description in *Section 8.2.6*.

Table 13. Diagnosis parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VR1_uv	VR1 under voltage threshold	CONF3 LOW	2.96	3.05	3.2	V
VR1_uv_2		CONF3 MID	4.49	4.65	4.84	V
VR1_uv_3		CONF3 HIGH	5.38	5.58	5.8	V
VR1_ov	VR1 over voltage threshold	CONF3 LOW	3.4	3.55	3.65	V
VR1_ov_2		CONF3 MID	5.17	5.38	5.54	V
VR1_ov_3		CONF3 HIGH	6.2	6.42	6.64	V
VR2_uv	VR2 under voltage threshold	Measured on FB2 (= 0.8 V nominal value)	0.72	0.74	0.77	V
VR2_ov	VR2 over voltage threshold	Measured on FB2 (= 0.8 V nominal value)	0.83	0.86	0.88	V
VADC_uv	VADC under voltage threshold	CONF1 LOW	3.1	3.17	3.25	V
VADC_uv_1		CONF1 HIGH	4.7	4.8	4.92	V
VADC_ov	VADC over voltage threshold	CONF1 LOW	3.36	3.45	3.57	V
VADC_ov_2		CONF1 HIGH	5.1	5.2	5.35	V
VS_uv_l	Battery under voltage threshold	-	3.5	-	-	V
VS_uv_h		-	-	-	4.2	V
VS_ov_l	Battery over voltage threshold	-	25	-	-	V
VS_ov_h		-	27.5	-	30	V
CP_uv	Charge Pump under voltage threshold	-	VS+2.8	VS+3.1	VS+3.4	V
$t_{FILT_uv_VR1}$	VR1 under-voltage filtering time	Guaranteed by scan	-	200	-	µs
$t_{FILT_uv_VR2}$	VR2 under-voltage filtering time	Guaranteed by scan	-	200	-	µs
$t_{FILT_uv_VADC}$	VADC under-voltage filtering time	Guaranteed by scan	-	200	-	µs
$t_{FILT_ov_VR1}$	VR1 over-voltage filtering time	Guaranteed by scan	-	200	-	µs
$t_{FILT_ov_VR2}$	VR2 over-voltage filtering time	Guaranteed by scan	-	200	-	µs
$t_{FILT_ov_VADC}$	VADC over-voltage filtering time	Guaranteed by scan	-	200	-	µs
$t_{FILT_VS_uv}$	Vs under-voltage filtering time	Guaranteed by scan	-	64	-	µs
$t_{FILT_VS_ov}$	Vs over-voltage filtering time	Guaranteed by scan	-	64	-	µs
$t_{FILT_CP_uv}$	CP under-voltage filtering time	Guaranteed by scan	-	64	-	µs
RSTN1_l	RSTN1 low level	1 mA input current	-	-	1	V
RSTN2_l	RSTN2 low level	1 mA input current	-	-	1	V
ADCMON_l	ADCMON low level	1 mA input current	-	-	1	V
t_{RSTN1_act}	RSTN1 active pulse duration	Guaranteed by scan	-	15	-	ms

Table 13. Diagnosis parameters (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{RSTN2_act}	RSTN2 active pulse duration	Guaranteed by scan	-	15	-	ms
t_{ADCMON_act}	ADCMON active pulse duration	Guaranteed by scan	-	15	-	ms
TWN_I	TWN low level	1 mA input current	-		1	V
T_{W_L}	Thermal warning temperature low threshold	Guaranteed by design	150	-	-	°C
T_{W_H}	Thermal warning temperature high threshold	Guaranteed by design	-	-	165	°C
T_{SD}	Thermal shutdown temperature	Guaranteed by design	180	185	190	°C
$T_{wn_deglitch}$	Thermal warning deglitch time	Guaranteed by scan	-	10	-	µs
R_INT_RPU	Internal resistive VDDIO pull-up resistance on RSTN1, RSTN2, ADCMON pins	-	14K	-	28K	Ω
R_INT_RPD	Internal resistive pull-down resistance on RSTN1, RSTN2, ADCMON pins	-	1.5M	-	3M	Ω

7 Watchdog

The device hosts a watchdog control unit. The µC must trigger the watchdog with a toggle on WDI pin within a configurable time period t_{WDT} (also called normal window) which depends on external capacitance at pin WDT and is specified as t_{WDT}(Cwdt). The feedback of the watchdog control can be checked monitoring output pin WDO.

Accuracy of the window (including internal spread) is shown in the table below with reference to the case a 47 nF cap is mounted:

$$t_{WDT}(Cwdt) = t_{WDT}(47\ nF) * Cwdt/47\ nF$$

As soon as L9001 is in ACTIVE mode and resets of the VDD regulators are high (only the enabled regulators are considered), the watchdog is switched on and opens a long window which is 10 times the normal window. If the watchdog is correctly served before the end of this window, subsequent normal windows are opened as described in *Figure 6*.

In order to serve the watchdog, WDI must toggle from low state to high state. A correct toggle is recognized when high state at WDI lasts as long as t_{WDI_h} and low state as short as t_{WDI_l}; when there is a correct WDI toggle, a WDI internal flag is set. At the end of the timing window t_{WDT}(Cwdt), the flag is checked and if it is set to 1, the system is working properly, the flag is reset to 0 and the cycle goes on. If the flag is still at 0, a watchdog failure is generated. It follows that more than one WDI toggle can occur in the time window.

WDO is an open drain output (low active). In case of watchdog failure the output WDO is driven low for the specified time t_{WDO}; the output WDO will be relased after this time unless the device enters latch mode (see *Section 8.2* and *Figure 6* for details).

Watchdog failure is also counted as failure condition for LATCH mode enter after 4 consecutive failures as explained in *Section 8*.

In software development mode (FLASH mode) watchdog is disabled. This can be done by forcing WDT>WDT_thi. The device can regain Active mode if WDT<WDT_tho; the function is also switched off when entering LOW POWER mode, and is switched on again when re-entering ACTIVE mode (see *Section 8.1* for details)

When WDT pin is connected to a fixed voltage, watchdog functionality is frozen, but regulators still function normally.

Table 14. Watchdog parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{WDT(47nF)}$	Watchdog timer window length reference working point	t_{WDT} with C(WDT) = 47 nF	35	40	45	ms
$t_{WDT_lw(47nF)}$	Watchdog timer long window	t_{WDT_lw} with C(WDT) = 47 nF	350	400	450	ms
t_{WDO}	WDO active pulse duration	-	-	16	-	ms
Cwdt	WDT pin capacitor	Application info	1	47	100	nF
t_{WDI_h}	Minimum high level WDI duration to trigger WD	-	-	50	-	µs
t_{WDI_l}	Minimum low level WDI duration	-	3	-	10	µs
WDI_h	WDI input high level threshold	-	-	-	1.5	V
WDI_l	WDI input low level threshold	-	1.05	-	-	V

Table 14. Watchdog parameters (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
WDO_l	WDO output low level	1 mA input current	-	-	1	V
WDT_thi	WDT threshold to enter FLASH mode	-	-	-	7.4	V
WDT_tho	WDT threshold to exit FLASH mode	-	6.1	-	-	V

This is an example of the functioning of the SPS w.r.t. timings, RST_1, RST_2, WD_EN:

Figure 5. Example of Watchdog functioning

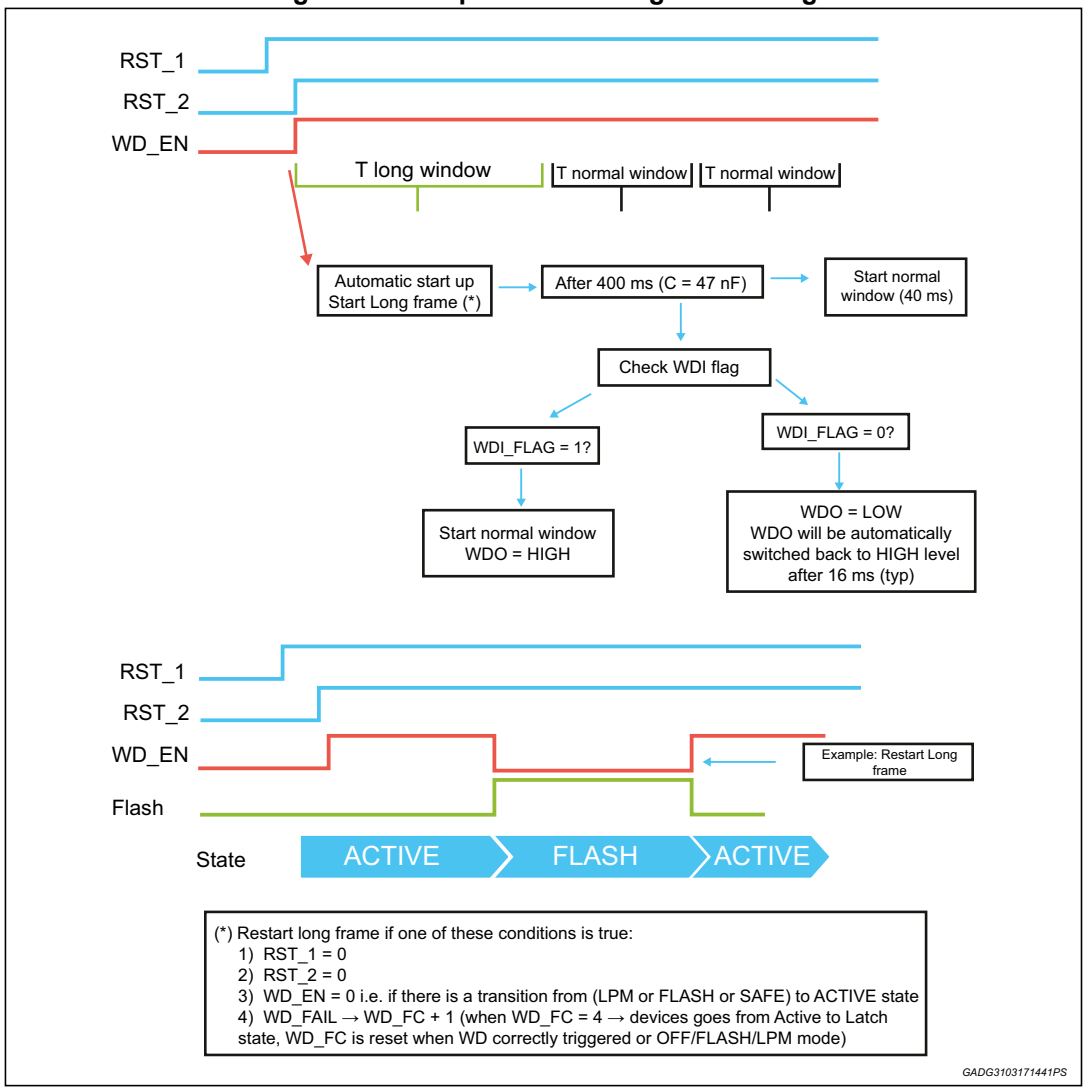
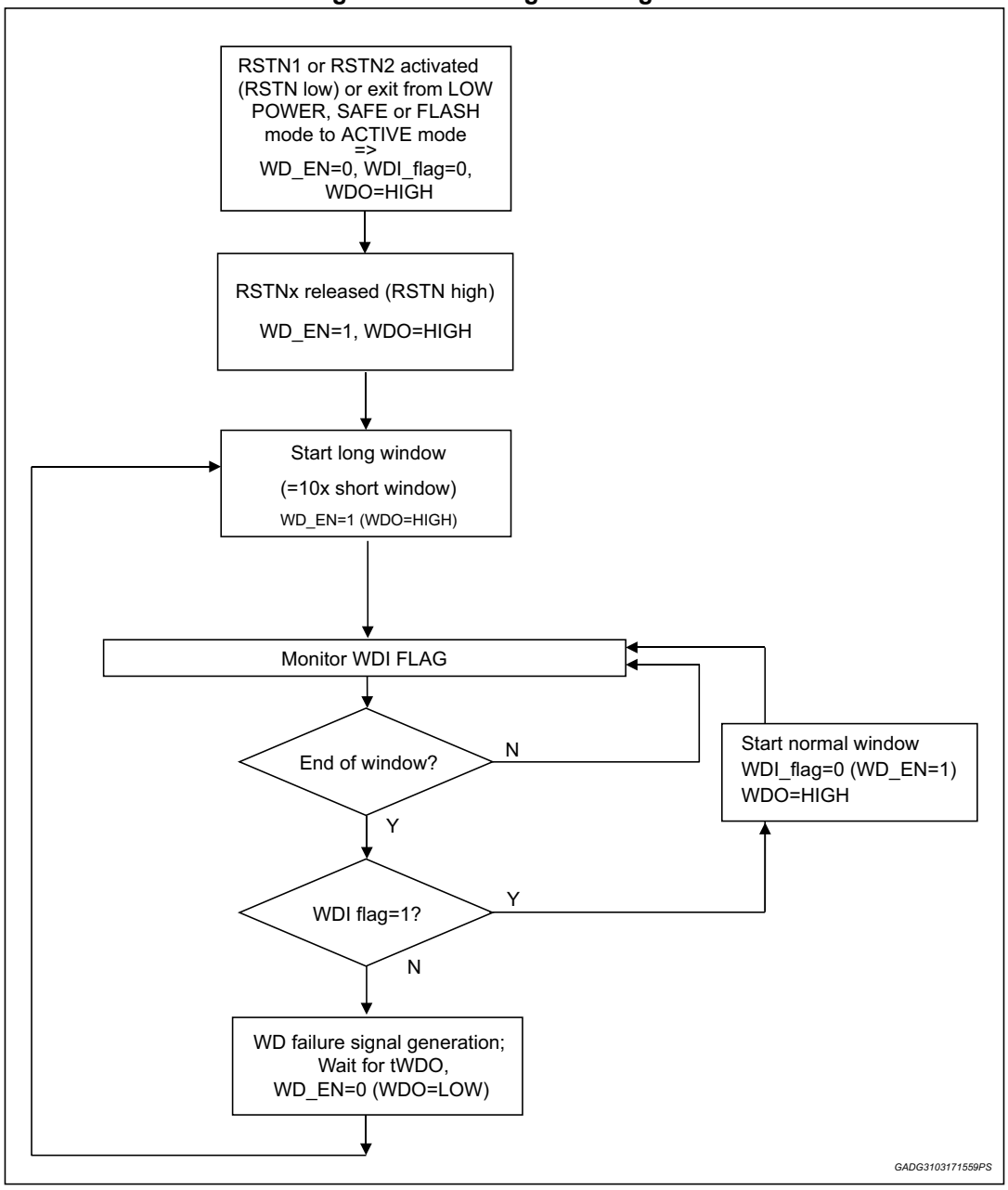


Figure 6. Watchdog flow diagram



8 Operation modes

8.1 Operation modes condition

The device can operate in different modes, depending on the internal or external triggering conditions.

Table 15. Operation modes description

Mode	Description	Operating condition
OFF	Off state	All functions switched off
ACTIVE	Normal operation	All functions available
FLASH	Super-user mode for SW development or FLASH mode (external triggered)	All functions available, WD disabled
LOW POWER	Reduced consumption mode (external triggered)	VDD1 and VDD2 regulators in bypass mode, ADCLDO switched off, WD disabled.
SAFE	Safe state automatically entered in case of failure (over temperature shutdown, VS overvoltage, VS undervoltage, and charge pump undervoltage)	All output voltages are switched off. Monitoring is still active.
LATCH	Latch state automatically entered in case of persistent failures (over temperature, charge pump undervoltage or watchdog)	All output voltages are switched off, all monitoring is switched off.

8.2 Description of the operation modes

A description of the operation modes is given here and a graphical view is depicted in *Figure 7*; additional transitions details are given in and .

8.2.1 OFF mode

OFF mode corresponds to the state when the device is switched off. From OFF mode when VS is greater than 5.5 V and WAKE is high, L9001 moves to ACTIVE mode.

8.2.2 ACTIVE mode

ACTIVE mode corresponds to the normal activity of the device where all functions are available. WAKE is High, VS is inside the operative range and no Failure is detected. When entering ACTIVE mode from OFF or SAFE state, the regulators are powered-up. From this state L9001 can move to LOW POWER state, FLASH state or SAFE state. A table to clarify transitions from and to ACTIVE mode is included in .

8.2.3 FLASH mode

FLASH mode corresponds to a state where a super-user is performing activities like SW development. All functions are available like in ACTIVE mode except the Watchdog, which is switched off. This mode is entered when WDT>WDT_thi. The device regains Active mode if WDT<WDT_tho (see *Section 7* for details)

8.2.4 LOW POWER mode

Low power mode corresponds to a state where the system needs to decrease the overall power consumption with a reduced level of functionality. In this state, ADCLDO is switched off, regulators VDD1 and VDD2 are working in bypass mode and Watchdog, over temperature, regulators over & under voltage are all disabled.

The state can be entered by ACTIVE state by rising STBY pin. Depending on the active VDD regulators (i.e. the regulators which have not been disabled in the application), the low power mode is managed in a different way.

When only VDD1 regulator is enabled and the STBY pin is asserted high, the device goes in LOW POWER mode if VR1 current is lower than ICMP1_l. In this case only the bypass LDO drives the wanted output voltage while the switch mode operation is deactivated. When VR1 current turns higher than ICMP1_h, the device goes back to ACTIVE mode.

When only VDD2 regulator is enabled and the STBY pin is asserted high, the device goes in LOW POWER mode if VR2 current is lower than ICMP2_l. In this case only the bypass LDO drives the wanted output voltage. When VR2 current turns higher than ICMP2_h, the device goes back to ACTIVE mode.

When both regulators are enabled and the STBY pin is asserted high and the total overall current generated by VDD1 regulator is lower than ICMP1_l, the device goes in LOW POWER mode and only the bypass LDOs drive the output voltages while the switch mode operation (or linear mode, depending on the configuration) is deactivated. When the total overall current turns higher than ICMP1_h, the device goes back to ACTIVE mode.

For further details on transitions from and to low power mode please refer to AN5163.

8.2.5 SAFE mode

SAFE mode corresponds to a state that is entered automatically when a fail-safe triggering condition is generated in ACTIVE state. These failure conditions are four: over temperature shutdown, VS overvoltage, VS undervoltage, and charge pump undervoltage. When in SAFE mode, all output regulators and watchdog are switched off, monitoring and charge pump are still active. Exit from SAFE state occurs only if Failure condition disappears.

8.2.6 LATCH mode

LATCH mode corresponds to a state that is entered automatically when the system has persistent failures which are blocking the functionality and so it must be stopped or restarted. Thus the only way out of LATCH state is going to OFF state and then again in ACTIVE, otherwise the system will remain in LATCH state indefinitely.

In LATCH state all output regulators and WD are switched off, monitoring and charge pump are also switched off, and WDO is low.

In particular, the failures that can trigger LATCH state are: over temperature shutdown (OTSD), charge pump undervoltage (CP_UV) and watchdog fail.

The IC has two separate failure counters:

- WD_FC which counts fails on watchdog;
- FC which counts fails on OTSD and CP_UV.

Each time a failure is detected, the correspondent failure counter is incremented; LATCH mode occurs when either the FC failure counter or the WD_FC has reached a threshold of 4 failures.

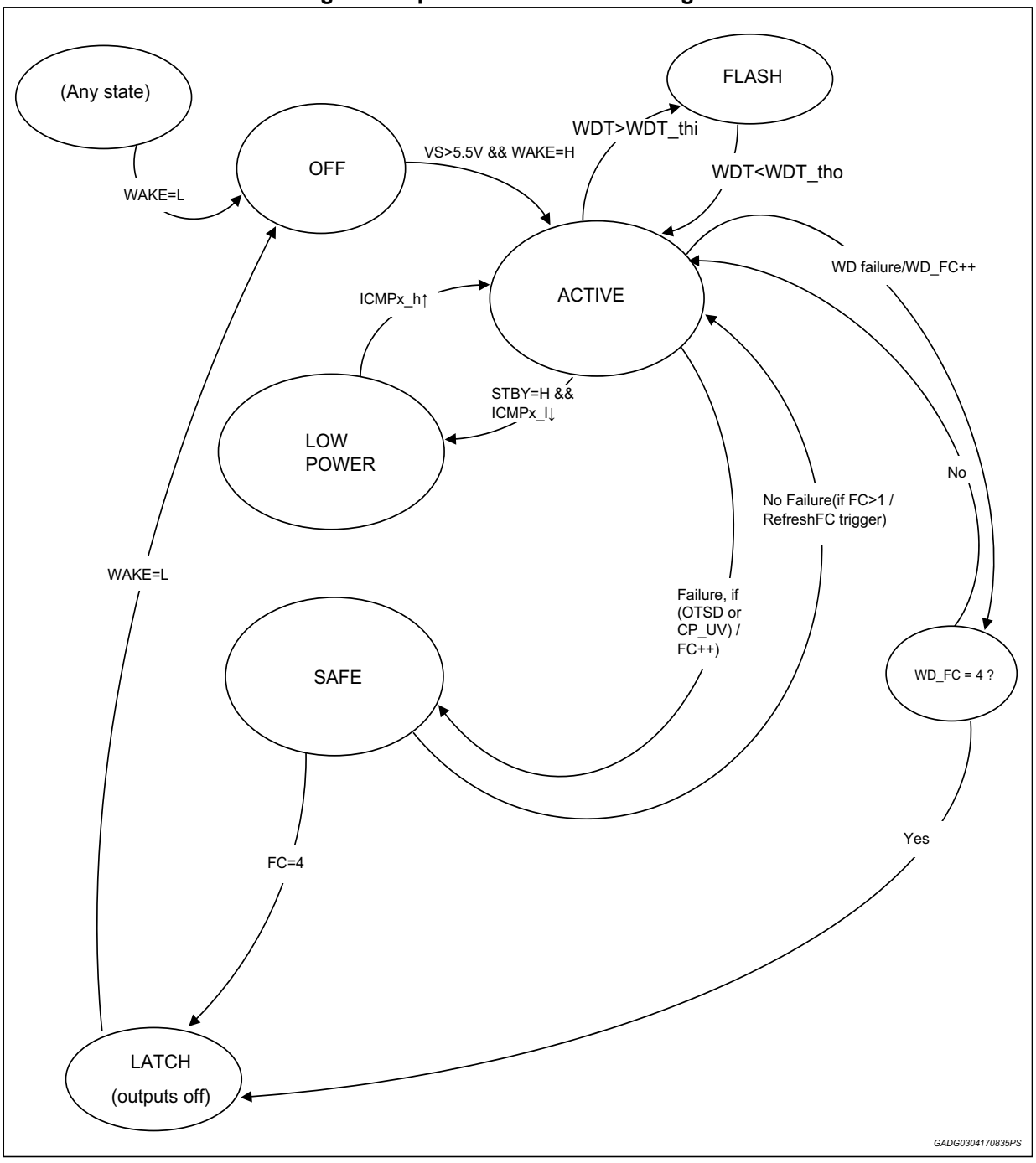
When a watchdog failure is generated by the watchdog unit (see *Section 7* for details) the counter WD_FC is incremented by 1. WD_FC is reset if the watchdog is correctly served or when the device is in OFF or FLASH or LOW POWER mode. It means that if there are 4 consecutive watchdog failures, WD_FC reaches a value of 4 and as a consequence the system goes in LATCH mode.

While for WD_FC the failures must be consecutive to trigger LATCH state, for OTSD or CP_UV fails, a so called Refresh failure counter is implemented to filter out sporadic / not persistent failures triggering FC counter.

When OTSD or CP_UV fails are detected, L9001 enters SAFE state (see *Section 6* for details) and FC counter is incremented. Once the Failure condition disappears the system goes back to ACTIVE state, the power-up sequence for each regulator is launched, and Refresh Failure counter is started. If a FC trigger condition is detected again within 100 ms (30 s if previous failure was OTSD), the system goes again in SAFE state and FC counter is again incremented. Otherwise, if no Failure is detected in ACTIVE state within 100 ms (30 s if previous failure was OTSD), the FC counter is reset.

A table to clarify transitions from and to SAFE mode and the refresh failure counter is also included in .

Figure 7. Operation modes state diagram



8.2.7 Operation modes parameters

Table 16. Consumption parameters

Symbol	Parameter	Description	Min.	Typ.	Max.	Unit
I_LPM	Low-power mode consumption	Current consumption when in LOW POWER mode (considering both regulators enabled, internal device only consumption and excluding external load currents)	100	-	150	µA
I_QC	Quiescent current of VS	Device switched off (WAKE = L)	-	-	10	µA

Table 17. STBY pin parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
STBY_Hth	STBY pin threshold to enter LOW POWER mode (STBY = H)	-	1.3	1.43	1.55	V
STBY_Lth	STBY pin threshold to exit LOW POWER mode (STBY = L)	-	0.95	1.08	1.2	V
STBY_PD	STBY pull down current	STBY = 5 V	-	55	80	µA

Table 18. Charge pump capacitors

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{cp}	CP output capacitor	-	-	220	-	nF
C_{cp2}	CP switching capacitor	-	-	68	-	nF

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

9.1 PowerSSO-24 (exposed pad) package information

Figure 8. PowerSSO-24 (exposed pad) package outline

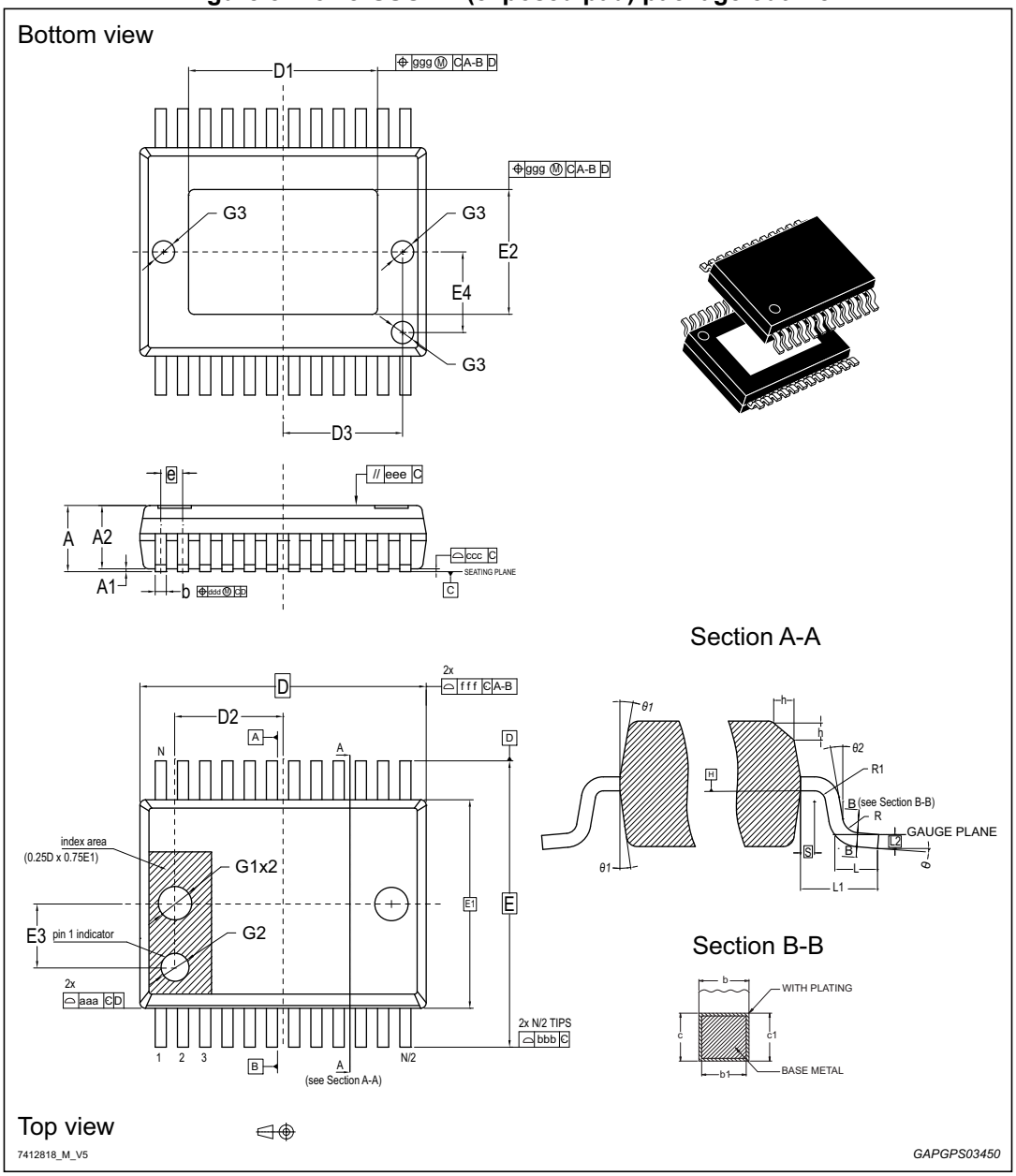


Table 19. PowerSSO-24 (exposed pad) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	0°	-	8°	0°	-	8°
Θ1	5°	-	10°	5°	-	10°
Θ2	0°	-	-	0°	-	-
A	-	-	2.45	-		0.0965
A1	0.0	-	0.1	0.0		0.0039
A2	2.15	-	2.35	0.0846		0.0925
b	0.33	-	0.51	0.013		0.0201
b1	0.28	0.40	0.48	0.011	0.0157	0.0189
c	0.23	-	0.32	0.0091		0.0126
c1	0.20	0.20	0.30	0.0079	0.0079	0.0118
D[2]	10.30 BSC			0.4055 BSC		
D1	VARIATION					
D2	-	3.65	-	-	0.1437	-
D3	-	4.30	-	-	0.1693	-
e	0.80 BSC			0.0315 BSC		
E	10.30 BSC			0.4055 BSC		
E1[2]	7.50 BSC			0.2953 BSC		
E2	VARIATION					
E3	-	2.30	-	-	0.0906	-
E4	-	2.90	-	-	0.1142	-
G1	-	1.20	-	-	0.0472	-
G2	-	1.0	-	-	0.0394	-
G3	-	0.80	-	-	0.0315	-
h	0.30	-	0.40	0.0118	-	0.0157
L	0.55	0.70	0.85	0.0217	-	0.0335
L1	1.40 REF			0.0551 REF		
L2	0.25 BSC			0.0098 BSC		
N	24 (# lead)					
R	0.30	-	-	0.0118	-	-
R1	0.20	-	-	0.0079	-	-
S	0.25	-	-	0.0098	-	-

Table 19. PowerSSO-24 (exposed pad) package mechanical data (continued)

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Tolerance of form and position						
aaa		0.20			0.0079	
bbb		0.20			0.0079	
ccc		0.10			0.0039	
ddd		0.20			0.0079	
eee		0.10			0.0039	
ffff		0.20			0.0079	
ggg		0.15			0.0059	
VARIATIONS						
Option A						
D1	6.5	-	7.1	0.2559	-	0.2795
E2	4.1	-	4.7	0.1614	-	0.1850
Option B						
D1	4.9	-	5.5	0.1929	-	0.2165
E2	4.1	-	4.7	0.1614	-	0.1850

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is ‘0.25 mm’ per side D and ‘0.15 mm’ per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.

Appendix A

The following table summarizes what happens if a fault condition is detected in ACTIVE state indicating the next state and the behavior of FC, Refresh FC counter and thresholds.

Table 20. Clarify transitions from and to ACTIVE mode

Fail / Current status	ACTIVE (no overtemperature & no CP undervoltage)	ACTIVE (after overtemperature fault)	ACTIVE (after CP undervoltage fault)	ACTIVE (after overtemperature & CP undervoltage)
VS undervoltage	– SAFE state – FC = FC – Refresh FC threshold = default (30 s) – Refresh FC is not triggered when device comes back in ACTIVE	– SAFE state – FC = FC – Refresh FC threshold = 30 s – Refresh FC restart from 0 when device comes back in ACTIVE	– SAFE state – FC = FC – Refresh FC threshold = 100 ms – Refresh FC restart from 0 when device comes back in ACTIVE	– SAFE state – FC = FC – Refresh FC threshold = 30 s – Refresh FC restart from 0 when device comes back in ACTIVE
Overtemperature	– SAFE state – FC = FC+1 – Refresh FC threshold = 30 s – Refresh FC is triggered when device comes back in ACTIVE	– FC = FC+1 →SAFE state if FC < 4 – FC = FC+1 →SAFE state and the next clk cycle Latch state if FC = 4 – Refresh FC threshold = 30 s – Refresh FC restart from 0 if device comes back in ACTIVE	– FC = FC+1 →SAFE state if FC < 4 – FC = FC+1 →SAFE state and the next clk cycle Latch state if FC = 4 – Refresh FC threshold replaced from 100 ms to 30 s – Refresh FC restart from 0 if device comes back in ACTIVE	– FC = FC+1 →SAFE state if FC < 4 – FC = FC+1 →SAFE state and the next clk cycle Latch state if FC = 4 – Refresh FC threshold = 30 s – Refresh FC restart from 0 if device comes back in ACTIVE
CP undervoltage	– SAFE state – FC = FC+1 – Refresh FC threshold = 100 ms – Refresh FC is triggered when device comes back in ACTIVE	– FC = FC+1 →SAFE state if FC < 4 – FC = FC+1 →SAFE state and the next clk cycle Latch state if FC = 4 – Refresh FC threshold = 30 s – Refresh FC restart from 0 if device comes back in ACTIVE	– FC = FC+1 →SAFE state if FC < 4 – FC = FC+1 →SAFE state and the – next clk cycle Latch state if FC = 4 – Refresh FC threshold = 100 ms – Refresh FC restart from 0 if device comes back in ACTIVE	– FC = FC+1 →SAFE state if FC < 4 – FC = FC+1 →SAFE state and the next clk cycle Latch state if FC = 4 – Refresh FC threshold = 30 s – Refresh FC restart from 0 if device comes back in ACTIVE

Appendix B

The following table summarizes what happens if a fault condition is detected in SAFE state indicating the next state and the behavior of FC, Refresh FC counter and thresholds.

Table 21. Clarify transitions from and to SAFE mode

Fail / Current status	SAFE due to VS undervoltage	SAFE due to Overtemperature	SAFE due to CP undervoltage
VS undervoltage	–	– SAFE state – FC = FC – Refresh FC threshold = 30 s – Refresh FC restart from 0 when device comes back in ACTIVE	– SAFE state – FC = FC – Refresh FC threshold = 100 ms – Refresh FC restart from 0 when device comes back in ACTIVE
Overtemperature	– FC= FC+1 → SAFE state if FC < 4 – FC = FC+1 → Latch state if FC = 4 – Refresh FC threshold = 30 s – Refresh FC restart from 0 if device comes back in ACTIVE	–	– SAFE state – FC = FC (it is already incremented one time) – Refresh FC threshold = 30 s – Refresh FC restart from 0 when device comes back in ACTIVE
CP undervoltage	– FC= FC+1 → SAFE state if FC < 4 – FC= FC+1 →Latch state if FC = 4 – Refresh FC threshold = 100 ms – Refresh FC restart from 0 if device comes back in ACTIVE	– SAFE state – FC = FC (it is already incremented one time) – Refresh FC threshold = 30 s – Refresh FC restart from 0 when device comes back in ACTIVE	–

Revision history

Table 22. Document revision history

Date	Revision	Changes
13-Dec-2017	1	Initial release.
24-Jan-2019	2	Updated: – Title in cover page; – *Table 5: Supply voltage range on page 13*; – *Table 9: VDD1 regulator parameters on page 15*; – *Table 10: VDD2 regulator parameters on page 17*; – *Section 8.2.4: LOW POWER mode on page 28*.

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