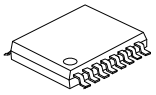
L8200 *LINEAR INTEGRATED CIRCUIT*

SINGLE LNB-BIAS, CONTROL AND POWER MANAGEMENT SOLUTION



TSSOP-16

QFN-16(3x3)

■ DESCRIPTION

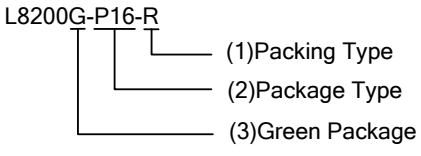
The UTC **L8200** is a single chip power management and control solution for LNB's. The highly integrated solution provides all the required FET and mixer bias, control detection and decoding, local oscillator switching and a stable power supply for the IF amplifier, and additional support functions. Packaged in a small 16 pin QFN package or 16 pin TSSOP package the UTC **L8200** only requires 3 external components providing a very small compact solution. Being at the heart of the LNB monitoring the control, power management and environmental conditions the UTC **L8200** is able to provide reliable solution eliminating effects such as false switching and over loading.

■ FEATURES

* Single chip LNB bias, control and power management
* Integrated regulated supply for LNB
* Zero Gate FET switching
* Voltage detection for polarization switching
* 22kHz tone detector with signal rejection for band switching
* Programmable mixer and FET bias

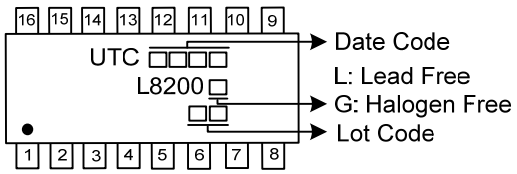
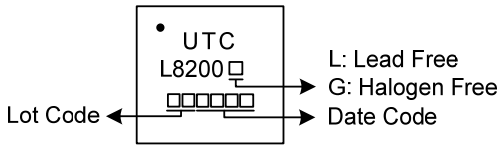
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
L8200L-P16-R	L8200G-P16-R	TSSOP-16	Tape Reel
L8200L-Q16-3030-R	L8200G-Q16-3030-R	QFN-16(3×3)	Tape Reel

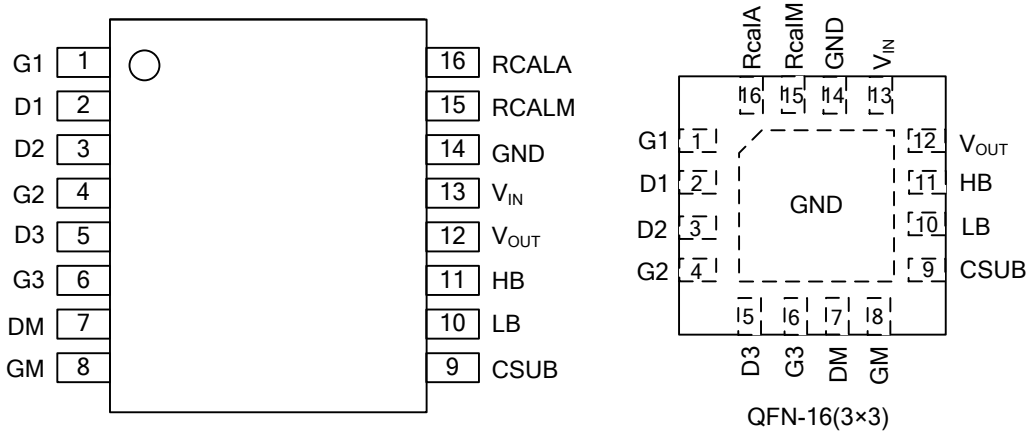


(1) R: Tape Reel
(2) P16: TSSOP-16, Q16-3030: QFN-16(3×3)
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

TSSOP-16	QFN-16(3×3)
	

■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin No.		PIN NAME	DESCRIPTION
TSSOP-16	QFN-16(3×3)		
1	1	G1	To G of fet 1
2	2	D1	To D of fet 1
3	3	D2	To D of fet 2
4	4	G2	To G of fet 2
5	5	D3	To D of fet 3
6	6	G3	To G of fet 3
7	7	DM	To Drain of mix fet
8	8	GM	To Gate of mix fet
9	9	CSUB	connect an external cap to produce -2.5V
10	10	LB	To LB OSC.
11	11	HB	To HB OSC.
12	12	V_{OUT}	5V voltage output terminal
13	13	V_{IN}	Power supply（include both voltage and tone signal）
14	14	GND	GND
15	15	RCALM	Connect 22kohm to set Idm to 10mA
16	16	RCALA	Connect 22kohm to set Id1, Id2, Id3 to 10mA

■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{IN}	-0.6 ~ 25 continuous	V
Supply Current		I_{IN}	120	mA
Power Dissipation	TSSOP-16	P_D	1.3	W
	QFN-16(3×3)		2	W
Operating Temperature Range		T_{OPR}	-40 ~ +85	°C
Storage Temperature Range		T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

Measured at T_A=25°C, V_{IN}=13V, R_{CALA}=R_{CALM}=22kΩ(setting Ids to 10 mA) unless otherwise specified.

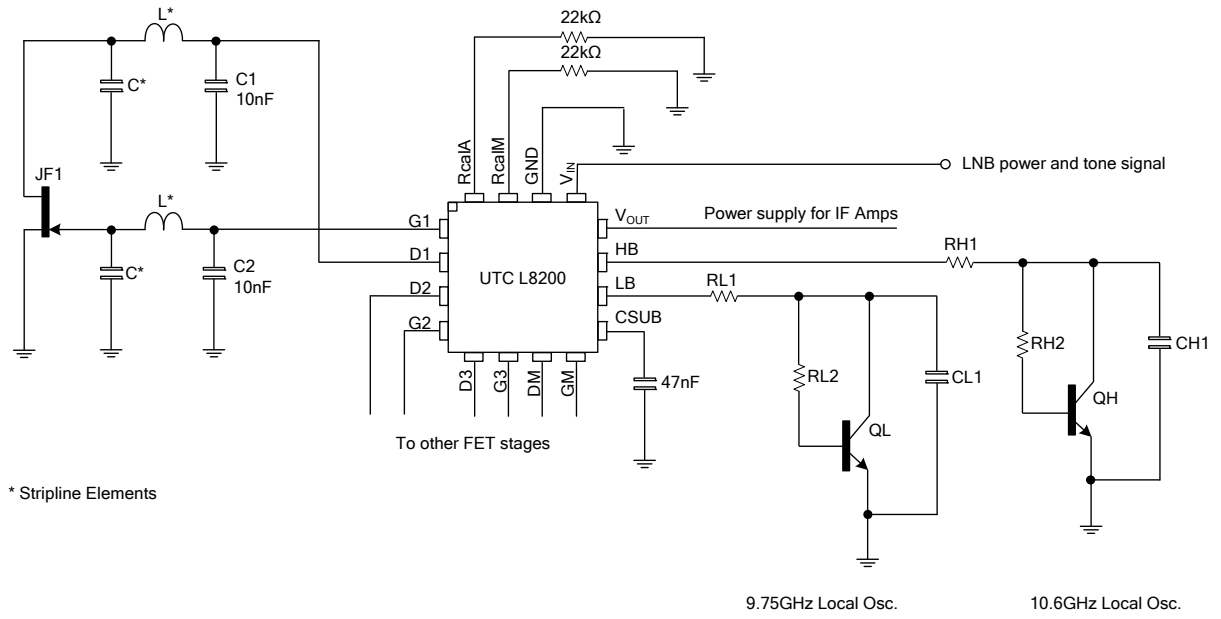
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage Operating Range	V_{IN}		8		22	V
Supply Current						
No Load Supply Current (Note 1)	I_{CC}	I_{D1}=I_{D2}=I_{DM}=0mA		2	3	mA
Max Total Load Current		QFN-16(3×3)			80	mA
Max Bias Load Current (Note 2)		I_{D1} or I_{D2}+ I_{D3}+I_{DM}			40	mA
Max Osc Load Current (Note 2)		LB or HB			50	mA
Max Iout Load Current (Note 2)					50	mA
V_{OUT}	V_{OUT}	V_{IN}=10.5V~21V, I_{OUT}=30mA	4.75	5	5.25	V
Substrate Voltage	V_{SUB}	(Internally generated) I_{SUB}=0mA	-3.0	-2.5	-2.0	V
		I_{SUB}=-20uA			-2.0	V
V_{POL} Threshold	V_{POL}	Applied via V_{IN} pin	14.1	14.7	15.4	V
Pol Switching Speed	T_{POL}	$V_{IN\ Low}$=13V, $V_{IN\ High}$=18V			1	ms
Output Noise						
Drain Voltage		$C_{GATE-GND}$ =4.7nF $C_{DRAIN-GND}$ =10nF			0.02	Vpk-pk
Gate Voltage		$IC_{GATE-GND}$ =4.7nF $C_{DRAIN-GND}$ =10nF			0.005	Vpk-pk
Tone Detector						
Tdetect Threshold	V_{TONE}	Test Circuit 1	100	170	300	mV
Rejection Freq (Note 3)		Test Circuit 1, V(AC)I_N=1Vp/p sq.w.	1.0	7.5		kHz
LO Output Stage						
LB V_{OUT} Low	V_{LB}	II=0, Test Circuit 1 Tone enabled	-0.05	0	0.05	V
LB V_{OUT} High		II=50mA, Test Circuit 1 Tone enabled	4.5	5.0	5.25	V
HB V_{OUT} Low	V_{HB}	II=0, Test Circuit 1 Tone enabled	-0.05	0	0.05	V
HB V_{OUT} High		II=50mA, Test Circuit 1 Tone enabled	4.5	5.0	5.25	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gate Characteristics						
G1 Output						
Voltage Off	V_{G1O}	I_{D1}=0, V_{IN}=14V, I_{G1}=0	-0.05	0	0.05	V
Voltage Low	V_{G1L}	V_{IN}=15.5V, I_{D1}≤12mA, I_{G1}=-10uA	-3.0	-2.5	-2.0	V
Voltage High	V_{G1H}	V_{IN}=15.5V, I_{D1}≥8mA, I_{G1}=0	0.35	0.5	1.0	V
G2 Output						
Voltage Off	V_{G2O}	V_{IN} =15.5V, I_{D2}=0, I_{G2}=0	-0.05	0	0.05	V
Voltage Low	V_{G2L}	V_{IN}=14V, I_{D2}≤12mA, I_{G2}=-10uA	-3.0	-2.5	-2.0	V
Voltage High	V_{G2H}	V_{IN}=14V, I_{D2}≥8mA, I_{G2}=0	0.35	0.5	1.0	V
G3/Gm Output						
Voltage Low	V_{G3L}/V_{GmL}	I_{D3}/m≤12mA, I_{G3}/m=-10uA	-3.0	-2.5	-2.0	V
Voltage High	V_{G3H}/V_{GmH}	I_{D3}/m≥8mA,I_{G3}/m=0	0.35	0.5	1.0	V
Drain Characteristics						
D1 Output						
Voltage High	V_{D1}	V_{IN}=15.5V, I_{D1}=10mA	1.8	2.0	2.2	V
Leakage Current	I_{LEAK1}	V_{IN}=14V, V_{D1}=0.5			10	uA
D2 Output						
Voltage High	V_{D2}	V_{IN}=14V, I_{D2}=10mA	1.8	2.0	2.2	V
Leakage Current	I_{LEAK2}	V_{IN}=15.5V, V_{D2}=0.5			10	uA
D3 Output						
Voltage High	V_{D3}	V_{IN}=15.5V, I_{D3}=10mA	1.8	2.0	2.2	V
Dm Output						
Voltage High	V_{DM}	I_{DM}=10mA	0.5	0.6	0.7	V
D1, 2, 3 and M						
Delta V_D vs. V_{IN}	ΔV_{DV}	V_{IN}=9~21V		0.5		%/V
Delta V_D vs. T_J	ΔV_{DT}	T_J= -40 ~ +85°C		50		ppm
FET Current Range		I_{D1}, I_{D2} & I_{D3}	0		15	mA
Mixer Current Range		I_{DM}	0		10	mA
Drain Current	I_D	I_{D1}, I_{D2}, I_{D3} & I_{DM}, R_{CALA} & R_{CALM}=22kΩ	8	10	12	mA
Delta I_D vs. V_{CC}	ΔI_{DV}	V_{CC}=9~21V		0.5		%/V
Delta I_D vs. T_J	ΔI_{DT}	T_J=-40~+85°C		0.05		%/°C

Notes: 1. These parameters are related to R_{CAL} values.
2. The total combined load currents should not exceed the stated maximum load current.
3. The UTC **L8200** series will also reject DiSEqC and other common switching tone bursts.

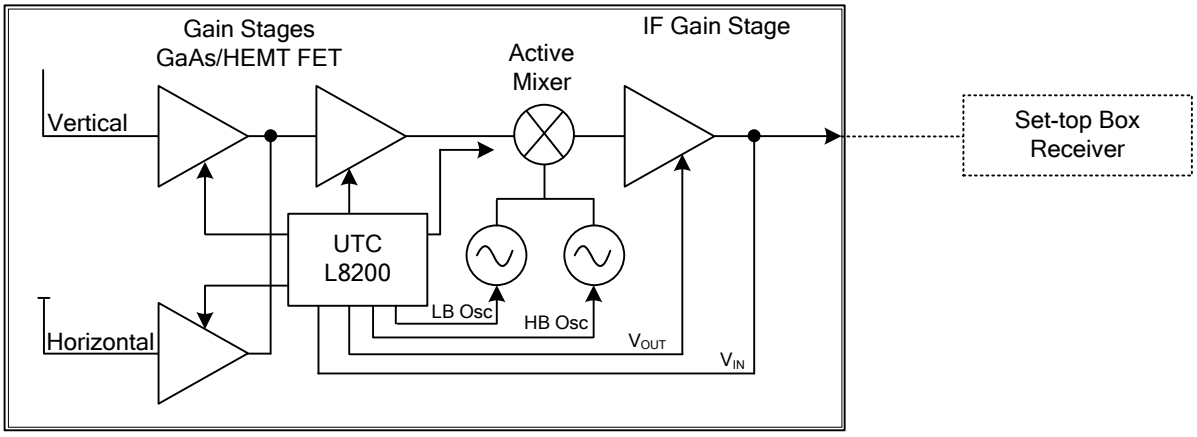
■ TYPICAL APPLICATION CIRCUIT



Capacitors C1 and C2 ensure that residual power supply and substrate generator noise is not allowed to affect other external circuits which may be sensitive to RF interference. They also serve to suppress any potential RF feed through between stages via the UTC **L8200**. These capacitors are required for all stages used. Values of 10nF and 4.7nF respectively are recommended however this is design dependent and any value between 1nF and 100nF could be used. The capacitor CSUB is an integral part of the UTC **L8200** 's negative supply generator. The negative bias voltage is generated on-chip using an internal oscillator. The required value of capacitor CSUB is 47nF. This generator produces a low current supply of approximately -3V. Although this generator is intended purely to bias the external FETs, it can be used to power other external low current circuits via the CSUB pin. Resistor R_{CALA} sets the drain current at which all external amplifier FETs are operated and R_{CALM} sets the mixer bias current. If any bias control circuit is not required, its related drain and gate connections may be left open circuit without affecting the operation of the remaining bias circuits. The UTC **L8200** have been designed to protect the external FETs form adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range -3.0V~1V under any conditions, including power up and power down transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current. UTC **L8200** incorporates over and under voltage protection so is the receiver or installation develops a fault the LNB will shut down and restart once operating conditions are back to normal.

■ SINGLE UNIVERSAL BLOCK DIAGRAM

The following block diagram below shows the main elements of a single universal LNB. A single chip solution provides all the FET and mixer bias, control signal detect for polarization and band selection and all the necessary power management functions required within a single universal LNB.



Polarization and band switching on the UTC **L8200** uses the standard 13~17V and 22kHz as defined by Astra. The exception is that the devices voltage detector has a much tighter tolerance than required to increase field reliability.

The single V_{IN} pin is used internally for three functions, LNB and IC power supply, voltage detection and tone detection. The IC's is self powering via an internal regulator which utilizes the 13~17V control voltage from the satellite receiver. The regulated voltage is used to supply the IC and is also outputted to the V_{OUT} pin to provide the power supply for the remaining element of the LNB such as the IF amplifiers. The 13~17V from the receiver is feed via a tight tolerance voltage detector with integrated filtering which removes unwanted signals or interference. The results from the detectors output enables one of 2 bias circuits to turn one of either Fet1 or FET2 on. The internal tone detector allows the device to detect the 22kHz tone which is superimposed on the LNB power line (13~17V signal), this is achieved with no external filtering components. The tone detector rejects all unwanted signals including transients from other parts of the LNB system. The tone detector controls a drive circuits which powers and one of two oscillators, normally used to switch between low and high band in universal applications. The functional table below shows the operation of the FET and Mixer bias, oscillator output and the LNB power supply.

■ FUNCTION TABLE

INPUTS		OUTPUTS						
V_{IN} (V)	FIN (kHZ)	FET1	FET2	FET3	MIXER	LB(V)	HB(V)	V_{OUT} (V)
<14.1	0	Disabled	Active	Active	Active	5.0	0	5.0
>15.4	0	Active	Disabled	Active	Active	5.0		5.0
<14.1	22	Disabled	Active	Active	Active	0	5.0	5.0
>15.4	22	Active	Disabled	Active	Active	0	5.0	5.0