# L7585G Full-Feature, Low-Power SLIC and Switch

## Features

- Low active power
- Quiet tip/ring polarity reversal
- Distortion-free on-hook transmission
- 35 V to 60 V power supply operation
- 14 operating states:
  - — Forward battery active
  - — Reverse battery active
  - — Ground start (3)
  - — Forward battery ring open
  - — Reverse battery ring open
  - — Reverse battery tip open
  - — High impedance
  - — Ringing (2)
  - — Low current (2)
  - — Disconnect
- Self-test in all operating states
- Independent, adjustable ac and dc parameters:
  - — Switchhook detector threshold
  - — Loop current limit
  - — dc feed resistance
  - — Termination impedance
- Integrated ringing access relay
- Integrated test-in relay
- Integrated relay driver
- Integrated ring trip detector
- Thermal protection
- 44-pin, metric quad flat package (MQFP)

## Description

The L7585G Full-Feature, Low-Power Subscriber Loop Interface Circuit (SLIC) and Switch integrates the battery feed, test access relay, and ringing relay that are necessary to interface a codec to the tip and ring of a subscriber loop into one low-power, low-cost package. It is built using a 90 V complementary bipolar (CBIC) process and a 320 V Bipolar-CMOS-DMOS (BCDMOS) process. The device is available in a 44-pin MQFP package.

The device can be connected directly to the Agere Systems Inc. T8531/T8536 16-Channel Programmable Codec Chip Set without the need for any ac interface components.

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## Architectural Diagram

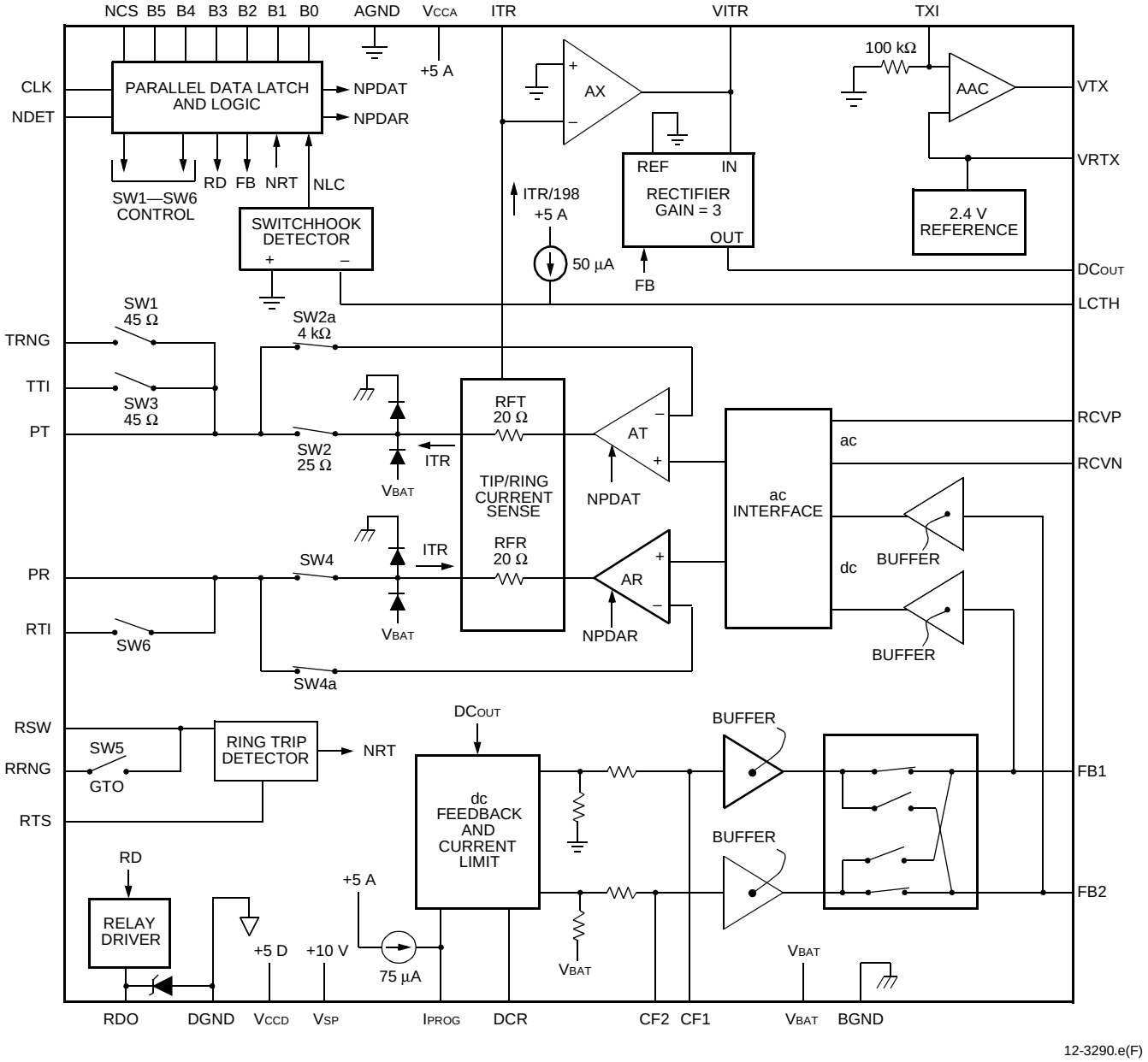


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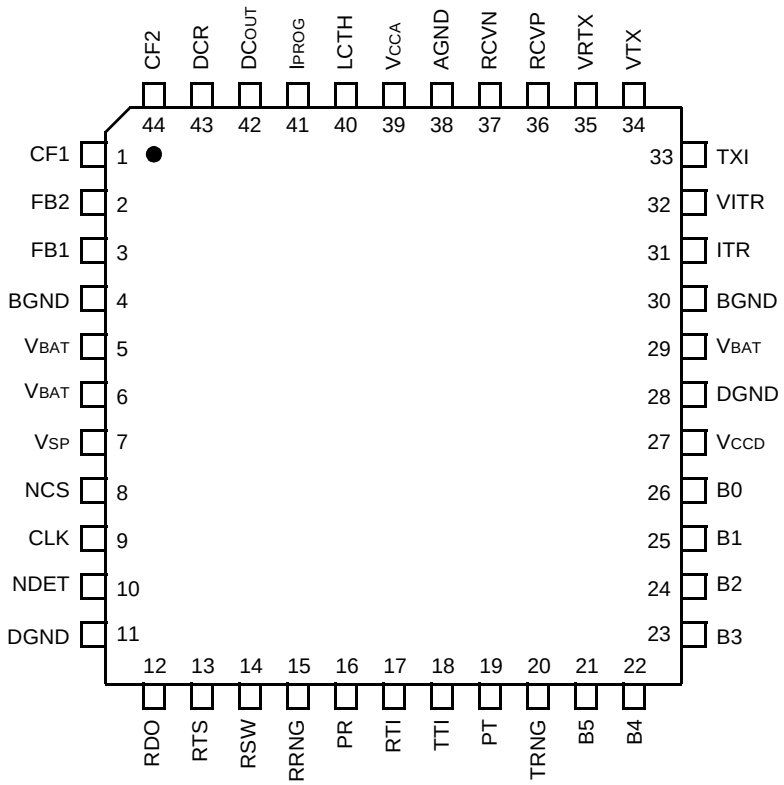
**Figure 1. Architectural Diagram**

## Pin Information




12-2571H (F)

**Figure 2. 44-Pin Diagram (MQFP)**

## Pin Information (continued)

**Table 1. Pin Descriptions**

| Pin | Symbol | Type | Name/Function |
|---|---|---|---|
| 1 | CF1 | I/O | **Filter Capacitor 1.** Connect a 0.22 µF, 100 V capacitor from this pin to pin CF2. |
| 2 | FB2 | I | **Forward Battery Slowdown 2.** A capacitor from FB1 to AGND and from FB2 to AGND will ramp the polarity reversal transition when quiet polarity reversal is required. If not needed, the pin can be left open. |
| 3 | FB1 | I | **Forward Battery Slowdown 1.** A capacitor from FB1 to AGND and from FB2 to AGND will ramp the polarity reversal transition when quiet polarity reversal is required. If not needed, the pin can be left open. |
| 4 | BGND | — | **Battery Ground.** Ground return for the battery ($V_{BAT}$) supply. |
| 5 | $V_{BAT}$ | — | **Battery Supply.** Negative high-voltage power supply. |
| 6 | $V_{BAT}$ | — | **Battery Supply.** Negative high-voltage power supply. |
| 7 | $V_{SP}$ | — | **+10 V Supply.** +10 V bias supply for switch circuitry. |
| 8 | NCS | I | **Not Channel Select.** A low-to-high transition on this logic input stores the data on pins B0—B5 into the input latches on the SLIC. When NCS is either high or low, the SLIC is unaffected by data on pins B0—B5. |
| 9 | CLK | I | **Clock.** Clock input. |
| 10 | NDET | O | **Not Detect.** When low, this logic output indicates either a ring trip or an off-hook condition, depending on the input state of the SLIC. If either the BCDMOS portion or CBIC portion of this device enters thermal shutdown, NDET will be forced low. |
| 11 | DGND | — | **Digital Ground.** Ground return for $V_{CCD}$ and relay driver flyback current. |
| 12 | RDO | O | **Relay Driver.** This output drives an external relay. RDO is low (relay operated) when a low input on B5 is latched into the SLIC. |
| 13 | RTS | I | **Ring Trip Sense.** Sense input for the ring trip detector. |
| 14 | RSW | O | **Ring Lead Ringing Access Switch.** Ringing relay connects this pin to pin RRNG. Connect this pin to pin PR through a 500 Ω current-limiting resistor. |
| 15 | RRNG | I | **Ring Lead Ringing Supply.** Connect this pin to the ringing supply. |
| 16 | PR | I/O | **Protected Ring.** The output of the ring driver and input to the transmit current sense circuit. Connect to the ring of the loop through overvoltage protection. |
| 17 | RTI | I | **Ring Lead Test-In.** Test-in relay connects this pin to PR. Connect RTI to the ring lead of the test-in bus. |
| 18 | TTI | I | **Tip Lead Test-In.** Test-in relay connects this pin to PT. Connect TTI to the tip lead of the test-in bus. |
| 19 | PT | I/O | **Protected Tip.** The output of the tip driver and input to the transmit current sense circuit. Connect to the tip of the loop through overvoltage protection. |
| 20 | TRNG | O | **Tip Lead Ringing Supply.** Ringing relay connects this pin to PT. Connect TRNG to the ringing supply return. |
| 21 | B5 | I | **Bit 5.** B0—B5 determine the state of the SLIC. See Operating States. |

Note: On the printed-wiring board (PWB), make the leads to BGND and $V_{BAT}$ as wide as possible for thermal and electrical reasons. Also, maximize the amount of PWB copper on all leads connected to this device for the lowest operating temperature.

## Pin Information (continued)

**Table 1. Pin Descriptions** (continued)

| Pin | Symbol | Type | Name/Function |
|---|---|---|---|
| 22 | B4 | I | **Bit 4.** B0—B5 determine the state of the SLIC. See Operating States. |
| 23 | B3 | I | **Bit 3.** B0—B5 determine the state of the SLIC. See Operating States. |
| 24 | B2 | I | **Bit 2.** B0—B5 determine the state of the SLIC. See Operating States. |
| 25 | B1 | I | **Bit 1.** B0—B5 determine the state of the SLIC. See Operating States. |
| 26 | B0 | I | **Bit 0.** B0—B5 determine the state of the SLIC. See Operating States. |
| 27 | $V_{CCD}$ | — | **+5 V Digital dc Supply.** +5 V supply for logic and switch circuitry. |
| 28 | DGND | — | **Digital Ground.** Ground return for $V_{CCD}$. |
| 29 | $V_{BAT}$ | — | **Battery Supply.** Negative high-voltage power supply. |
| 30 | BGND | — | **Battery Ground.** Ground return for the battery ($V_{BAT}$) supply. |
| 31 | ITR | I | **Tip/Ring Current.** A current output which is proportional to the differential current flowing from tip to ring. Connect a resistor from this pin to VITR. |
| 32 | VITR | O | **Tip/Ring Voltage Output.** The voltage at this output is directly proportional to the differential tip/ring current. A resistor from this pin to ITR sets the gain. |
| 33 | TXI | I | **Transmit ac Input.** Connect a 0.1 µF capacitor from this pin to VITR. |
| 34 | VTX | O | **Transmit ac Output Voltage.** The ac voltage at this output is 7.2 times the ac voltage at pin TXI. The dc voltage is equal to the dc voltage on pin VRTX. |
| 35 | VRTX | O | **Transmit ac Reference Voltage.** The dc voltage at this output (2.4 V nominal) is the dc reference for the transmit signal output VTX. |
| 36 | RCVP | I | **Receive ac Signal Input (Noninverting).** This high-impedance input controls the ac differential voltage on tip and ring. |
| 37 | RCVN | I | **Receive ac Signal Input (Inverting).** This high-impedance input controls the ac differential voltage on tip and ring. |
| 38 | AGND | — | **Analog Ground.** Ground return for $V_{CCA}$. |
| 39 | $V_{CCA}$ | — | **+5 V Analog dc Supply.** +5 V supply for analog circuitry. |
| 40 | LCTH | I | **Loop Closure Threshold Input.** Connect a resistor to $DC_{OUT}$ to set the off-hook threshold. |
| 41 | $I_{PROG}$ | I | **Current-Limit Program Input.** A resistor to $DC_{OUT}$ sets the dc current limit. |
| 42 | $DC_{OUT}$ | O | **dc Output.** This output is a voltage that is directly proportional to the differential tip/ring current. |
| 43 | DCR | I | **dc Resistance.** Ground for dc feed resistance of 180 Ω, or short to $DC_{OUT}$ for 600 Ω. Intermediate values can be set with a resistor divider from $DC_{OUT}$ to ground, the tap of which is connected to DCR. |
| 44 | CF2 | I/O | **Filter Capacitor 2.** Connect a 0.1 µF, 100 V capacitor from this pin to AGND and a 0.22 µF, 100 V capacitor from this pin to pin CF1. |

Note: On the printed-wiring board (PWB), make the leads to BGND and $V_{BAT}$ as wide as possible for thermal and electrical reasons. Also, maximize the amount of PWB copper on all leads connected to this device for the lowest operating temperature.

## Operating States

The L7585 has 14 operating states. These states are selected using 4 bits, B0—B3, according to the truth table shown in Table 2. The operation of the L7585 is undefined for unassigned states. Additionally, bit B4 independently operates the test-in access contacts so that all states are available for self-test; and bit B5 independently operates a relay driver, regardless of the status of bits B0—B4. All 6 bits are loaded via the parallel data interface and chip select lead NCS.

**Table 2. B0—B3 Input State Coding**

| B3 | B2 | B1 | B0 | State |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | Forward Battery Active |
| 1 | 1 | 1 | 0 | Ground Start/Tip Open |
| 1 | 1 | 0 | 1 | Ground Start/Tip Ground |
| 1 | 1 | 0 | 0 | Forward Battery Ring Open |
| 1 | 0 | 1 | 1 | Ringing (Battery Backed) |
| 1 | 0 | 1 | 0 | Disconnect State |
| 1 | 0 | 0 | 1 | Forward Battery Low-Current Active State |
| 1 | 0 | 0 | 0 | High Impedance |
| 0 | 1 | 1 | 1 | Reverse Battery Active |
| 0 | 1 | 1 | 0 | Reverse Battery Tip Open |
| 0 | 1 | 0 | 1 | Ground Start/Tip Amplifier |
| 0 | 1 | 0 | 0 | Reverse Battery Ring Open |
| 0 | 0 | 1 | 1 | Ringing (Earth Backed) |
| 0 | 0 | 1 | 0 | Unassigned |
| 0 | 0 | 0 | 1 | Reverse Battery Low-Current Active State |
| 0 | 0 | 0 | 0 | High Impedance |

**Table 3. B4—B5 Input State Coding**

| Bit | | State |
|---|---|---|
| B4 | 1<br>0 | Test-in contacts off.<br>Test-in contacts on. |
| B5 | 1<br>0 | Relay driver off.<br>Relay driver on. |

### Forward Battery Active State

- Normal talk and forward battery feed state.
- All circuits are powered up and active.
- Pin PT is positive with respect to pin PR (forward battery).
- SW2, SW2a, SW4, and SW4a closed; SW1, SW3, SW5, and SW6 open.
- NDET reflects the status of the switchhook detector.

### Ground Start/Tip Open State

- Ground start idle supervision state.
- Ring lead continuity test state (tone injected at the receive port) in forward battery.
- Same as forward battery active state, but with SW2 and SW2a open, and the tip drive amplifier powered down.
- Pin PT is high impedance (>100 kΩ).
- The ring current limit is approximately equal to the value programmed for the high-current active state current limit. Current limit is achieved by reducing the ring lead voltage only (see Table 6).
- NDET indicates an off-hook when the ring current (flowing into PR) is twice the value programmed for the switchhook detector in the forward battery active state.

## Operating States (continued)

### Ground Start/Tip Ground State

- Ground start busy supervision state.
- Same as ground start/tip open state but with SW1 closed.

### Forward Battery Ring Open State

- Tip lead continuity test state (tone injected at the receive port) in forward battery.
- Same as forward battery active state, but with SW4 and SW4a open, and the ring drive amplifier powered down.
- Pin PR is high impedance (>100 kΩ).
- Tip current limit is twice the low-current active state current limit.
- NDET indicates an off-hook when the tip current (flowing out of PT) is twice the value programmed for the switchhook detector in the forward battery active state.

### Ringing States (2)

- Normal ringing state.
- Tip and ring drive amplifiers are powered down.
- SW1 and SW5 closed; SW2, SW2a, SW3, SW4, SW4a, and SW6 open.
- NDET reflects the status of the ring trip detector.
- Bit B3 indicates whether the ringing voltage applied to the ringing bus is either battery backed (B3 = 1) or earth backed (B3 = 0). Although B3 has no direct effect on the state of the SLIC, it can be used by the ring trip detector to enhance ring trip detection.

### Disconnect State

- All circuits are powered up and active.
- SW2, SW2a, SW4, and SW4a closed; SW1, SW3, SW5, and SW6 open.
- PT and PR are at the same potential to deny current to the loop.

### Forward Battery Low-Current Active State

- Normal talk and forward battery feed state.
- All circuits are powered up and active.
- Pin PT is positive with respect to pin PR (forward battery).
- SW2, SW2a, SW4, and SW4a closed; SW1, SW3, SW5, and SW6 open.
- NDET reflects the status of the switchhook detector.
- Current limit is lowered to approximately 0.66 times the normal limit.

### High-Impedance State

- Disconnect state.
- Tip and ring drive amplifiers are powered down (all bias currents off).
- Pins PT and PR are high impedance (>100 kΩ).
- SW1, SW2, SW2a, SW3, SW4, SW4a, SW5, and SW6 open.
- NDET is undefined.

### Reverse Battery Active State

- Normal talk and reverse battery feed state.
- Same as forward battery active state, but PR is positive with respect to PT.

### Reverse Battery Tip Open State

- Ring lead continuity test state (tone injected at the receive port) in reverse battery.
- SW2 and SW2a open and the tip drive amplifier powered down.
- Pin PT is high impedance (>100 kΩ).
- Pin PR is held between –1.7 V and –2.3 V for PR currents less than ±20 mA. PR current limit is the SW4 break switch current limit (250 mA < I < 85 mA).
- NDET indicates an off-hook when the ring current (flowing out of PR) is twice the value programmed for the switchhook detector in the reverse battery active state.

## Operating States (continued)

### Ground Start/Tip Amplifier State

- Current limiting is achieved by reducing ring lead voltage only. This state is the same as Ground Start/ Tip Open, but with SW2 and SW2A closed and the tip amplifier powered up.
- Ring lead current limit is approximately the difference of the high-current active state limit and the current flowing out of the tip lead.
- On-hook transmission not to exceed –3 dBm with up to 5 mA flowing out of the tip lead (maximum current flow into the tip lead is permissible). Larger signal and/or current may cause distortion.
- NDET indicates an off-hook when the current flowing out of the tip plus the current flowing into the ring is twice the value programmed for the switchhook detector.

### Reverse Battery Ring Open State

- Tip lead continuity test state (tone injected at the receive port) in reverse battery.
- Same as reverse battery active state, but with SW4 and SW4a open, and the ring drive amplifier powered down.
- Pin PR is high impedance (>100 kΩ).
- Tip current limit is twice the low-current active state current limit.
- NDET indicates an off-hook when the tip current (flowing into PT) is twice the value programmed for the switchhook detector in the reverse battery active state.

### Reverse Battery Low-Current Active State

- Normal talk and reverse battery feed state.
- Same as forward battery active state, but PR is positive with respect to PT.
- Current limit is lowered to approximately 0.66 times the normal limit.

## Absolute Maximum Ratings ($T_A$ = 25 °C)

Stresses exceeding the values listed under absolute maximum ratings may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods of time may adversely affect device reliability.

| Parameter | Value | Unit |
|---|---|---|
| +5 V dc Supplies ($V_{CCA}$ and $V_{CCD}$) | –0.5 to +7.0 | V |
| +10 V dc Bias Supply ($V_{SP}$) | –0.5 to +15 | V |
| Office Battery Supply ($V_{BAT}$) | –63 to +0.5 | V |
| Logic Input Voltage | –0.5 to $V_{DDD}$ + 0.5 | V |
| Logic Input Clamp Diode Current, per Pin | ±20 | mA |
| Logic Output Voltage | –0.5 to $V_{DDD}$ + 0.5 | V |
| Logic Output Current, per Pin (excluding relay driver) | ±35 | mA |
| Operating Temperature Range | –40 to +125 | °C |
| Storage Temperature Range | –40 to +125 | °C |
| Relative Humidity Range | 5 to 95 | %RH |
| Ground Potential Difference (BGND to AGND) | ±3 | V |
| Ground Potential Difference (DGND to AGND) | ±3 | V |

Note: Analog voltages are referenced to AGND, digital (logic) voltages are referenced to DGND, and battery voltages are referenced to BGND. The IC can be damaged unless all ground connections are applied before and are removed after all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. Some of the known examples of conditions that cause such potentials during powering are the following: 1) an inductor connected to tip and ring that can force an overvoltage on $V_{BAT}$ through external components if the $V_{BAT}$ connection chatters; and 2) inductance in the $V_{BAT}$ lead that could resonate with the $V_{BAT}$ filter capacitor to cause a destructive overvoltage.

## Electrical Characteristics

In general, minimum and maximum values are testing requirements. However, some parameters may not be tested in production because they are guaranteed by design and device characterization. Typical values reflect the design center or nominal value of the parameter; they are for information only and are not a requirement. Minimum and maximum values apply across the entire temperature range (–40 °C to +85 °C) and entire battery range (–35 V to –60 V). Unless otherwise specified, typical is defined as 25 °C, $V_{CCA}$ = +5.0 V, $V_{CCD}$ = +5.0 V, $V_{SP}$ = +10 V, $V_{BAT}$ = –48 V. Positive currents flow into the device.

**Table 4. Operating Conditions and Powering**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Temperature Range | –40 | — | 85 | °C |
| Humidity Range | 5 | — | 95* | %RH |
| Supply Voltages: | | | | |
| $V_{CCA}$ | 4.75 | 5.0 | 5.5 | V |
| $V_{CCD}$ | 4.75 | 5.0 | 5.5 | V |
| $V_{SP}$ | 8.0 | 10 | 12.0 | V |
| $V_{BAT}$ | –35 | –48 | –60 | V |
| $V_{CCA}$—$V_{CCD}$ | — | — | ±0.5 | V |
| $D_{GND}$—$A_{GND}$ | — | — | ±0.25 | V |
| Supply Currents (all states, no loop current): | | | | |
| $I_{CCA}$ + $I_{CCD}$ (+5 V) | — | 4.9 | 7.0 | mA |
| $I_{VSP}$ (+10 V) | — | 45 | 200 | µA |
| $I_{BAT}$ (–48 V) | — | –3.1 | –4.0 | mA |
| Total Power Dissipation (all states, no loop current) ($V_{CC}$ = +5 V; $V_{SP}$ = +10 V; $V_{BAT}$ = –48 V) | — | 175 | 200 | mW |
| Power Supply Rejection (tip/ring and transmit)†: | | | | |
| $V_{CCA}$ (500 Hz—3 kHz; 50 mVrms ripple) | 30 | 40 | — | dB |
| $V_{CCD}$ (500 Hz—3 kHz; 50 mVrms ripple) | 45 | — | — | dB |
| $V_{SP}$ (500 Hz—3 kHz; 250 mVrms ripple) | 45 | — | — | dB |
| $V_{BAT}$ (500 Hz—3 kHz; 50 mVrms ripple) | 45 | — | — | dB |
| Thermal†: | | | | |
| Thermal Resistance (still air) | — | — | 47 | °C/W |
| Operating $T_{JC}$ | — | — | 155 | °C |

* Not to exceed 26 grams of water per kilogram of dry air.
† This parameter is not tested in production; it is guaranteed by design and device characterization.

**Table 5. Ring Trip Detector**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Voltage at input that will cause ring trip after appropriate zero crossings. | ±2.5 | ±3 | ±3.5 | V |
| Voltage at input that will cause immediate ring trip. | ±12 | ±15 | ±18 | V |
| Ringing Source[1]: | | | | |
| Frequency (f) | 19 | 20 | 28 | Hz |
| dc Voltage | –39.5 | — | –57 | V |
| ac Voltage | 60 | — | 105 | Vrms |
| Ring Trip (NDET = 0)[2, 3]: | | | | |
| Loop Resistance | 2000 | — | — | Ω |
| Trip Time | — | — | 200 | ms |
| NDET Valid | — | — | 80 | ms |

1. The ringing source may be either of the following:
   a) The ringing source consists of the ac and dc voltages added together (battery-backed ringing); the ringing return is ground. In this case, bit B3 will always be a 1 when ringing is applied.
   b) The ringing source consists of only the ac voltage (earth-backed ringing); the ringing return is the dc voltage. In this case, bit B3 will always be a 0 when ringing is applied.
2. NDET must also indicate ring trip when the ac ringing voltage is absent (<5 Vrms) from the ringing source.
3. Pretrip ringing must not be tripped by a 10 kΩ resistor in parallel with an 8 µF capacitor applied across tip and ring.

## Electrical Characteristics (continued)

**Table 6. Battery Feed Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Tip or Ring Drive Current = dc + Longitudinal + Signal Currents | — | 65 | — | — | mA |
| ac Signal Current | — | 10 | — | — | mArms |
| Longitudinal Current Capability per Wire[1] | — | 8.5 | 15 | — | mArms |
| dc Loop Current Limit[2] ($R_{LOOP}$ = 100 Ω): | $I_{LIM}$ | | | | |
| Programmability Range | | 5 | — | 45 | mA |
| Current Limit with $V_{BAT}$ = –51.5 V and $R_{PROG}$ = 64.9 kΩ | | 44 | 42 | 56 | mA |
| Low-current Mode[2] ($R_{LOOP}$ = 100 Ω, $V_{BAT}$ = –51.5 V, and $R_{PROG}$ = 64.9 kΩ) | | 25 | 27.5 | 30 | mA |
| Ground Start Ring Grounded ($R_{LOOP}$ = 100 Ω) Current Limit[3]: $V_{BAT}$ = –51.5 V, $R_{PROG}$ = 64.9 kΩ | | 38 | 43 | 47 | mA |
| Loop Closure Current Detector Threshold[4] Programming Accuracy | $I_{LCD}$ | — | — | ±7 | % |
| Open Loop Voltages (DCR = 0 V): | — | | | | |
| Common-mode Voltage | | — | ($V_{BAT}$ + 1.8)/2 | — | V |
| Differential Voltage | | \|$V_{BAT}$ + 7.0\| | \|$V_{BAT}$ + 6.5\| | \|$V_{BAT}$ + 6.0\| | V |
| Disconnect State PT/PR Voltage | \|PT-PR\| | — | — | ±100 | mV |
| Ground Start Ring Lead Open or Shorted to Ground: PT and CF1 Voltage | — | –1.7 | –2.0 | –2.3 | V |
| dc Feed Resistance: | — | | | | |
| DCR Grounded | | 130 | 150 | 170 | Ω |
| DCR Connected to $DC_{OUT}$[5] | | 480 | 505 | 630 | Ω |
| dc Gains: | — | | | | |
| PT/PR Current to $DC_{OUT}$ Voltage[6]: | | | | | |
| Forward Battery | | –118 | — | –132 | V/A |
| Reverse Battery | | 118 | — | 132 | V/A |
| DCR Voltage[7] to PT/PR Differential Voltage | | 3.13 | 3.33 | 3.53 | — |
| Loop Resistance Range[8] (3.17 dBm overload into 600 Ω): $I_{LOOP}$ = 20 mA at $V_{BAT}$ = –51.5 V | — | 1890 | 1930 | — | Ω |
| Longitudinal to Metallic Balance—*IEEE*® Std. 455: | — | | | | |
| 50 Hz to 1 kHz | | 58[9] | 70 | — | dB |
| 1 kHz to 3 kHz | | 48 | 66 | — | dB |
| Metallic to Longitudinal (harm) Balance: | — | | | | |
| 200 Hz to 4 kHz | | 35 | — | — | dB |

1. The longitudinal current is independent of dc loop current.
2. Current limit, $I_{LIM}$, is programmed by a resistor, $R_{PROG}$, from pin IPROG to pin DCOUT. $R_{PROG}$ = 1.667 x ($I_{LIM}$ – 4); $R_{PROG}$ in kΩ and $I_{LIM}$ in mA. The current limit versus loop voltage has a slope of 10 kΩ. The low-current mode current limit is approximately 0.66 times the high current limit. The ground start ring lead ground current limit is approximately equal to the high current limit and has a slope of about 5 kΩ.
3. In transmission applications, for compliance with TR-57, ground start ring lead I-V characteristics at high battery, it is expected that the high-current active current limit will be set to 28 mA.
4. Loop closure detector current, $I_{LCD}$, is programmed by a resistor, RLCTH, from pin LCTH to pin DCOUT. RLCTH = 2.5 x $I_{LCD}$; RLCTH in kΩ and $I_{LCD}$ in mA. $I_{LCD}$ is the tip to ring (forward battery) or ring to tip (reverse battery) current at which the loop closure detector indicates an off-hook.
5. dc feed resistance may be adjusted between 180 Ω and 600 Ω using a resistor divider between DCOUT and DCR. The open loop differential voltage may also be increased by applying a negative voltage to pin DCR. See dc Gains, pin DCR.
6. DCOUT gain depends on the resistor RGX1 from pin VITR to pin ITR. This gain assumes 8250 Ω, the recommended value. Positive current is defined as the differential current flowing from PT to PR.
7. Positive voltage on pin DCR has no effect on the PT/PR voltage.
8. At tip and ring, assuming 82.5 Ω protection resistors.
9. At tip and ring with matched 82.5 Ω protection resistors when feedback is connected for either 600 Ω or 900 Ω termination impedance.

## Electrical Characteristics (continued)

**Table 7. Analog Signal Pins**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| DCOUT: | | | | |
| Output Offset (no loop current) | — | — | ±200 | mV |
| Output Drive Current | 0.25 | — | –3.0 | mA |
| Output Voltage Swing (+0.25 mA/–3 mA load): | | | | |
| Maximum | $V_{BAT}$ | — | $V_{CCA}$ | V |
| Minimum | –10 | — | 0.5 | V |
| Output Short-circuit Current | — | — | ±20 | mA |
| Output Load Resistance | 5 | — | — | kΩ |
| Output Load Capacitance[1] | — | — | 50 | pF |
| VITR and VTX: | | | | |
| Output Offset (no loop current)[2] | — | — | ±100 | mV |
| Output Drive Current | ±1 | — | — | mA |
| Output Voltage Swing (±1 mA load): | | | | |
| Maximum | –10 | — | $V_{CCA}$ | V |
| Minimum (VITR) | ±3.5 | — | — | V |
| Minimum (VTX) | –3.5 | — | $V_{CCA}$ – 1.0 | V |
| Output Short-circuit Current | — | — | ±20 | mA |
| Output Load Resistance | 4 | — | — | kΩ |
| Output Load Capacitance[1] | — | — | 50 | pF |
| VRTX: | | | | |
| Output Voltage | 2.2 | 2.4 | 2.6 | V |
| Output Drive Current | ±500 | — | — | µA |
| Output Short-circuit Current | — | — | ±15 | mA |
| Output Load Capacitance[1] | — | — | 50 | pF |
| RSW: | | | | |
| Impedance to Ground | 3 | — | — | MΩ |
| DCR: | | | | |
| Input Voltage Range[3] | –8 | — | 0 | V |
| Input Bias Current | — | — | ±1 | µA |
| Input Impedance | 500 | — | — | kΩ |
| TXI: | | | | |
| Input Impedance | 75 | — | — | kΩ |
| Input Voltage Compliance | ±0.4 | — | — | V |
| Input Clamp Voltage | ±0.4 | — | ±0.8 | V |
| RCVP and RCVN: | | | | |
| Input Voltage Range | –2.5 | — | $V_{CCA}$ | V |
| Input Bias Current | — | — | ±1.5 | µA |
| Input Impedance | 10 | — | — | MΩ |
| PT and PR: | | | | |
| Overvoltage (from external source; continuous) | — | — | ±265 | V |
| FB1 and FB2: | | | | |
| ac Output Impedance | — | — | 10 | kΩ |
| Output Short-circuit Current | ±27 | — | ±34 | µA |
| CF1 and CF2: | | | | |
| Output Impedance[1] | 180 | — | 375 | kΩ |

1. This parameter is not tested in production; it is guaranteed by design and device characterization.
2. VTX offset is measured with respect to pin VRTX.
3. Positive voltages from 0 V to $V_{CCA}$ are permitted at input DCR; however, voltages above 0 V have no effect on either the dc feed resistance or tip/ring voltage.

## Electrical Characteristics (continued)

Transmit direction is tip/ring to VTX. Receive direction is RCVP(N) to tip/ring.

**Table 8. Transmission Characteristics**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| ac Termination Impedance[1] | 200 | — | 1200 | Ω |
| Return Loss[2]: | | | | |
| 200 Hz—500 Hz | 25 | — | — | dB |
| 500 Hz—3400 Hz | 29 | — | — | dB |
| Total Harmonic Distortion (200 Hz—4 kHz)[3]: | | | | |
| Off-hook | — | — | 0.3 | % |
| On-hook | — | — | 1 | % |
| Transmit Gain (f = 1 kHz)[4]: | | | | |
| PT/PR Current to (VTX—VRTX) | –291 | –300 | –309 | V/A |
| Receive Gain (f = 1 kHz): | | | | |
| (RCVP—RCVN) to (PT—PR) | 1.94 | 2 | 2.06 | — |
| Gain vs. Frequency (transmit and receive)[3] (600 Ω termination; 1 kHz reference): | | | | |
| 200 Hz—300 Hz | –0.3 | 0 | 0.05 | dB |
| 300 Hz—3.4 kHz | –0.05 | 0 | 0.05 | dB |
| 3.4 kHz—20 kHz | –3.0 | 0 | 0.05 | dB |
| 20 kHz—266 kHz | — | — | 2.0 | dB |
| Gain vs. Level (transmit and receive; 0 dBV reference)[3]: | | | | |
| –50 dB to +3 dB | –0.05 | 0 | 0.05 | dB |
| Transhybrid Loss[2]: | | | | |
| 200 Hz—500 Hz | 25 | — | — | dB |
| 500 Hz—3400 Hz | 29 | — | — | dB |
| Idle-channel Noise (tip/ring; 600 Ω termination): | | | | |
| Psophometric | — | — | –77 | dBmp |
| C-message | — | — | 13 | dBrnC |
| 3 kHz Flat | — | — | 20 | dBrn |
| Idle-channel Noise ((VTX—VRTX); 600 Ω termination): | | | | |
| Psophometric | — | — | –77 | dBmp0 |
| C-message | — | — | 13 | dBrnC0 |
| 3 kHz Flat | — | — | 20 | dBrn0 |
| EMC, per EN 300 386-2 and EN61000-4-6 (3 Vrms, 80% modulation, 105 kHz—80 MHz, 150 Ω source impedance)[3] | — | — | –40 | dBm, 600 Ω |

1. Set by external components in conjunction with the T7531A/T7536 codecs. Any complex impedance R1 + R2 || C between 200 Ω and 1200 Ω can be synthesized.
2. Return loss and transhybrid loss are functions of device gain accuracies and the external hybrid circuit. Guaranteed performance assumes 1% tolerance external resistors and capacitors.
3. This parameter is not tested in production; it is guaranteed by design and device characterization.
4. VTX gain depends on the resistor RGX1 from pin VITR to pin ITR. This gain assumes an ideal 8250 Ω, the recommended value. Positive current is defined as the differential current flowing from PT to PR. The transmit signal at VTX is measured with respect to pin VRTX.

## Electrical Characteristics (continued)

**Table 9. Data Interface and Logic (Logic Inputs [CLK, NCS, and B0—B5] and Outputs [NDET])**

| Parameter[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level Input Voltage | $V_{IH}$ | 2 | $V_{CCD}$ | V |
| Low-level Input Voltage | $V_{IL}$ | 0 | 0.8 | V |
| Input Bias Current (high and low) | $I_{IN}$ | — | ±10 | µA |
| High-level Output Voltage ($I_{OUT}$ = –100 µA) | $V_{OH}$ | $V_{CCD}$ – 1.5 | $V_{CCD}$ | V |
| Low-level Output Voltage ($I_{OUT}$ = 180 µA) | $V_{OL}$ | 0 | 0.4 | V |
| Output Short-circuit Current ($V_{OUT}$ = $V_{CCD}$) | $I_{OSS}$ | 1 | 35 | mA |
| Output Load Capacitance[2] | $C_{OL}$ | 0 | 50 | pF |

1. Unless otherwise specified, all logic voltages are referenced to DGND.
2. This parameter is not tested in production; it is guaranteed by design and device characterization.

**Table 10. Timing Requirements (CLK, B0—B5, and NCS)[1, 2]**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| CLK and NCS Rise and Fall Time (10% to 90%) | tR, tF | 0 | 50 | ns |
| Maximum Input Capacitance | CIN | — | 5 | pF |
| Minimum Setup Time from B0—B5 Valid to NCS<br>$V_{IH}$ = 2 V<br>$V_{IH}$ = 2.5 V | <br>tSDS<br>tSDS | <br>250<br>150 | <br>—<br>— | <br>ns<br>ns |
| Minimum Hold Time from NCS to B0—B5 Not Valid<br>$V_{IH}$ = 2 V<br>$V_{IH}$ = 2.5 V | <br>tHDS<br>tHDS | <br>150<br>10 | <br>—<br>— | <br>ns<br>ns |
| Minimum Pulse Width of NCS | tWCS | 195 | — | ns |
| CLK Frequency | fCLK | 0.9 | 2.2 | MHz |
| Minimum Pulse Width of CLK | tWCK | 195 | — | ns |

1. Unless otherwise specified, all times are measured from the 50% point of logic transitions.
2. These parameters are not tested in production; they are guaranteed by design and device characterization.

**Table 11. Relay Driver (RDO)**

| Parameter[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Off-state Output Current ($V_{RDO}$ = $V_{CCD}$) | $I_{OFF}$ | — | ±10 | µA |
| On-state Output Voltage ($I_{RDO}$ = 40 mA) | $V_{ON}$ | 0 | 0.60 | V |
| On-state Output Voltage ($I_{RDO}$ = 20 mA) | $V_{ON}$ | 0 | 0.40 | V |
| Clamp Diode Reverse Current ($V_{RDO}$ = 0) | $I_R$ | — | ±10 | µA |
| Clamp Diode On Voltage ($I_{RDO}$ = 80 mA) | $V_{OC}$ | 6 | 20 | V |
| Turn-on Time[2] | $t_{ON}$ | — | 10 | µs |
| Turn-off Time[2] | $t_{OFF}$ | — | 10 | µs |

1. Unless otherwise specified, all logic voltages are referenced to DGND.
2. This parameter is not tested in production; it is guaranteed by design and device characterization.

## Electrical Characteristics (continued)

**Table 12. Ringing Return Access Switch (SW1)**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Off-state: | | | | |
| Maximum Differential Voltage | — | — | ±320[1] | V |
| dc Leakage Current ($V_{SW}$ = ±320 V) | — | — | ±10 | µA |
| Feedthrough Capacitance[2] | — | — | 15 | pF |
| On-state (See On-State Switch V-I Characteristics section.): | | | | |
| Resistance ($R_{ON}$) | — | 45 | 90 | Ω |
| Maximum Differential Voltage ($V_{max}$) | — | — | 320[1] | V |
| Foldback Voltage Breakpoint 1 ($V_1$) | 120 | — | — | V |
| Foldback Voltage Breakpoint 2 ($V_2$) | 200 | — | — | V |
| Current Limit ($I_{LIMIT1}$) | 120 | 220 | 360 | mA |
| Current Limit ($I_{LIMIT2}$) | 2 | — | — | mA |
| dV/dT Sensitivity[2, 3] | — | 200 | 2000 | V/µs |

1. At 25 °C, maximum voltage rating has a temperature coefficient of +0.167 V/°C.
2. This parameter is not tested in production; it is guaranteed by design and device characterization.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dt sensitivity at 200 V/µs typical with no switch turn-on. In the case of dV/dt induced turn-on at higher dV/dt and amplitude, the design objective is no damage to at least 2000 V/µs and full voltage. A known condition that can cause damage is initial current flow prior to the application of the dV/dt and the sudden application of reverse bias with dV/dt induced switch turn-off. In this case, no damage will occur for dV/dt up to 2000 V/µs as guaranteed by design and characterization.

**Table 13. Test-In Access Switches (SW3 and SW6)**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Off-state: | | | | |
| Maximum Differential Voltage | — | — | ±320[1] | V |
| dc Leakage Current ($V_{SW}$ = ±320 V) | — | — | ±10 | µA |
| Feedthrough Capacitance[2] | — | — | 15 | pF |
| On-state (See On-State Switch V-I Characteristics section.): | | | | |
| Resistance ($R_{ON}$) | — | 45 | 90 | Ω |
| Maximum Differential Voltage ($V_{max}$) | — | — | 60 | V |
| Current Limit ($I_{LIMIT}$) Switches SW3 and SW6[3] | 85 | — | — | mA |
| dV/dT Sensitivity[2, 4] | — | 200 | 2000 | V/µs |

1. At 25 °C, maximum voltage rating has a temperature coefficient of +0.167 V/°C.
2. This parameter is not tested in production; it is guaranteed by design and device characterization.
3. Test in access switches current limit will be > tip and ring break switches current limit.
4. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dt sensitivity at 200 V/µs typical with no switch turn-on. In the case of dV/dt induced turn-on at higher dV/dt and amplitude, the design objective is no damage to at least 2000 V/µs and full voltage. A known condition that can cause damage is initial current flow prior to the application of the dV/dt and the sudden application of reverse bias with dV/dt induced switch turn-off. In this case, no damage will occur for dV/dt up to 2000 V/µs as guaranteed by design and characterization.

## Electrical Characteristics (continued)

**Table 14. Tip and Ring Break Switches (SW2 and SW4)**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Off-state: | | | | |
| Maximum Differential Voltage | — | — | ±320[1] | V |
| dc Leakage Current ($V_{SW}$ = ±320 V) | — | — | ±20 | µA |
| Feedthrough Capacitance[2] | — | — | 50 | pF |
| On-state (See On-State Switch V-I Characteristics section.): | | | | |
| Resistance ($R_{ON}$) | — | 25 | 50 | Ω |
| Maximum Differential Voltage ($V_{max}$) | — | — | 320[1] | V |
| Foldback Voltage Breakpoint 1 ($V_1$) | 60 | — | — | V |
| Foldback Voltage Breakpoint 2 ($V_2$) | $V_1$ + 0.5 | — | — | V |
| Current Limit ($I_{LIMIT1}$) | 85 | 160 | 250 | mA |
| Current Limit ($I_{LIMIT2}$) | 2 | — | — | mA |
| dV/dT Sensitivity[2, 3] | — | 200 | 2000 | V/µs |

1. At 25 °C, maximum voltage rating has a temperature coefficient of +0.167 V/°C.
2. This parameter is not tested in production; it is guaranteed by design and device characterization.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dt sensitivity at 200 V/µs typical with no switch turn-on. In the case of dV/dt induced turn-on at higher dV/dt and amplitude, the design objective is no damage to at least 2000 V/µs and full voltage. A known condition that can cause damage is initial current flow prior to the application of the dV/dt and the sudden application of reverse bias with dV/dt induced switch turn-off. In this case, no damage will occur for dV/dt up to 2000 V/µs as guaranteed by design and characterization.

**Table 15. Tip and Ring Feedback Switches (SW2a and SW4a)**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Off-state: | | | | |
| Maximum Differential Voltage | — | — | ±320[1] | V |
| dc Leakage Current ($V_{SW}$ = ±320 V) | — | — | ±10 | µA |
| Feedthrough Capacitance[2] | — | — | 15 | pF |
| On-state (See On-State Switch V-I Characteristics section.): | | | | |
| Resistance ($R_{ON}$) | — | 4 | 10 | kΩ |
| Maximum Differential Voltage ($V_{max}$) | — | — | 320[1] | V |
| Current Limit ($I_{LIMIT}$) | 0.5 | — | 20 | mA |
| dV/dT Sensitivity[2, 3] | — | 200 | 2000 | V/µs |

1. At 25 °C, maximum voltage rating has a temperature coefficient of +0.167 V/°C.
2. This parameter is not tested in production; it is guaranteed by design and device characterization.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dt sensitivity at 200 V/µs typical with no switch turn-on. In the case of dV/dt induced turn-on at higher dV/dt and amplitude, the design objective is no damage to at least 2000 V/µs and full voltage. A known condition that can cause damage is initial current flow prior to the application of the dV/dt and the sudden application of reverse bias with dV/dt induced switch turn-off. In this case, no damage will occur for dV/dt up to 2000 V/µs as guaranteed by design and characterization.

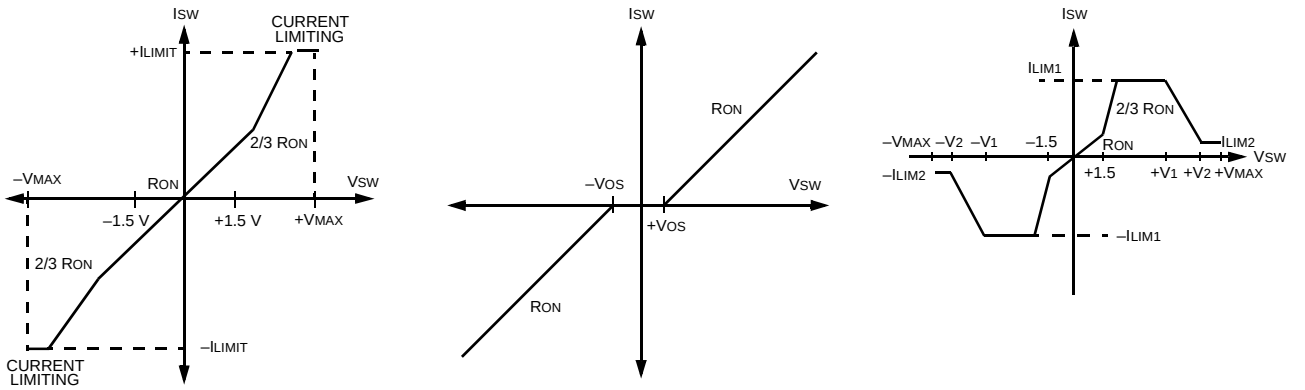
## Electrical Characteristics (continued)

**Table 16. Ringing Access Switch (SW5)**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Off-state: | | | | |
| Maximum Differential Voltage | — | — | ±475 | V |
| dc Leakage Current ($V_{SW}$ = ±500 V) | — | — | ±20 | µA |
| dc Leakage Current ($V_{SW}$ = ±250 V) | — | — | ±1 | µA |
| Feedthrough Capacitance[1] | — | 1 | — | pF |
| On-state (See On-State Switch V-I Characteristics section.): | | | | |
| Crossover Offset Voltage ($V_{OS}$; ISW = ±1 mA) | — | — | 3 | V |
| Resistance ($R_{ON}$) | — | — | 10 | Ω |
| Surge Current (10 µs x 1000 µs pulse)[1] | — | — | 2.5 | A |
| Release Current[1] | 0.1 | — | 2 | mA |
| dV/dT Sensitivity[1, 2] | — | 200 | 2000 | V/µs |
| Common-mode Voltage (maximum either switch terminal with respect to ground) | — | — | 320 | V |

1. This parameter is not tested in production; it is guaranteed by design and device characterization.
2. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dT sensitivity.
3. Applied voltage is 100 Vp-p square wave at 100 Hz to measure dV/dt sensitivity at 200 V/µs typical with no switch turn-on. In the case of dV/dt induced turn-on at higher dV/dt and amplitude, the design objective is no damage to at least 2000 V/µs and full voltage. A known condition that can cause damage is initial current flow prior to the application of the dV/dt and the sudden application of reverse bias with dV/dt induced switch turn-off. In this case, no damage will occur for dV/dt up to 2000 V/µs as guaranteed by design and characterization.

## On-State Switch I-V Characteristics




**A. SW2a, SW3, SW4a, SW6** **B. SW5** **C. SW1, SW2, SW4**

**Figure 3. On-State Switch I-V Characteristics**

# Applications

## Tip/Ring Protection

The L7585 SLIC has integrated overvoltage tertiary protection diodes in the tip and ring paths. The device also has an integrated thermal shutdown circuit which places tip/ring drivers in a high-impedance state when the die temperature exceeds 160 °C.

The SLIC requires the following to survive lightning and power cross requirements:

- Fusible elements or PTCs
- Current-limiting resistors
- A secondary protector

Thermal fuse/surge resistor modules that satisfy the various requirements can be purchased from *MMC*™. Protection resistors should have a tolerance of ±1% and a ratio tolerance of ±0.5%. The suppressor breakover voltage of the secondary protector should be set as low as possible. Select a value just above the maximum peak ring signal and maximum battery voltage.

## NDET Under Fault Condition

- The state of NDET is not guaranteed with loss of battery.
- In the ringing state, RRNG floating or with only dc on the ringing source, NDET will produce an off-hook because there are not zero crossings of ringing to cause an on-hook.
- In the ringing state with only ac (>40 Vrms) on the ringing source, an on-hook will be produced after the second zero crossing of the ringing waveform, because there is no dc component to the ringing current.
- In the ringing state, if the resistor between RSW and PR is open, there will likely be a large voltage at the ringing input (due to capacitive loading) and ring trip will be asserted after the second zero crossing of ringing. Because there is no guarantee of the load at PR in this condition, there can be no guarantee of the state on NDET in this condition.
- If the device enters into thermal shutdown due to a fault that causes an off-hook, the off-hook indication will be stable as the device cycles in and out of thermal shutdown. If the fault does not cause an off-hook, NDET will cycle between on- and off-hook as the device cycles in and out of thermal shutdown.

## Power, Clocking, and Layout

The SLIC requires +5 V ($V_{CCA}$ and $V_{CCD}$) and a negative battery voltage ($V_{BAT}$) to operate. The integrated switches require a 10 V or 12 V supply ($V_{SP}$) and a TTL clock (CLK) to operate. CLK requires a frequency between 1.0 MHz to 2.048 MHz with a 50% duty cycle. SW1, SW3, and SW6 will not operate without CLK applied.

A four- or six-layer board is recommended. Analog and battery grounds should be laid out as a plane and a layer, and tied together at the device. Digital ground can also be tied to this plane or run separately. $V_{SP}$ is referenced to DGND. $V_{CC}$ can be run as individual traces and can reside on the same layer as signal paths. $V_{CCA}$ and $V_{CCD}$ can be tied together at the SLIC. Placement of the talk battery is not critical.

The ring bus should be on a separate layer from the SLIC/codec interface signal leads, and traces should run perpendicular if the traces must cross. TXI, VITR, and ITR are the sensitive nodes on the SLIC. Transmit runners should be run in pairs, and receive runners should be run in pairs between the SLIC and the codec. A channel-to-channel spacing should be maintained.

## Applications (continued)

### Ring Trip

Ring trip is set by the value of RS1.

The ring trip threshold at the ring trip inputs is ±2.5 V minimum, ±3.5 V maximum.

A resistor value of 500 Ω, as shown in Figure 4, will set the ring trip current threshold to ±6.0 mA typical.

Ring trip is asserted upon entering the ringing mode until the second zero crossing of ringing. This is either a positive-going zero crossing (between –40 V and –30 V at –50 V $V_{BAT}$) or a negative-going zero crossing (between –10 V and –20 V at –50 V $V_{BAT}$). The different threshold for positive-going and negative-going zero crossings is the result of hysteresis of approximately 20 V.

Ring trip will not be asserted unless the ring trip threshold is exceeded for two zero crossings. This is either a positive-going zero crossing (between –40 V and –30 V at –50 V $V_{BAT}$) or a negative-going zero crossing (between –10 V and –20 V at –50 V $V_{BAT}$). The different threshold for positive-going and negative-going zero crossings is the result of hysteresis of approximately 20 V.

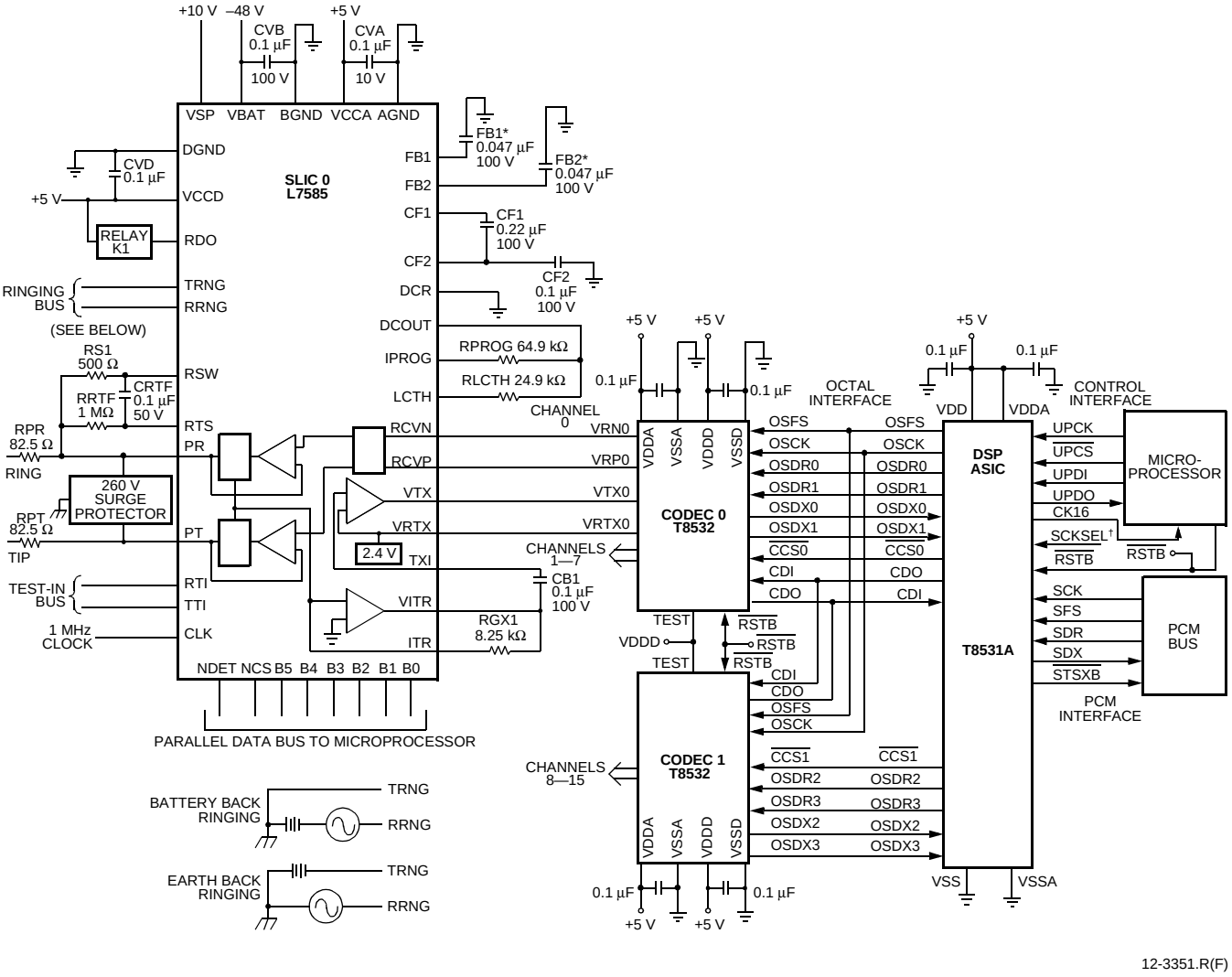
Note that since the ringing voltage is monitored at RSW, one zero crossing can occur at switch turn-on depending on initial conditions.

Ring trip is asserted immediately if the ring trip input is 15 V ± 3 V.

### False On-Hook Transients

- If the L7585G is off-hook in the ground-start/tip open state, the ground-start/tip ground state, or the ground-start/tip amplifier state, due to an applied ring ground, and it is switched to the forward battery active state, it will not generate a false on-hook longer than 10 ms in duration. This applies for loop resistances of 0 Ω to 2000 Ω, providing that all of the following criteria are satisfied:
  - — A loop closure is applied before the L7585G switches to the forward battery active state.
  - — The loop closure resistance (telephone set) is less than 430 Ω.
  - — The ring ground and loop closure are applied at the same end of the loop.
  - — If the ring ground is removed while the L7585G is in the forward battery active state, then the ring ground resistance must be greater than 225 Ω when the dc current limit is 40 mA, or greater than 430 Ω when the dc current is 28 mA.

## Application Diagram




* Optional for quiet reverse battery.
† 4.096 MHz operation; for 2.048 MHz operation, tie SCKSEL to VSS.

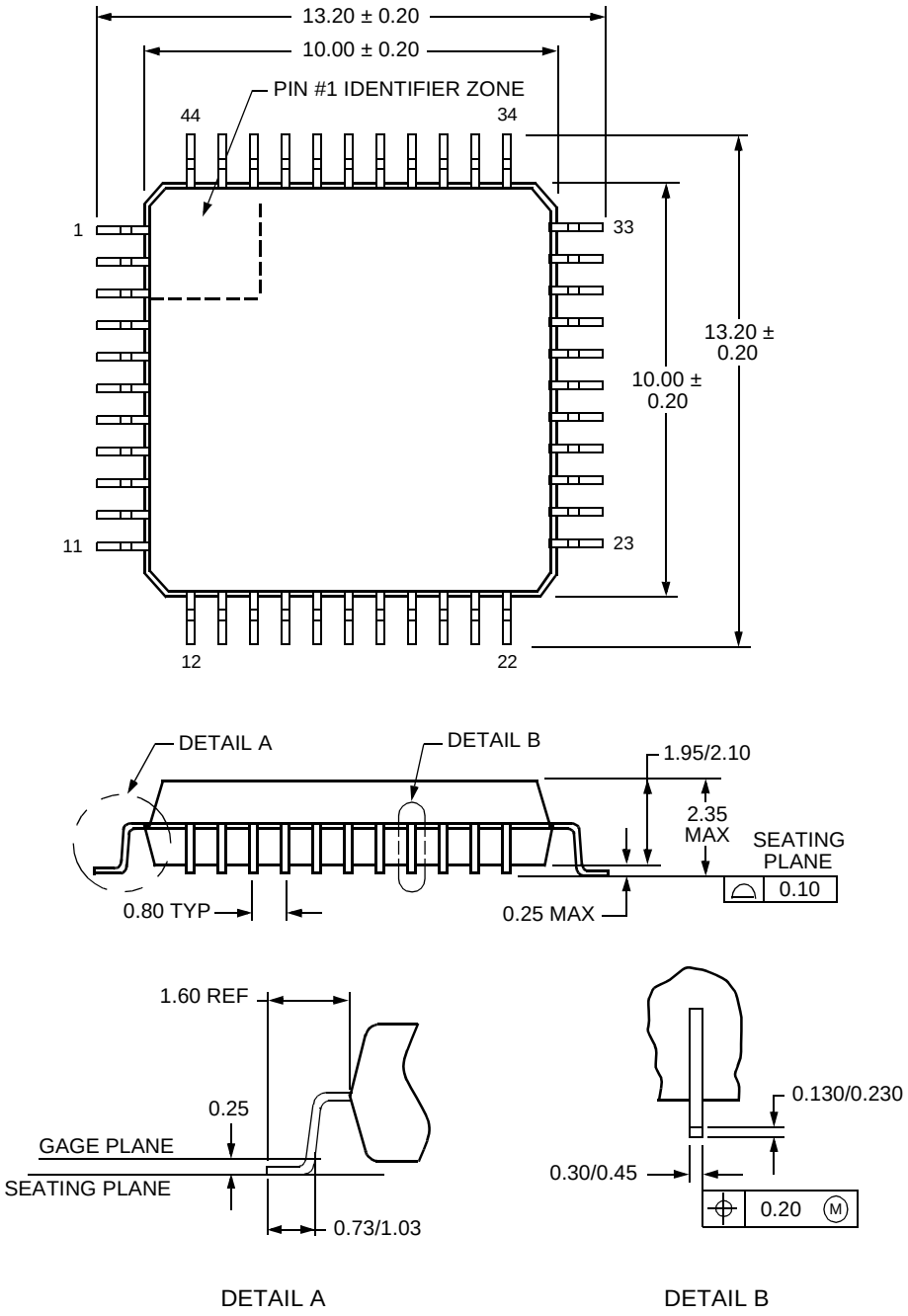
**Figure 4. 16-Channel Line Card Solution**

## Outline Diagram

### 44-Pin MQFP

Dimensions are in millimeters.

**Note:** The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Communications Sales Representative.




5-2111 (F)

## Ordering Information

| Device Part No. | Description | Package | Comcode |
|---|---|---|---|
| LUCL7585GBE-D | Full-Feature, Low-Power SLIC and Switch | 44-Pin MQFP (Dry Bag) | 108559683 |
| LUCL7585GBE-DT | Full-Feature, Low-Power SLIC and Switch | 44-Pin MQFP (Tape and Reel, Dry Bag) | 108559691 |

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September 2001
DS01-313ALC (Replaces DS00-217ALC)