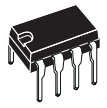
L6562AT

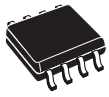
Transition-mode PFC controller

Features

- Guaranteed for extreme temperature range (outdoor)
- Proprietary multiplier design for minimum THD
- Very accurate adjustable output overvoltage protection
- Ultra-low (30 µA) start-up current
- Low (2.5 mA) quiescent current
- Digital leading-edge blanking on current sense
- Disable function on E/A input
- 1% (@ T_J = 25 °C) internal reference voltage
- -600/+800 mA totem pole gate driver with active pull-down during UVLO and voltage clamp



DIP-8



SO-8

- DIP-8/SO-8 packages

Applications

PFC pre-regulators for:

- Street lighting
- IEC61000-3-2 compliant SMPS (Flat TV, monitors, desktop PC, games)
- Electronic ballast

Figure 1. Block diagram

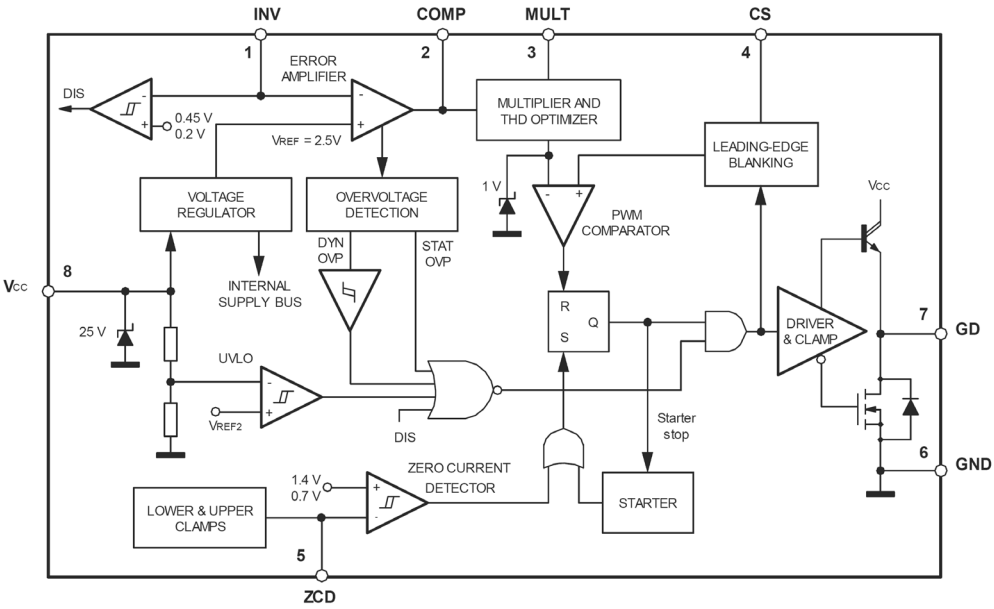


Table 1. Device summary

Order codes	Package	Packaging
L6562ATN	DIP-8	Tube
L6562ATD	SO-8	Tube
L6562ATDTR		Tape and reel

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1 Description

The L6562AT is a current-mode PFC controller operating in transition mode (TM). Coming with the same pin-out as its predecessors L6561 and L6562, it offers improved performance.

The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1% @T_J = 25 °C) internal voltage reference.

The device features extremely low consumption (60 µA max. before start-up and < 5.5 mA operating) and includes a disable function suitable for IC remote ON/OFF, which makes it easier to comply with energy saving requirements (Blue Angel, EnergyStar, Energy2000, etc.).

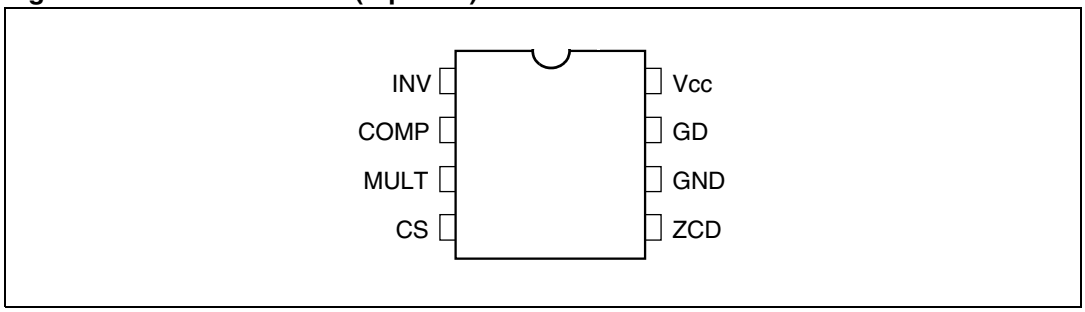
An effective two-step OVP enables to safely handle over-voltages either occurring at start-up or resulting from load disconnection.

The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable to drive high current MOSFETs or IGBTs. This, combined with the other features and the possibility to operate with the proprietary fixed-off-time control, makes the device an excellent low-cost solution for EN61000-3-2 compliant SMPS in excess of 350 W.

2 Pin settings

2.1 Pin connection

Figure 2. Pin connection (top view)



2.2 Pin description

Table 2. Pin description

Pin N°	Name	Description
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into this pin through a resistor divider. The pin doubles as an ON/OFF control input.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off. The pin is equipped with 200 ns leading-edge blanking for improved noise immunity.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.
8	Vcc	Supply voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22 V min. to provide more headroom for supply voltage changes.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	8	IC supply voltage ($I_{CC} \leq 20$ mA)	Self-limited	V
I_{GD}	7	Output totem pole peak current	Self-limited	A
---	1 to 4	Analog inputs and outputs	-0.3 to 8	V
I_{ZCD}	5	Zero current detector max. current	±10	mA

4 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value		Unit
		SO8	DIP8	
R_{thJA}	Max. thermal resistance, junction-to-ambient	150	100	°C/W
P_{TOT}	Power dissipation @T_A = 50 °C	0.65	1	W
T_J	Junction temperature operating range	-40 to 150		°C
T_{STG}	Storage temperature	-55 to 150		°C

5 Electrical characteristics

-40 °C < T_J < +125 °C, V_{CC} = 12 V, C_O = 1 nF; unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	10.5		22.5	V
Vcc_{On}	Turn-on threshold	(1)	11.7	12.5	13.3	V
Vcc_{Off}	Turn-off threshold	(1)	9.5	10	10.5	V
Hys	Hysteresis		2.2		2.8	V
V_Z	Zener voltage	I_{CC} = 20 mA	22.5	25	28	V
Supply current						
$I_{start-up}$	Start-up current	Before turn-on, V_{CC} = 11 V		30	60	µA
I_q	Quiescent current	After turn-on		2.5	3.9	mA
I_{CC}	Operating supply current	@ 70 kHz		3.5	5.5	mA
I_q	Quiescent current	During OVP (either static or dynamic) or $V_{INV} \leq$ 150 mV		1.7	2.2	mA
Multiplier input						
I_{MULT}	Input bias current	V_{MULT} = 0 to 4 V			-1	µA
V_{MULT}	Linear operation range		0 to 3			V
$\frac{\Delta V_{cs}}{\Delta V_{MULT}}$	Output max. slope	V_{MULT} = 0 to 1 V, V_{COMP} = Upper clamp	1	1.1		V/V
K	Gain (2)	V_{MULT} = 1 V, V_{COMP} = 4 V,	0.32	0.38	0.47	V
Error amplifier						
V_{INV}	Voltage feedback input threshold	T_J = 25 °C	2.475	2.5	2.525	V
		10.5 V < V_{CC} < 22.5 V (1)	2.44		2.545	
	Line regulation	V_{CC} = 10.5 V to 22.5 V		2	5	mV
I_{INV}	Input bias current	V_{INV} = 0 to 3 V			-1	µA
Gv	Voltage gain	Open loop	60	80		dB
GB	Gain-bandwidth product			1		MHz
I_{COMP}	Source current	V_{COMP} = 4 V, V_{INV} = 2.4 V	-2	-3.5	-5	mA
	Sink current	V_{COMP} = 4 V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper clamp voltage	I_{SOURCE} = 0.5 mA	5.1	5.7	6	V
	Lower clamp voltage	I_{SINK} = 0.5 mA (1)	2.1	2.25	2.4	V
V_{INVdis}	Disable threshold		150	200	250	mV
V_{INVen}	Restart threshold		380	450	520	mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Output overvoltage						
I_{OVP}	Dynamic OVP triggering current		19.5	27	30.5	µA
Hys	Hysteresis	(3)		20		µA
	Static OVP threshold	(1)	2.1	2.25	2.4	V
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			-1	µA
t_{LEB}	Leading edge blanking		100	200	300	ns
$td_{(H-L)}$	Delay to output			175		ns
V_{CS}	Current sense clamp	V_{COMP} = Upper clamp, Vmult = 1.5 V	1.0	1.08	1.16	V
Vcs_{offset}	Current sense offset	V_{MULT} = 0		25		mV
		V_{MULT} = 2.5 V		5		
Zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5 mA	5.0	5.7	6.5	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 2.5 mA	-0.5	0	0.5	V
V_{ZCDA}	Arming voltage (positive-going edge)	(3)		1.4		V
V_{ZCDT}	Triggering voltage (negative-going edge)	(3)		0.7		V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 4.5 V		2		µA
I_{ZCDsrc}	Source current capability		-1.5			mA
I_{ZCDsnk}	Sink current capability		1.5			mA
Starter						
t_{START}	Start timer period		75	190	300	µs
Gate driver						
V_{OL}	Output low voltage	I_{sink} = 100 mA		0.6	1.2	V
V_{OH}	Output high voltage	I_{source} = 5 mA	9.5	10.3		V
I_{srcpk}	Peak source current		-0.6			A
I_{snkpk}	Peak sink current		0.8			A
t_f	Voltage fall time			30	70	ns
t_r	Voltage rise time			60	130	ns
V_{Oclamp}	Output clamp voltage	I_{source} = 5 mA; Vcc = 20 V	10	12	15	V
	UVLO saturation	Vcc = 0 to V_{CCon}, I_{sink} = 2 mA			1.1	V

1. All the parameters are in tracking
2. The multiplier output is given by: $V_{cs} = K \cdot V_{MULT} \cdot (V_{COMP} - 2.5)$
3. Parameters guaranteed by design, functionality tested in production.

6 Typical electrical characteristic

Figure 3. Supply current vs supply voltage

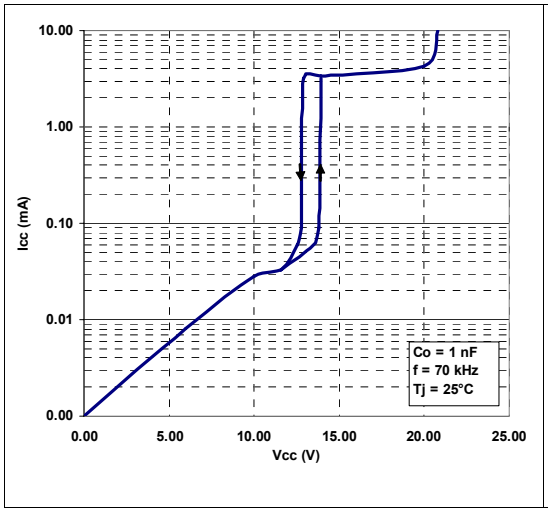


Figure 4. Start-up and UVLO vs T_J

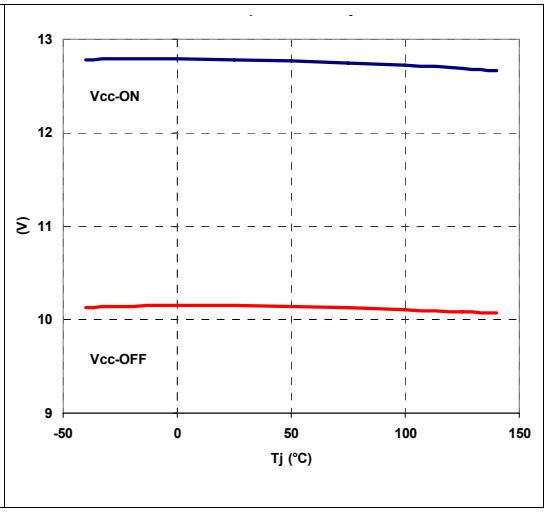


Figure 5. IC consumption vs T_J

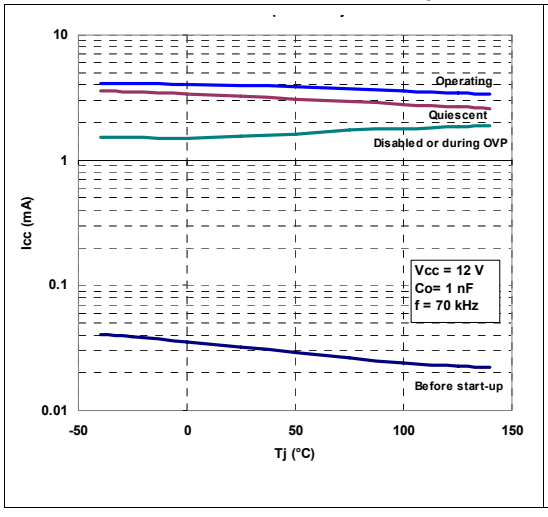


Figure 6. Vcc Zener voltage vs T_J

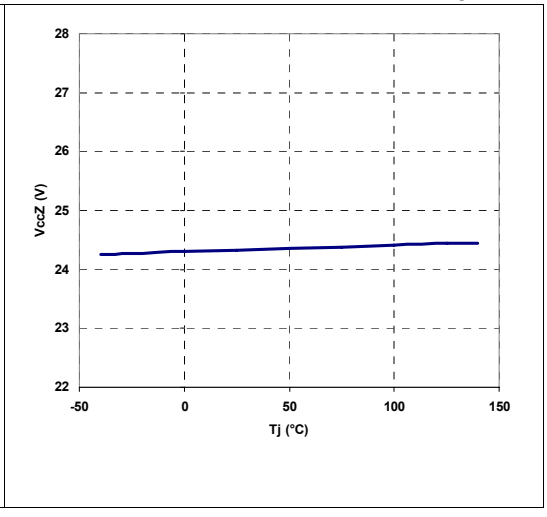


Figure 7. Feedback reference vs T_J

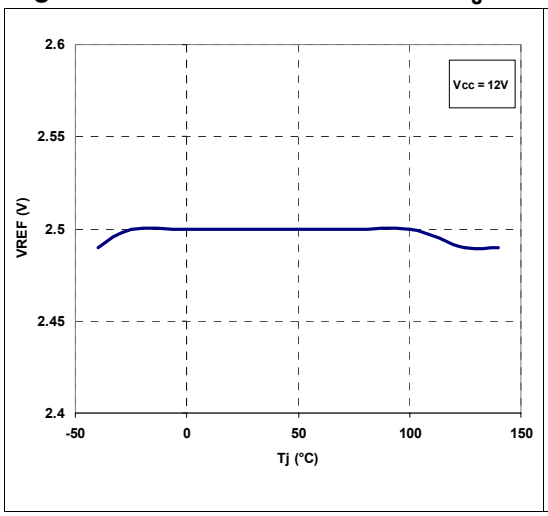


Figure 8. OVP current vs T_J

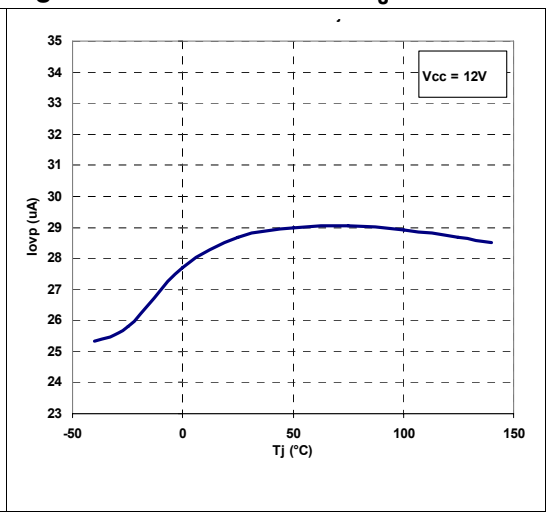


Figure 9. E/A output clamp levels vs T_J

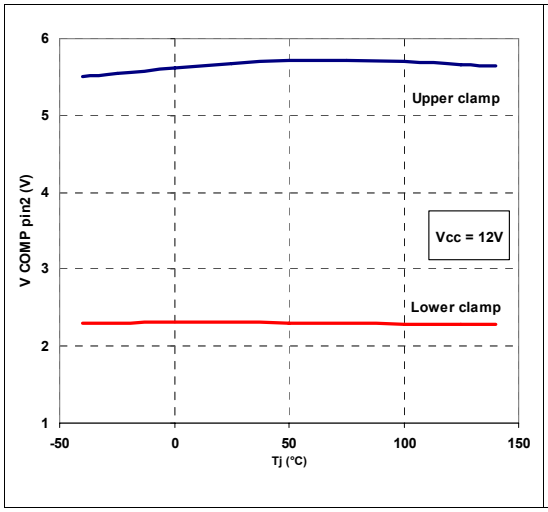


Figure 10. Delay-to-output vs T_J

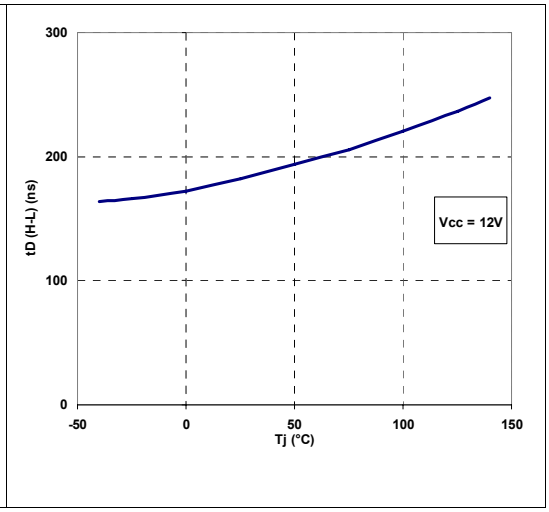


Figure 11. Multiplier characteristic

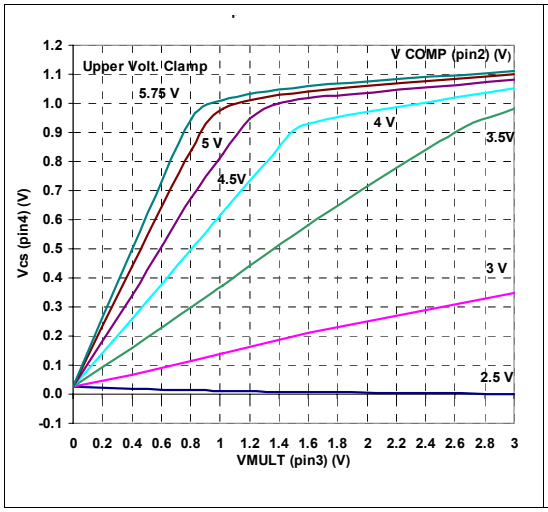


Figure 12. Vcs clamp vs T_J

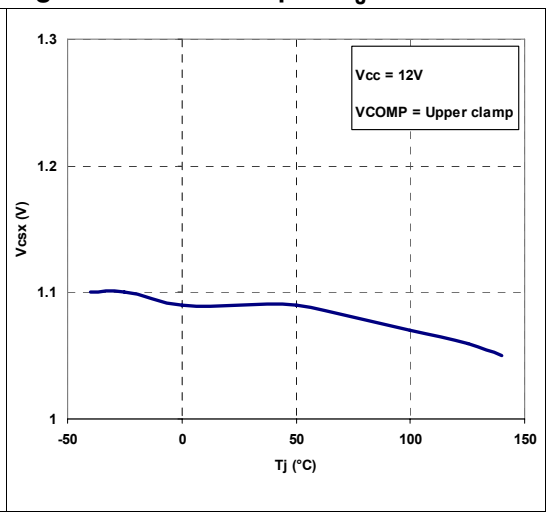


Figure 13. ZCD clamp levels vs T_J

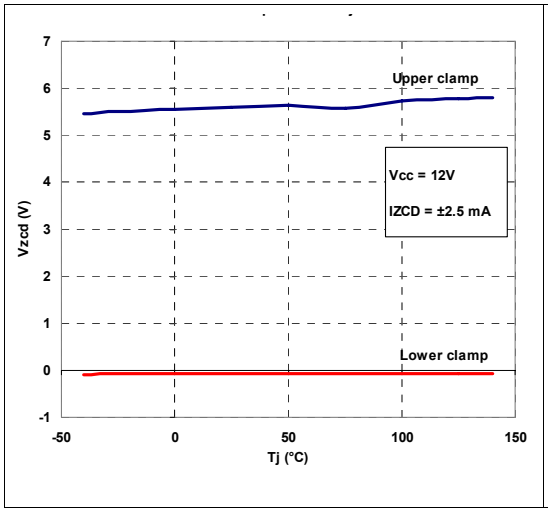


Figure 14. Start-up timer vs T_J

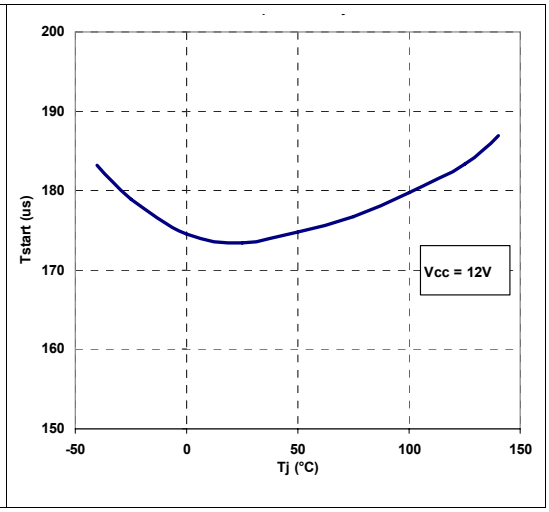


Figure 15. Gate-driver output low saturation

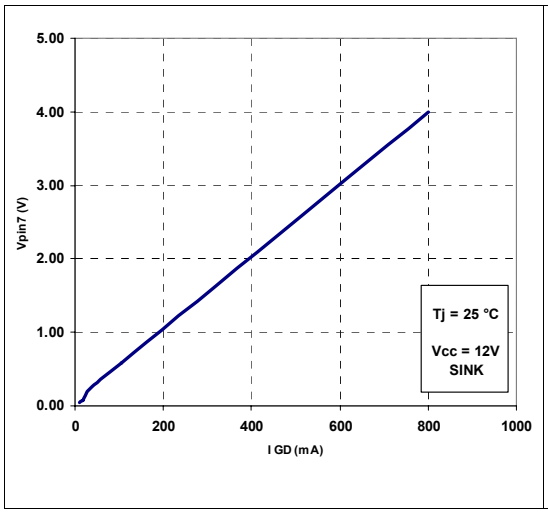


Figure 16. Gate-drive output high saturation

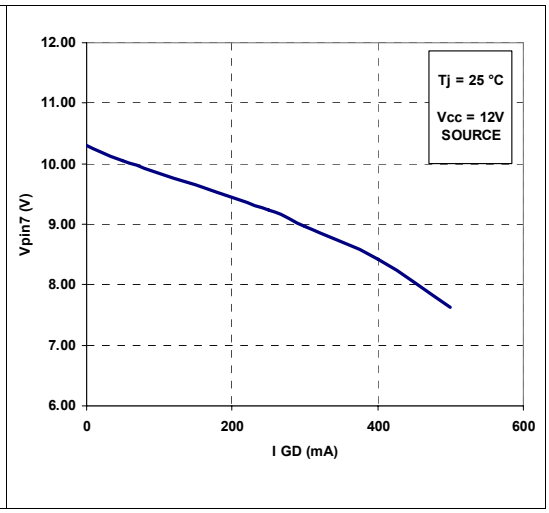


Figure 17. Gate-drive clamp vs T_J

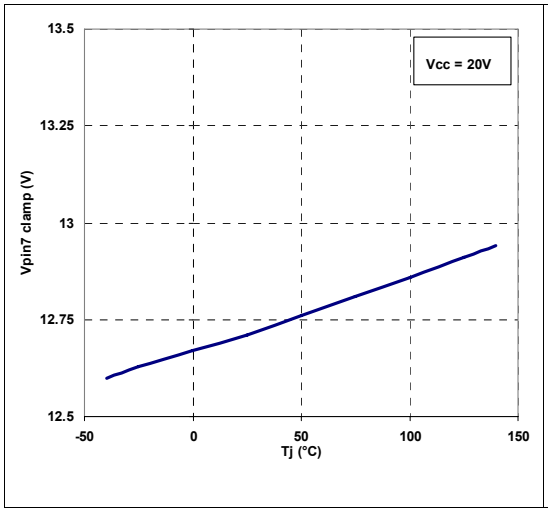
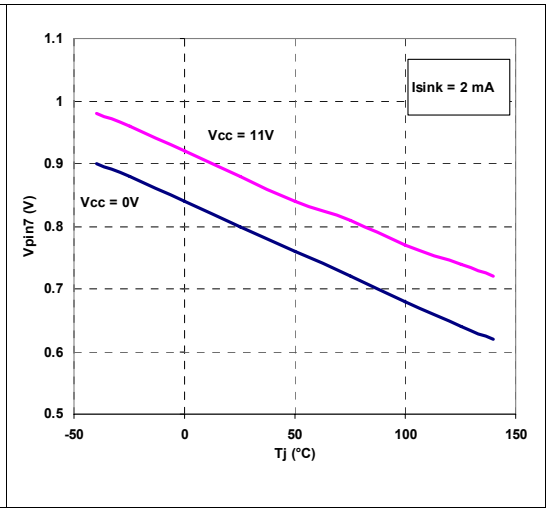


Figure 18. Output gate drive low saturation vs T_J during UVLO



7 Application information

7.1 Overvoltage protection

Under steady-state conditions, the voltage control loop keeps the output voltage Vo of a PFC pre-regulator close to its nominal value, set by the resistors R1 and R2 of the output divider. Neglecting ripple components, the current through R1, I_{R1}, equals that through R2, I_{R2}. Considering that the non-inverting input of the error amplifier is internally referenced at 2.5 V, also the voltage at pin INV will be 2.5 V, then:

Equation 1

$$I_{R2} = I_{R1} = \frac{2.5}{R2} = \frac{V_O - 2.5}{R1}$$

If the output voltage experiences an abrupt change $\Delta Vo > 0$ due to a load drop, the voltage at pin INV will be kept at 2.5 V by the local feedback of the error amplifier, a network connected between pins INV and COMP that introduces a long time constant to achieve high PF (this is why ΔVo can be large). As a result, the current through R2 will remain equal to 2.5/R2 but that through R1 will become:

Equation 2

$$I'_{R1} = \frac{V_O - 2.5 + \Delta V_O}{R1}$$

The difference current $\Delta I_{R1}=I'_{R1}-I_{R2}=I'_{R1}-I_{R1}= \Delta Vo/R1$ will flow through the compensation network and enter the error amplifier output (pin COMP). This current is monitored inside the device and if it reaches about 24 µA the output voltage of the multiplier is forced to decrease, thus smoothly reducing the energy delivered to the output. As the current exceeds 27 µA, the OVP is triggered (Dynamic OVP): the gate-drive is forced low to switch off the external power transistor and the IC put in an idle state. This condition is maintained until the current falls below approximately 7 µA, which re-enables the internal starter and allows switching to restart. The output ΔVo that is able to trigger the Dynamic OVP function is then:

Equation 3

$$\Delta V_O = R1 \cdot 20 \cdot 10^{-6}$$

An important advantage of this technique is that the OV level can be set independently of the regulated output voltage: the latter depends on the ratio of R1 to R2, the former on the individual value of R1. Another advantage is the precision: the tolerance of the detection current is 13%, i.e. 13% tolerance on ΔVo. Since $\Delta Vo << Vo$, the tolerance on the absolute value will be proportionally reduced.

Example: Vo = 400 V, ΔVo = 40 V. Then: R1 = 40 V/27 µA ≈ 1.5 MΩ;
R2 = 1.5 MΩ ·2.5/(400-2.5) = 9.43 kΩ. The tolerance on the OVP level due to the L6562AT will be 40·0.13 = 5.3 V, that is ± 1.2 %.

When the load of a PFC pre-regulator is very low, the output voltage tends to stay steadily above the nominal value, which cannot be handled by the Dynamic OVP. If this occurs, however, the error amplifier output will saturate low; hence, when this is detected the external power transistor is switched off and the IC put in an idle state (static OVP). Normal operation is resumed as the error amplifier goes back into its linear region. As a result, the device will work in burst-mode, with a repetition rate that can be very low.

When either OVP is activated the quiescent consumption of the IC is reduced to minimize the discharge of the Vcc capacitor and increase the hold-up capability of the IC supply system.

7.2 Disable function

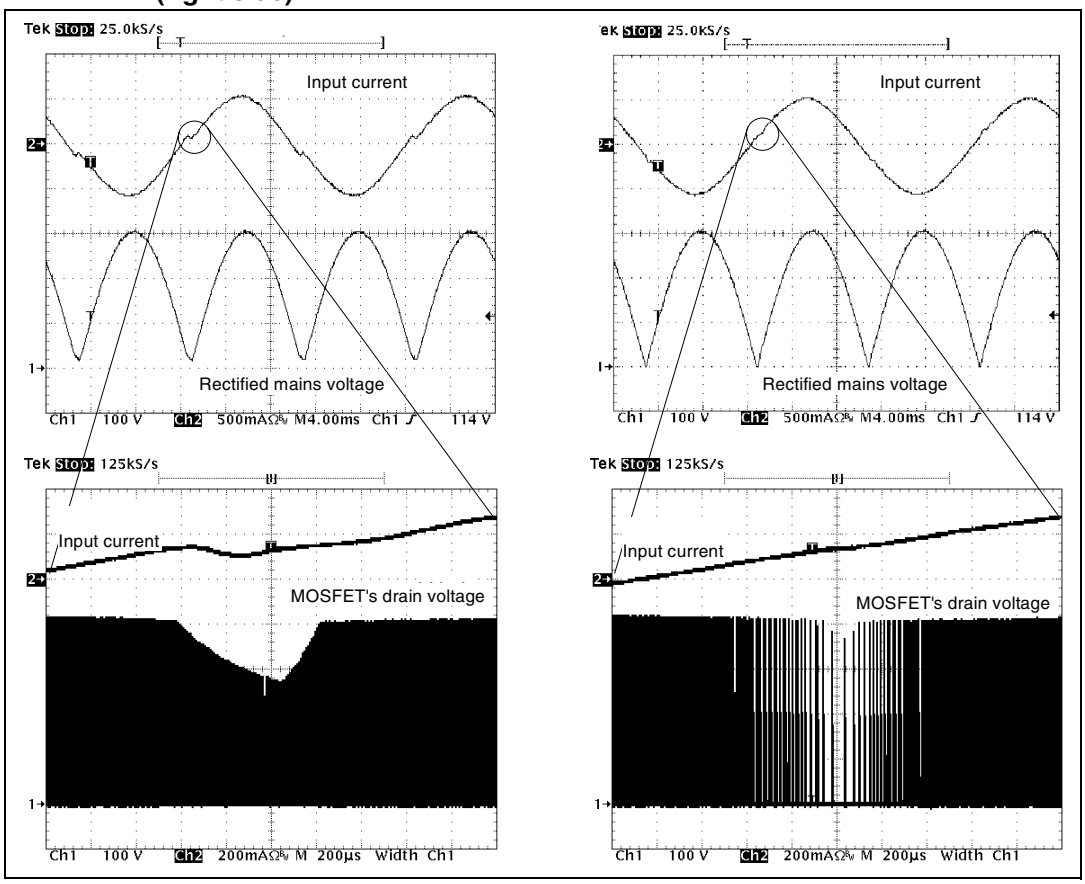
The INV pin doubles its function as a not-latched IC disable: a voltage below 0.2 V shuts down the IC and reduces its consumption at a lower value. To restart the IC, the voltage on the pin must exceed 0.45 V. The main usage of this function is a remote ON/OFF control input that can be driven by a PWM controller for power management purposes. However it also offers a certain degree of additional safety since it will cause the IC to shutdown in case the lower resistor of the output divider is shorted to ground or if the upper resistor is missing or fails open.

7.3 THD optimizer circuit

The device is equipped with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (total harmonic distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

Figure 19. THD optimization: standard TM PFC controller (left side) and L6562AT (right side)



To overcome this issue the circuit embedded in the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This will result in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge. The effect of the circuit is shown in figure 2, where the key waveforms of a standard TM PFC controller are compared to those of the L6562AT.

Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid.

To maximally benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - thus making the action of the optimizer circuit little effective.

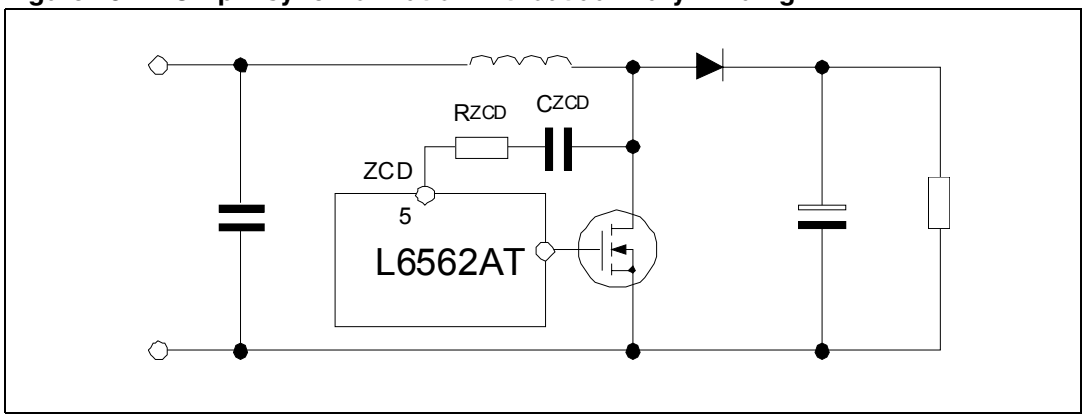
7.4 Operating with no auxiliary winding on the boost inductor

To generate the synchronization signal on the ZCD pin, the typical approach requires the connection between the pin and an auxiliary winding of the boost inductor through a limiting resistor. When the device is supplied by the cascaded DC-DC converter, it is necessary to introduce a supplementary winding to the PFC choke just to operate the ZCD pin.

Another solution could be implemented by simply connecting the ZCD pin to the drain of the power MOSFET through an R-C network as shown in figure 3: in this way the high-frequency edges experienced by the drain will be transferred to the ZCD pin, hence arming and triggering the ZCD comparator.

Also in this case the resistance value must be properly chosen to limit the current sourced/sunk by the ZCD pin. In typical applications with output voltages around 400 V, recommended values for these components are 22 pF (or 33 pF) for C_{ZCD} and 330 kΩ for R_{ZCD}. With these values proper operation is guaranteed even with few volts difference between the regulated output voltage and the peak input voltage

Figure 20. ZCD pin synchronization without auxiliary winding



7.5 Comparison between the L6562AT and the L6562

The L6562AT is not a direct drop-in replacement of the L6562, even if both have the same pin-out. One function (Disable) has been relocated.
Table 2 compares the two devices, i.e. those parameters that may result in different values of the external components. The parameters that have the most significant impact on the design, i.e. that definitely require external component changes when converting an L6562-based design to the L6562AT, are highlighted in bold.

Table 6. L6562AT vs L6562

Parameter	L6562	L6562AT
IC turn-on and turn-off thresholds (typ.)	12/9.5 V	12.5/10 V
Turn-off threshold spread (max.)	±0.8 V	±0.5 V
IC consumption before start-up (max.)	70 uA	60 uA
Multiplier gain (typ.)	0.6	0.38
Current sense reference clamp (typ.)	**1.7 V**	**1.08 V**
Current sense propagation delay (delay-to-output) (typ.)	200 ns	175 ns
Dynamic OVP triggering current (typ.)	**40 µA**	**27 µA**
ZCD arm/trigger/clamp thresholds (typ.)	2.1/1.4/0.7 V	1.4/0.7/0 V
Enable threshold (typ.)	0.3 V (1)	0.45 V (2)
Gate-driver internal drop (max.)	2.6 V	2.2 V
Leading-edge blanking on current sense	No	Yes
Reference voltage accuracy (overall)	**2.4%**	**1.8%**

1. Function located on pin 5 (ZCD)
2. Function located on pin 1 (INV)

The lower value (-36%) for the clamp level of the current sense reference voltage allows the use of a lower sense resistor for the same peak current, with a proportional reduction of the associated power dissipation. Essentially, the advantage is the reduction of the power dissipated in a single point (hotspot), which is a considerable benefit in applications where heat removal is critical, e.g. in adapters enclosed in a sealed plastic case. The lower value for the dynamic OVP triggering current allows the use of a higher resistance value (+48%) for the upper resistor of the divider sensing the output voltage of the PFC stage (keeping the same overvoltage level) with no significant increase of noise sensitivity. This reduction goes in favor of standby consumption in applications required to comply with energy saving regulations.

8 Application examples and ideas

Figure 21. Demonstration board wide-range mains: electrical schematic

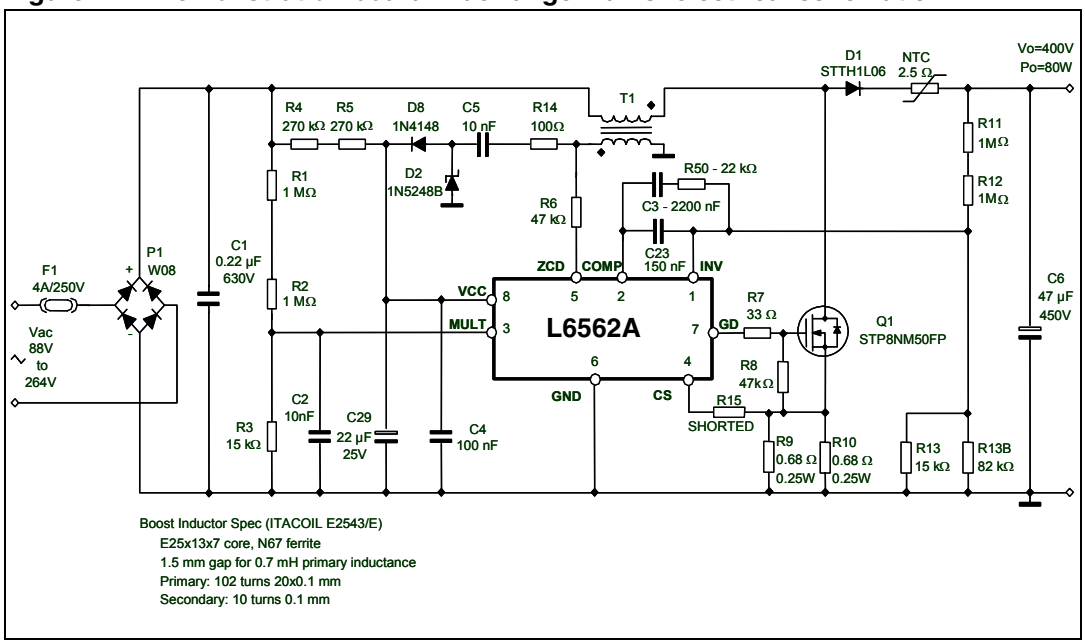
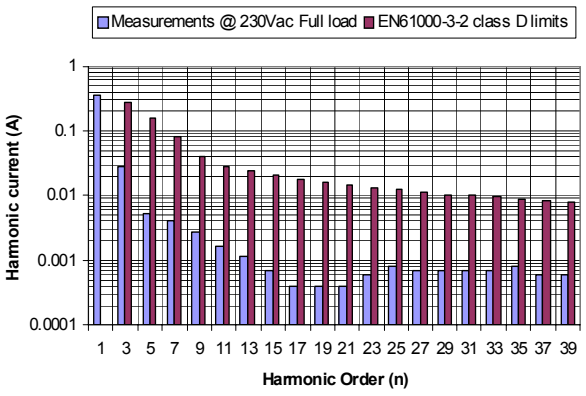
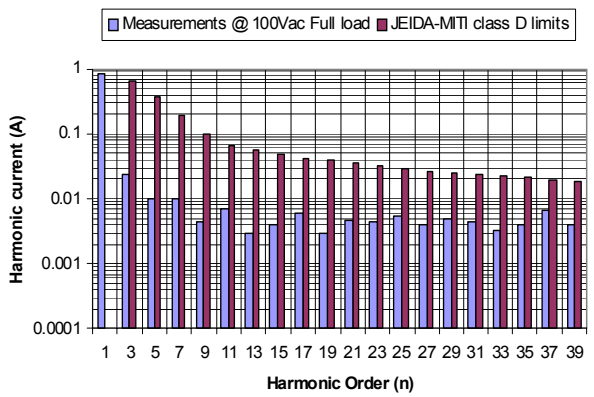


Figure 22. L6562A 80W TM PFC evaluation board: compliance to EN61000-3-2 standard



Vin = 230 Vac - 50 Hz, Pout = 80 W
THD = 10.48%, PF = 0.973

Figure 23. L6562A 80W TM PFC evaluation board: compliance to JEIDA-MITI standard



Vin = 100 Vac - 50 Hz, Pout = 80 W
THD = 3.18%, PF = 0.997

Figure 24. L6562A 80W TM PFC evaluation board: input current waveform @230 V-50 Hz – 80W load

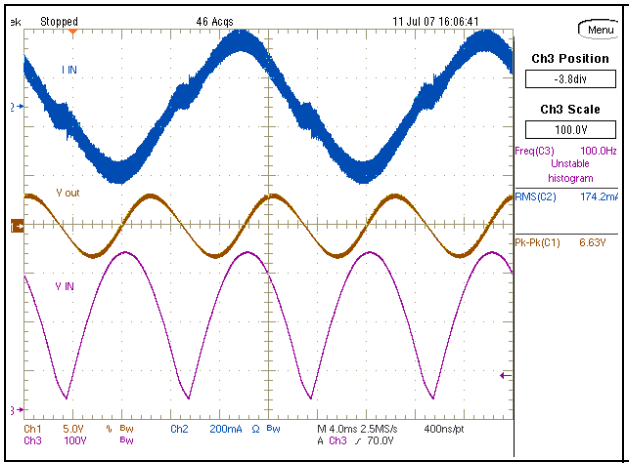


Figure 25. L6562A 80W TM PFC evaluation board: input current waveform @100 V-50 Hz – 80 W load

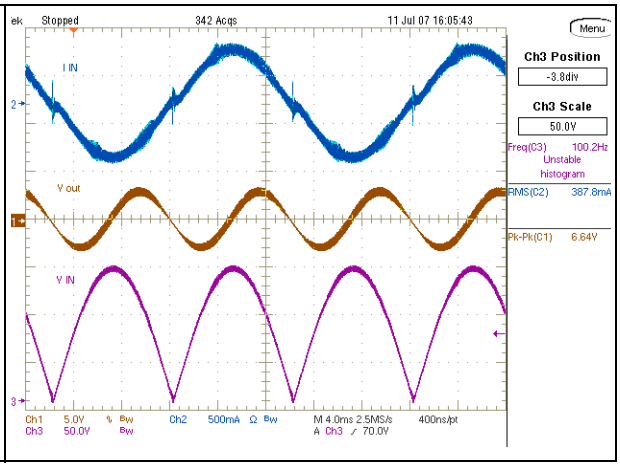


Figure 26. L6562A 80W TM PFC evaluation board: power factor vs Vin

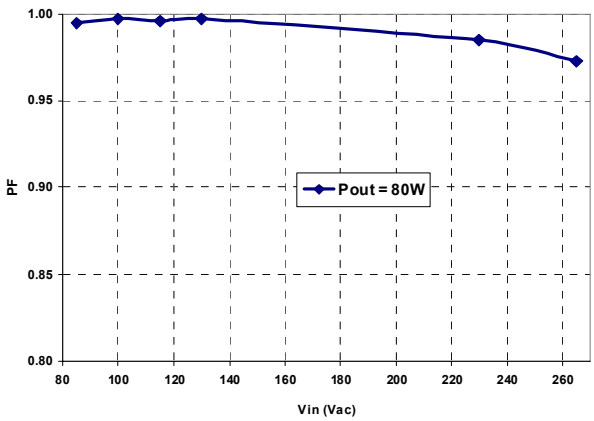


Figure 27. L6562A 80W TM PFC evaluation board: THD vs Vin

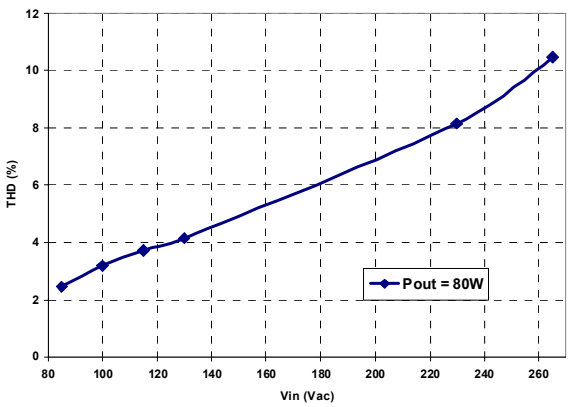


Figure 28. L6562A 80W TM PFC evaluation board: efficiency vs Vin

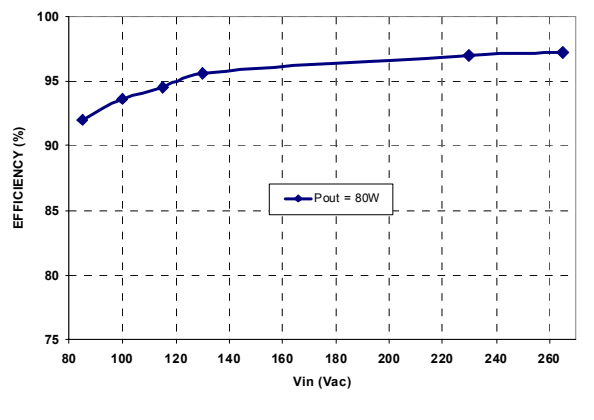


Figure 29. L6562A 80W TM PFC evaluation board: static Vout regulation vs Vin

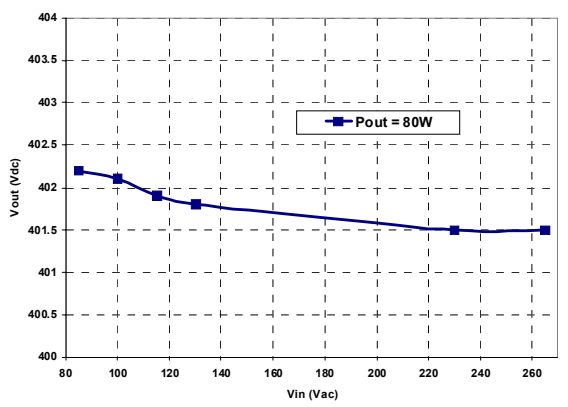
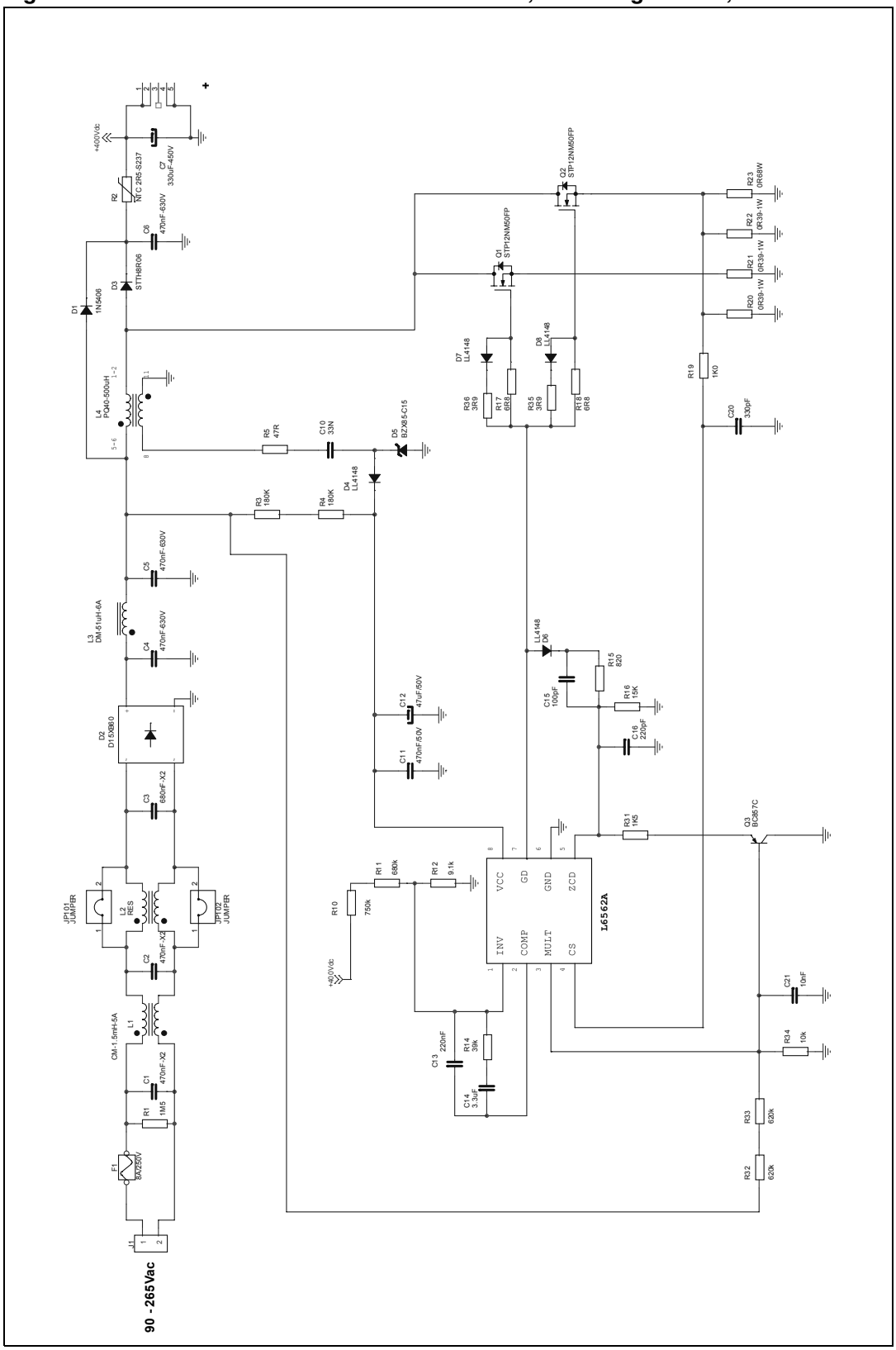


Figure 30. Demonstration board EVL6562A-400W, wide-range mains, FOT



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
ECOPACK® is an ST trademark.

Table 7. DIP-8 mechanical data

Dim.	mm			Inch		
	Min	Typ	Max	Min	Typ	Max
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

Figure 31. Package dimensions

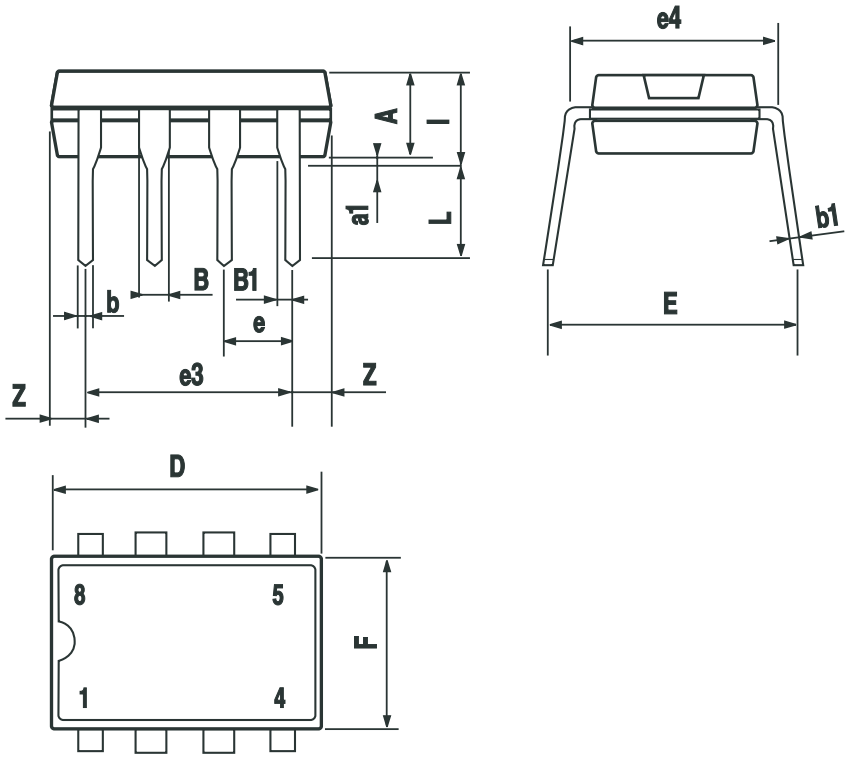
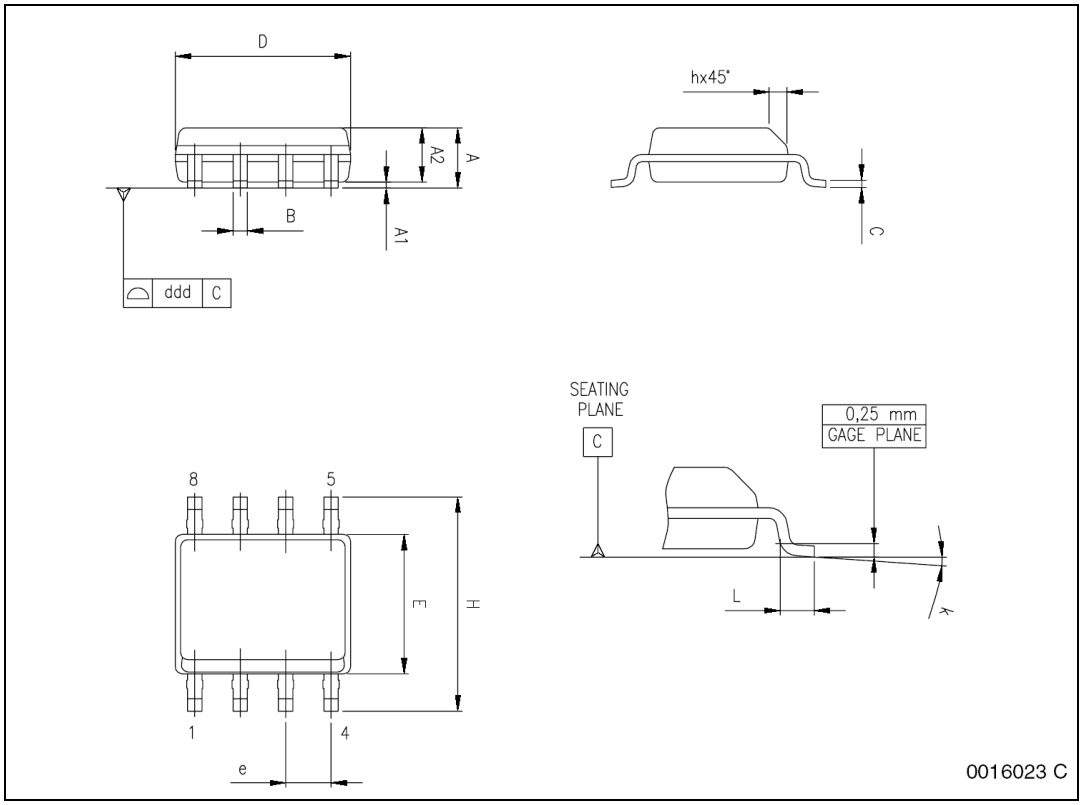


Table 8. SO-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 32. Package dimensions



10 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Jan-2009	1	First release
04-Mar-2009	2	Updated *Table 5 on page 6*

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