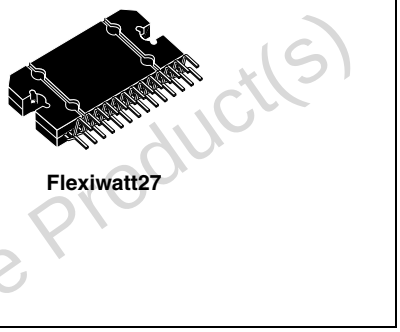
L5955

Multiple multifunction voltage regulator for car radio

Features

- 2 stand-by regulators:
  3.3V (125mA)
  1.5V (300mA)
- 6 regulators:
  10V (40mA)
  8.5V (200mA)
  3.3V (850mA)
  8/10V (1A)
  5/3.3/1.8V (200mA)
  1.8/2.5V(200mA)
- All regulators are low dropout outputs
- The different outputs voltage are controlled by I^2C Bus.
- Reg3 on/off controlled by enable
- Reg1, Reg2, Reg4, Reg5, Reg6 on/off controlled by I^2CBus.
- 3 high side drivers:
  2A (HSD1)
  0.45A (HSD2 & HSD3)
- No external charge pump capacitors are required
- Stand-by mode controlled by EN pin for I^2C Bus and Reg1, Reg2, Reg3, Reg4, Reg5, Reg6, HSD1, HSD2, HSD3
- LVW function externally selectable
- Individual thermal shutdown



Flexiwatt27

- Independent current limiting
- Short circuit protection
- Load dump protection and overvoltage shutdown

Description

The L5955 is an integration of three high side drivers, six regulators and two stand-by regulators with RESET function developed to provide the power to a complete audio system.

The outputs of the IC are controlled by I^2C bus and Enable pin.

The device is equipped with sequencing and slew rate controls for the st-by regulators.

Obsolete Product(s) - Obsolete Product(s)

Table 1. Device summary

Order code	Package	Packing
L5955	Flexiwatt27	Tube

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1 Block and pin connection diagrams

Figure 1. Block diagram

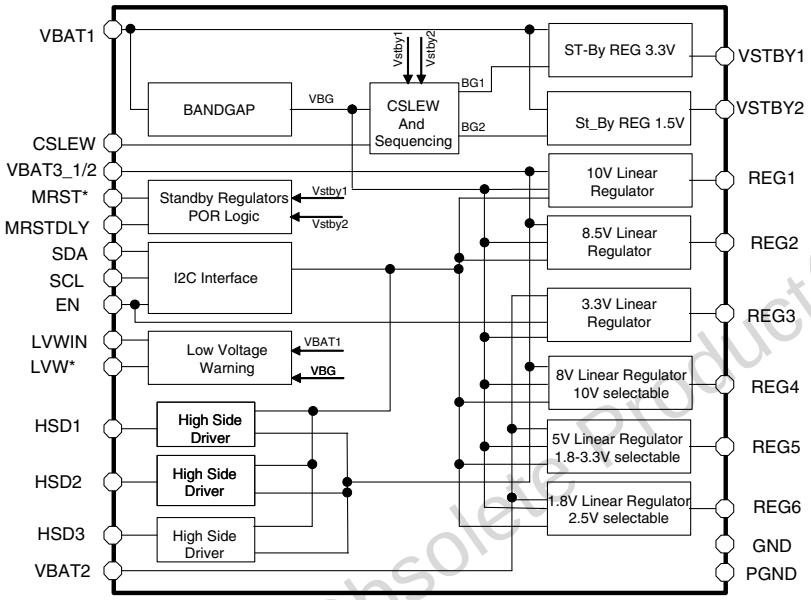
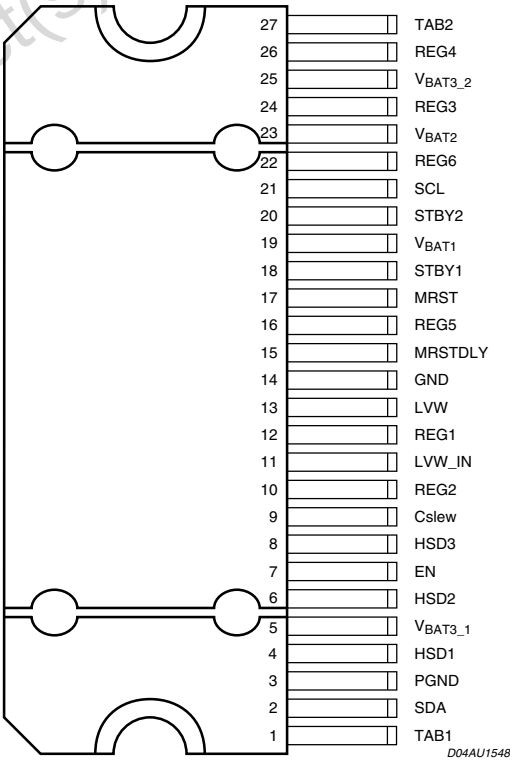


Figure 2. Pin connection (top view)



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2 Electrical specification

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VS1, VS2, VS3_1, VS3_2	DC operating supply voltage	0.6 to 26.5	V
VS1, VS2, VS3_1, VS3_2	Transient supply over voltages, rise time = 10ms delay time = 115ms	34	V
$V_{S1,2,3_1,3_2,ovs}$	Overvoltage shutdown	27	V
V_{in}	Input voltages (EN, SDA, SCL, LVW, MRST, MRSTDLY, CSLEW)	-0.6 to 5.5	V
V_{out}	Output control voltage	-0.6 to 18	V
T_{op}	Operating temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-40 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	1	°C/W

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2.3 Electrical characteristics

Table 4. Electrical characteristics

(Refer to the application circuit, V_{bat} =V_{bat1}+V_{bat2}+V_{bat3}= 14V, I_{ST-BY1} = 0.5mA, I_{ST-BY2} = 0.5mA, I_{REG1} = I_{REG2} = I_{REG3} = I_{REG4} = I_{REG5} = I_{REG6} = 5mA, R_{HSD1} = R_{HSD2} = R_{HSD3} = 16Ω)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{qST-BY}	Stand-by quiescent current	V_{bat} = 14V, EN = 0. I_{ST-BY1} = Istby2=100uA, IQ(Vbat)=Ivbat1+Ivabt2+Ivbat3			170	µA
I_q	Maximum quiescent current	V_{bat} = 14V, EN=VSTBY1 Istby1=125mA Istby2=300mA I_{REG1} = 40mA I_{REG2} = 200mA, I_{REG3} = 850mA I_{REG4} = 1A, I_{REG5} = 250mA I_{REG6} = 200mA, I_{HSD1} = 2A $I_{HSD2,3}$ = 450mA		100		mA
I_{EN}	Enable input current	V_{bat} = 14V; 5V<Enable ≥ 0V;			10	µA
V_{IL} V_{IH}	Enable threshold voltage	V_{bat} = 14V;	 2		0.8	V V
$V_{L\ MRST}$	MRST output voltage	V_{ST-BY1} = 0.5V to V_{TH} (ST-BY1) V_{ST-BY2} = 0.5V to V_{TH} (ST-BY2) Rising	0 0		0.4 0.4	V
$V_{H\ MRST}$		V_{ST-BY1} = V_{TH} (ST-BY1) to 0.5V V_{ST-BY2} = V_{TH} (ST-BY2) to 0.5V Falling	0 0		0.4 0.4	V
$V_{TH\ MRST}$	MRST output voltage threshold	Force V_{ST-BY1} & V_{ST-BY2} Low until MRST asserted	V_{ST-BY2} · 0.93 V_{ST-BY1} · 0.93		V_{ST-BY2} · 0.97 V_{ST-BY1} · 0.97	V V
$t_{d\ MRST}$	MRST delay time	see *Figure 4*		13		µs
$t_{por\ MRST}$	Power on reset delay time	CMRSTLY = 220nF see *Figure 4*	20			ms
$t_{f\ MRST}$	MRST fall time	R_{RST} = 47kΩ, C_{RST} = 50pF see *Figure 4*			1	µs
$I_{SCR\ MRST}$	MRSTDLY current	MRSTDLY = 0	6		12	µA
I_{LKG} MRSTDLY	MRSTDLY leakage current	MRSTDLY = 5V			6	µA
V_{sat} MRSTDLY	MRSTDLY saturation voltage	$I_{MRSTDLY}$ =0.5mA	0		0.4	V
V_{TH}	LVWIN input voltage threshold	1.25 V (nominal)	1.22		1.28	V
I_{LKG}	lvwin input leakage current				2	µA
V_{OH}	LVW output voltage	I_{OH}=-100µA	V_{STBY1} -0.2		V_{STBY1}	V

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical characteristics (continued)

(Refer to the application circuit, $V_{bat} = V_{bat1}+V_{bat2}+V_{bat3}$= 14V, I_{ST-BY1} = 0.5mA, I_{ST-BY2} = 0.5mA, $I_{REG1} = I_{REG2} = I_{REG3} = I_{REG4} = I_{REG5} = I_{REG6}$ = 5mA, $R_{HSD1} = R_{HSD2} = R_{HSD3}$ = 16Ω)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL}	LVW output voltage	I_{OL} = 100µA	0		0.2	V
T_S	Thermal shutdown for HSDS, REGS, V_{ST-BY1}, V_{ST-BY2}	HSDS, REGS, V_{ST-BY1}, V_{ST-BY2} min. load. Increase T_{amb} until HSDS, REGS, $V_{ST-BY1,2}$ Disabled		170		°C
$T_{S\ HYS}$	Thermal shutdown hysteresis for HSDS, REGS, V_{ST-BY1}, V_{ST-BY2}	HSDS, REGS, V_{ST-BY1}, V_{ST-BY2} min. load. Decrease T_{amb} until HSDS, REGS, $V_{ST-BY1,2}$ Disabled		10		°C
I_o	CSLEW output current		7		14	µA
t_{on}	ST-BY1, ST-BY2. minimum turn on time	C_{SLEW}=7nF; see *Figure 5*	1.6			ms
3.3V/125mA V_{ST-BY1}						
V_{ST-BY1}	Output voltage	I_{ST-BY1} = 125mA	3.14		3.46	V
ΔV_{line}	Line regulation	7V ≤ V_{BAT} ≤ 18V (Measure ΔVreg1 across V_{BAT} range)			10	mV
ΔV_{load}	Load regulation	0.5mA ≤ I_{ST-BY1} ≤ 125mA (Measure ΔVreg1 across V_{BAT} range)			50	mV
I_{q1}	Δ Quiescent current (measure ΔI_{BAT})	I_{ST-BY1} = 2mA, V_{BAT} = 14V, I_{ST-BY1} = 125mA, V_{BAT} = 14V			150 10	µA mA
$V_{DROPOUT}$	Dropout voltage (measure V_{BAT} - V_{ST-BY1} when V_{ST-BY1}drops 0.1V)	I_{ST-BY1} = 125mA I_{ST-BY1} = 5mA			2.6 1.2	V V
I_{lim1}	Current limit		160		350	mA
ΔV_{lead}	V_{ST-BY1} absolute differential output voltage	force V_{ST-BY2} Low; Measure V_{ST-BY1} - V_{ST-BY2}			2.5	V
ΔV_{lag}		force V_{ST-BY1} Low; Measure V_{ST-BY1} - V_{ST-BY2}			0.25	V
SVR1	Supply voltage rejection ST-BY1	f_o = 120-10kHz, V_{BAT} = 14V with 1.0Vp-p AC, f_o = 20-20kHz, V_{BAT} = 14V with 1.0Vp-p AC	50 45			dB dB
1.5V/300mA V_{ST-BY2}						
V_{ST-BY2}	Output voltage	I_{ST-BY2} = 300mA	1.425		1.575	V
ΔV_{line}	Line regulation	7V ≤ V_{BAT} ≤ 18V (measure Δ V_{ST-BY2} across V_{BAT} range)			50	mV

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Table 4. Electrical characteristics (continued)

(Refer to the application circuit, $V_{bat} = V_{bat1}+V_{bat2}+V_{bat3}$= 14V, I_{ST-BY1} = 0.5mA, I_{ST-BY2} = 0.5mA, $I_{REG1} = I_{REG2} = I_{REG3} = I_{REG4} = I_{REG5} = I_{REG6}$ = 5mA, $R_{HSD1} = R_{HSD2} = R_{HSD3}$ = 16Ω)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ΔV_{load}	Load regulation	0.5mA ≤ I_{ST-BY2} ≤ 300mA			100	mV
$V_{DROPOUT}$	Dropout voltage (measure V_{BAT} - V_{ST-BY2} when V_{ST-BY2} drops0.1V)	I_{ST-BY2} = 300mA I_{ST-BY2} = 5mA			4.1 3	V V
I_{lim2}	Current limit		360		700	mA
SVR3	Supply voltage rejection ST-BY2	f_o = 120-10kHz, V_{BAT} = 14V with 1.0Vp-p AC, f_o = 20-20kHz, V_{BAT} = 14V with 1.0Vp-p AC	50 45			dB dB
10V/40mA REG1 output						
V_{REG1}	Output voltage	I_{REG1} = 40mA	9.50	10	10.5	V
ΔV_{line}	Line regulation	11.4V ≤ V_{BAT}≤ 18V (measure Δ V_{REG1} across V_{BAT} range)			55	mV
ΔV_{load}	Load regulation	5mA ≤ I_{REG1} ≤ 40mA			55	mV
$V_{DROPOUT}$	Dropout voltage (measure V_{BAT} - V_{REG1} when V_{REG1} drops 0.1V)	I_{REG1} = 40mA I_{REG1} = 5mA			1200 300	mV mV
I_{lim1}	Current limit		60		200	mA
SVR	Supply voltage rejection (guaranteed by characterization-test at 1kHz with 50dB Limit)		50			dB
8.5V/200mA REG2 output						
V_{REG2}	Output voltage	I_{REG2} = 200mA	8.3	8.5	8.7	V
ΔV_{line}	Line regulation	9.6V ≤ V_{BAT} ≤ 18V (measure Δ V_{REG2} across V_{BAT} range)			50	mV
ΔV_{load}	Load regulation	5mA ≤ I_{REG2} ≤ 200mA			50	mV
$V_{DROPOUT}$	Dropout voltage (measure V_{BAT} - V_{REG2} when V_{REG2} drops 0.1V)	I_{REG2} = 200mA I_{REG2} = 5mA			1100 600	mV mV
I_{lim2}	Current limit		225		525	mA
SVR	Ripple rejection (guaranteed By characterization-test at 1kHz with 50dB limit)		50			dB
3.3V/850mA REG3 output						
V_{REG3}	Output voltage	I_{REG3} = 850mA	3.14		3.46	V
ΔV_{line}	Line regulation	7V ≤ V_{BAT} ≤ 18V (Measure Δ V_{REG2} Across V_{BAT} range)			40	mV
ΔV_{load}	Load regulation	5mA ≤ I_{REG3} ≤ 850mA			100	mV
$V_{DROPOUT}$	Dropout voltage (measure V_{BAT} - V_{REG3} when V_{REG3} drops 0.1V)	I_{REG3} = 850mA I_{REG3} = 5mA			3.46 2.86	V V

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical characteristics (continued)

(Refer to the application circuit, $V_{bat} = V_{bat1}+V_{bat2}+V_{bat3}$= 14V, $I_{ST\text{-}BY1}$ = 0.5mA, $I_{ST\text{-}BY2}$ = 0.5mA, $I_{REG1} = I_{REG2} = I_{REG3} = I_{REG4} = I_{REG5} = I_{REG6}$ = 5mA, $R_{HSD1} = R_{HSD2} = R_{HSD3}$ = 16Ω)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{lim4}	Current limit		1.25		2.5	A
SVR	Ripple rejection (guaranteed by characterization-test at 1kHz with 50dB Limit)		50			dB
8V/10V/1A REG4 output						
V_{REG4}	Output voltage	I_{REG4} = 1A	7.6 9.50		8.4 10.5	V V
ΔV_{line}	Line regulation	11.4V ≤ V_{BAT} ≤ 18V, For V_{REG4}=10V 9.3V<V_{BAT}<18V For V_{REG4}=8V (measure Δ V_{REG4} across V_{BAT} range)			50 50	mV mV
ΔV_{load}	Load regulation	5mA ≤ I_{REG4}≤ 1A			150	mV
$V_{DROPOUT}$	Dropout voltage (measure V_{BAT} - V_{REG4} when V_{REG4} drops 0.1V)	I_{REG4} = 1A I_{REG4} = 5mA			1.100 600	mV mV
I_{lim4}	Current limit		1.5		3	A
SVR	Ripple rejection (guaranteed By characterization-test at 1kHz with 50dB Limit)		50			dB
1.8-3.3-5V/250mA REG5 output						
V_{REG5}	Output voltage	I_{REG5} = 250mA	1.71 3.14 4.75		1.89 3.46 5.25	V V V
ΔV_{line}	Line regulation	7V ≤ V_{BAT} ≤ 18V for V_{REG5}=1.8V, 3.3V 9V<V_{BAT}>18V for V_{REG5}=5V (measure Δ V_{REG5} across V_{BAT} range)			40	mV
ΔV_{load}	Load regulation	5mA ≤ I_{REG5} ≤ 250mA			100	mV
$V_{DROPOUT}$	Dropout voltage (measure V_{BAT} - V_{REG5} when V_{REG5} drops 0.1V)	I_{REG5} = 250mA @ V_{REG5}=1.8V I_{REG5} = 5mA @ V_{REG5}=1.8V I_{REG5} = 250mA @ V_{REG5}=3.3V I_{REG5} = 5mA @ V_{REG5}=3.3V I_{REG5} = 250mA @ V_{REG5}=5V I_{REG5} = 5mA @ V_{REG5}=5V			4.89 4.29 3.46 2.86 1.85 1.25	V V V V V V
I_{lim5}	Current limit		300		700	mA
SVR	Ripple rejection (guaranteed by characterization-test at 1kHz with 50dB limit)		50			dB

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical characteristics (continued)

(Refer to the application circuit, $V_{bat} = V_{bat1}+V_{bat2}+V_{bat3}$= 14V, $I_{ST\text{-}BY1}$ = 0.5mA, $I_{ST\text{-}BY2}$ = 0.5mA, $I_{REG1} = I_{REG2} = I_{REG3} = I_{REG4} = I_{REG5} = I_{REG6}$ = 5mA, $R_{HSD1} = R_{HSD2} = R_{HSD3}$ = 16Ω)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1.8-2.5V/200mA REG6 output						
V_{REG6}	Output voltage	I_{REG6} = 200mA	1.71 2.38		1.89 2.62	V V
ΔV_{line}	Line regulation	7V ≤ V_{BAT} ≤ 18V (measure Δ V_{REG6} across V_{BAT} range)			40	mV
ΔV_{load}	Load regulation	5mA ≤ I_{REG6} ≤ 200mA			50	mV
$V_{DROPOUT}$	Dropout voltage (measure V_{BAT} - V_{REG6} when V_{REG6} drops 0.1V)	I_{REG6} = 200mA @ V_{REG6}=1.8V I_{REG6} = 5mA @ V_{REG6}=1.8V I_{REG6} = 200mA @ V_{REG6}=2.5V I_{REG6} = 5mA @ V_{REG6}=2.5V			4.89 4.29 4.22 3.62	V V V V
I_{lim6}	Current limit		240		600	mA
SVR	Ripple rejection (guaranteed by characterization-test at 1kHz with 50dB limit)		50			dB
2A HSD1						
V_{sat}	Output saturation voltage	IHSD1 = 1A continuous time operation IHSD1=2A t=5seconds			0.6 1.2	V V
I_{leak1}	Output leakage current	All Driver Outputs are Off			50	µA
I_{lim}	Current limiting	R_{HSD1} = 0.5Ω	2.4		4	A
0.45A HSD2 & HSD3						
V_{sat}	Output saturation voltage	IHSD2,3 = 300mA continuous time operation IHSD2,3=450mA t=5 seconds			0.6 1.2	V V
$I_{leak2,3}$	Output leakage current	All driver outputs are Off			50	µA
I_{lim}	Current limiting	$R_{HSD2,3}$ = 0.5Ω	0.550		1	A
Characteristics for I^2C						
V_{IL}	LOW level input voltage				1.5	V
V_{IH}	HIGH level input voltage		3			V
V_{HYS}	Input hysteresis		0.2			V
V_{OL1} V_{OL1}	LOW level output	Sink current = 3mA Sink current = 6mA			0.4 0.6	V V
I_1	Input current	0.5V ≤ V_I ≤ 4.5V			10	µA
f_{SCL}	SCL clock frequency				400	kHz

Obsolete Product(s) - Obsolete Product(s)

3 Functional description

The three high side drivers are one 2A output (HSD1) and two 450mA outputs (HSD2 & 3).

The six regulator outputs are 10V at 40mA (REG1), 8.5V at 200mA (REG2), 3.3V at 850mA (REG3), 8/10V at 1A (REG4), 1.8V/3.3V/5V at 250mA (REG5) and 1.8V/2.5V at 200mA (REG6).

The two stand-by regulators are 3.3V at 125mA (ST-BY1) and 1.5V at 300mA (ST-BY2).

ST-BY1 and ST-BY2 are equipped with Reset function.

ST-BY1 and ST-BY2 share one Reset output (MRST).

A slew rate limiter and a sequencing function control ST-BY1 and ST-BY2 turn on/off.

The 8.5V regulator output (REG2) has a tighter tolerance output than the other regulator outputs.

The 8.5V output is a ±2.5% (5% total range) output over temperature to improve performance and reduce cost on the 8.5V output. The other outputs are ±5% over temperature.

The two STAND-BY regulators are switched on/off from battery line.

The REG3 is switched on/off by Enable pin which also activate the I^2C BUS.

The other Regulators and HSD's are turned on/off independently by I^2C BUS, which also controls the regulators' output voltages.

With ENABLE pin set to 0 the total current sunk from the battery line minimized.

Figure 3. Reset and power-on reset schematic

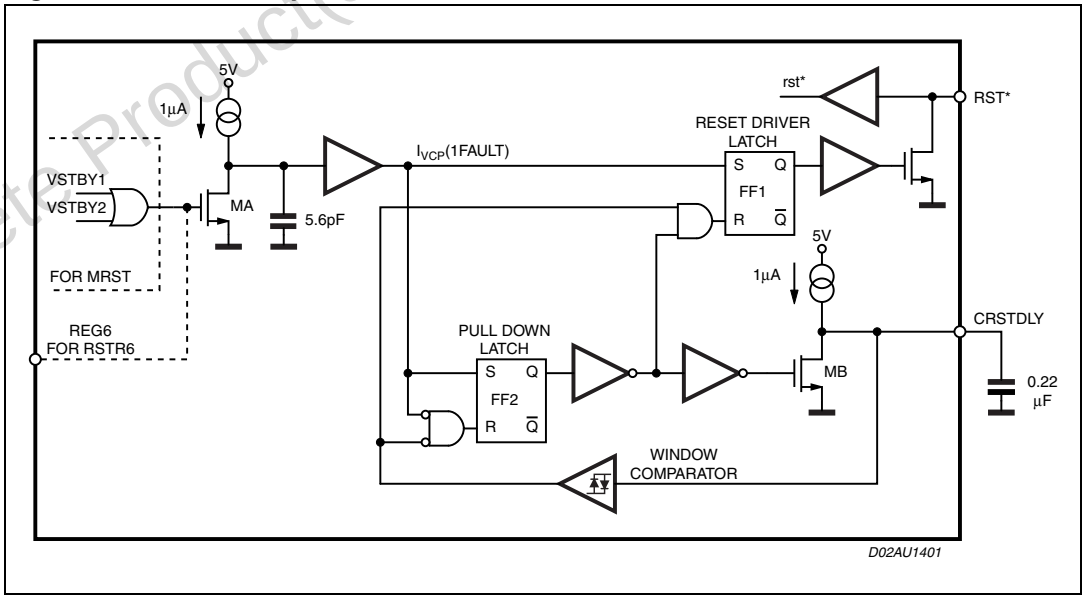

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Figure 4. Reset timing

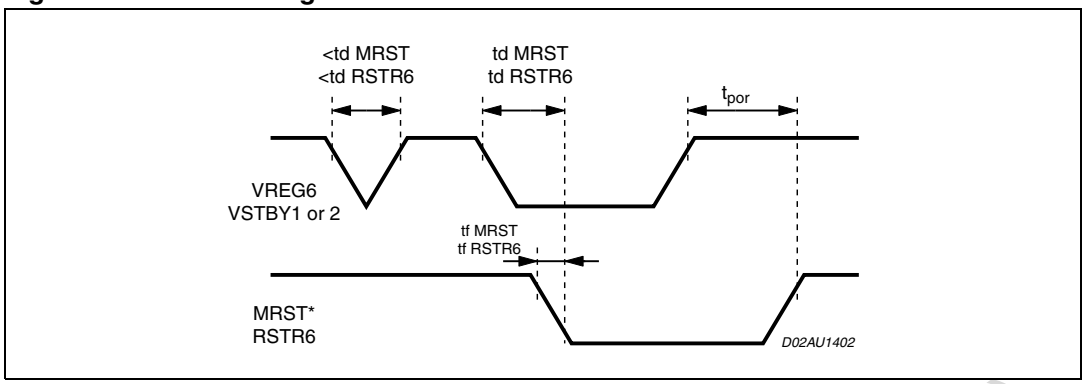

Figure 5. SLEW function

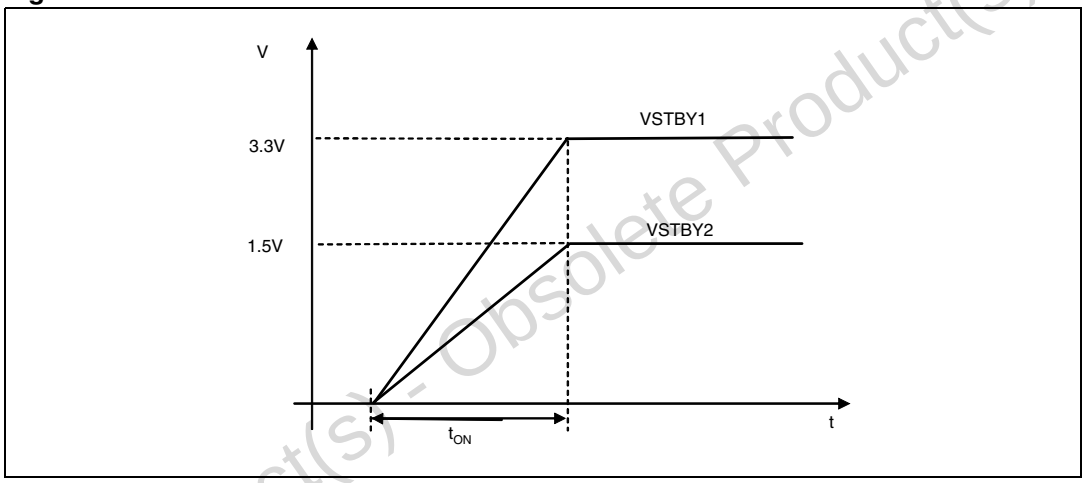

Figure 6. Sequencing function

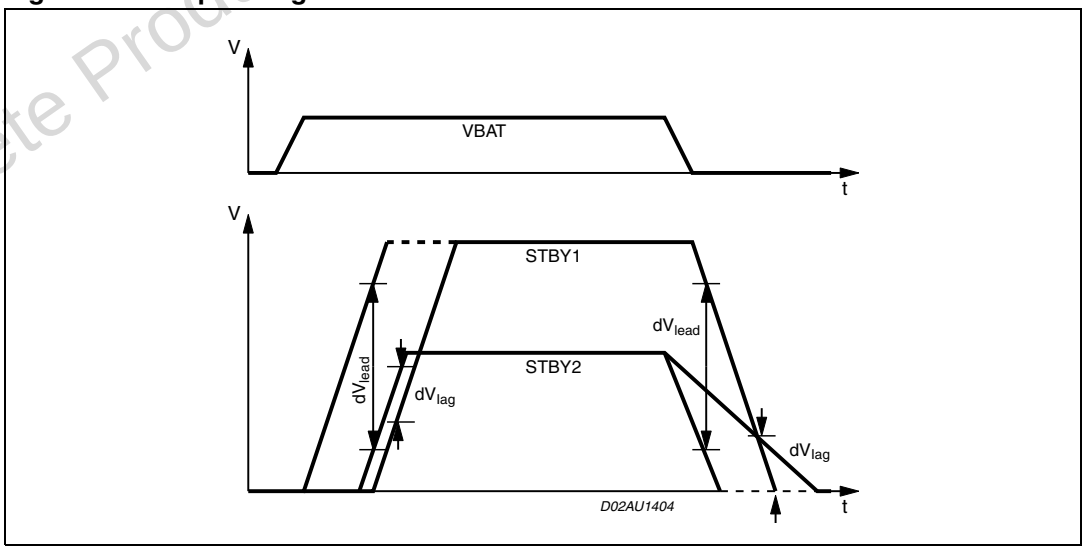

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Figure 7. Definition of timing on the I²C Bus.

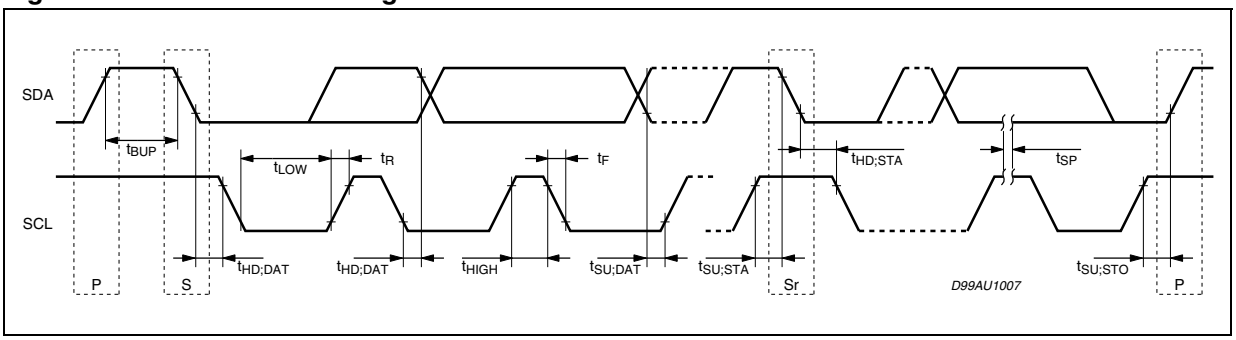
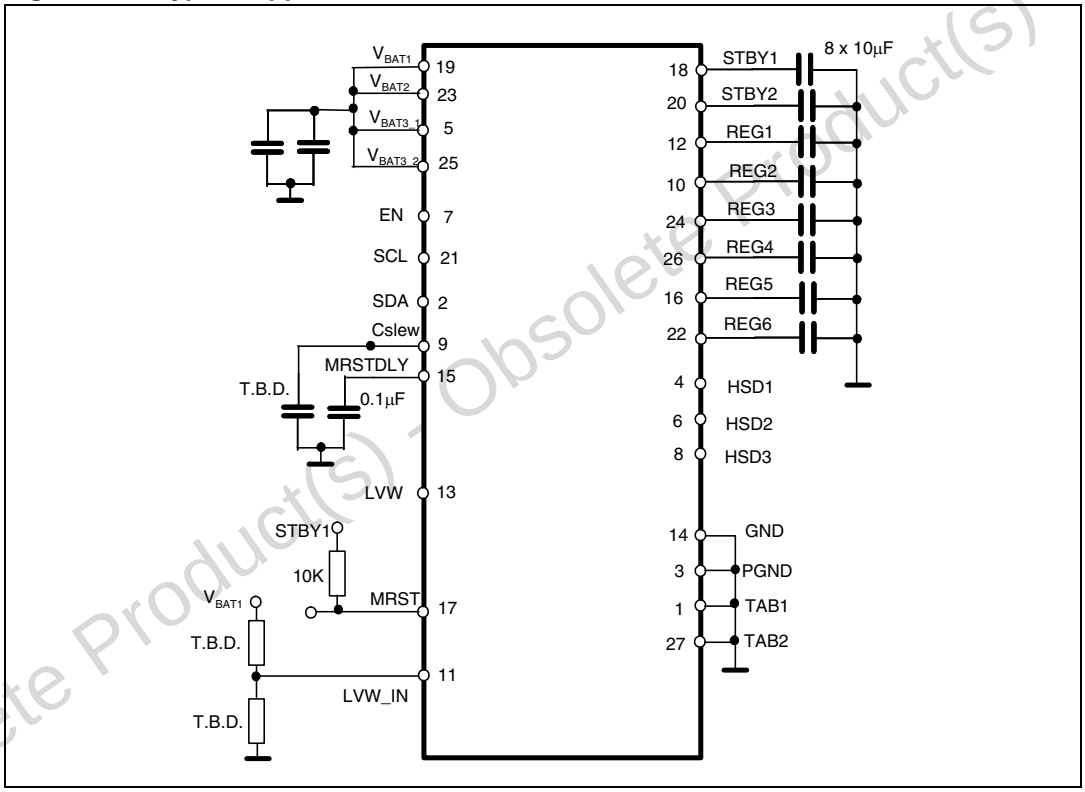


Figure 8. Typical application circuit



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3.1 Write mode:

	Chip address									Data byte											
S								0	A									A	..	..	P
	MSB							LSB		MSB							LSB				

S = START condition - SDA goes from high to low while SCL is high

A = Acknowledge - the device being written to, pulls down on data line (SDA) during the acknowledge clock pulse.

P = STOP condition - SDA goes from low to high while SCL is high.

3.2 Chip address byte:

Table 5. Chip address byte

Chip address							Read/write
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
0	0	0	1	0	0	0	0

3.3 Data byte:

Table 6. Data byte

b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Data byte 0							
REG6 SET	REG5 SET2	REG5 SET1	REG4 SET		HSD3EN	HSD2EN0	HSD1EN0
Data byte 1							
	REG6EN	REG5EN	REG4EN		REG2EN	REG1EN	

Default mode is 0000 0000 which corresponds to all outputs being off, low power mode.

Table 7. Data byte 0 description

Name	Description	State	Definition	bit
REG6 SET	REG6 output voltage configuration	0	1.8V	b7
		1	2.5V	b7
REG5 SET1 REG5 SET2	REG5 output voltage configuration	00	5.0V	b5, b6
		01	3.3V	b5, b6
		10	1.8V	b5, b6
		11	x	b5, b6
REG4 SET	REG4 output voltage configuration	0	8.0V	b4
		1	10.0V	b4
HSD3EN	HSD3 Enable	0	Off	b2
		1	On	b2
HSD2EN	HSD2 Enable	0	Off	b1
		1	On	b1
HSD1EN	HSD1 Enable	0	Off	b0
		1	On	b0

Obsolete Product(s) - Obsolete Product(s)

Table 8. Data byte 1 description

Name	Description	State	Definition	bit
REG6 EN	REG6 Enable	0	Off	b6
		1	On	
REG5 EN	REG5 Enable	0	Off	b5
		1	On	
REG4 EN	REG4 Enable	0	Off	b4
		1	On	
REG2 EN	REG2 Enable	0	Off	b2
		1	On	
REG1 EN	REG1 Enable	0	Off	b1
		1	On	

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4 Package information

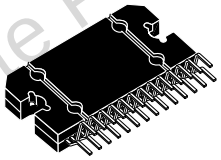
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. the category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 9. Flexiwatt27 (vertical) mechanical data and package dimensions

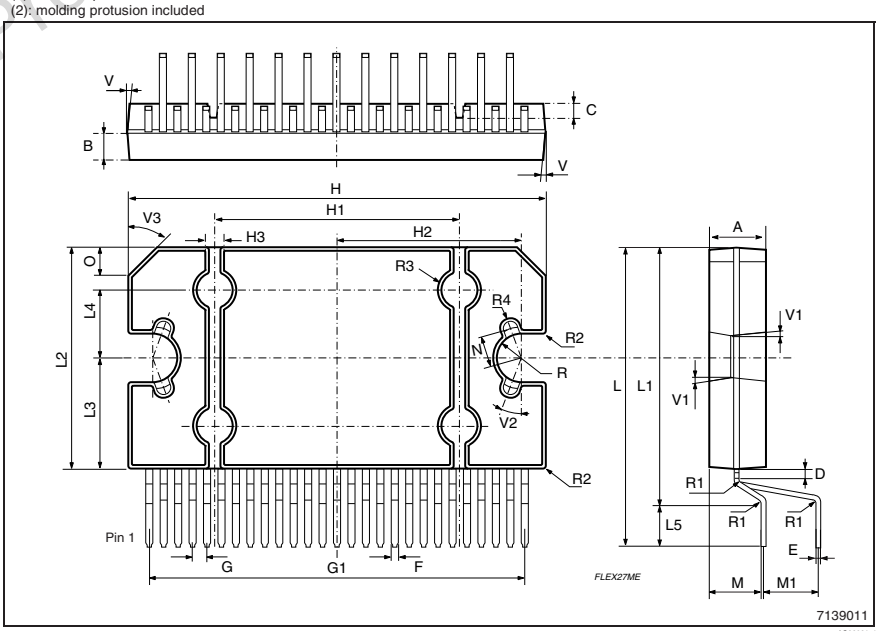
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included
(2): molding protusion included

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)



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5 Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Aug-2007	1	Initial release.
17-Sep-2013	2	Updated Disclaimer.

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