L161
Micropower Quad Comparator

FEATURES

- Programmable Supply Current
- Ultra-Low Power Consumption
- Four Comparators on Single Chip
- Direct CMOS Logic Compatibility
- Input Sensing Near Ground

BENEFITS

- Allows User to Program Speed/Power Trade-Off
- Minimizes System Power Requirements
- Reduces Board Space
- Simplifies Logic Interface
- Simplifies Single-Supply Operation

APPLICATIONS

- Smart Munitions
- Battery-Operated Systems
- Miniaturized Systems
- CMOS Logic Systems
- Level Detectors
- Window Comparators
- Oscillators and Ramp Generators

DESCRIPTION

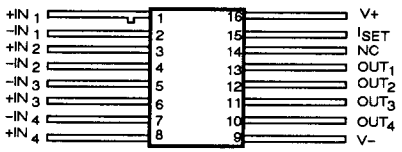
The L161 is a monolithic quad comparator featuring control of both DC and AC parameters with a single power-supply current setting resistor. Operation at very low supply current levels with power dissipation typically in the microwatt region makes the L161 ideally suited for battery operation. The programmable supply current feature allows the user to optimize the speed-power trade-off to the specific application, truly minimizing system power dissipation. The L161 is fabricated in a standard bipolar process, resulting in a wide range of operating supply voltages and currents, and allowing low-drift operation over the entire military temperature range. The L161 is available in the 16-pin plastic DIP. Performance grades include a military, A suffix (–55 to 125°C), industrial, B suffix (–25 to 85°C), and commercial, C suffix (0 to 70°C) operation.

For more information on the L161, please refer to Siliconix Application Note AN76-7.

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PIN CONFIGURATION

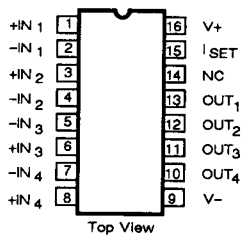
Flat Package



Top View

Order Numbers: L161AL/883

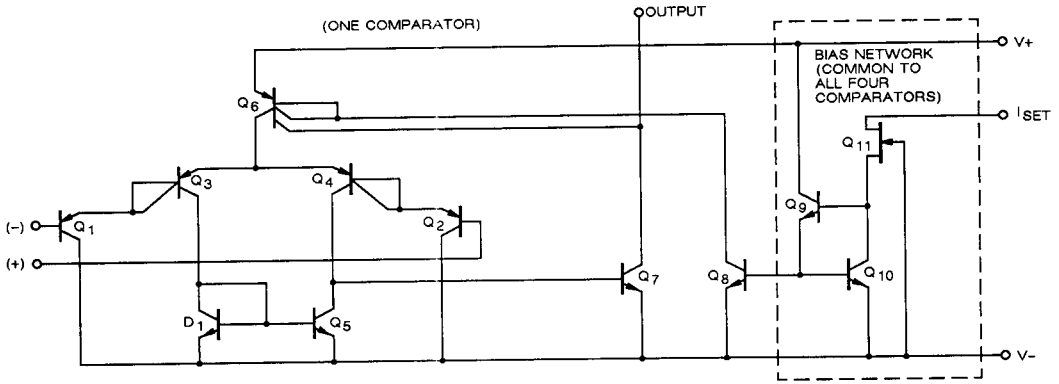
Dual-In-Line Package



Top View

Order Numbers:
Side Braze: L161AP, L161BP
Plastic: L161CJ

SCHEMATIC DIAGRAM (ONE COMPARATOR)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18 V

Differential Input Voltage ..... ±30 V

Input Voltage* ..... ±18 V

Output Short Circuit Duration** ..... Indefinite

Operating Temperature
- (A Suffix) ..... -55 to +125°C
- (B Suffix) ..... -25 to +85°C
- (C Suffix) ..... 0 to +70°C

Storage Temperature
- (A and B Suffix) ..... -65 to 150°C
- (C Suffix) ..... -65 to 125°C

Power Dissipation (Package)***
- Flat Package ..... 750 mW
- 16-pin DIP (Side braze) ..... 900 mW
- 16-pin Plastic DIP ..... 470 mW

* For supply voltages < ±18 V, maximum input voltage is equal to the supply voltage.

** Continuous short circuit current is allowed for case temperature to +125°C and ambient temperature to +70°C.

*** All leads welded or soldered to PC board. Derate 10 mW/°C above 75°C for the flat package, 12 mW/°C above 75°C for the side braze DIP and 6.3 mW/°C above 25°C for the plastic DIP.

LOW POWER ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_S = ±3 V, I_{SET} = 10 µA, R_L = 10 MΩ	LIMITS 1=25°C 2=125,85,70°C 3=-25,-55,0 °C		A SUFFIX		B,C SUFFIX		UNIT
			TEMP	TYP [c]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
INPUT									
Input Offset Voltage	V_{OS}		1 2,3	1 1		3 5		6	mV
Input Offset Current	I_{OS}		1	1		20		25	nA
Input Bias Current	I_{BT}		1	20		100		200	

LOW POWER ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_S = ±3 V, I_{SET} = 10 µA, R_L = 10 MΩ	LIMITS: 1=25°C, 2=125,85,70°C, 3=-25,-55,0 °C		A SUFFIX		B,C SUFFIX		UNIT
			TEMP	TYP [c]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
OUTPUT									
DC Open Loop Voltage Gain	A_{VOL}		1,2 3	30 30	20 10		10 5		V/mV
Low Output Voltage [d]	V_{OL}	R_L = 20 kΩ	1	-2.95		-2.6		-2.6	V
High Output Voltage [d]	V_{OH}	R_L = 200 kΩ	1	2.9	2.5		2.5		V
DYNAMIC									
Common Mode Range	CMR	Positive Limit Negative Limit	1	1.3 -3.0					V
Response Time	t	100 mV Overdrive C_L = 10 pF	1	5					µs
Common Mode Rejection Ratio	CMRR	V_{IN} = CMR	1	90	75		75		dB
SUPPLY									
Power Supply Rejection Ratio	PSRR		1	80	65		65		dB
Supply Current [e]	I_S	All Outputs Low R_L = ∞	1 2,3	210 210		325 325		325 350	µA

HIGH POWER ELECTRICAL CAHRACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions [d] Unless Otherwise Specified: V_S = ± 15 V, I_{SET} = 100 µA, R_L = 2 MΩ	LIMITS: 1=25°C, 2=125,85,70°C, 3=-25,-55,0 °C		A SUFFIX		B,C SUFFIX		UNIT
			TEMP	TYP [c]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
INPUT									
Input Offset Voltage	V_{OS}		1 2,3	1.5 1.5		3 6		6	mV
Input Offset Current	I_{OS}		1	5		60		90	nA
Input Bias Current	I_{BT}		1 2,3	100 100		400 500		800	nA

HIGH POWER ELECTRICAL CHARACTERISTICS [a]

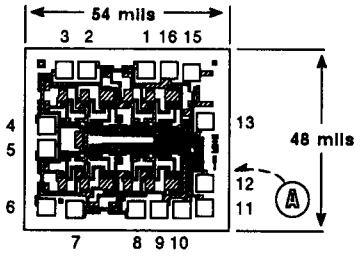
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_S = ±15 V, I_{SET} = 100 µA, R_L = 2 MΩ	LIMITS 1=25°C 2=125,85,70°C 3=-25,-55,0°C		A SUFFIX		B,C SUFFIX		UNIT
			TEMP	TYP [c]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
OUTPUT									
DC Open Loop Voltage Gain	A_{VOL}		1,2 3	100 100	50 25		30 15		V/mV
Low Output Voltage [d]	V_{OL}	R_L = 20 kΩ	1	-14.9		-14.6		-14.6	V
High Output Voltage [d]	V_{OH}	R_L = 200 kΩ	1	14.9	14.5		14.5		V
DYNAMIC									
Common Mode Range	CMR	Positive Limit	1	13					V
		Negative Limit	1	-15					
Response Time	t	100 mV Overdrive C_L = 10 pF	1	1					µs
Common Mode Rejection Ratio	CMRR	V_{IN} = CMR	1	90	75		75		dB
SUPPLY									
Power Supply Rejection Ratio	PSRR		1	80	65		65		dB
Supply Current [e]	I_S	All Outputs Low R_L = ∞	1 2,3	2.1 2.1		3.75 4.0		3.75 4.0	mA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The output current drive of the L161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs.
e. The output pull-down current is typically 75-100 times the pull-up current.
Set current (I_{SET}) and supply current (I_{SUPPLY}) can be determined by the following formulas:

$$I_{SET} = \frac{[\,(V+) - (2V_{BE}) - (V-)\,]}{R_{SET}}$$

$$I_{SUPPLY} = 21 \times I_{SET}$$

DIE TOPOGRAPHY

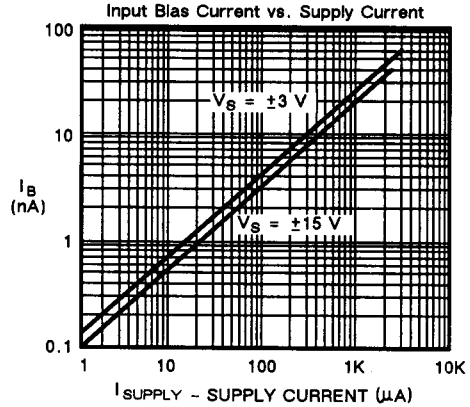


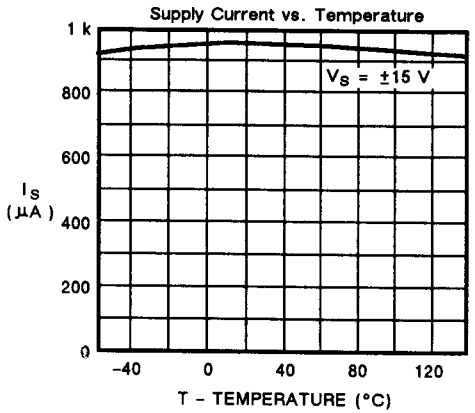
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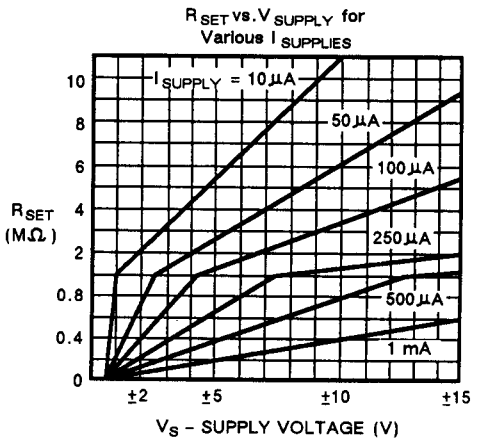
IBAJA
20 PNP Transistors
11 NPN Transistors
1 Epi FET

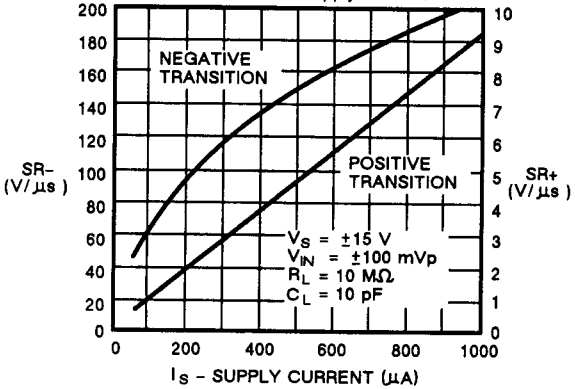
Pad No.	Function
1	$+IN_1$
2	$-IN_1$
3	$+IN_2$
4	$-IN_2$
5	$-IN_3$
6	$+IN_3$
7	$-IN_4$
8	$+IN_4$
9	V- (substrate)
10	OUT_4
11	OUT_3
12	OUT_2
13	OUT_1
15	I_{SET}
16	V+

TYPICAL CHARACTERSITICS







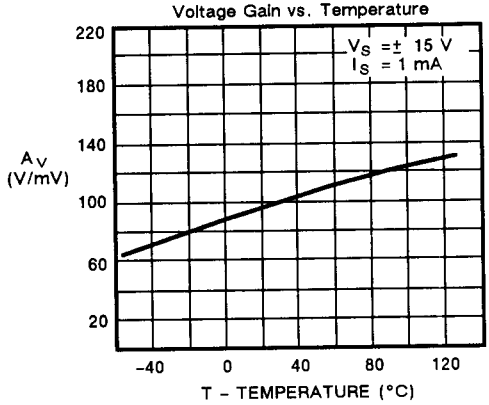


NOTE: The output current drive of each comparator in the L161 is non-symmetrical. The pull-up current is typically $2[V+ - 1 - (V-)/R_{SET}]$ and the pull-down current capability is typically from 75 to 150 times the pull-up current.

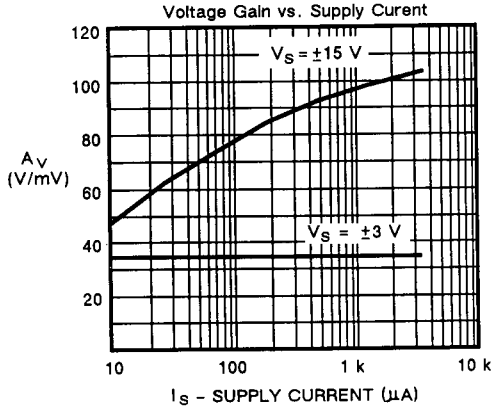
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TYPICAL CHARACTERSITICS (Cont'd)

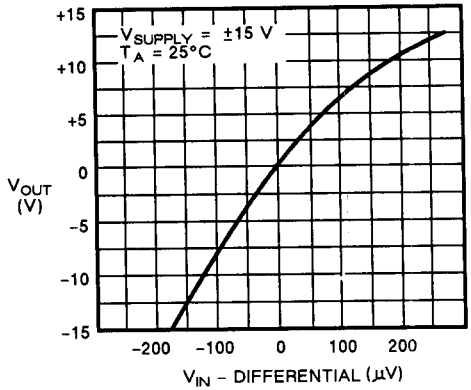
Voltage Gain vs. Temperature



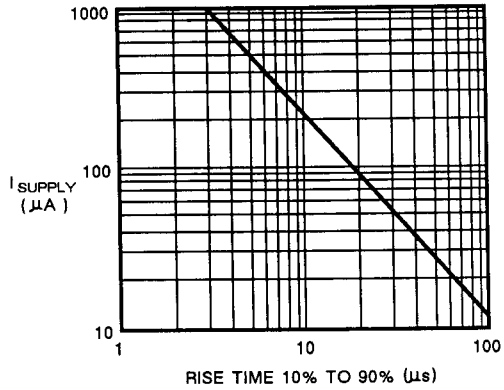
Voltage Gain vs. Supply Current



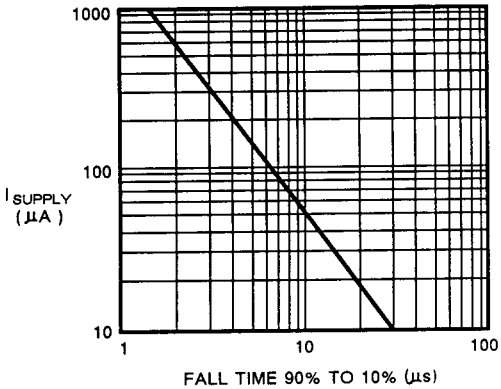
Transfer Characteristic



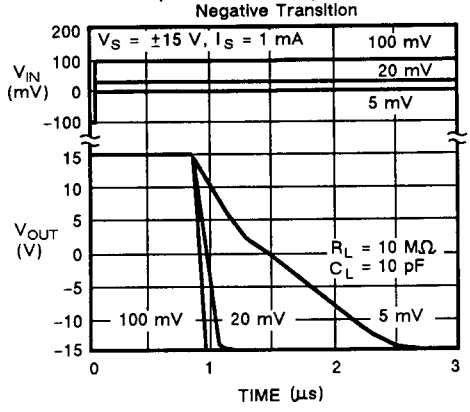
Rise Time vs. Supply Current with One CMOS Load



Fall Time vs. Supply Current with One CMOS Load

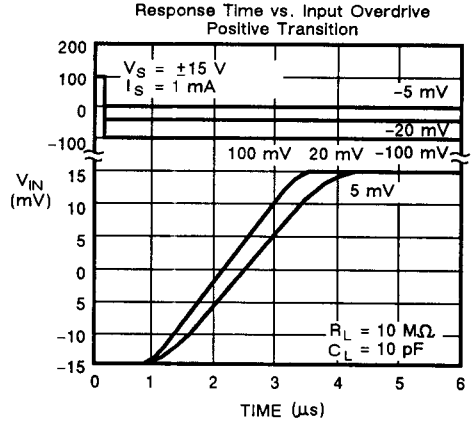


Response Time vs. Input Overdrive Negative Transition



NOTE: The output current drive of each comparator in the L161 is non-symmetrical. The pull-up current is typically $2[(V+) -1 -(V-)/R_{SET}]$ and the pull-down current capability is typically from 75 to 150 times the pull-up current.

TYPICAL CHARACTERSITICS (Cont'd)



NOTE: The output current drive of each comparator in the L161 is non-symmetrical. The pull-up current is typically $2[(V+) -1 -(V-)/R_{SET}]$ and the pull-down current capability is typically from 75 to 150 times the pull-up current.

APPLICATIONS

The L161 is a monolithic quad micropower comparator with an external control for varying its AC and DC characteristics. The variation of a single programming resistor will simultaneously alter parameters such as supply current, input bias current, slew rate, output drive capability, and gain. By making this resistor large, operation at very small supply current levels and power dissipations -- typically in the low microwatt region -- is possible. The L161 is therefore ideal for systems requiring minimum power drain, such as battery-powered instrumentation, aerospace systems, CMOS designs, and remote security systems.

The L161 is fabricated using standard bipolar processing. The circuit (Figure 1) is composed of five majcr blocks -- four comparators and a common bias network. Q1 - Q6 and D1 form a darlington differential amplifier with double-to-single ended conversion. Q6 is a dual current source whose outputs are exactly twice the current flowing through Q8. The collector current of Q8 is a function of the current supplied externally to Q9 - Q10, which in turn is known as the set current or I_{SET}. This set current is established by a resistor connected between the I_{SET} terminal and a voltage source, most commonly the positive supply. Q11 prevents excessive current from flowing through Q9 and Q10 in the event the I_{SET} terminal is shorted to the positive supply; it has no effect on circuit operation under normal conditions.

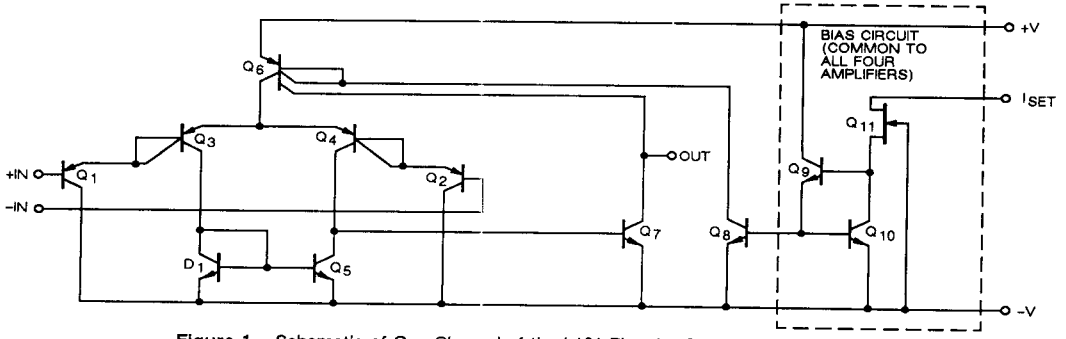


Figure 1. Schematic of One Channel of the L161 Plus the Common Bias Network

SETTING THE SET CURRENT

The set current can be expressed as:

$$I_{SET} = \frac{((V+) - (2\ V_{BE}) - (V-))}{R_{SET}} \quad (1)$$

where V+ is the voltage to which the control resistor is connected, V- is the negative supply voltage, V_{BE} is the base emitter drop of Q9 or Q10 (about 0.7 V), and R_{SET} is the value of the external control resistor or set resistor. Equation 1 is simply a derivative of Ohms Law. There is also an analytical relationship between I_{SET} and the total supply current:

(2)

I_{SUPPLY} = (I_{SET} (current sourced by Q6 to Q8)

+2 I_{SET} (current sourced to the differential amplifier by Q6)

+2 I_{SET} (current sourced to the comparator output by Q6))

X 4 (the total number of comparators)

+I_{SET} (current sourced through Q11, Q10, and Q9 to V-)

= (I_{SET} + 2 I_{SET} + 2 I_{SET}) X 4 + I_{SET}

= 21 I_{SET}

The output current pulldown capability (I_{OL}) of the L161 is about 2 orders of magnitude greater than the high output drive current, (I_{OH}), which allows wire-ORing the outputs. I_{OH} is simply the current sourced by Q6:

$$I_{OH} = 2 \times I_{SET} \quad (3)$$

I_{OL} is found by multiplying the current sourced by the collector of Q6 by the gain Q7:

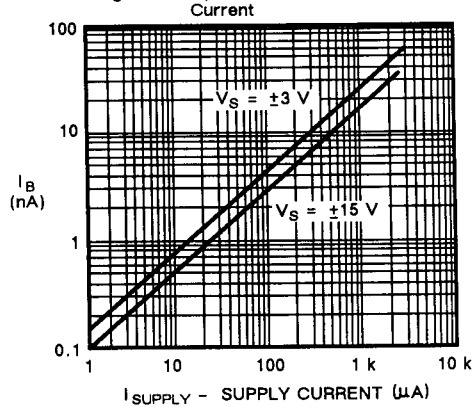
$$I_{OL} = \beta\ (Q_7) \times 2\ I_{SET} \quad (4)$$

The beta of Q7 is about 75-150.

INPUT BIAS CURRENT

Input bias current is a function of the betas of input devices Q1 - Q2 and I_{SET}. This is difficult to express analytically because β varies greatly with both processing and collector current; however it is roughly proportional to the set current and can easily be determined experimentally (see Figure 2).

Figure 2. Input Bias Current vs. Supply Current



GAIN

Gain varies logarithmically with changes in supply voltage and linearly with changes in set current. Primary causes are the decrease in output impedance of Q7 with decreasing supply voltage and an increase in transistor betas with increasing set current. Other AC parameters such as slew rate and transition time are also effected by set current; however, current dependent parameters such as beta and chip capacitances make mathematical expressions imprecise. These relationships have been determined empirically and are presented in Figure 3 and 4.

Figure 3. Slew Rate vs. Supply Current

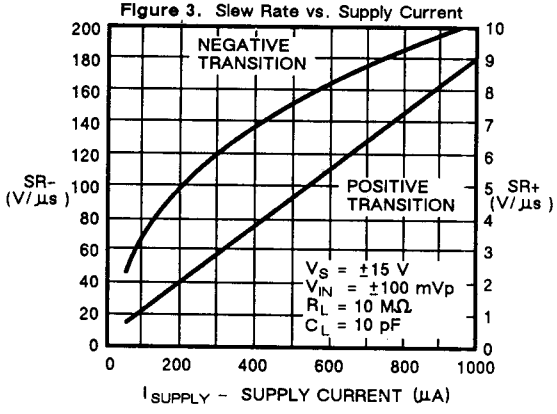
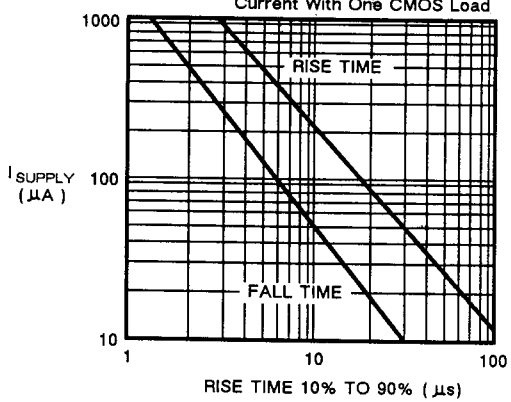
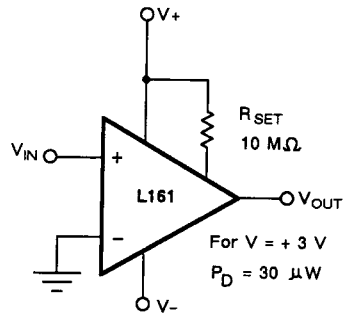


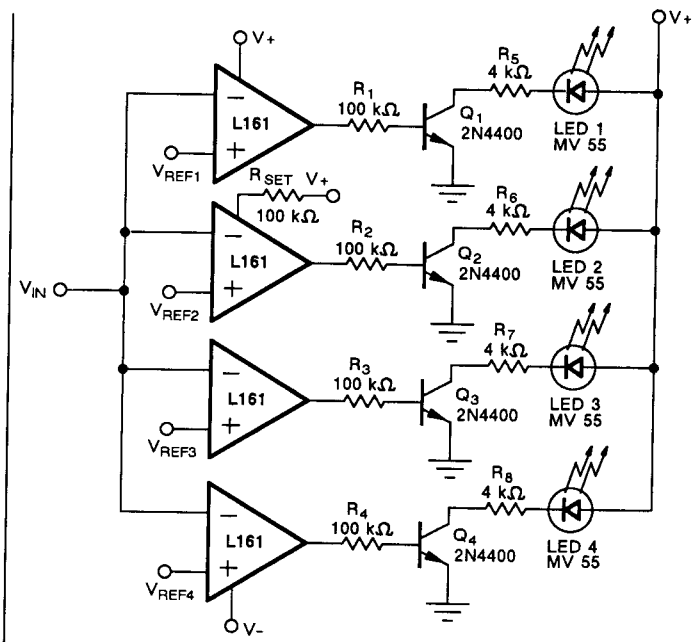
Figure 4. Rise and Fall Times vs. Supply Current With One CMOS Load



The designer's ability to program the key parameters of the L161 enables him to program just enough supply current to meet his design objectives. This coupled with the L161's performance using only microwatts of power makes it ideal for any micropower or battery-powered system, as well as a replacement for existing higher power comparators. The following applications illustrate the flexibility and unique capabilities of the L161.

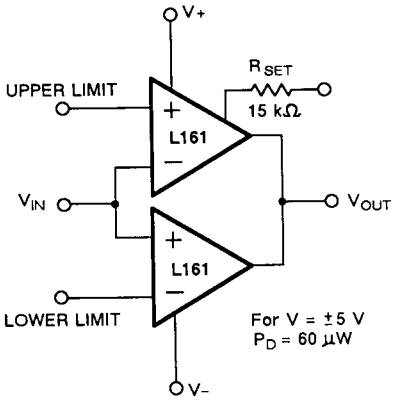


Zero Crossing Detector

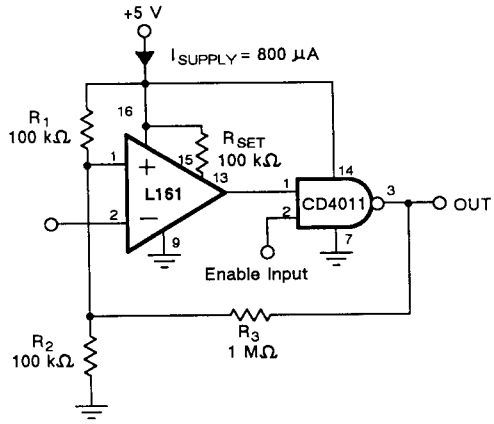


Voltage Level Detector

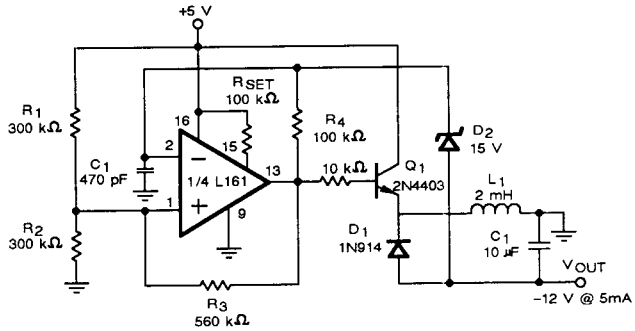
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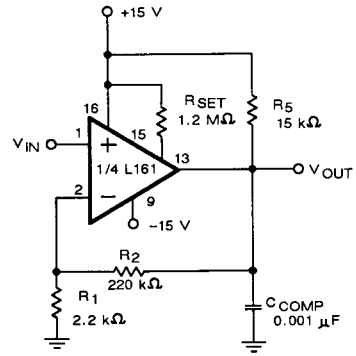
Double Ended Limit Detector



CMOS Line Receiver

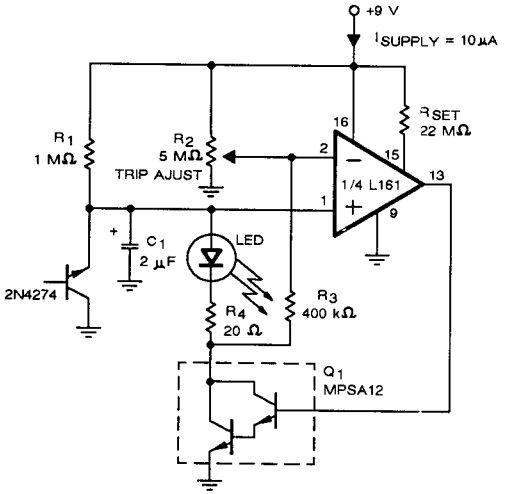


A Regulated DC to DC Converter

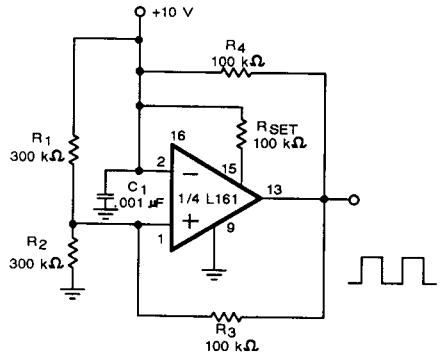


The L161 as an X100 Operational Amplifier

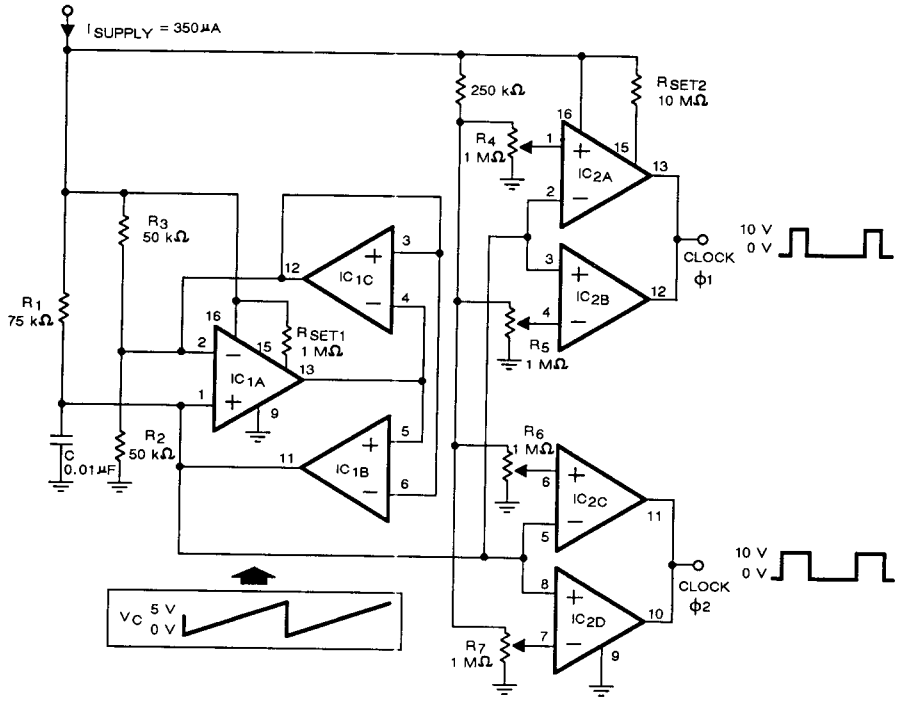
APPLICATIONS (Cont'd)



A Low Battery Indicator



Square Wave Oscillator



A Versatile 2 φ Pulse Generator

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